DIRAC: DIgital Readout Asic for hadronic Calorimeter

DHCAL meeting – LLR – january 2008, the 20th

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Outline

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Requirements: detectors

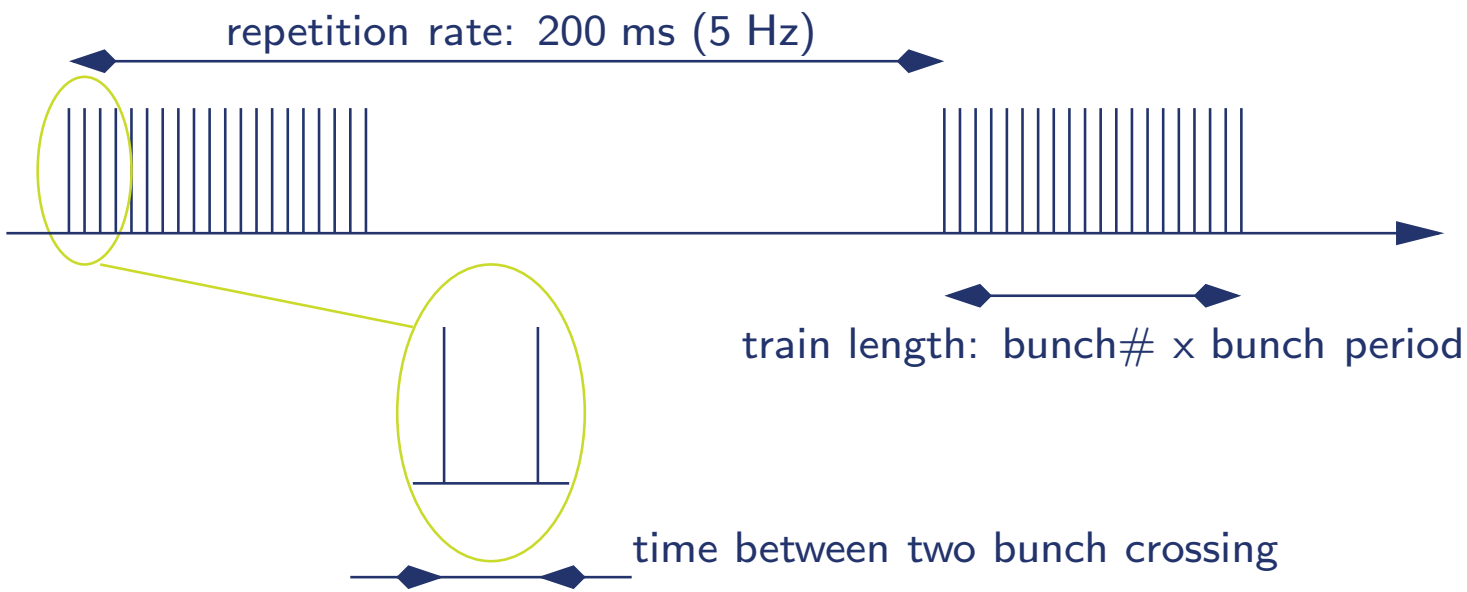
In order to build a Digital Hadronic CALorimeter with very high granularity at the ILC, frond end ASIC prototype must match different gaseous detectors to select which one is the best:

	GRPC	MicroMegas	GEM
Charge	0.1∼10 pC	1∼100 fC	1∼100 fC
C_{det} (1 cm^2)	60 pF	60 pF	60 pF
t_r	2 ns	<2 ns	<2 ns
width	20 ns	complex shape	20 ns

Requirements: beam structure

Front-end timing must respect beam clock characteristics:

	Minimum	Nominal	Maximum
Bunch#	1320	2625	5120
Period (ns)	189	369	480
Rate (Hz)		5	



Additionaly, the front end is shut down during inter-train period to save power.

Aims of this development

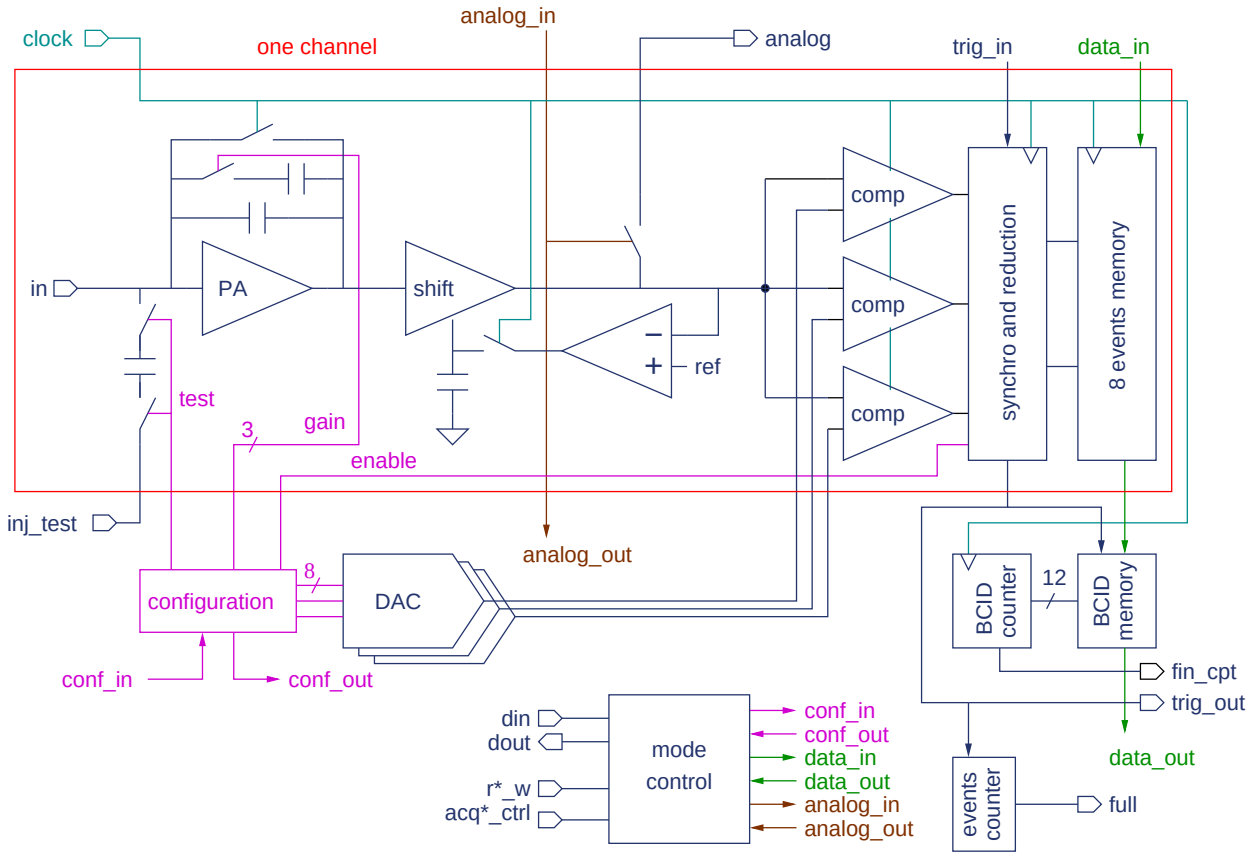
The design is driven by the following constraints:

- Low cost ASIC (about 30 millions of channels !);
- Low power ASIC (*idem* !);
- Decrease PCB complexity (6 layers, easy routing, few external components);
- Try to suppress calibration needs (electronic channel disparity requirements not so strong for a DHCAL).

Outline

Synoptic

Compare input charge to 3 thresholds (set by 3 DACs) and store the 2 bits energy information.



Gated integrator : less sensitive to signal shape (different detectors) !

Operation

Synchronous architecture on beam clock (trains and bunches):

During trains:

- Beam on: analog charge integration;
- Beam off: comparisons to thresholds, store results.

Outside trains:

- Standby analog front-end;
- Digital data readout;
- Slow control.

Main features summary

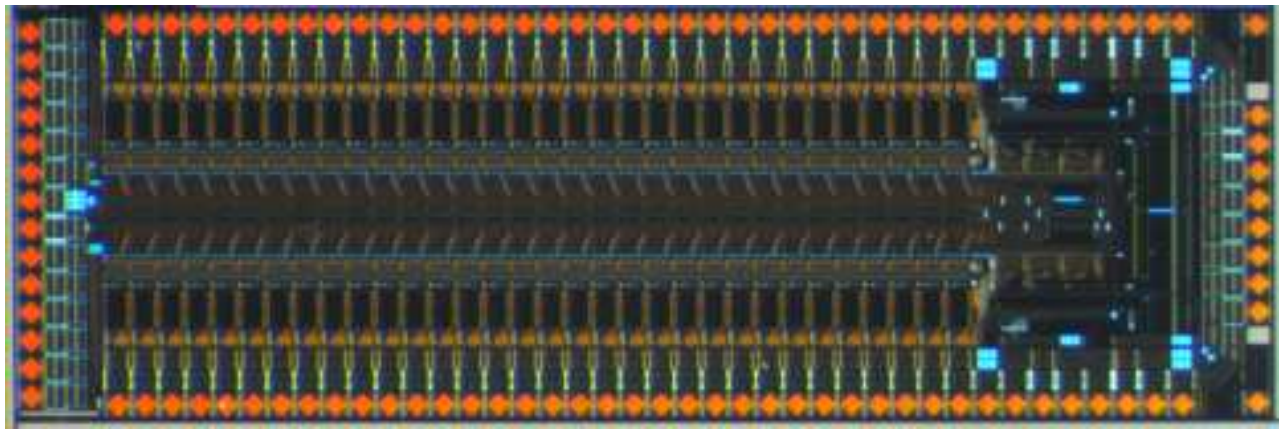
- 64 channels;
- Low-cost AMS CMOS 0.35 µm process technology;
- Power consumption $<$ 1 mW per channel + 1% power pulsing:
  $\rightarrow$ $<$ 10 µW per channel
- 2 gains: 100 mV/pC and 5 mV/fC;
- 3 thresholds, each on 8 bits for 1 V, *i.e.* 3.9 mV/DAC:
  $\rightarrow$ 0.8 fC/DAC (Micromegas, GEM)
  $\rightarrow$ 40 fC/DAC (RPC)
- 12 bits BCID counter;
- Internal memory of 8 events (2 bits per event);
- Analog input on each sides: easy PCB routing.

Characterisation summary

In Micromegas mode:

- S-curve width < 2.4 fC;
- Dispertion among channels 3.2 fC;
- Non-linearity ± 0.8 fC;
- Pedestal dispertion ± 7.7 fC;
- Power-on time < 1 µs, allowing 0.5 % duty cycle.

Photography



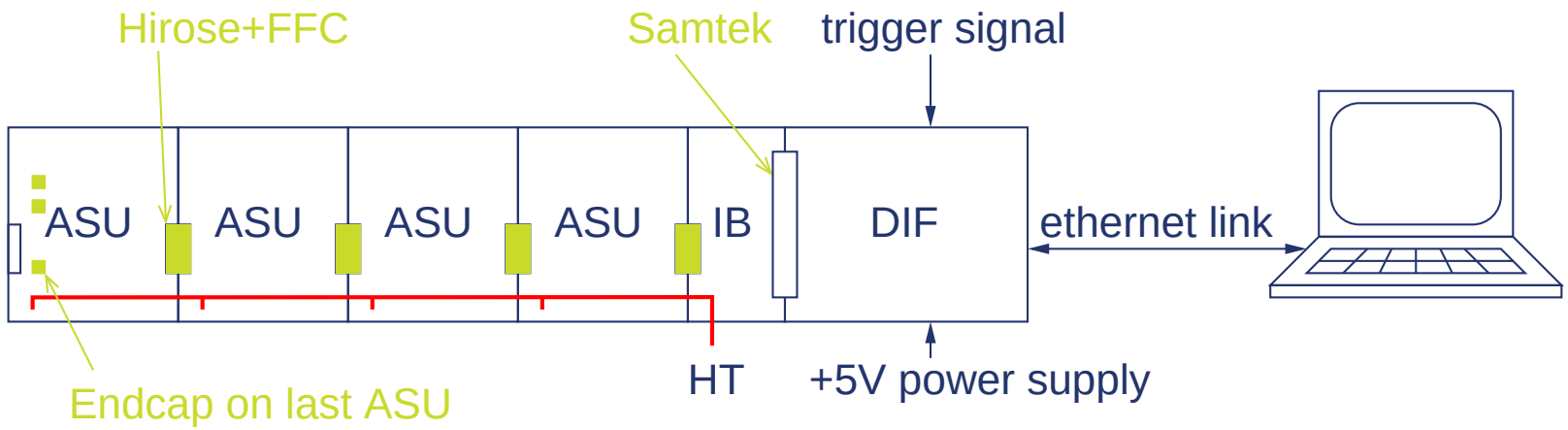
Only 1.5×4.7 mm^2

- Top and bottom: analog inputs;
- Right: analog power supply and bias;
- Left: digital I/O.

Outline

Assembly schematic overview

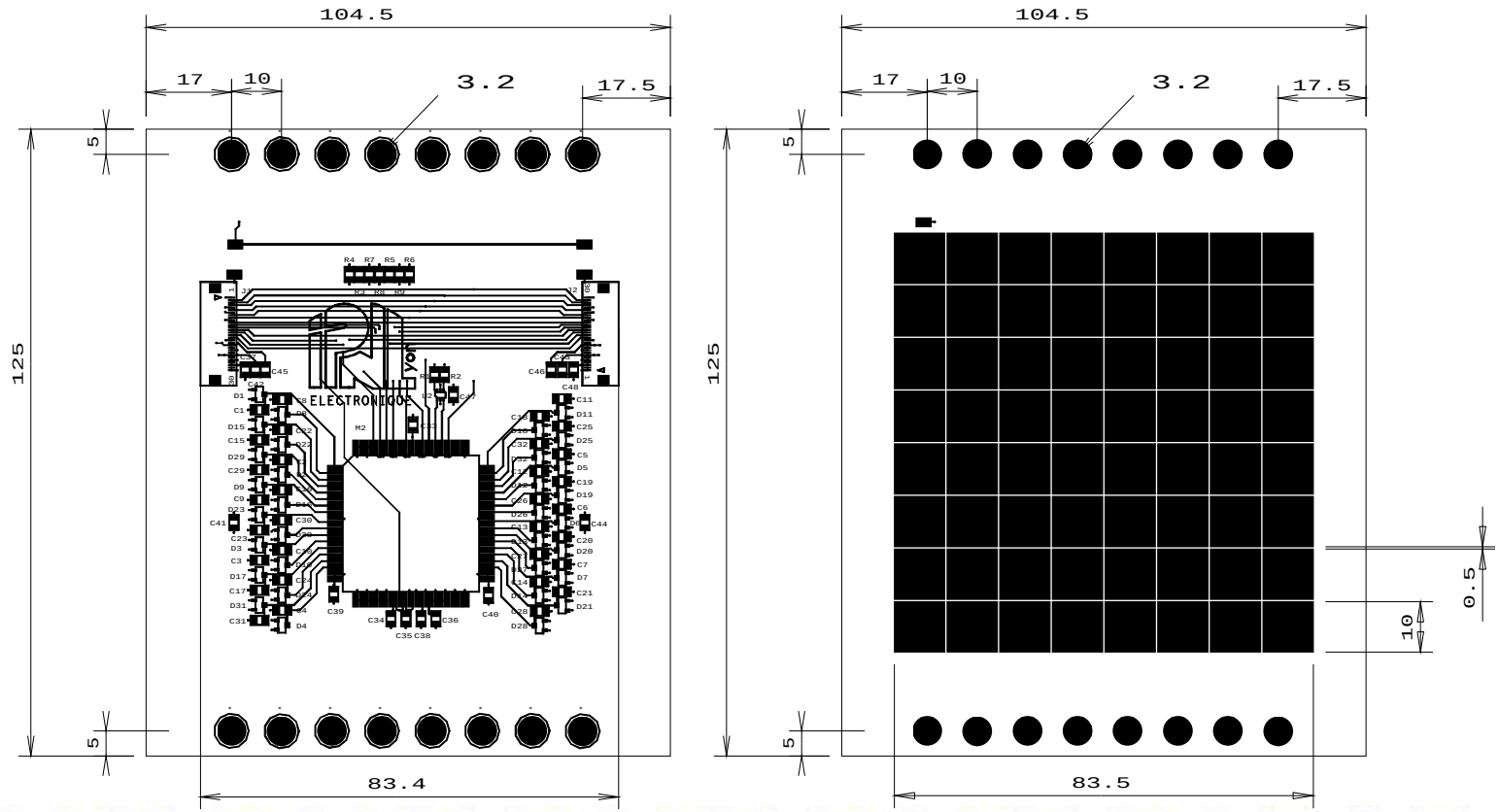
ASU: Active Sensor Unit
IB: Intermediate Board
DIF: Digital InterFace



Present: custom DAQ with ethernet for characterisation and august testbeam;
Futur: connection to the CALICE DIF and DAQ.

Active Sensor Unit boards

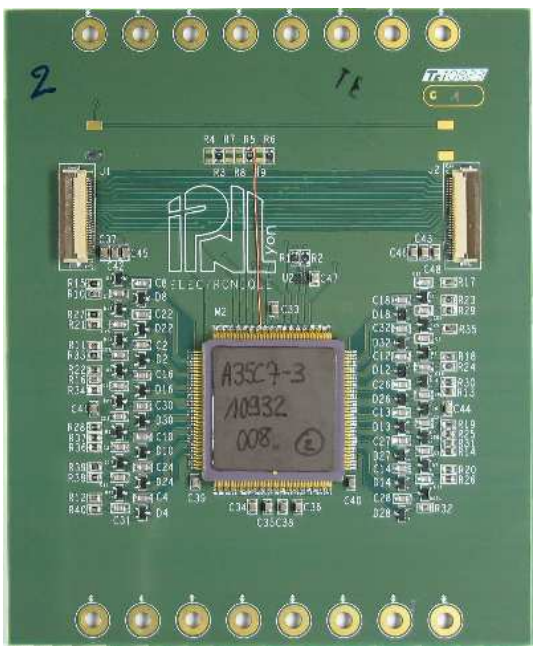
6 layers, 1.6 mm thick. Burried and blind vias for anode connection.
Digital daisy chain. 8×8 anodes of 1 cm^2 each.
MicroMegas sparks protections.
For Micromegas or RPC operation.

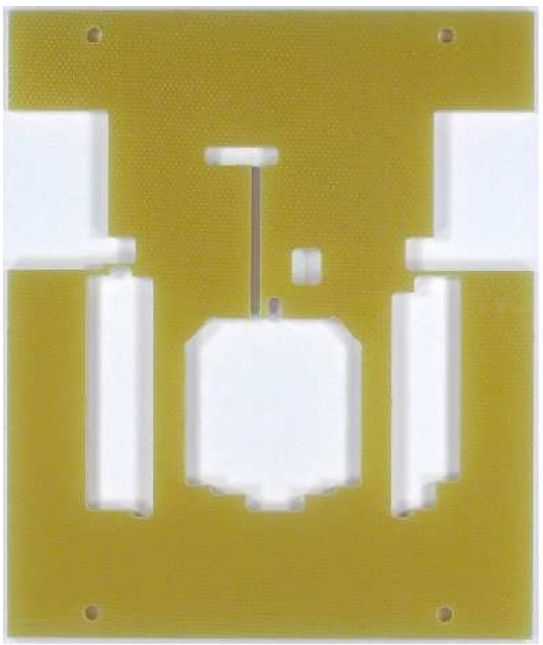


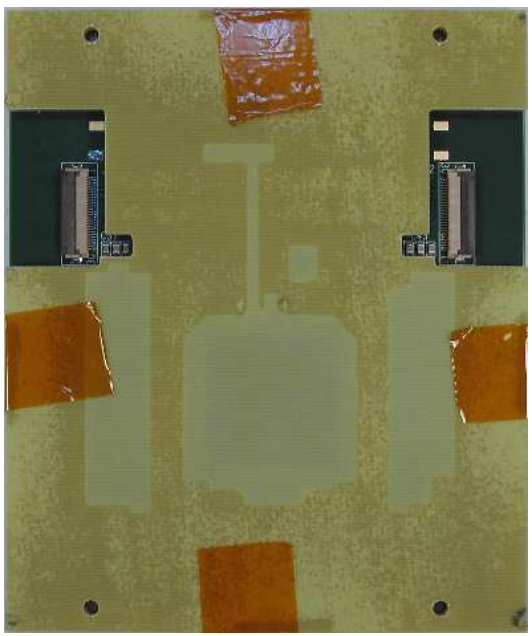
Micromegas Active Sensor Unit (1)

PCB and ASIC made by IPNL/IN2P3/CNRS
Bulk lamination by CERN (R. de Oliveira *et al.*)
Detector assembly and characterisation made by LAPP/IN2P3/CNRS (C. Adloff *et al.*).

PCB + glued epoxy mask (flat top needed for lamination)

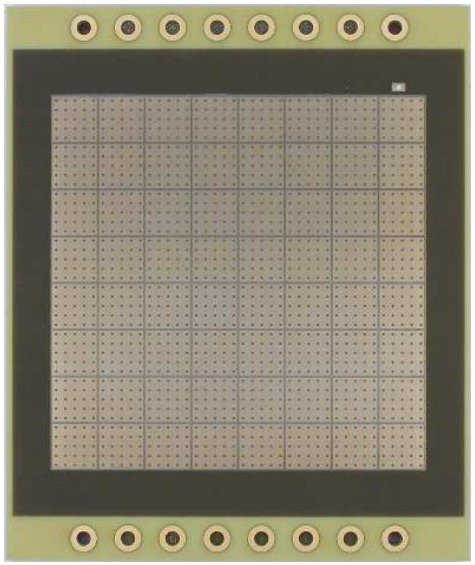


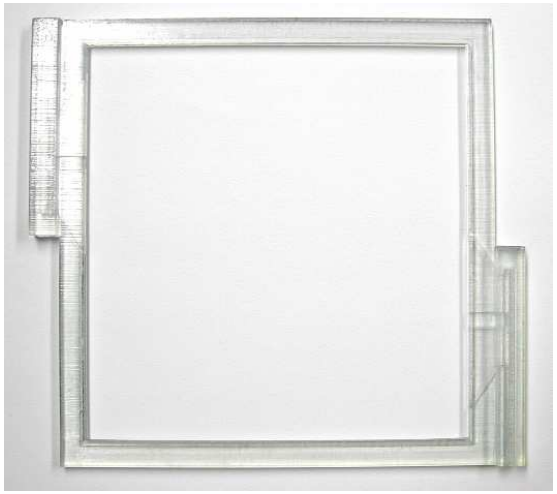


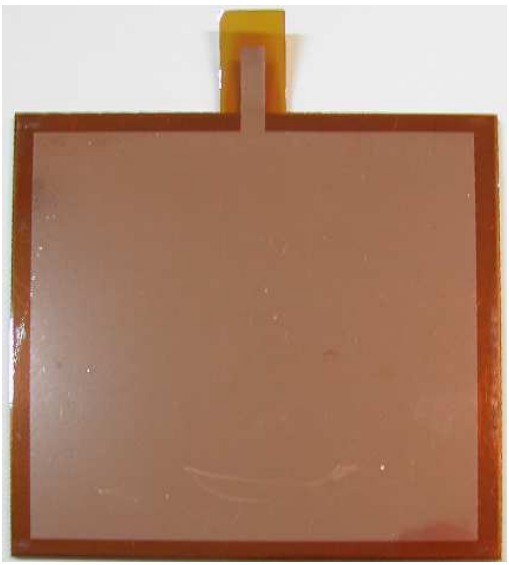


Micromegas Active Sensor Unit (2)

Laminated mesh on PCB + frame + drift cathode...

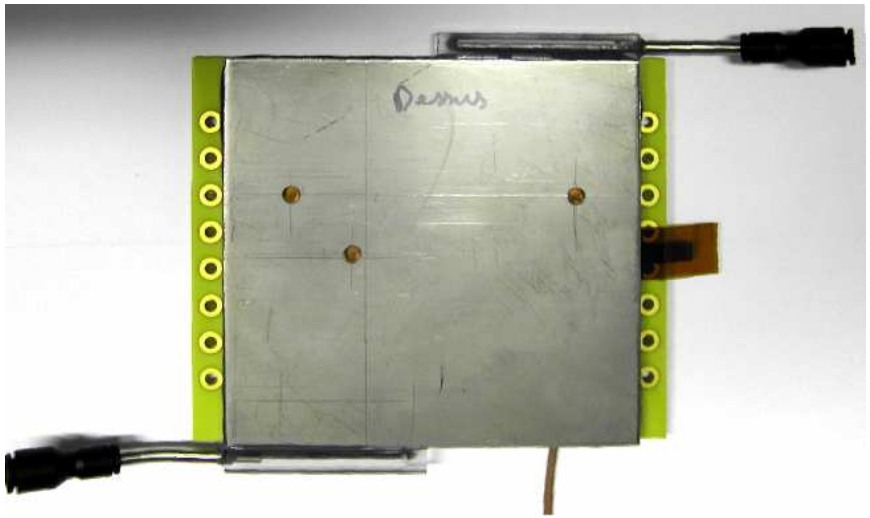


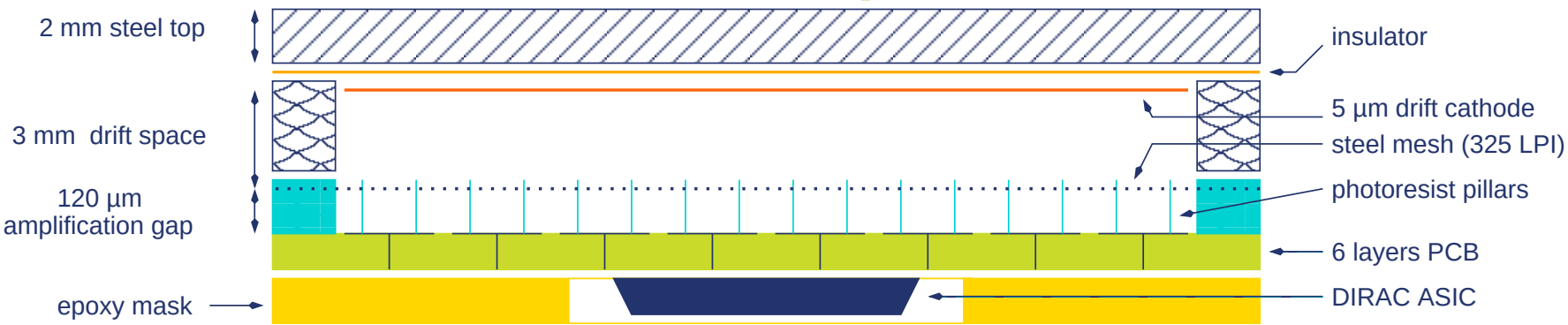




Micromegas Active Sensor Unit (3)

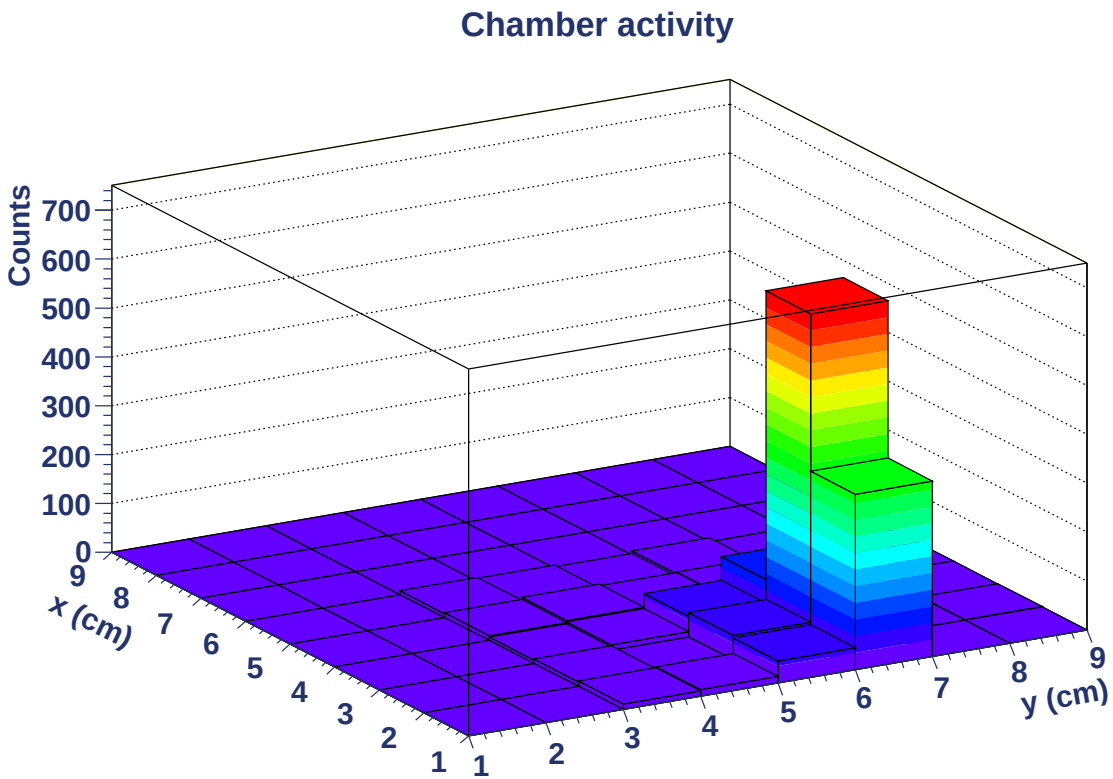
. . . add gaz inlets/outlets and HV connection: the first operational bulk micromegas chamber with embedded readout electronics!





Test beam results (1)

Pions 200 GeV
Detector fixed on a moving table.



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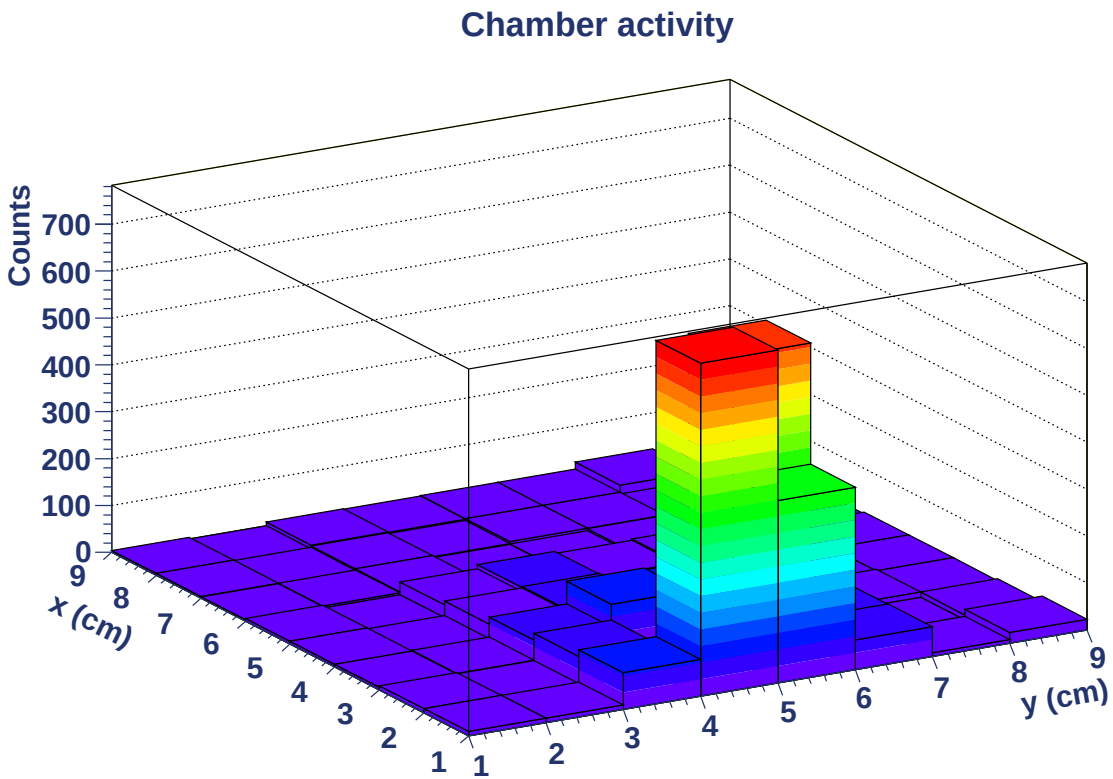

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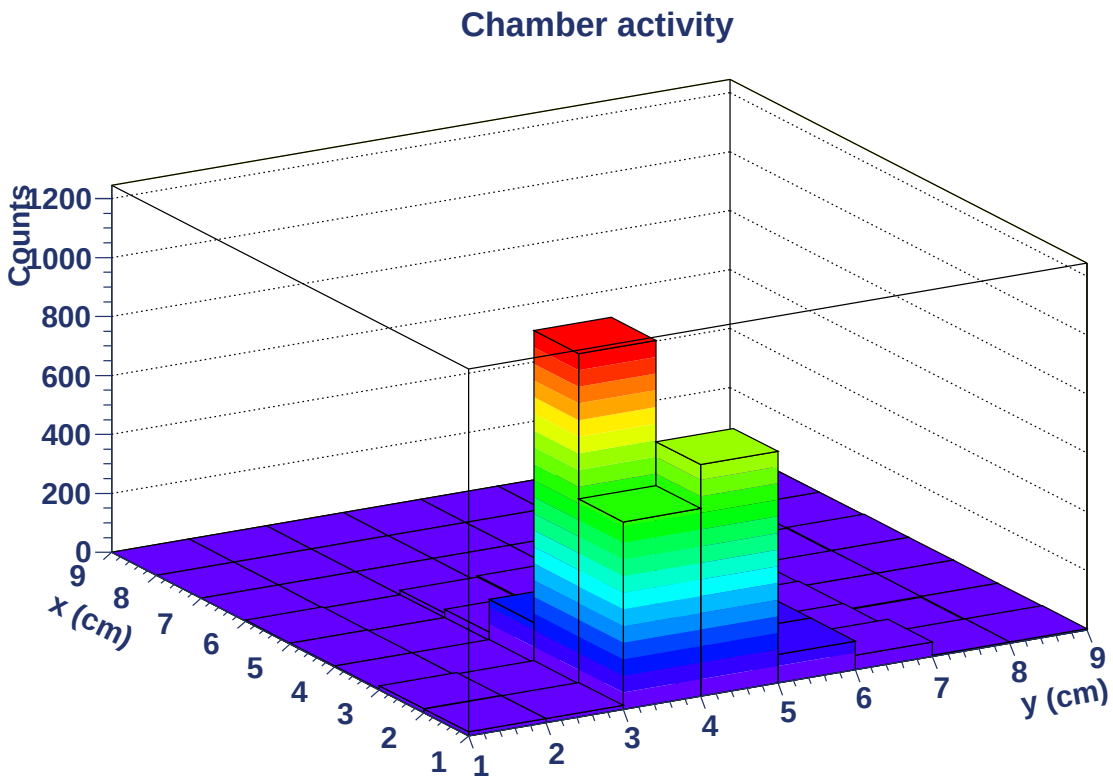
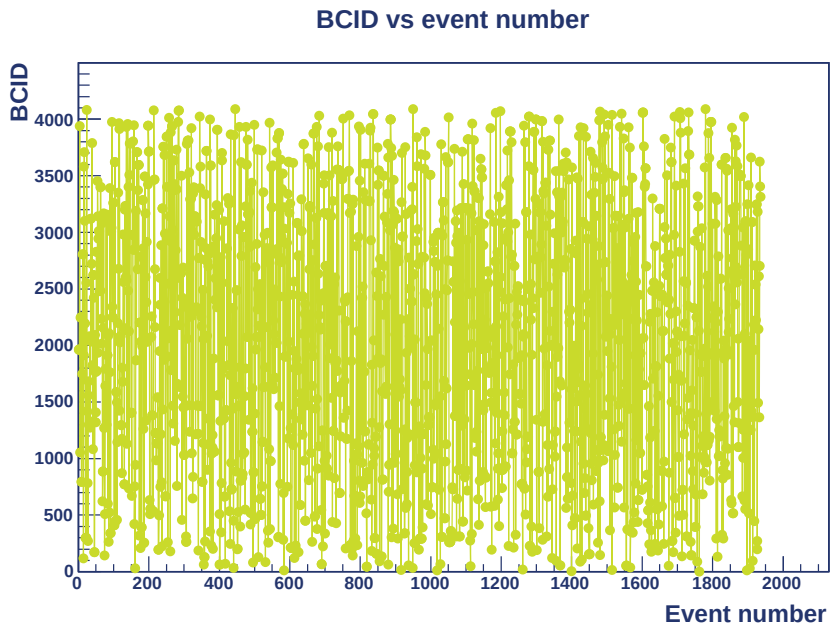


Test beam results (2)

Only 4 *hours* of beam at the end of august period: few statistics and no time for tuning, BUT:

- Multiplicity < 1.1 pad hited per trigger (thresholds: 19/32/56 fC).
- No (0 !) triggers when the beam is OFF.
- Good behavior: BCID are equally represented.



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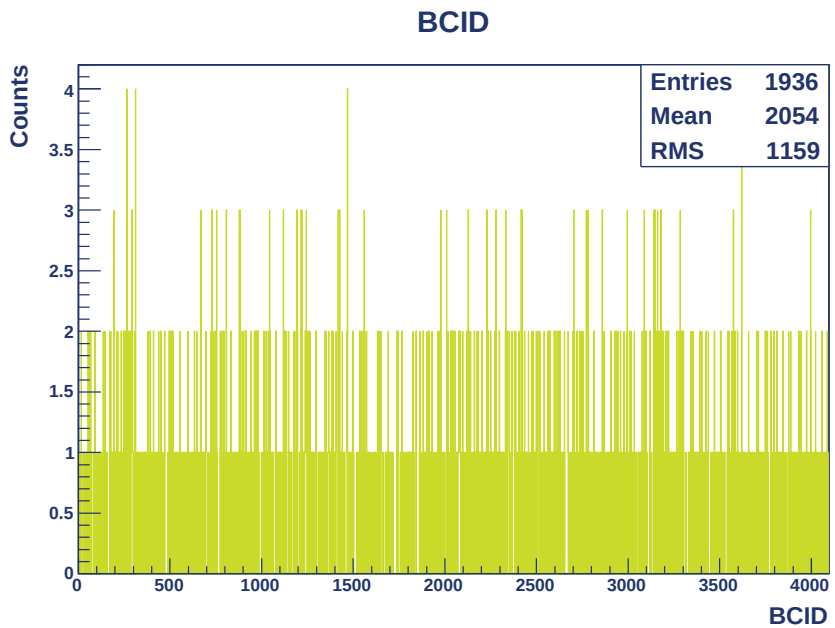

Outline

Improvements for DIRAC 2

- Internal trigger bug correction;
- Add trigger in/out capabilities;
- Add trigger masking feature in configuration;
- Add internal test circuitry;
- Add multiplexed analog readout (thanks to LPCCF/IN2P3);
- Add 2 MicroMegas gain (global configuration);
- Lower offset discriminator;
- Add LVDS clock (thanks to LAL/IN2P3);
- Power supply pinout improvements and simplification;

Plan for 2009

- At the end of january, we should have ASIC (IPNL), test board (ASU-like, designed at IPNL), DIF with firmware (LAPP, see G. Vouters talk) and acquisition software (IPNL, C. Combaret). G. Vouters has made a large work to synchronize ASIC with asynchronous data (cosmic and test beam) !
- Until the end of february/march, firmware and software will be tested, and then the fine characterisation of prototypes will be performed;
- Then, we will work toward large area ASUs (32 cm$\times$48 cm);
- In the same time, we will start the development of DIRAC 3.

DIRAC 3

Some extra features will be added to DIRAC version 3:

- Data reduction algorithm will be studied;
- By-pass mechanism will certainly be implemented;
- All digital part will be redesigned with automated tool to allow easier modification/reuse in the future;
- I2C-like configuration interface will be designed by Y. Zocaratto at IPNL (perhaps for readout too): 7 bits address (chip selection), R/W operation, 8 bits register selection and 8 bits data. Broadcast capabilities.

Altough I'll work soon at LAPP, DIRAC design will continue in collaboration with the electronic team of IPNL / MICRHAU.

Thank you for your attention !