Wojciech.Dulinski@ires.in2p3.fr

3D-3Tiers CMOS "Monolithic" Pixel Sensor for 2009 Submission

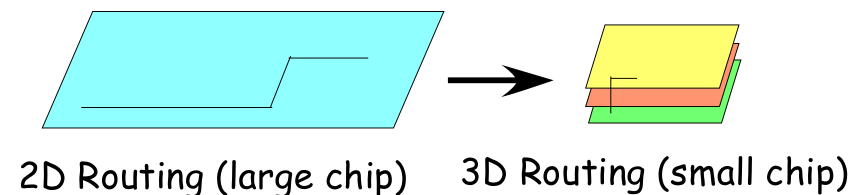
Wojciech Dulinski, IPHC Strasbourg

On the way towards fast, radiation tolerant and ultra thin CMOS sensors, we propose fully depleted epitaxial substrate with first stage buffer amplifier on the same wafer, capacitively coupled to the 3D readout electronics on top

Wojciech.Dulinski@ires.in2p3.fr

3D Integrated Circuits: introduction (Ray Yarema's slides)

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance. (Performance limited by interconnect)
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- HEP should watch industry and take advantage of the technology when applicable.



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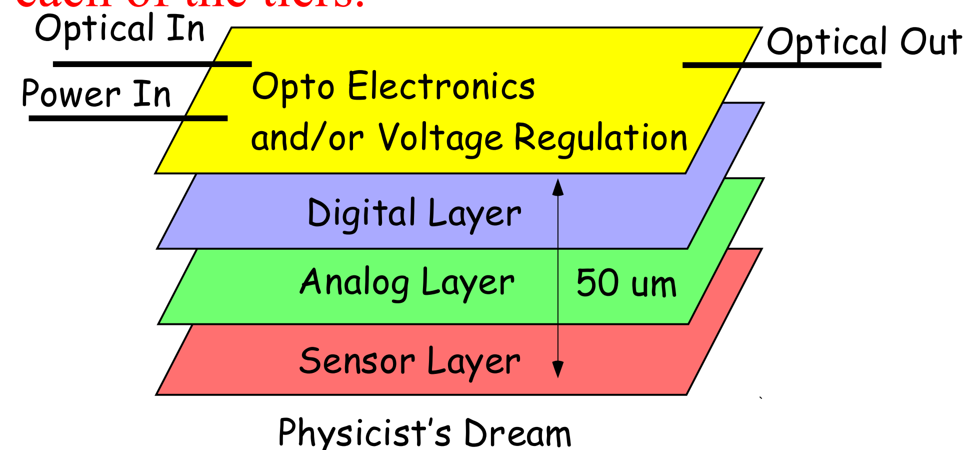
Key Technologies for 3 D Electronics or Vertical Scale Integration (Ray Yarema)

- **There are 4 key technologies**
  - Bonding between layers
  - Wafer thinning
  - Through wafer via formation and metallization
  - High precision alignment
- **Many of these technologies are also used in the development of SOI detectors**
- **3D offers advantages over SOI detectors**
  - Increased circuit density due to multiple tiers of electronics
  - Independent control of substrate materials for each of the tiers.
  - Ability to mate various technologies in a monolithic assembly
    - DEPFET + CMOS or SOI
    - CCD + CMOS or SOI
    - MAPS + CMOS or SOI



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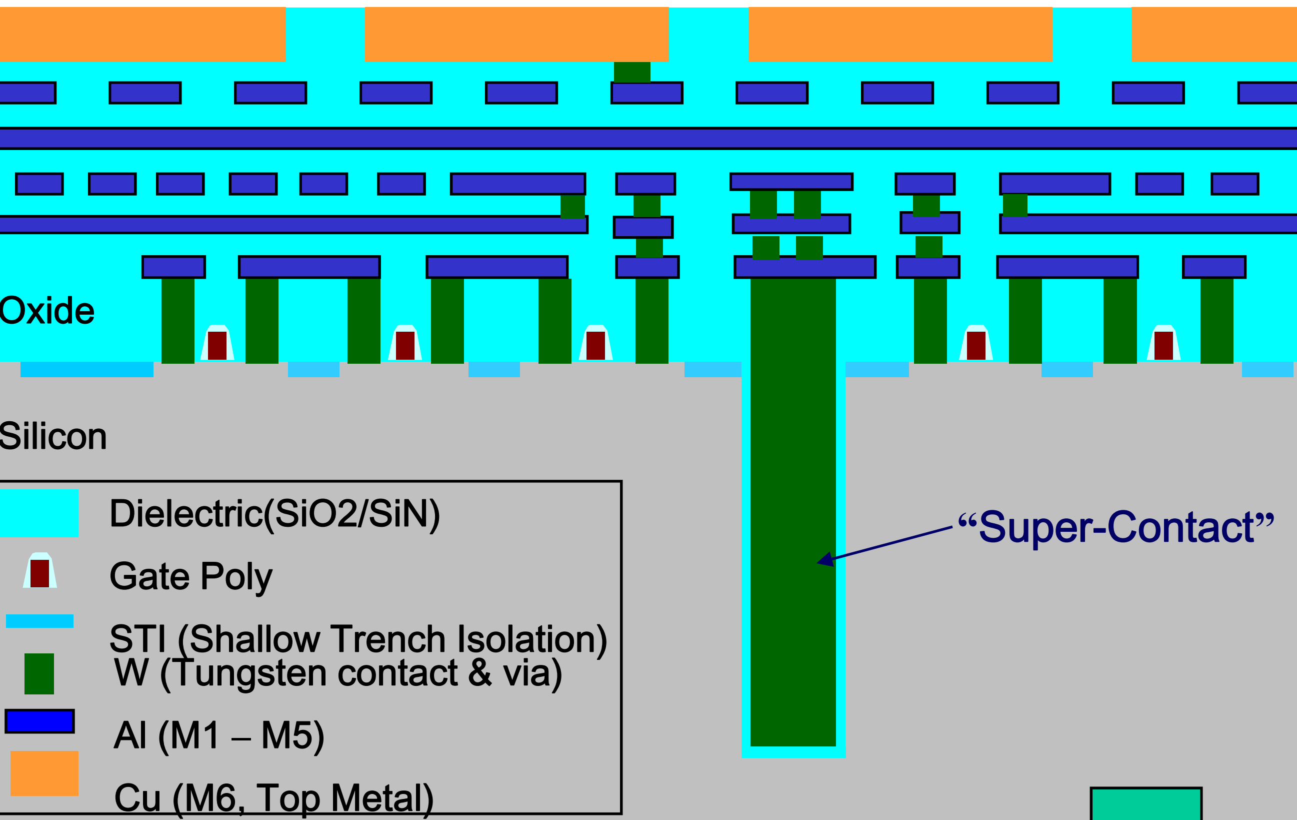
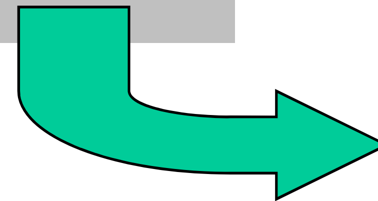
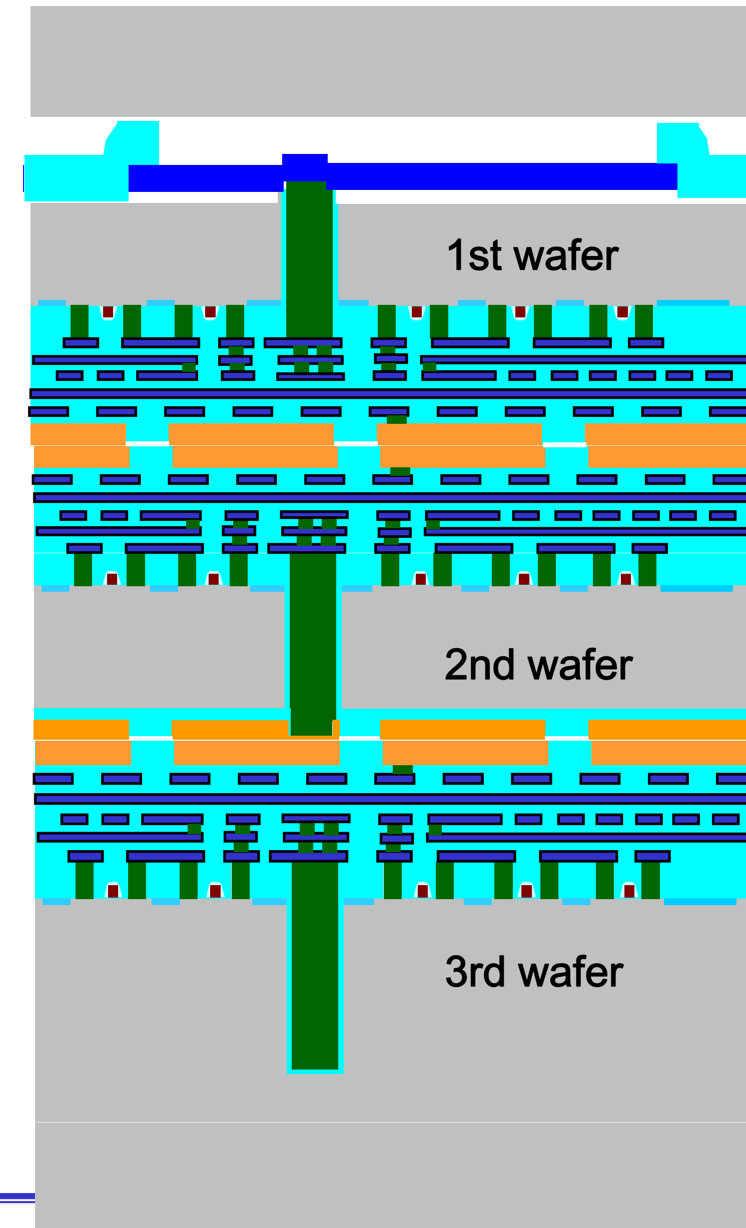
A Closer Look at Wafer-Level Stacking (Bob Patti, Tezzaron)







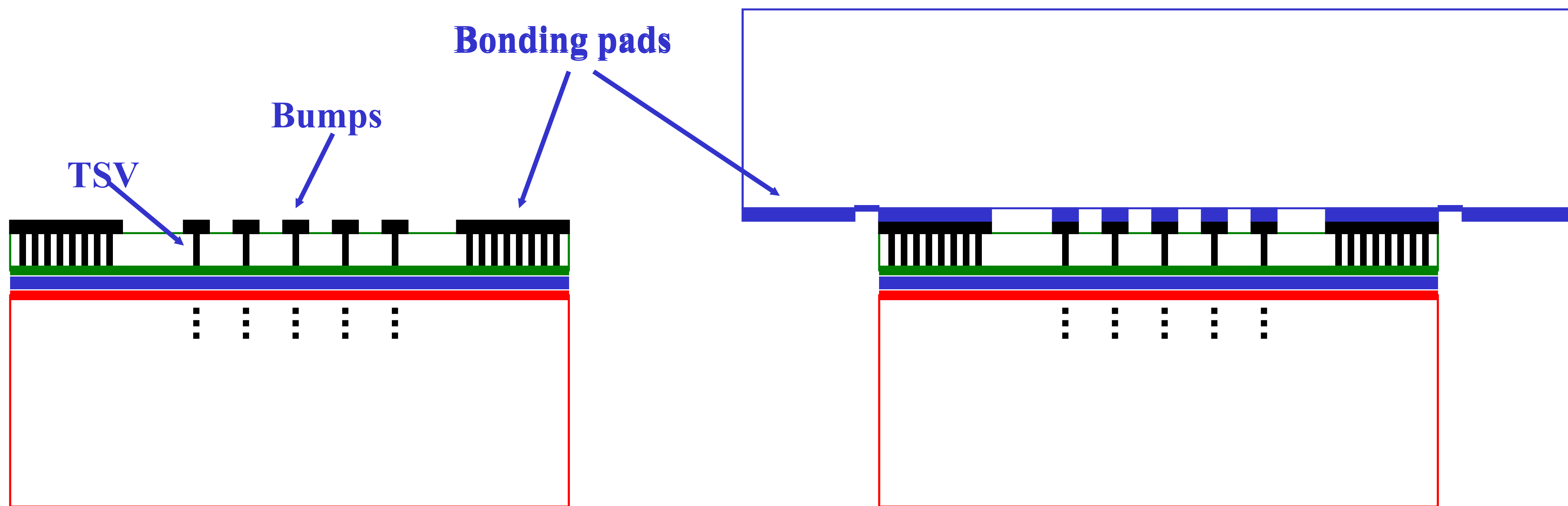
« Super-Contact → Via First »

Φ=1.2μm, h=6μm, min.pitch <3μm

C_p ~3fF, R_s<1Ω

Wojciech.Dulinski@ires.in2p3.fr

Our approach: Chartered 0.13 µm 2-tiers process USA-EU 3D-HEP Consortium (Fermilab, IN2P3, INFN…) + XFAB 0.6 PIN process



From Chartered (2 tiers)

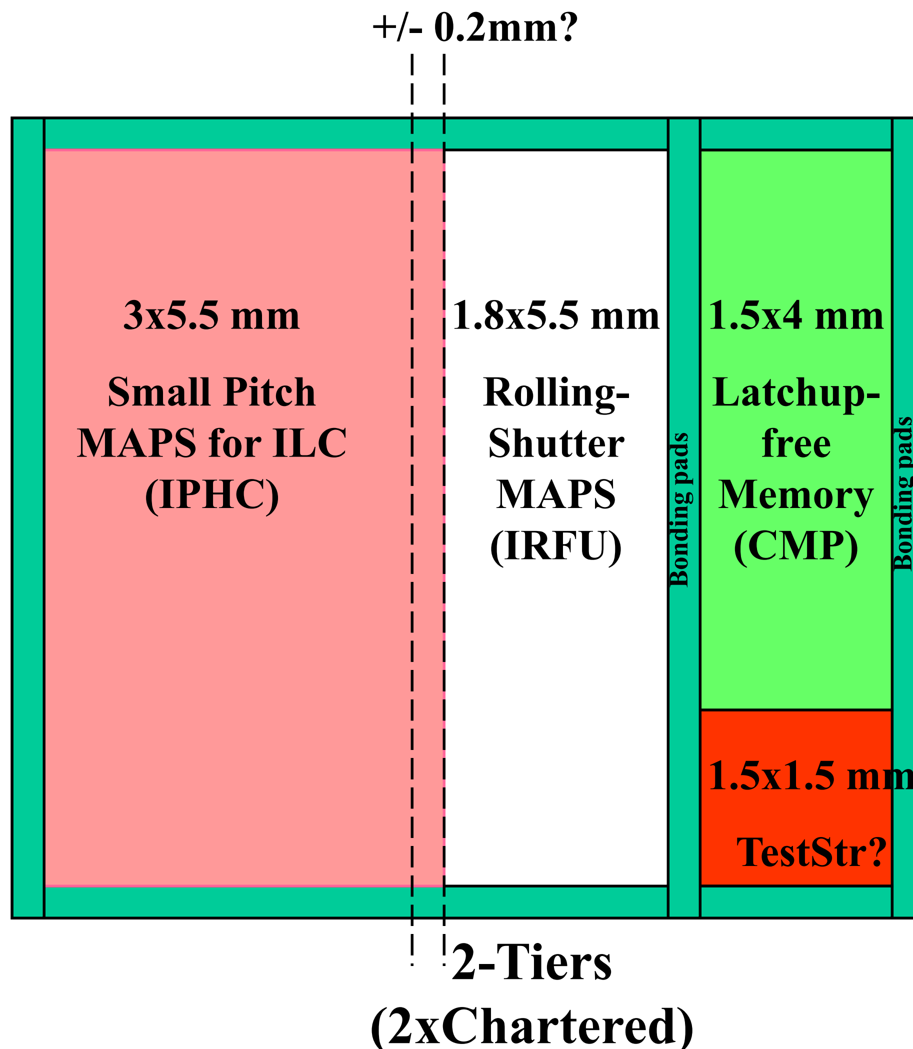
plus XFAB and Ziptronix (3 tiers)

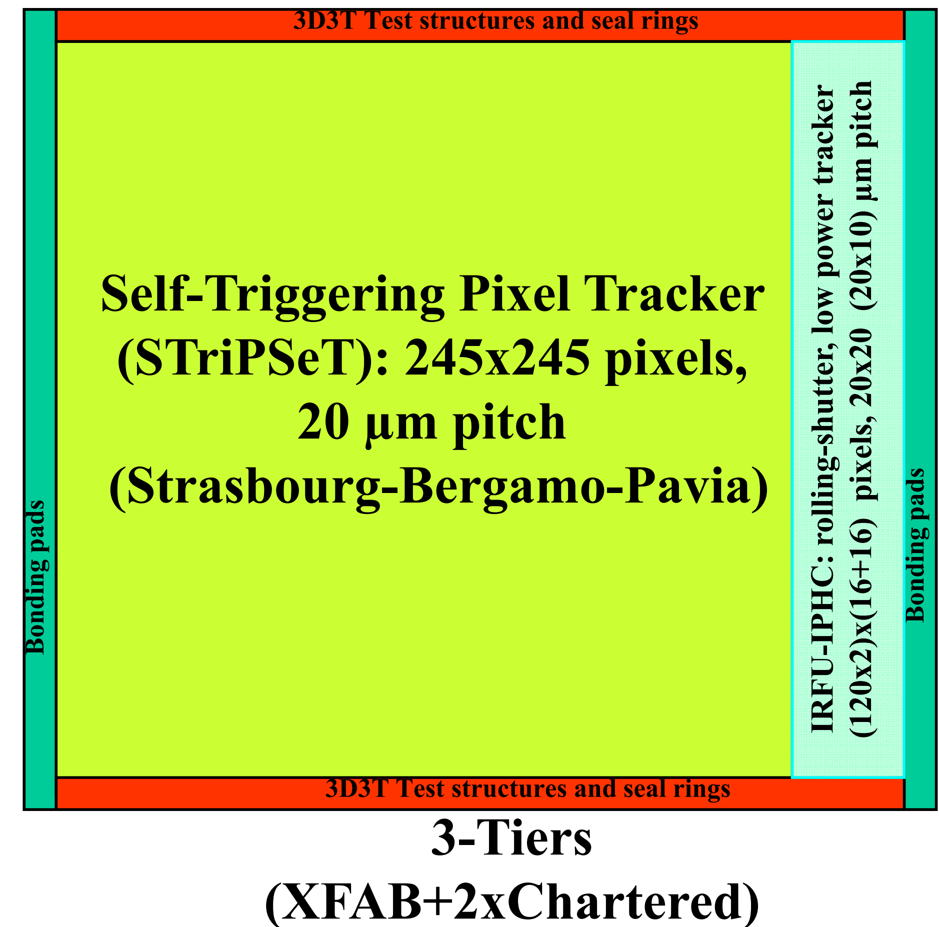
Wafer view at intermediate and after final stage (chip-to-XFAB wafer bonding)

Wojciech.Dulinski@ires.in2p3.fr

IPHC contribution to 2009 3D-Consortium submission: one sub-reticule for 2-Tiers and one sub-reticle for 3-Tiers, five sensor chips

Sub-reticle size: 6.3x5.5 mm^2





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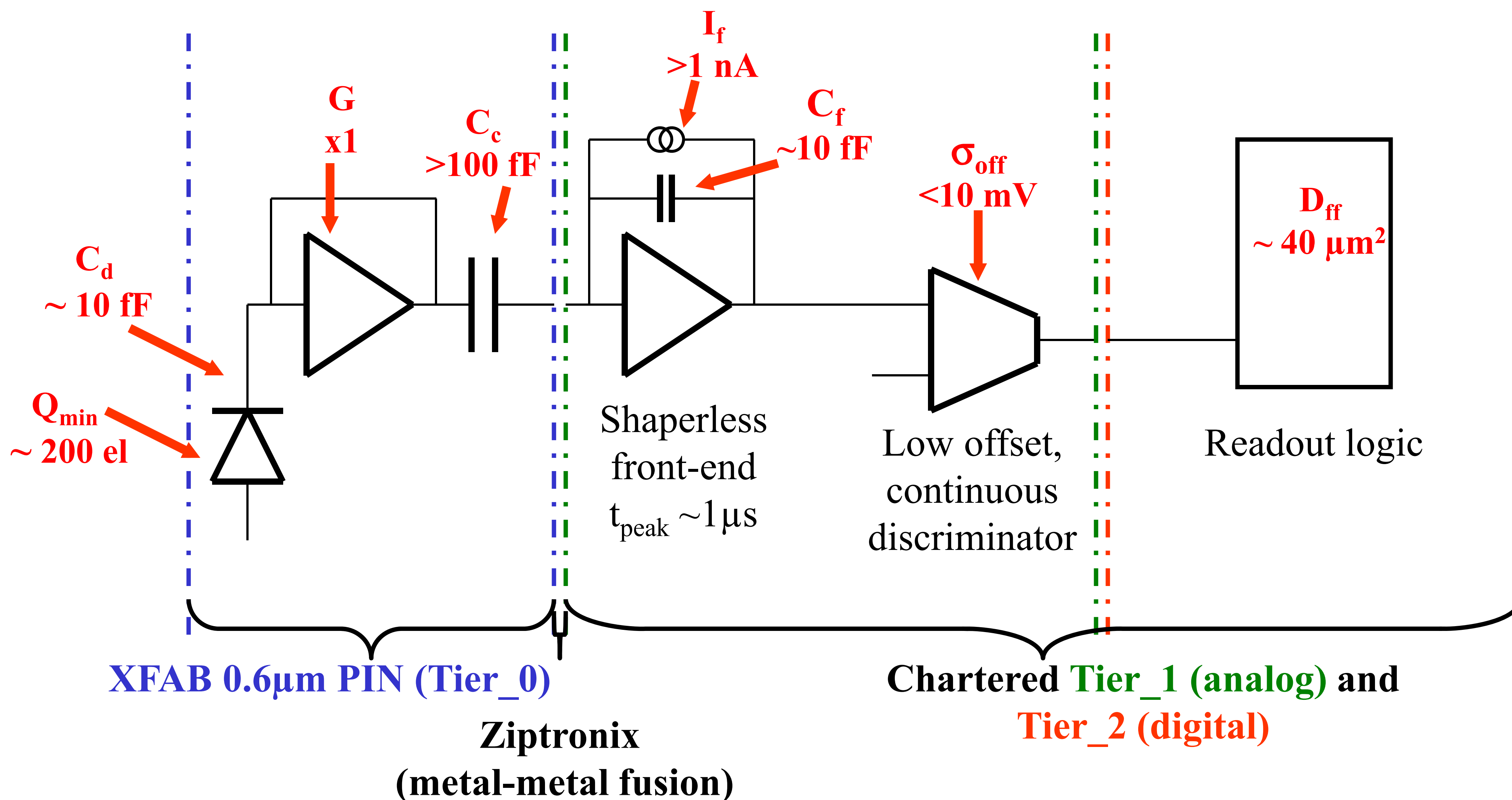
1. Self Triggering Pixel Strip-like Tracker (STriPSeT) Collaboration: Strasbourg-Bergamo-Pavia



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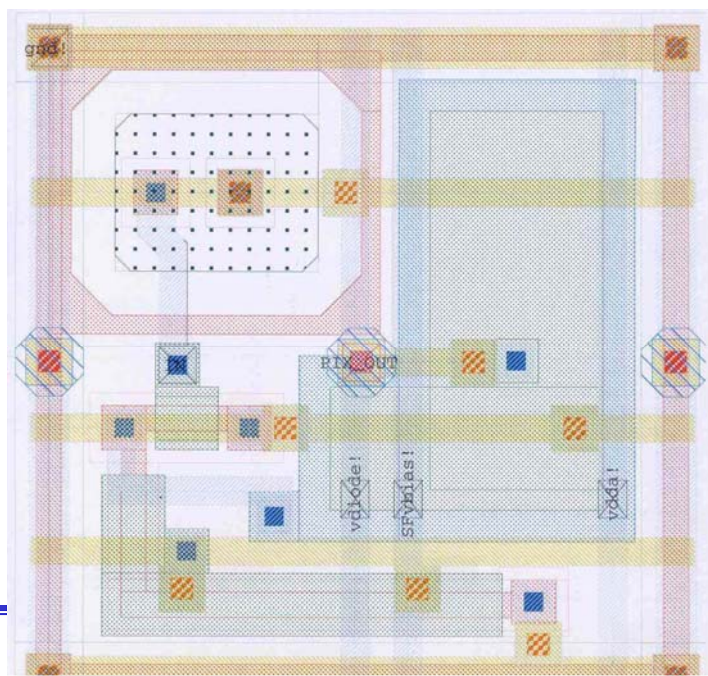
Principal arguments for use of XFAB-0.6

- fully depleted, 14 µm thick epitaxy
- for small pitch, charge contained in less than two pixels
- fast charge collection (~5ns) → should be radiation tolerant
- sufficient (rather good) S/N ratio defined by the first stage
- "charge amplification" (~x100) by capacitive coupling to the second stage
- first experimental results from our first pixel sensor in this process (Mimosa25) very promising!



20x20 µm pixel layout in XFAB-06.
Version: SF+CAPA (150 fF)

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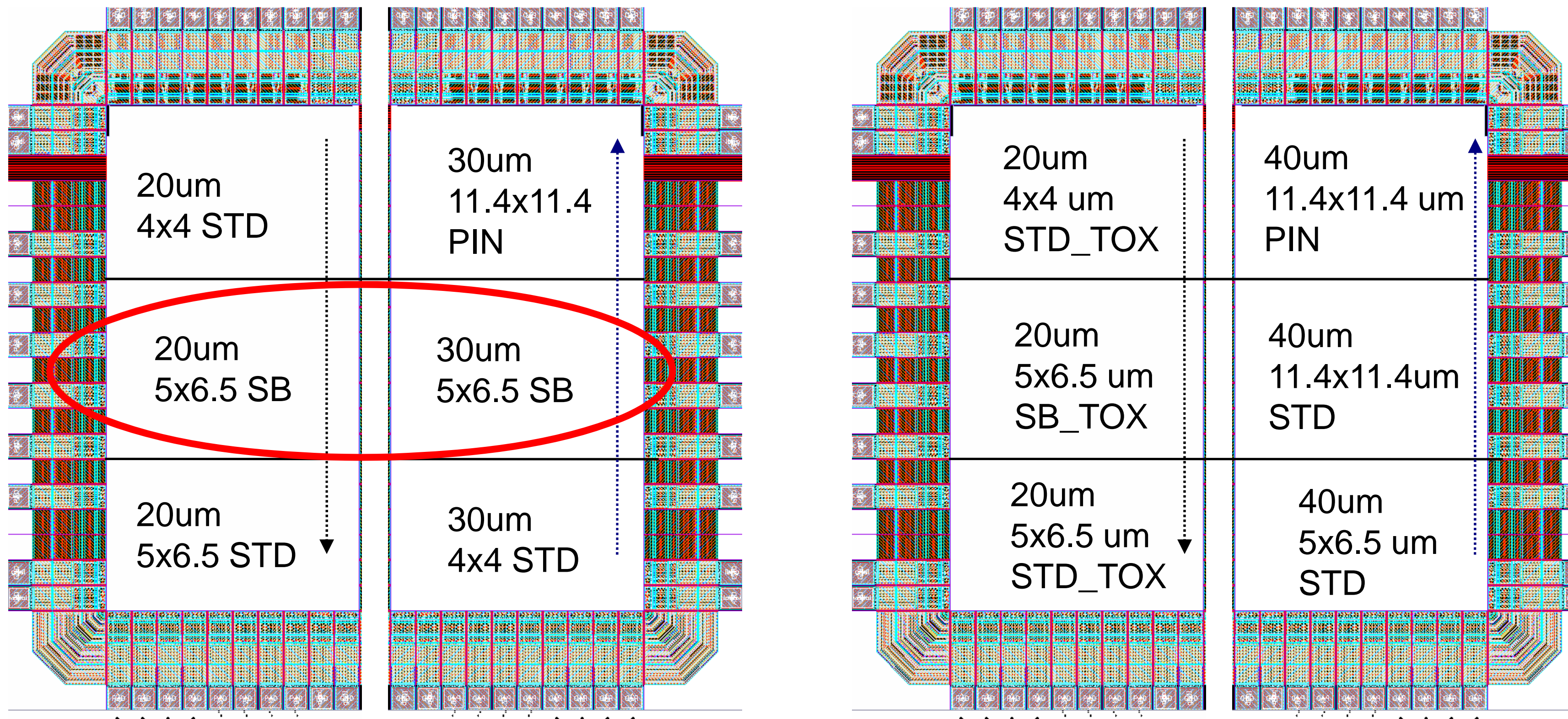
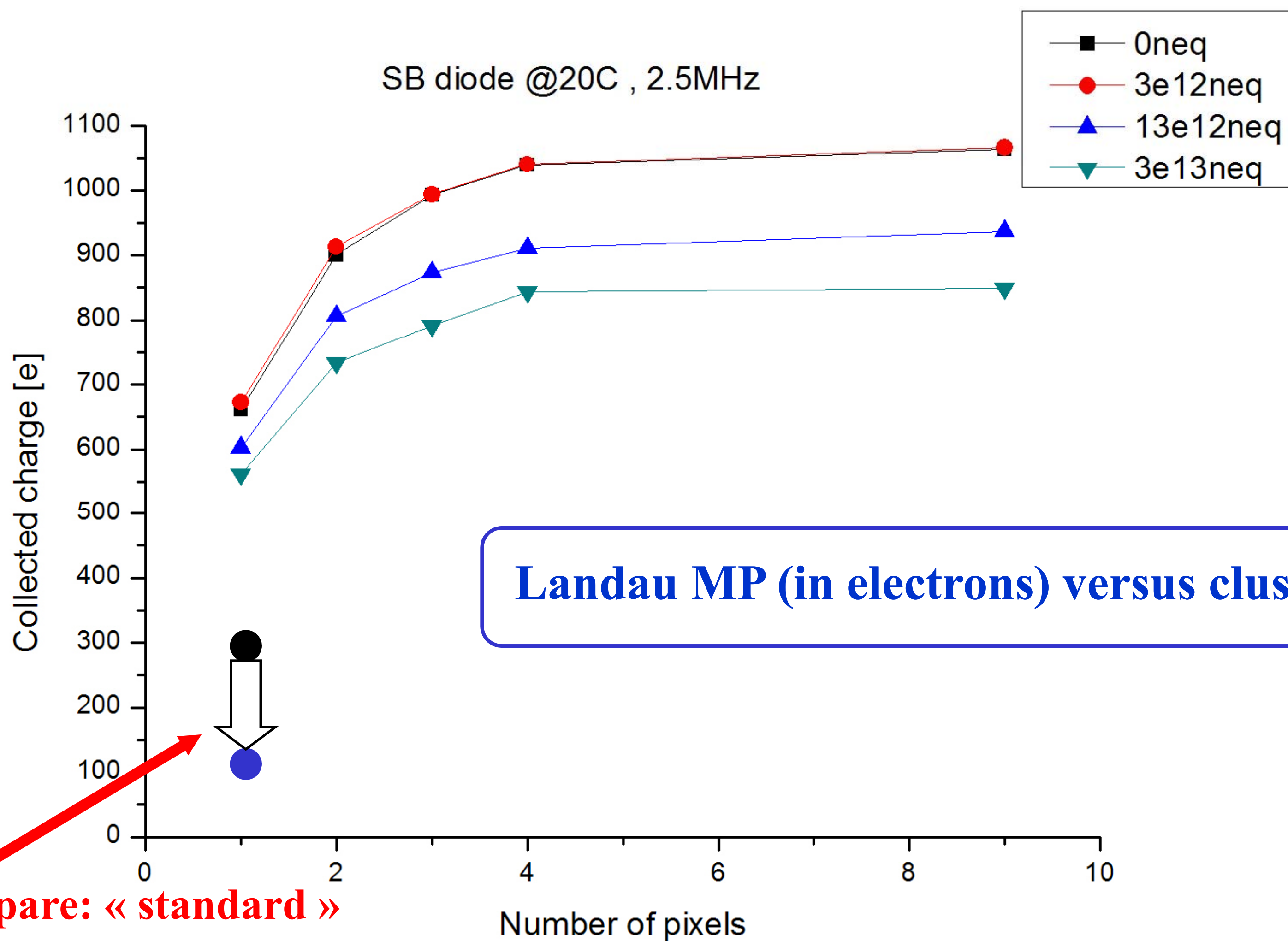
Mimosa-25 prototypes (XFAB-0.6 PIN, Aug-Dec 2008)



2 submitted chips

Wojciech.Dulinski@ires.in2p3.fr

Mimosa-25 on fully depleted epi substrate (XFAB): first tests results (Ru beta) 20 µm pitch, self-bias diode@4.5V before and after neutron irradiation



Landau MP (in electrons) versus cluster size

To compare: « standard » (non-depleted epi substrate) before and after 10^{13} n/cm^2

Wojciech.Dulinski@ires.in2p3.fr

Principal arguments for “shaperless front-end”

- simple (surface efficient?) but very satisfactory approach, in particular when minimum signal charge is of few thousand electrons (after “charge amplification”)

- shaping time of ~1 µs very convenient: good time resolution, insensitivity to the irradiation induced leakage current

- possible implementation of Time-over-Threshold ADC in the future…

- minimum signal at the entrance of comparator ~100 mV, so threshold dispersions of few mV tolerable

- structure already studied in details by Pavia&Bergamo group (expertise from several prototypes in another 0.13 µm process)

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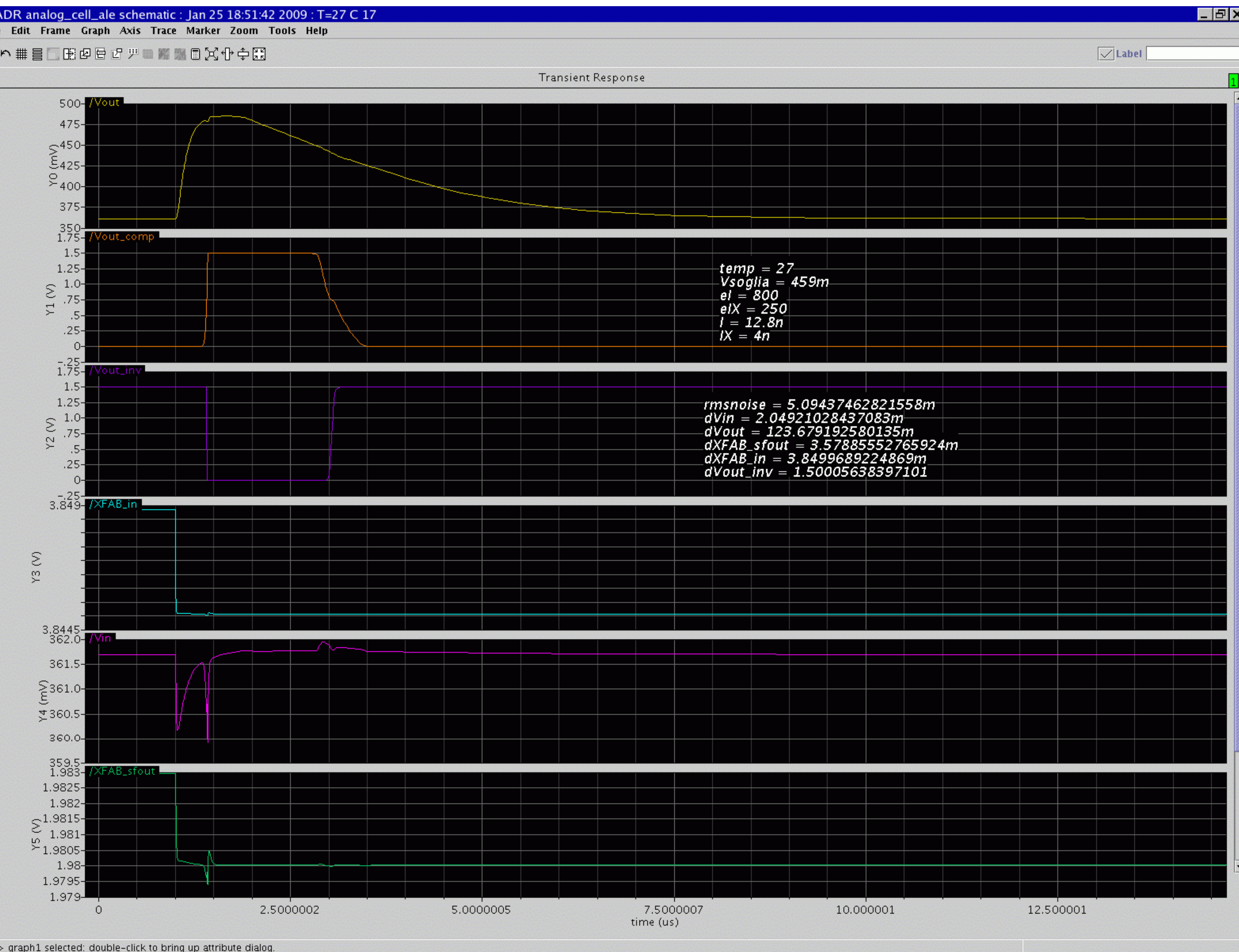
Combined simulation XFAB+Charterer (SF+ShaperlessFE)



Simulation:

pulse corresponding to 200 electrons injected into XFAB diode

Results:

Gain: ~500µV/el

ENC ~10 electrons!

Extra power from SF: <1µW/pixel

IF this is correct, we should expect: S/Landau>40

and

$Cut_{99\%eff}$/Noise>10

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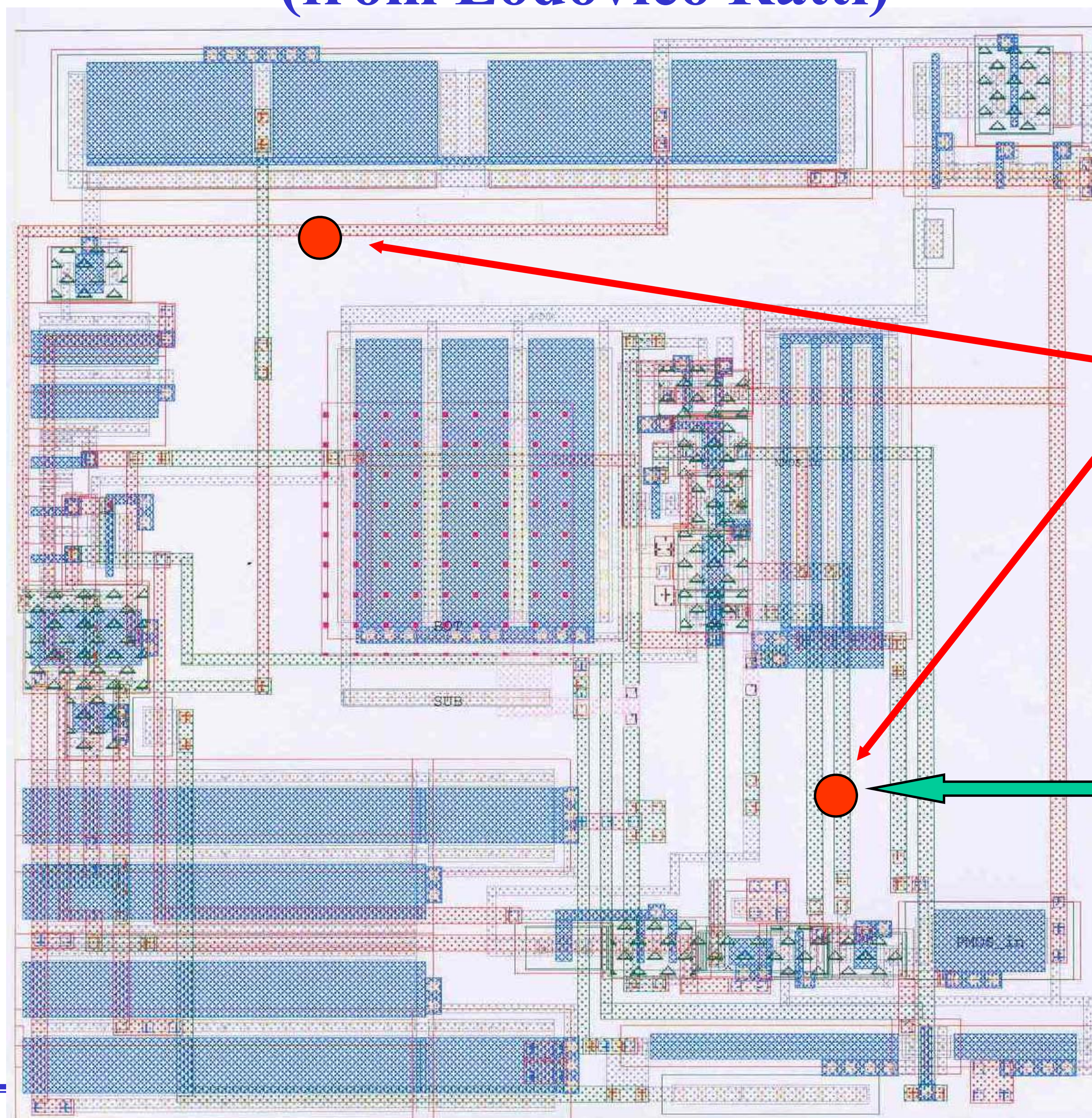
Self Triggering Pixel Strip-like Tracker: analog pixel (SFE) layout (from Lodovico Ratti)



SuperVias (Input and GND)

Input

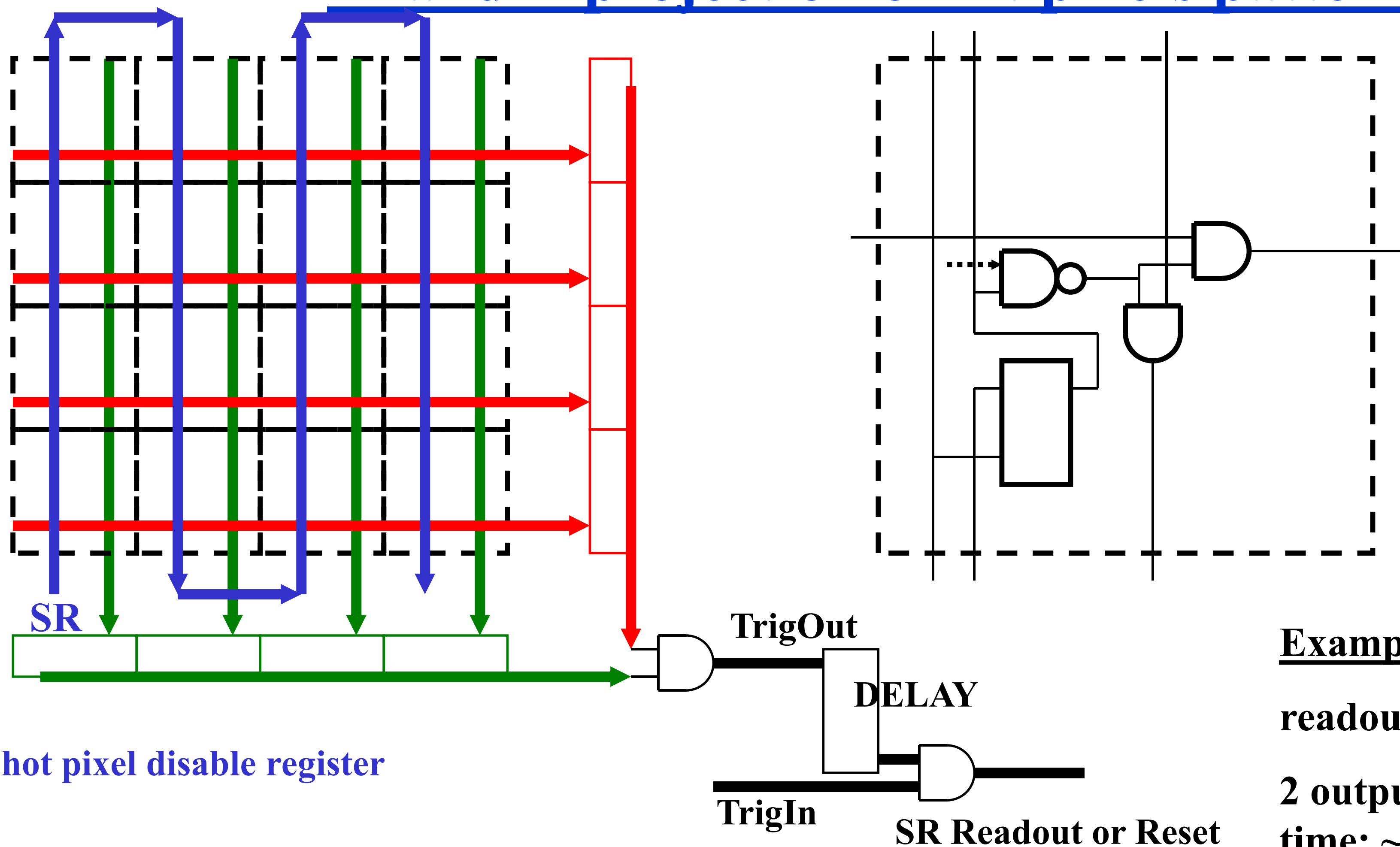
Principal arguments for “only digital” Tier_2

- excellent separation of analog and digital (no common substrate, several metal layers for blinding…)

- flexibility of the readout architecture, possible use of “front-line” CMOS process (<60nm) for this layer to increase complexity of digital processing at lower power budget

Wojciech.Dulinski@ires.in2p3.fr

STriPSeT: Data driven (self-triggering), sparsified binary readout. X and Y projection of hit pixels pattern



SR: hot pixel disable register

Example:

readout clock : 160 MHz

2 output lines ≡ Array readout time: ~2µs

Programmable Active Area (through pixel disable SR)

Readout compatible with existing IPHC-digital DAQ…

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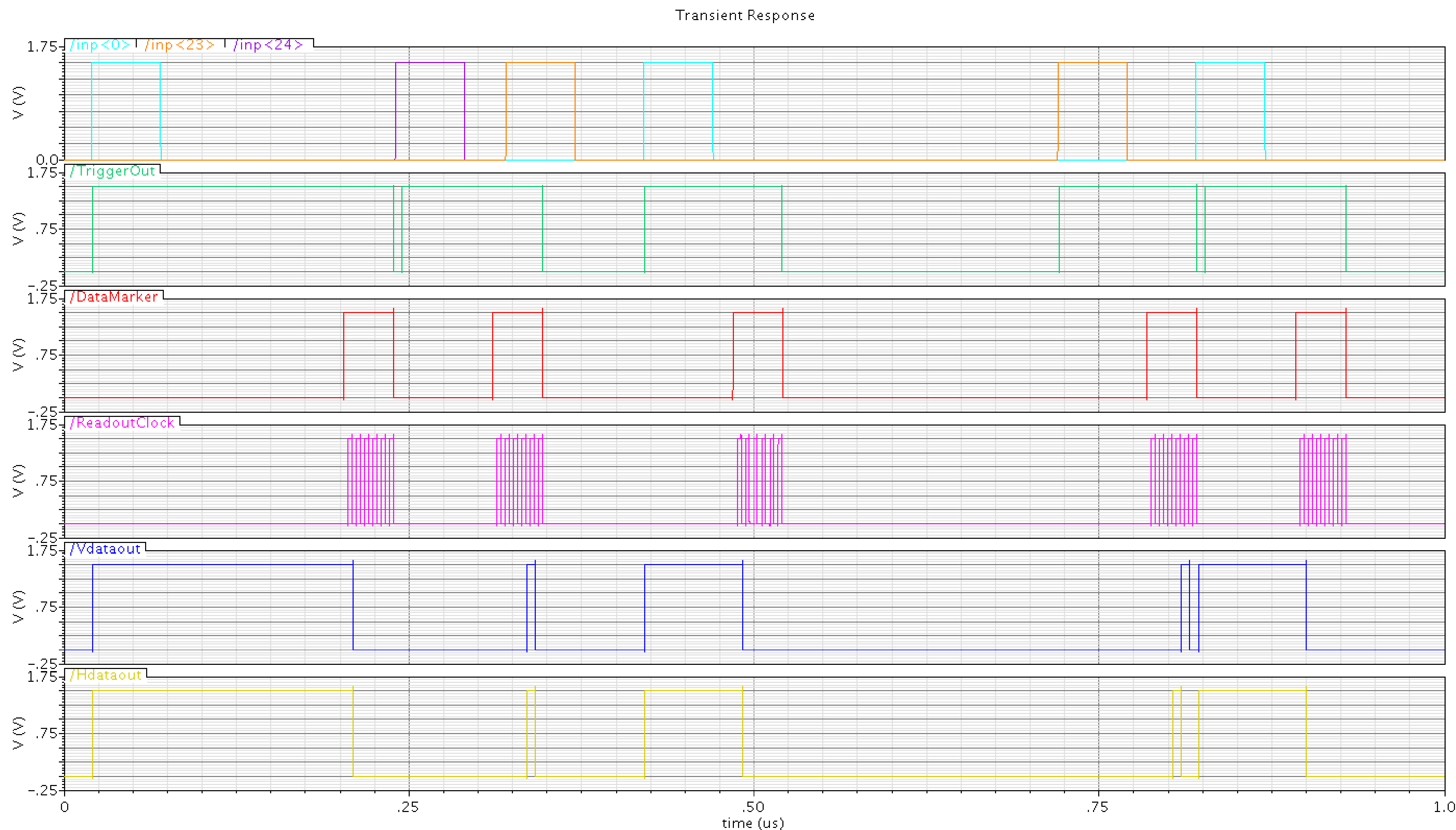
STriPSeT: example of SPICE simulation of 5x5 pixel array (parasitics corresponding to 250x250 pixels)

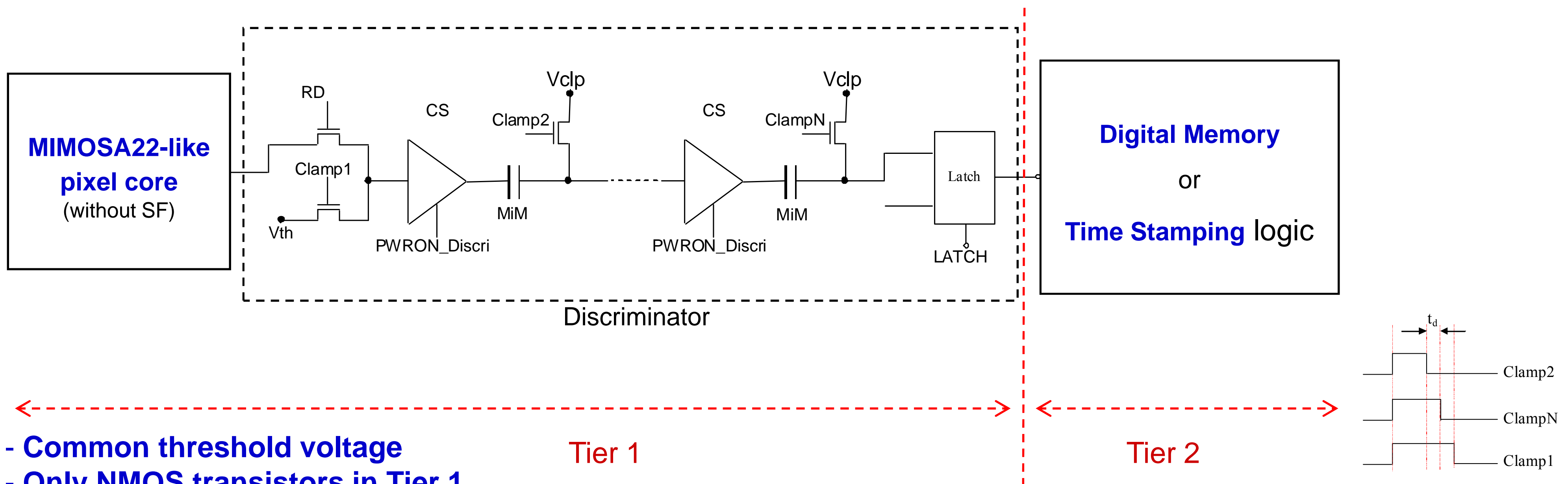


Data driven data flow, clock : 160 MHz. Total readout time of one event: ~2µs

Wojciech.Dulinski@ires.in2p3.fr

2. Rolling Shutter Mode MAPS: power efficient solution based on M26 approach for processing Collaboration: IRFU-IPHC

Pixel electronics



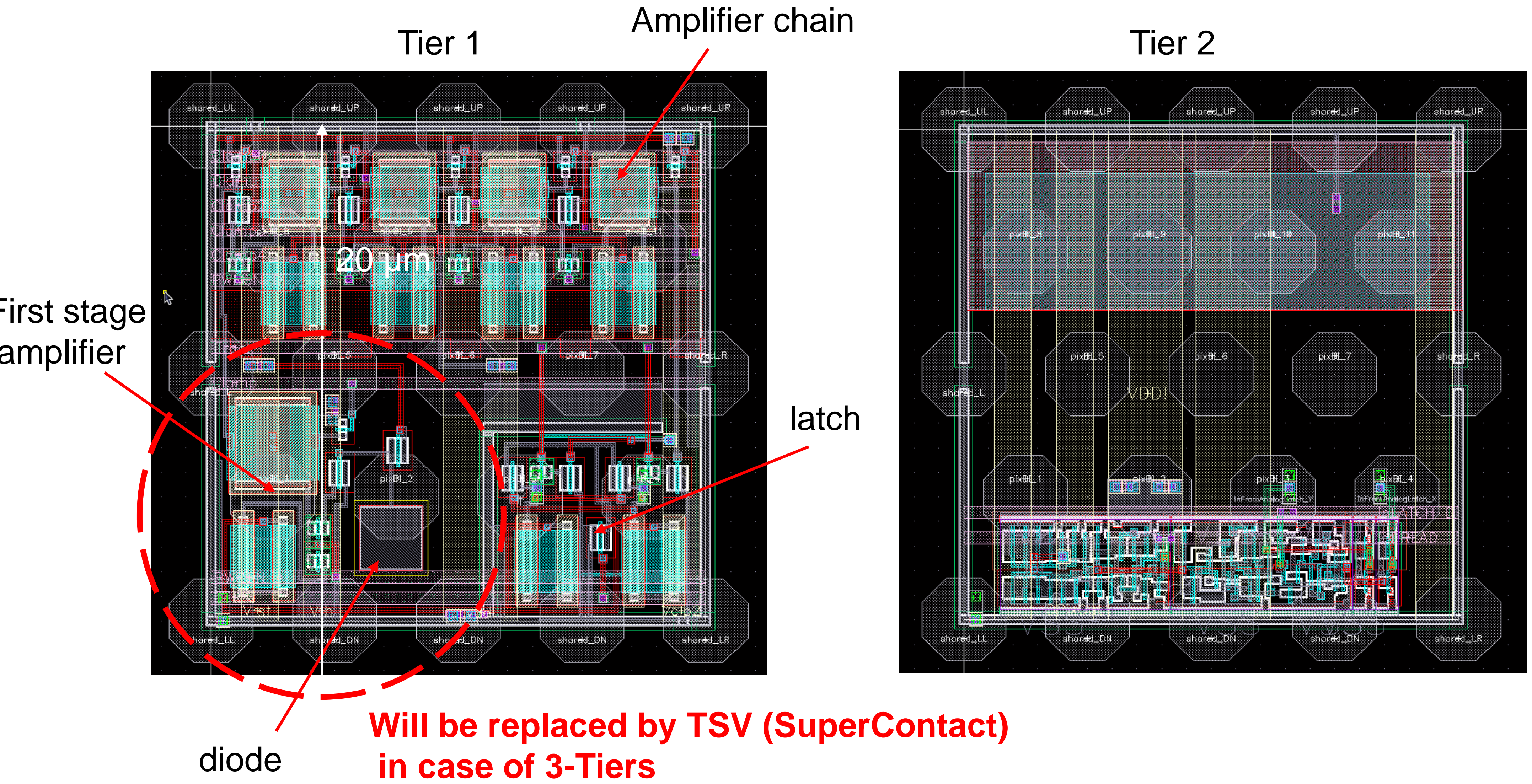
- Common threshold voltage
- Only NMOS transistors in Tier 1
- 20x20 µm pitch, 32x256 pixel array
- <u>Low power operation (rolling shutter)</u>

Example of power budget:

- 100 µW/pixel for 50ns processing
- To be compared with 500µW/pixel for 200 ns processing (Mimosa26)
- <u>Factor of 20 saving in analog power! This is due to 3D electronics…</u>

Wojciech.Dulinski@ires.in2p3.fr

Rolling Shutter Mode MAPS: analog and digital blocks. The analog is based on NMOS transistors only (from Yavuz Degerli)



Wojciech.Dulinski@ires.in2p3.fr

3-Tiers Project status and expected schedule

-Schematics and simulation finished

-Layout of most of building blocs finished

- Assembling: ~March

-Submission (Chartered): ~April

-Submission (XFAB): ~May

-Reception of wafers: ~July

-2 Tiers testing: ~July/August

-XFAB Tier bonding (at Ziptronix): September

-Final tests (and beam tests): October/November

My personal conclusion: a new class of "monolithic hybrid" sensors is emerging.
A lot of work, but a lot of fan as well…

Wojciech.Dulinski@ires.in2p3.fr

STriPSeT as part of a beam telescope

-Sensitive area: 5x5 sq.mm → not very big, but fit well Mimosa18 (high precision tracker)

-Expected (binary) resolution: ~5 µm → not very attractive

But:

-Time resolution of ~1 µs

- Can accept up to ~100 kHz particle rate

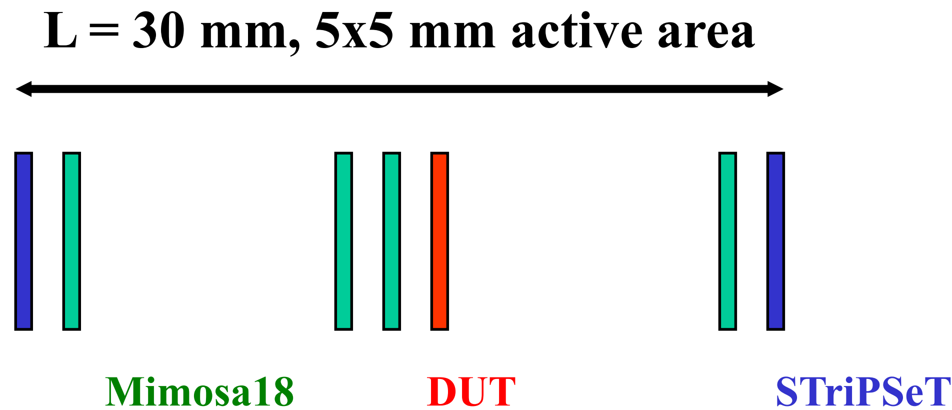
-Excellent noise performance: cut on S/N ratio of 10 should still be compatible with ~100% efficiency → very low fake counting rate

- Programmable pattern of active area

→ Good candidate for a (tracking) trigger layer?

Wojciech.Dulinski@ires.in2p3.fr

New step in telescope miniaturization, still increasing the speed and keeping high precision…



Thanks for your attention!