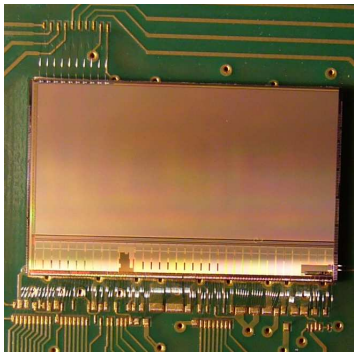
EUDET JRA1 Meeting, Strasbourg March 2009
Mimosa 26 Characterization Tools Development Status



Mimosa 26

OUTLINE

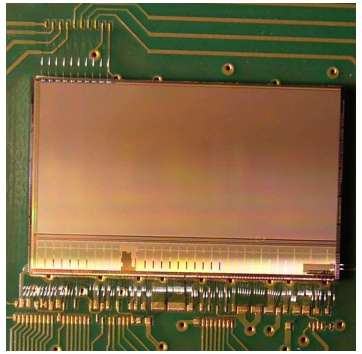
- **Hardware : PCB Design & Test** — W.Dulinski & M.Specht
- **Slow control : JTAG** — K.Jaaskelainen
- **DAQ System : Analogue & Digital** — M.Specht & G.Claus
- **Analysis software :**
  - Discriminators — M.Goffe & M.Gélin (IRFU - CEA)
  - Zero suppression — G.Doziere
- **First results …**

Mimosa 26 Steering and Readout

Mimosa 26 ?

- **Matrix of 648 k pixels : 576 lines x 1152 col – 13,7 mm x 21,5 mm – 18 µm pitch - 115,2 µs integration time**
  - **Normal digital data stream after Zero Suppression (ZS)**
- **Testability**
  - **Analogue Test data stream for pixels characterization (8 columns / 1152)**
  - **Discriminators Test data stream (before ZS) for discriminators & pixels characterization**

Steering



- **Configuration (operating modes, bias etc …) by JTAG slow control**
- **Main clock 80 MHz**
- **Start signal to synchronize multiple Mimosa 26**

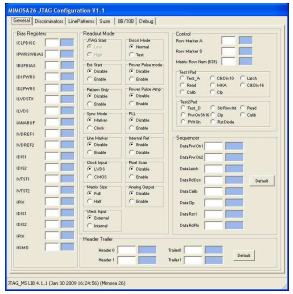
Readout

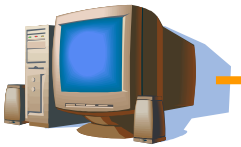
- **Normal ZS output** – **Full memory : 2 Outputs at 80 MHz / Half memory : 1 x 80 MHz or 2 x 40 Mhz**
- **Discriminators + Pixels test output** – **2 Digital outputs at 10 MHz**
- **Pixels test analogue output** – **8 Analogue outputs at 10 MHz**

Equipments Required to Test Mimosa 26

What we need to test / characterize Mimosa 26 ?

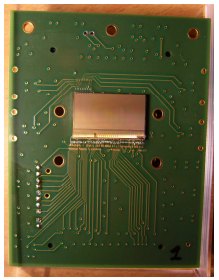
2 – Slow Control (JTAG) for Mimosa 26 Configuration



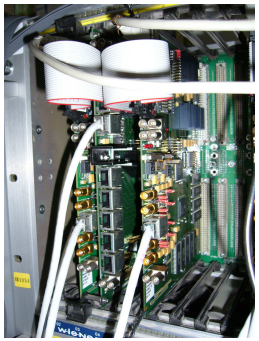


JTAG via PC // Port

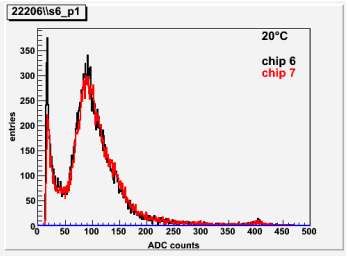
1 – PCB for Mimosa 26 Proximity & Auxiliary boards



3 – Analogue DAQ for Pixels Test



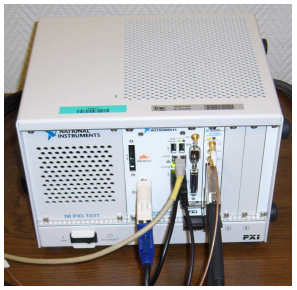
5 – Analysis software

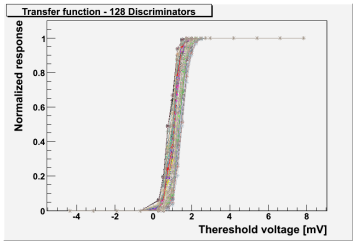


Fe^{55} charge collection

4 – Digital DAQ

- **Normal ZS output**
- **Discriminators + Pixel Test**





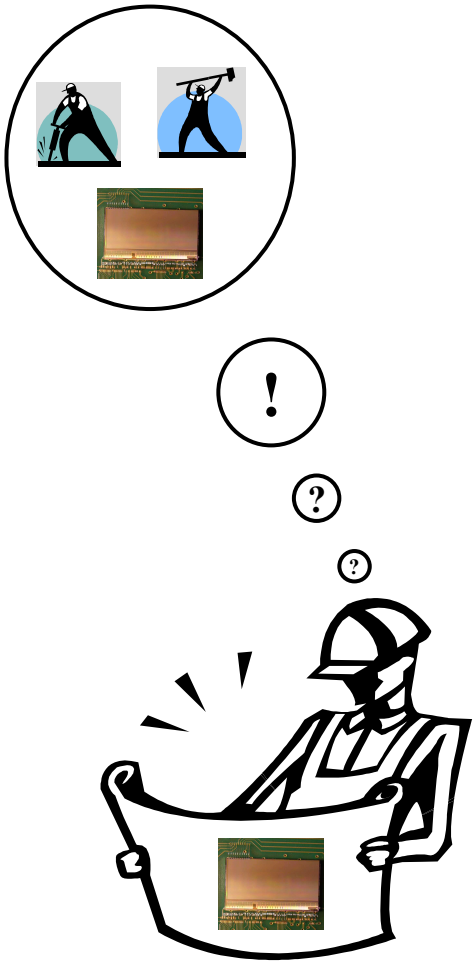
Discriminators transfer functions

We need …

1. PCB on which Mimosa 26 is bonded & Signals bufferization boards
2. Slow control to configure Mimosa 26
3. Analogue DAQ for pixels characterization
4. Digital DAQ for normal ZS output & discriminators characterization
5. Analysis software

Development of MAPS Test Tools

Constraints / Challenge



- New MAPS Design & Test Tools Development Are Running in Parallel !
  - No MAPS documentation available at beginning of test tools development … ☹
  - Final MAPS documentation ready when test tools development is done … 😐
- We want quickly preliminary results when MAPS is back from foundry …
  - It's not the moment to debug MAPS Test Tools (PCB, DAQ, Software)
  - We want to debug MAPS … Not Test Tools

How to be ready when MAPS is back from foundry ?

- Documentation
  - Discussions → Intermediate notes … But risk of misunderstanding can't be 0
- How to check JTAG slow control ?
  - Emulation of Mimosa 26 JTAG controller via FPGA board
- How to check DAQ hardware & software ?
  - Emulation of Mimosa 26 readout with a pattern generator

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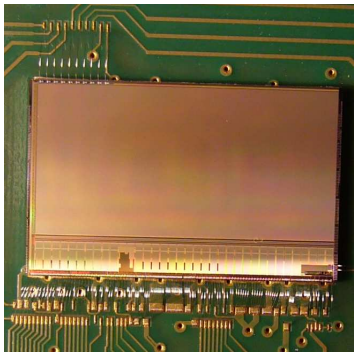

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Hardware : Mimosa 26 PCB

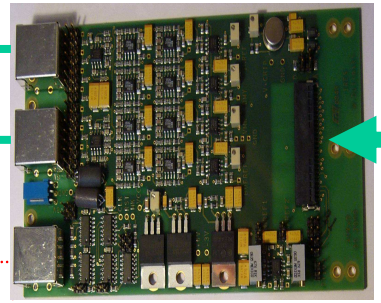
Analogue Data & Clock
To Analogue DAQ

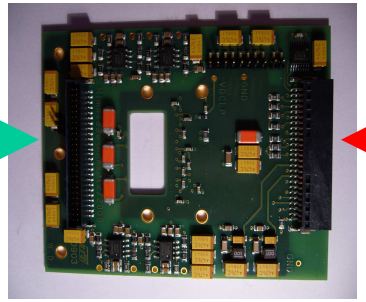
Boards for EUDET Telescope
compatible with mechanic

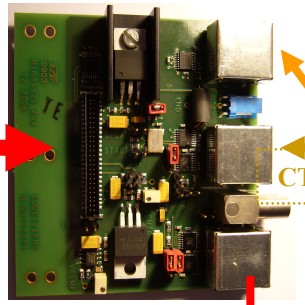
JTAG Interface Board
PC // Port ← → LVDS

A0 – A3

A4 – A7

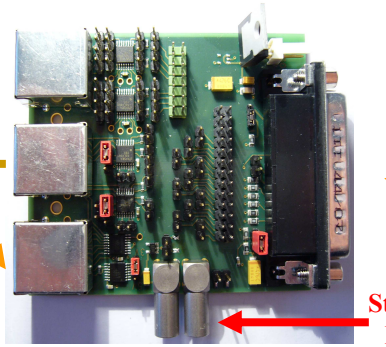






JTAG

CTRL



JTAG
From DAQ

Start & Speak
From DAQ

Sync - Clock

Digital Data – Sync – Clock : To Digital DAQ

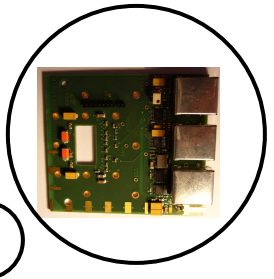
Analogue – 8 x Out
Auxiliary board

Mimosa 26
Proximity board

Digital
Auxiliary board

Analogue Test of Mimosa 26

Digital Test of Mimosa 26



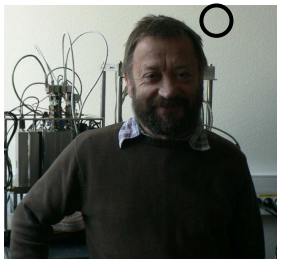
Four boards required to test Mimosa 26

- PCB development
- Boards assembly & Bonding by Micro-Technique Team
- Interface with micro-technique Team & Boards Testing

W.Dulinski

M.Imhoff – O.Clausse – C.Wabnitz – L.Ankenmann

M.Specht



Special Telescope Board

- *Proximity & Aux board*
- *Direct LVDS In/Out*
- *Require new mechanic*

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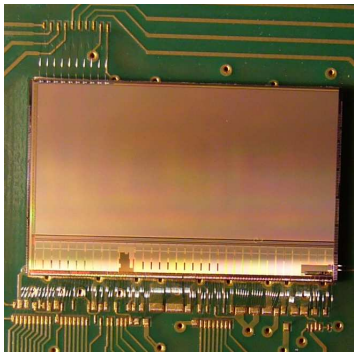

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Slow control : Mimosa 26 JTAG

A Windows application to Control the ~ 50 Configuration Parameters of Mimosa 26

- Uses JTAG slow control via PC parallel port
  - Software implementation of JTAG protocol (1997) – Upgrade of GUI & MAPS library for each new MAPS
- The whole chain has been checked by emulating Mimosa 26 JTAG controller with a XILINX Virtex 4
  - ~ 1 Month of development & test
- A COM interface allows to control JTAG application by a third party software
  - JTAG can be controlled by DAQ software

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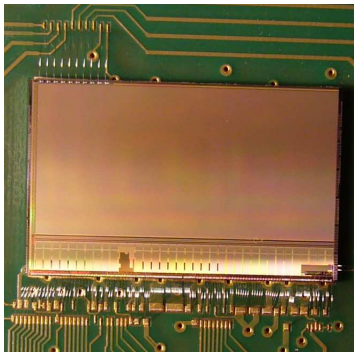

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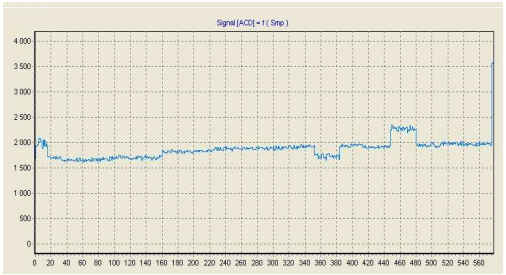
Analogue DAQ : Requirements

What we need ?

- Acquire eight output at 10 MHz
- On-line monitoring of raw data and CDS
- Store data on disk for off-line analysis

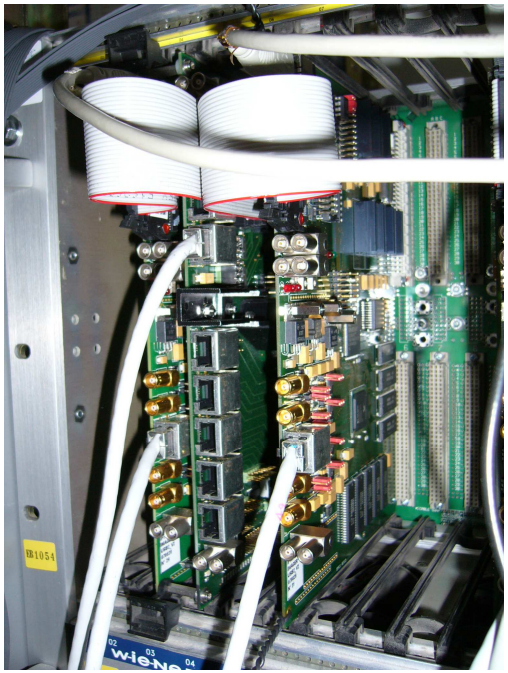
Monitoring of one frame



Development based on our “old” USB DAQ

- Upgrade of Mimosa 22 DAQ done for Phase 1 (~ 2 Months development + tests)
- The application done for Phase 1 can be also be used for Mimosa 26

USB DAQ : 2 Boards = 8 Inputs

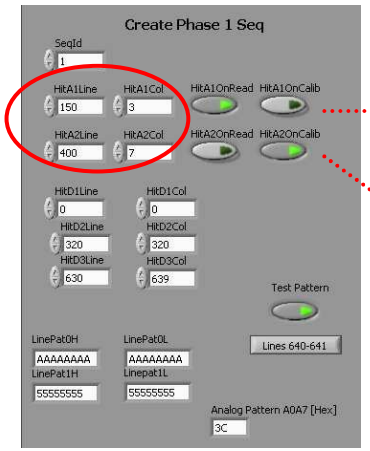


DAQ has been checked without Mimosa 26

- Mimosa 26 has been emulated with a pattern generator
- A software has been developed to easily emulate hits
  - GUI written under Labview
  - Conversion from Hits / Vectors table with a home made C framework

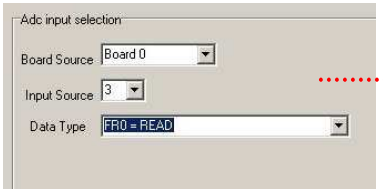
Analogue DAQ : System test

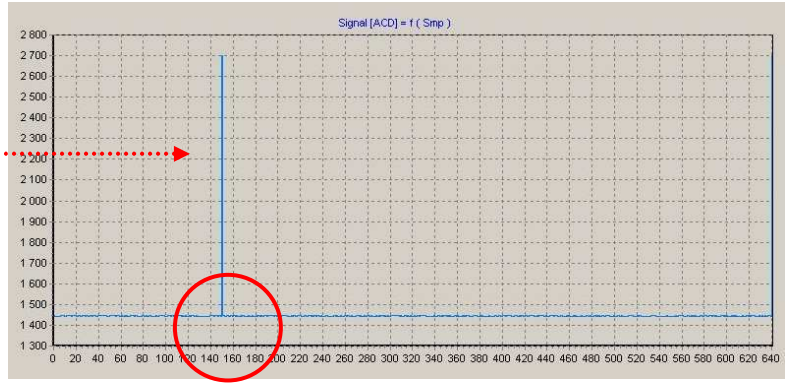
Emulator control
-Hit on read frame : line 150, column 3
-Hit on calib frame : line 400, column 7



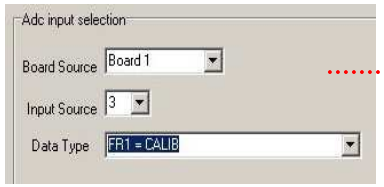
DAQ on-line monitoring

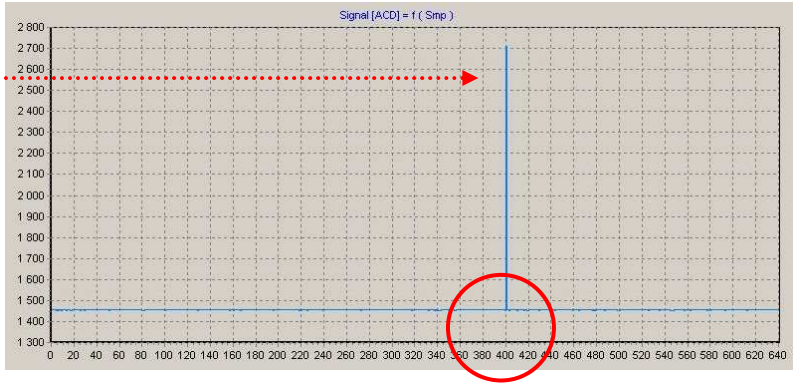
First analog hit :
Line 150 , Column 3, Read



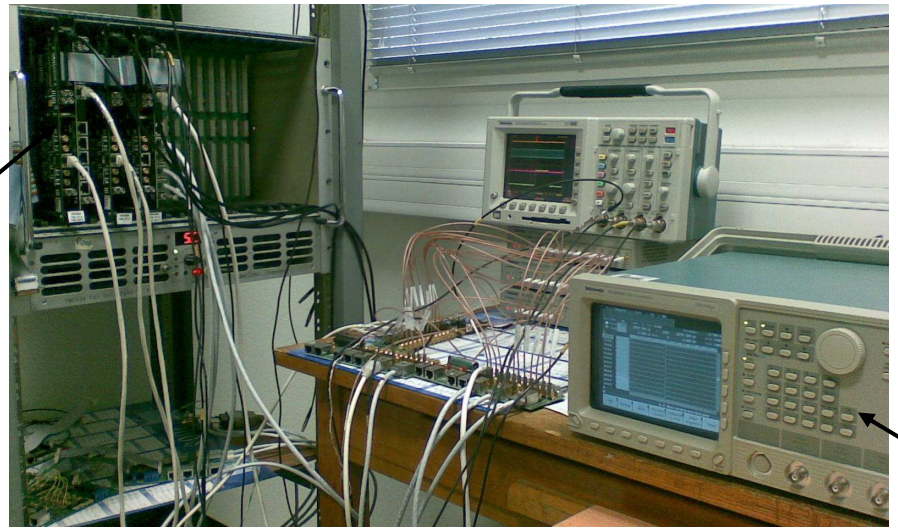


Second analog hit:
Line 400, Column 7, Calib





USB DAQ



Pattern Generator
Mimosa 26 Emulation

Software upgrade of DAQ has been checked
- **Hits emulation with pattern generator**
- **Hits position checked on monitoring**

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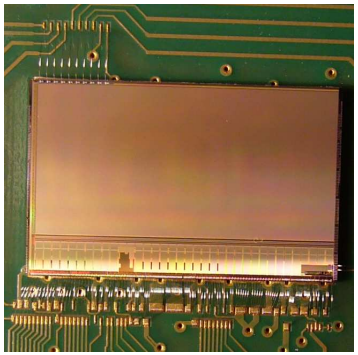

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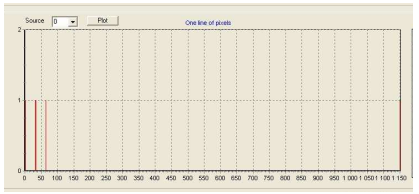
Digital DAQ : Requirements

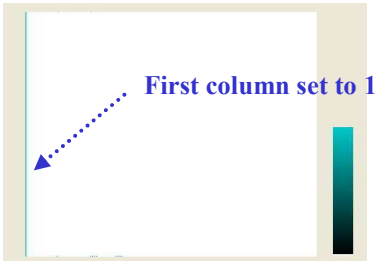
What we need ?

- Acquire two digital synchronous serial link at 80 MHz
- Check data integrity on the serial links
- On-line monitoring of discriminators state
- Plot of matrix after on chip data reduction
- Store data on disk for off-line analysis

One line = 1152 discriminators

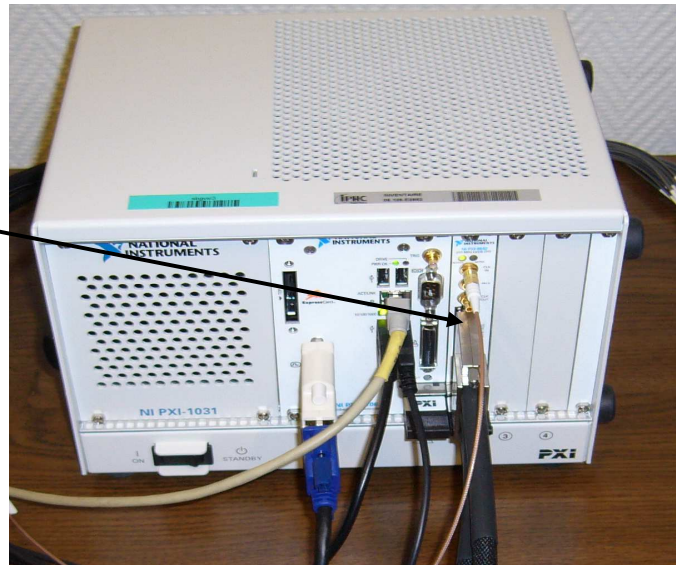


1/4 Matrix = 288 column x 576 lines



Development based on commercial PXI hardware from NI

- Acquisition board PXI 6562
  - 16 inputs – 200 MHz (SDR) / 400 MHz (DDR)
  - On board memory for 16 M Samples = 1820 frames
- How to read Mimosa 26 with a commercial board ?
  - Store a bunch of frame raw data in board memory
  - Do the deserialization / data formatting by on-line software
- DAQ checked by emulating Mimosa 26 with a pattern generator



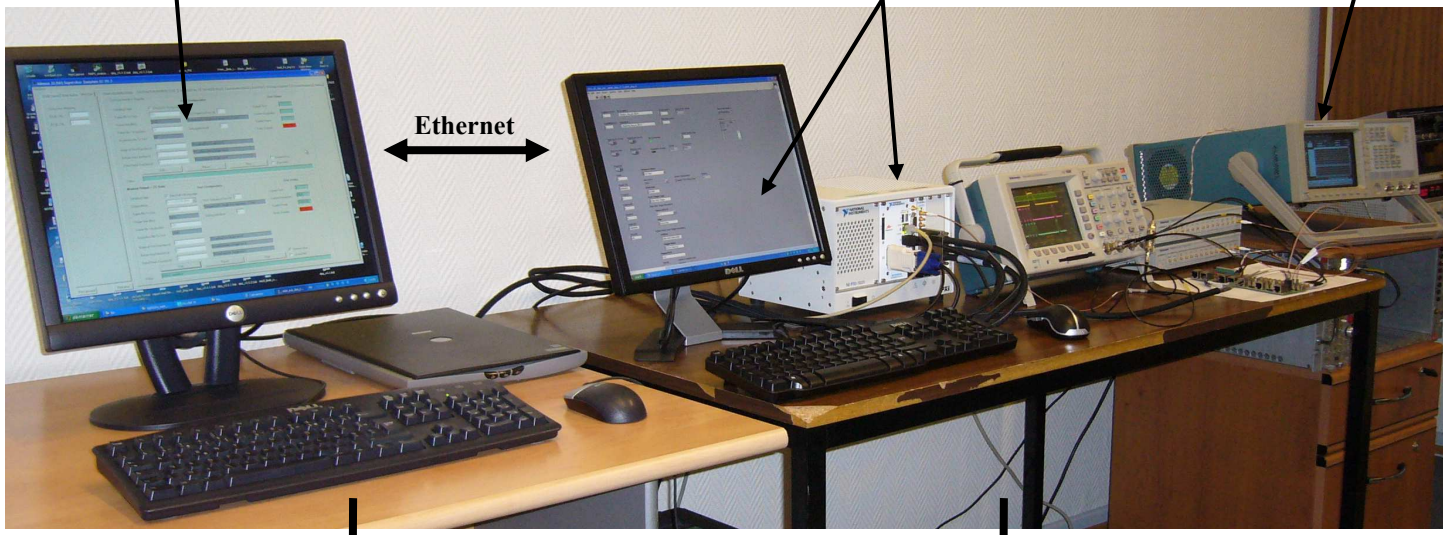
Digital DAQ : System Architecture

Client / Server : PXI Crate data server + Supervisor PC data client

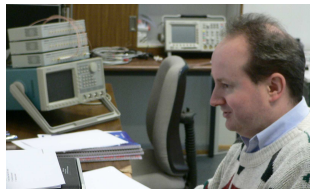
Supervisor
- PC Windows

PXI DAQ
- Digital acquistion board
- CPU board & HD
- Keyboard and monitor

Mi26 emulation with pattern generator
- 2 outputs 80 MHz / 8 Mhz
- ~ 10 k bits / frame



Function	• Graphical user interface (GUI)	• Acquisition board control
	• Monitoring & Analyse	• Data deserialisation
	• Data transfer via Ethernet (Client)	• Data transfer via Ethernet (Server)
Software / Language	• GUI → C++ Builder Borland	• GUI & NI Board driver → Labview
	• Processing → C & C++	• Deserialisation & Ethernet → C



Gilles CLAUS
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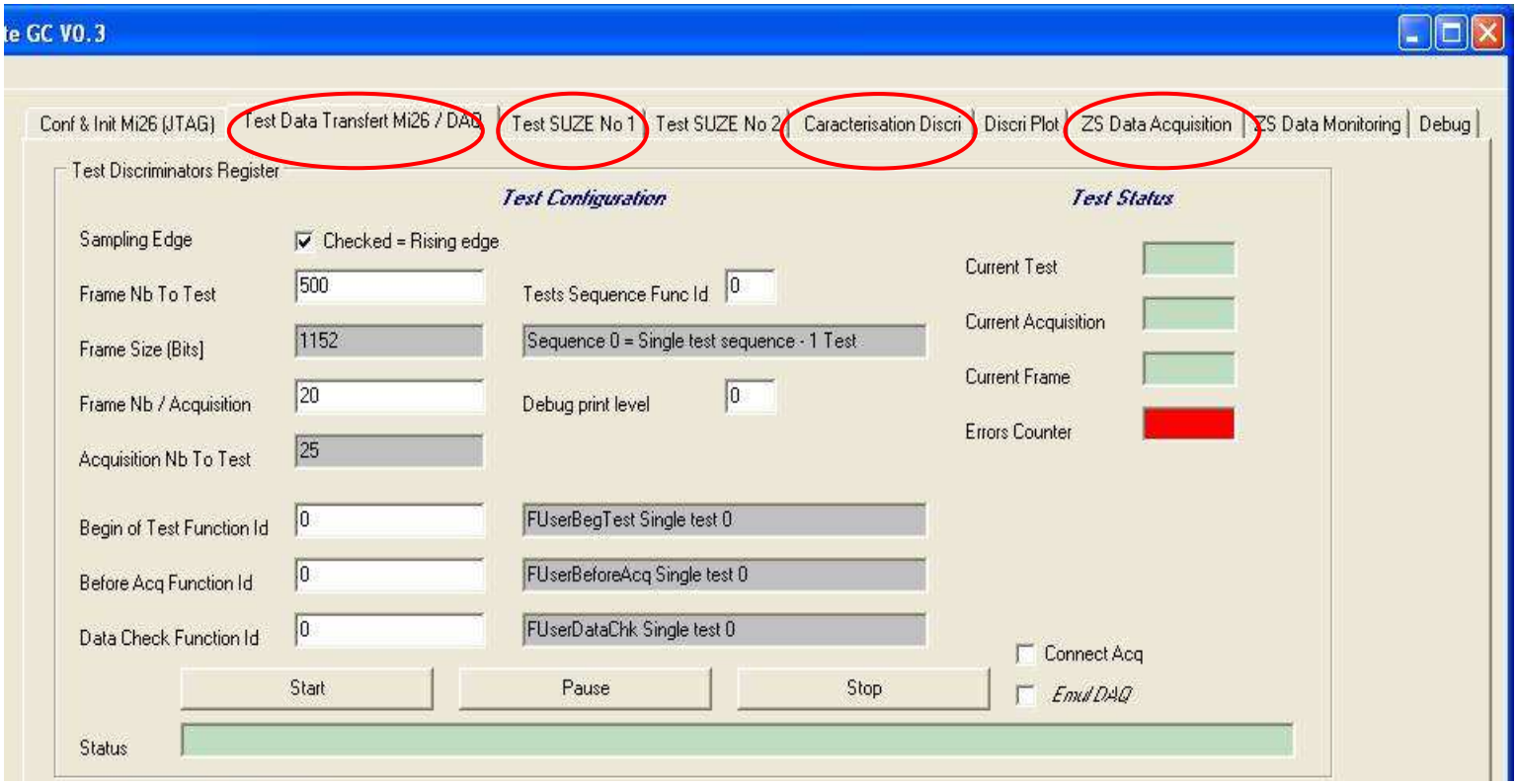
Digital DAQ : Supervisor software overview

Supervisor application : 4 Softwares in 1



Four main functions

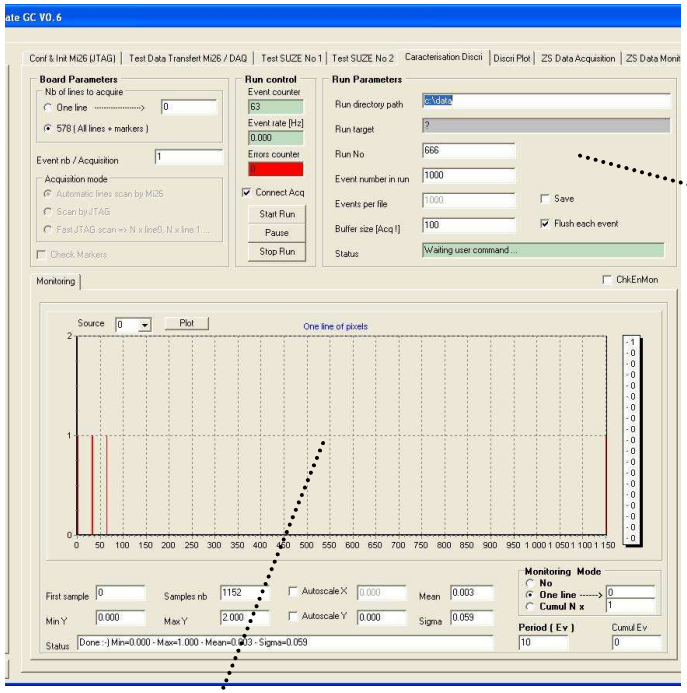
- Data transfer check Mi 26 / DAQ (Mi26 – HW – DAQ)
- DAQ Framework for Zero Suppression part of Mimosa 26 testing
- Discriminators characterization → on-line monitoring
- Normal output (ZS) data acquisition (Not ready – But not required for first tests)

➢ *Mimosa 26 has many operating modes … DAQ Client / Server architecture Development & Tests ~ 3 Months*

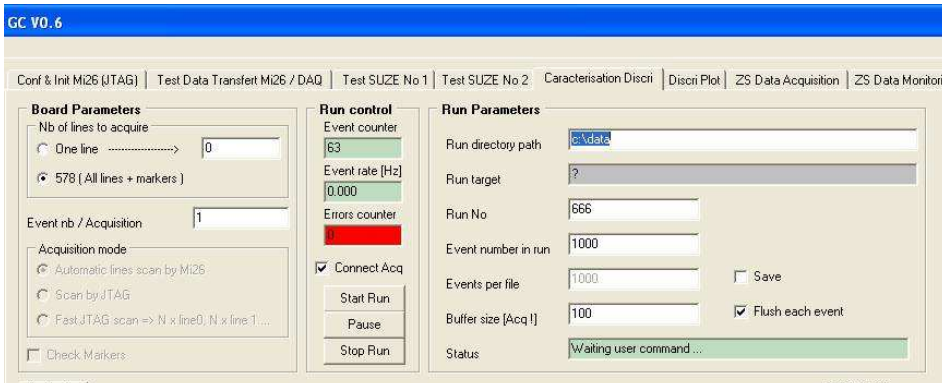
Digital DAQ : Digital outputs acquisition

Examples of DAQ Supervisor Monitoring : Discriminators

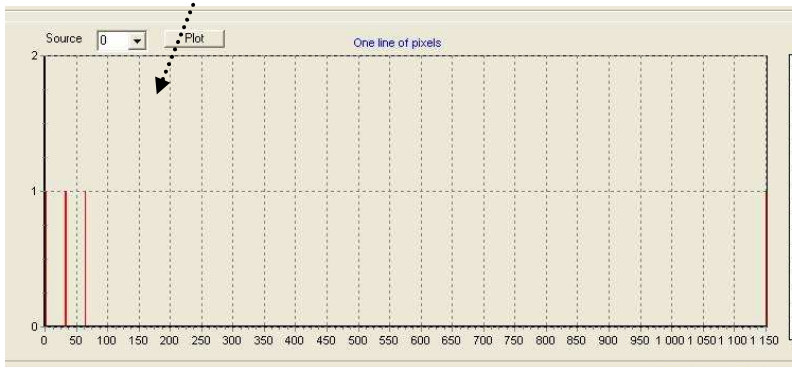
Discriminators characterization Panel



Run Control

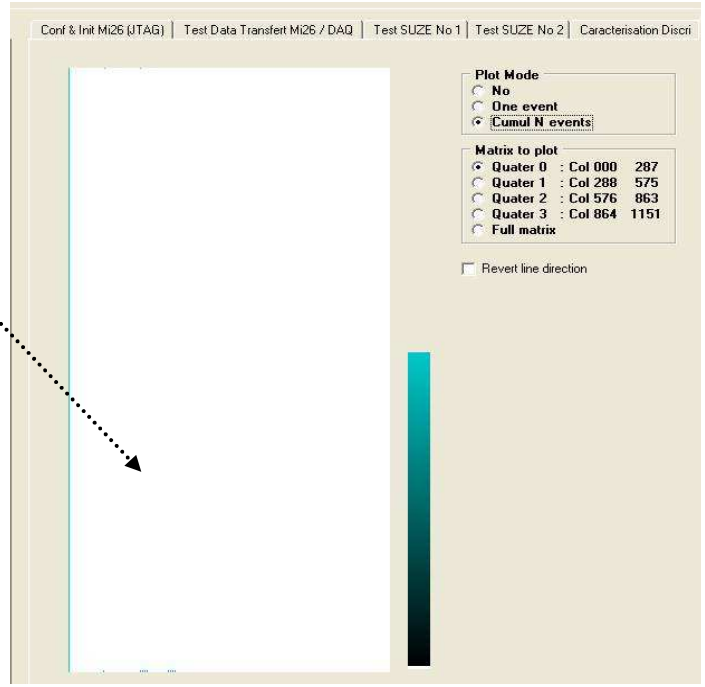


Monitoring of one line (One event / Cumul [%] over N events)



Plot of ¼ of Mimosa 26

Hit count [%] over N events



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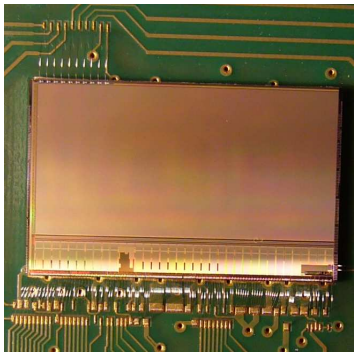

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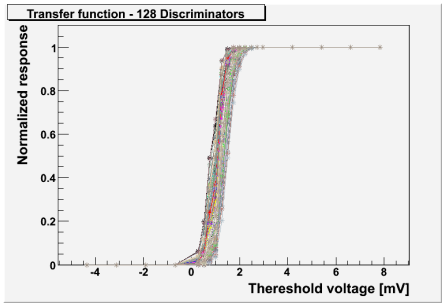
Analysis software : Discriminators & ZS Logic

What we need ?



- **Discriminators → Transfer function – Noise & Threshold dispersion**
  - **Mimosa 22 = 128 columns – Mimosa 26 = 1152 columns → Data to process x 10**
  - **Mimosa 22 analysis software too slow …**
  - **New development required (Mathieu GOFFE – Marie GELIN IRFU - Gilles CLAUS)**
    - **Process run files → Normalized "1 count [%]" for each pixel – for each threshold**
    - **ErrFunc fitting + Noise & Threshold distribution**
    - **Development & software test ~ 1,5 Month**

Marie GELIN
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Mathieu GOFFE
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- **Zero Suppression (ZS) Logic of Mimosa 26**
  - **Real data emulated by 2 lines of 1152 discriminators configured by JTAG**
  - **Test cycle : Set pattern – Acquire Data – Compare / Expected result**
  - **Test integrated in DAQ software**
  - **Development & Test of ZS logic ~ 1,5 Month**

Guy DOZIERE
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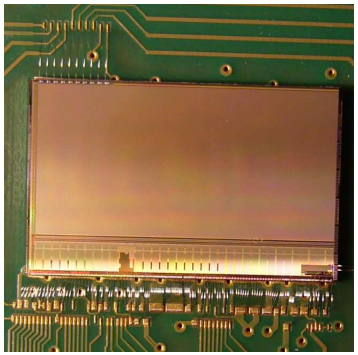
EUDET JRA1 Meeting, Strasbourg March 2009
Mimosa 26 Characterization Tools Development Status



Mimosa 26

OUTLINE

- Hardware : PCB Design & Test — W.Dulinski & M.Specht
- Slow control : JTAG — K.Jaaskelainen
- DAQ System : Analogue & Digital — M.Specht & G.Claus
- Analysis software :
  - Discriminators — M.Goffe & M.Gélin (IRFU)
  - Zero suppression — G.Doziere
- **First results …**

Status & First results : Wafers & Chips

- 3 Wafers had been produced in AMS 0.35 Opto 14 µm
- Half of one wafer has been diced in 41 chips
- 5 Mimosa 26 – (standard thickness) had been mounted on PCB

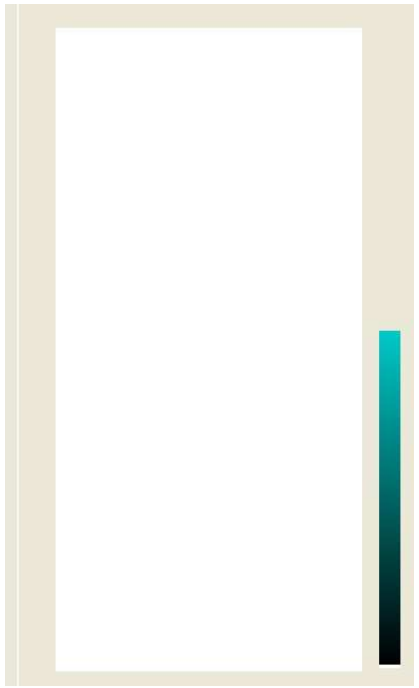
Status & First results : Mimosa 26 is alive ☺

- Mimosa 26 at IPHC on Wednesday 18 February afternoon — Do
- First chip has been bonded on end of morning Thursday 19 — Do + 1 Day
- JTAG OK + Digital frame seen on scop on Thursday evening — Do + 1,5 Day
- Interface with digital DAQ checked on Friday evening — Do + 2,5 Day
  - Digital data stream contains " fixed field " configurable by JTAG
    - Normal Zero Suppress data stream → Header, Frame counter, Trailer
    - Discriminators Test data stream → 2 lines pattern (odd / even line) of 1152 bits
  - Theses fields had been used to check interface Mimosa 26 / DAQ
  - Normal (Zero Suppression) data stream : 2 x 80 MHz - 1 x 80 MHz - 2 x 40 MHz
    - Header, Trailer checking / expected value → OK
    - Frame counter OK (visual check on consecutives frames)
    - Of course no check of data frame content : It's too early ;-)
  - Discriminators test data stream – Fixed line (No scanning)
    - Odd / even line pattern checking / expected value → OK
- Discriminators scanning mode checked on Tuesday 24 — Do + 6 Day
  - Small bug on this TEST MODE – Confirmed by simulation on Wednesday
  - Walk around found → But data of lines 0 & 573 are corrupted

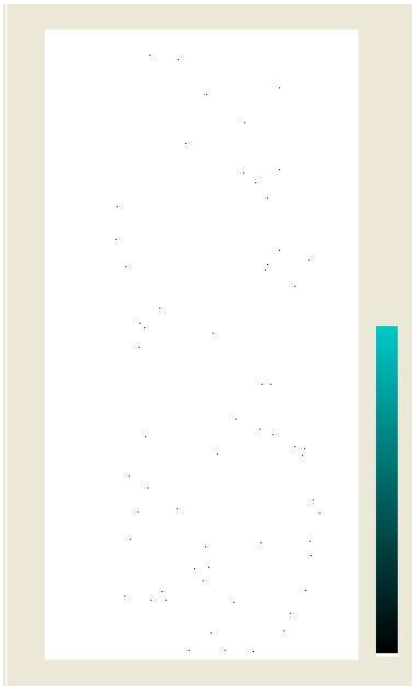
Status & First results : First tests with Fe^{55}

- First Fe^{55} hits seen on discriminators on Wednesday 25 — Do + 7 Day
  - In discriminators scanning test mode – Not after Zero Suppression (too early)

¼ Mimosa 26 WITHOUT Fe^{55}



¼ Mimosa 26 WITH Fe^{55}



- First run taken in analogue test mode on Friday 27 — Do + 9 Day
  - Preliminary result : Noise ~ 15 e- > 12 e- Mimosa 22
  - BUT Optimizations not done & Calibrations must be checked (uadc → e-) ➔ It's too early to give reliable results

Next steps : Minimal Test & Characterization level …

… required for EUDET Telescope

- **Standard characterization of Mimosa 26** — At least … 5 Weeks — M.GOFFE & M.GELIN
  - Pixel characterization via analogue outputs
  - Pixel + Discriminators characterization via digital test data stream
- **Brute force method test of ZS processing** — 2 Weeks — G.CLAUS
  - Convert ZS frame to Matrix Plot and test with ^{55} Fe / ^{106} Ru
- **Test of ZS logic** (Set pattern via JTAG – Get result via DAQ) — 4 Weeks — G.DOZIERE
- **Test of multiple MAPS synchronization** — 4 Weeks — G.CLAUS
  - MAPS to MAPS synchronization on data stream point of view
  - Test with " Lab Telescope " → ^{106} Ru source

We have seen quickly that Mimosa 26 is alive, it's encouraging …
but NOW … we should slow down … in order to provide well known sensors

Next steps : Try to define a planning

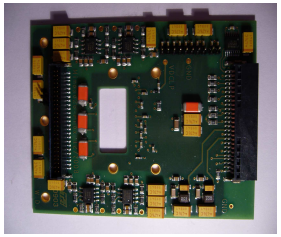
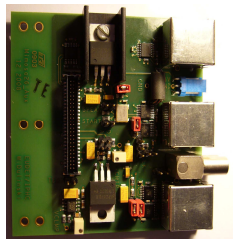
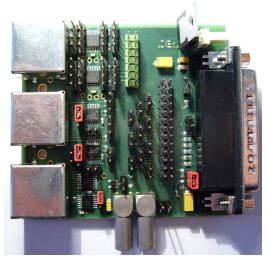
We will try to run three tasks in parallel … in 8 weeks … Possible ???

Week	Charaterization M.GOFFE & M.GELIN	System level testing G.CLAUS & M.SPECHT	Mimosa26 logic testing G.DOZIERE
1	Discriminator SW development	" Brute force method " testing of ZS processing **Test bench No 2 - D**	
2	Discriminator SW development	" Brute force method " testing of ZS processing **Test bench No 2 - D**	ZS logic testing **Test bench No 1 - D**
3	Analogue characterization Test bench No 2 - A	MAPS Synchronization **Test bench No 2 - D**	ZS logic testing **Test bench No 1 - D**
4	Analogue characterization Test bench No 2 - A	MAPS Synchronization **Test bench No 2 - D**	ZS logic testing **Test bench No 1 - D**
5	Digital characterization **Test bench No 2 - D**		ZS logic testing **Test bench No 1 - D**
6	Digital characterization **Test bench No 2 - D**	MAPS Synchronization **Test bench No 1 - D**	
7	Digital characterization **Test bench No 2 - D**	MAPS Synchronization **Test bench No 1 - D**	
8	" Buffer week " Error on time estimation	" Buffer week " Error on time estimation	

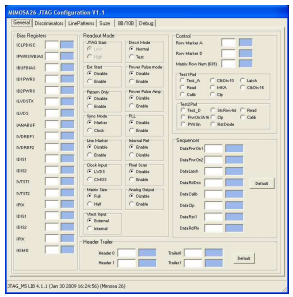
… but we will provide sensors (not characterized) for DAQ integration before

Next steps : Deliverable

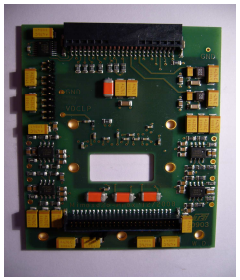
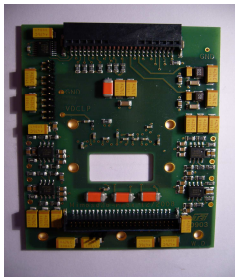
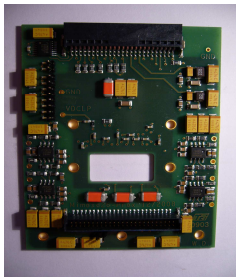
- **One Mimosa 26 + Digital auxiliary board** — **Now**

- **JTAG software (binary) + COM interface** — **Now**
  - If source code is required – Is it the priority ? — **?**



- **Three more Mimosa 26 (not characterized) + Digital auxiliary board** — **6 April**

Backup slides

Status / Planning of 5 December 2008 (Phone meeting)

Ready to start testing ?

- Test boards populated and tested
  - End of January
- JTAG slow control
  - Done and tested for 09/02/2009
- Analogue & Digital outputs acquisition
  - Done and tested for 16/02/2009
- Discriminators analysis software
  - Done and tested (emulated data) for 16/02/2009 → ~ 4 weeks late but not mandatory for first tests
- Software for Zero suppression processing (Suze) testing
  - Done and tested for 16/02/2009 → ~ 4 weeks late but not mandatory for first tests

=> We hope to have all test benchs ready for 16/02/2009 with uncertainty of -0 / +2 weeks
=> We need at least 2 weeks for Mimosa 26 testing (Not for characterization)

Conclusion

- Operational sensor for 01/03/2009 – 16/03/2009
  - In order to provide one Mimosa 26 for EUDET DAQ testing
- First characterization results for end of March
  - It's too early to provide reliable results

Digital DAQ : Commercial board ?

How to read Mimosa 26 with a commercial board ?

- It's obvious that commercial boards AS IS can't read "non standard" data stream
- PXI 6562 is a Parallel acquisition board NOT a Deserializer
- We have decided to use a software interface " between " Mimosa 26 / PXI 6562
  - Board acquire constant frame length : Deserialization and frame length detection are done by software
  - Mimosa 26 will run at nominal clock rate → Only mean event rate will be reduced (~ 1500 events / s)
  - Improvement of event rate can be done → Replace software interface by a FPGA

No development ? … Buy the HW & Develop the SW

- Client / Server architecture
  - Client : The DAQ supervisor application (Run control & Monitoring) running on a Windows PC
  - Server : The CPU on PXI crate is the data server (Board control & data deserialization)
- Saving time on HW → Improve the SW
  - More test & on-line monitoring tools included in DAQ software
  - Emulation of the whole DAQ chain with a pattern generator

Digital DAQ : Commercial board ? -

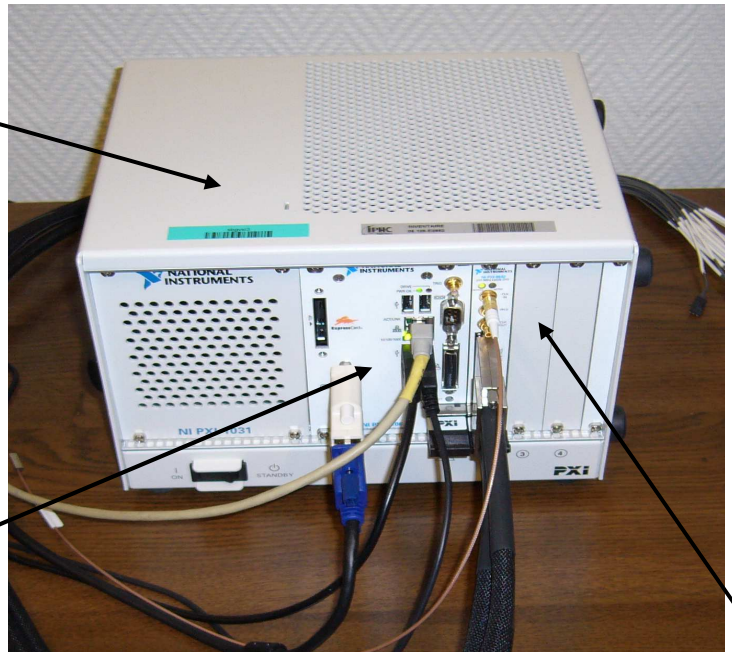
Why a DAQ PXI for Mimosa 26 ?

Two digital test bench are required to characterize Mimosa 26

- **Discriminateurs → DAQ PXI : 2 inputs 10 MHz 1152 b / frame**
- **SUZE → DAQ PXI : 2 inputs 80 MHz ~ 10 kb / frame**

PXI Crate 1031

- CPU board
- Digital acquisition board



CPU board – PXI 8106

- Intel 2,16 GHz
- 2 GB RAM
- HD 250 GB

DAQ Performances (for laboratory tests)

- Acquisition of bunch of 200–1800 consecutives frames
- No dead-dime during one bunch
- Mean event rate 1500 frames / s - 17 % / 8,6 Khz Mimosa 26

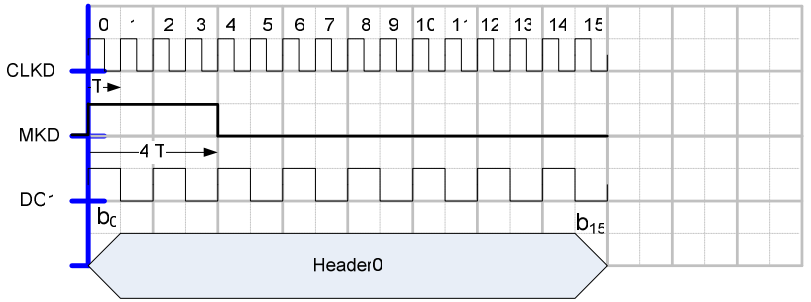
This is not a DAQ for beam telescope
- 8,6 KHz without dead time -
But this not the goal of this system.

Acquisition board PXI 6562

- 16 Inputs 200Mhz / 8 Inputs 400 Mhz
- 2 (16) MSamples / Input

Data format

- Header →32 bits
- Frame counter → 32 bits
- Data length (useful part of data) → 32 bits
- Data = “Data length” W16 (Words of 16 bits)
- Trailer → 32 bits
- Padding zero
- Zero at end of frame → 2 or 4 W16 (depends on readout configuration)



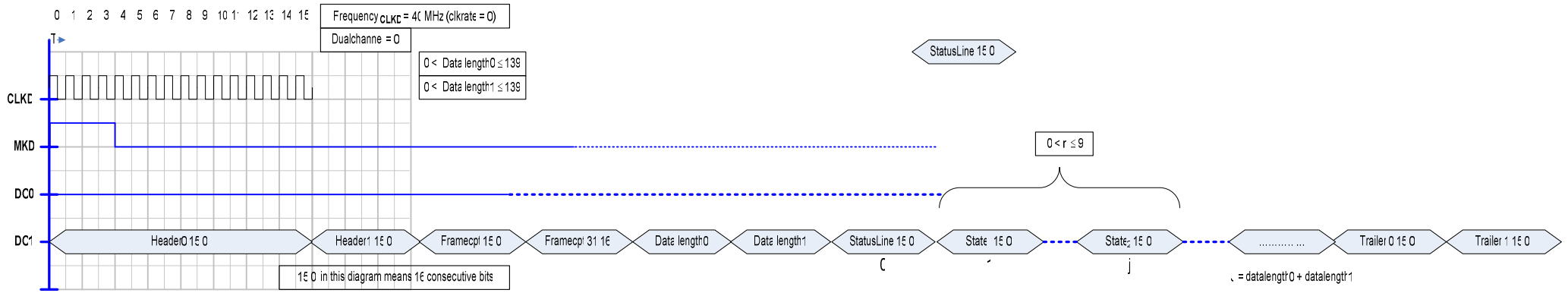
Status/ line															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0-3)				Bit(0-10)											
number of *States*				The address of the line											OVF

State															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0-1)		Bit(0-10)													
number of hit pixels		the address of the column											not used		

Mimosa 26 ZS readout modes : Configurations 0 & 1

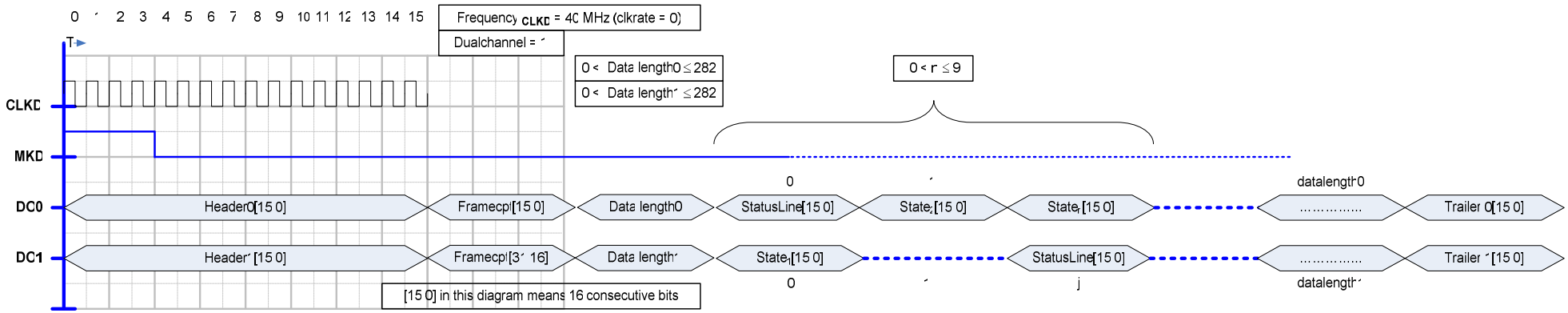
Configuration 0 : 1 link at 40 MHz

- Provides ¼ of states memory size : 278 W16 (word of 16 bits)



Configuration 2 : 2 links at 40 MHz

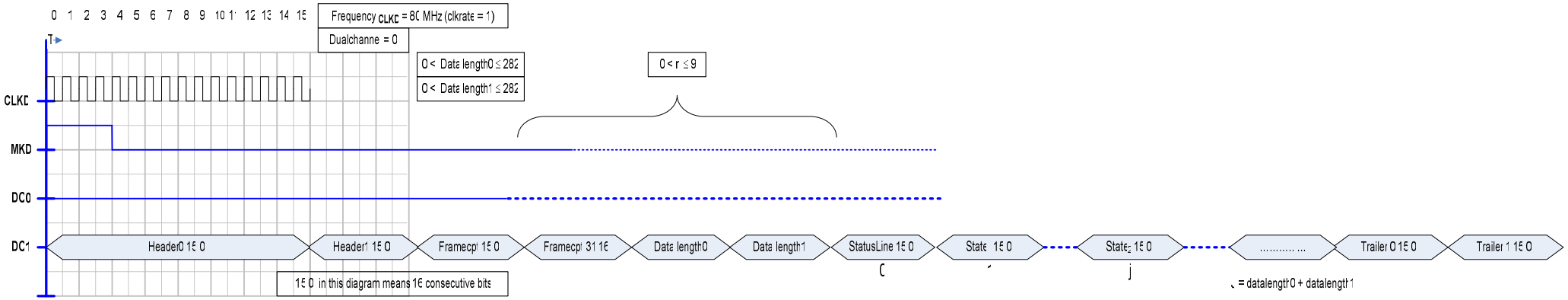
- Provides 1/2 of states memory size : 564 W16 (word of 16 bits) – 286 W16 / link



Mimosa 26 ZS readout modes : Configurations 2 & 3

Configuration 2 : 1 link at 80 MHz

- Provides 1/2 of states memory size : 564 W16 (word of 16 bits)



Configuration 3 : 2 links at 80 MHz

- Provides the whole states memory size : 1140 W16 (word of 16 bits) – 570 W16 / link