

LOI Content: Electronics and DAQ

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Overall Architecture



SiD has a coherent approach to the electronics architecture that seems to fit all the baseline subsystems. Figure 1 shows the simplified block diagram for the data-acquisition from the front-end electronics to the online-farm and storage system. The subsystems with the exception of the Vertex detector (for which the sensor technology is not yet selected) and the FCAL (which has approximately unit occupancy) are read out by variants of KPiX as the front-end Application-Specific Integrated Circuit (ASIC).







- Figure 2 shows a simplified block diagram of the KPiX, processing signals from 1,000 detector channels. The low level charge signal at the input is processed by the charge amplifier in two ranges with automatic range switching controlled by the range threshold discriminator. Calibration is provided covering the full range. Leakage compensation is available for DC-coupled detectors.
- Internal or external trigger options can be selected Up to four sets of signals for each channel can be stored in one acquisition cycle. Time is stored in digital format, the amplitude as a voltage on a capacitor for subsequent digitization in a Wilkinson-type ADC. At the end of the acquisition and digitization cycle nine words of digital information are available for each of the 1024 cells of the KPiX chip. The data is read out serially from the ASIC before the next acquisition cycle begins.





Sub-System	KPiX Count	Channels/KPiX
Tracker	22066	1024
EMCAL	99076	1024
HCAL	35412	1024
Muons	8834	64
Total	165388	

Table 1 lists the number of KPiX ASICs for each subsystem. Tracker, EMCAL, and HCAL use 1,000-channel ASICs while the Muon sub-system uses a 64-channel version.



Overall Architecture



As illustrated in Figure 1, several front-end ASICs (KPiX, FCAL or Vertex ASICs) are connected to a Level-1 Concentrator (L1C) board using electrical LVDS. The concentrator board main functions are to fan out upstream signals to the front-end modules, to fan-in data from the front-end modules for transmission to the Level 2 Concentrator (L2C) boards, and to perform zero-suppression and sorting of the event data. Just as an example, for the EMC Barrel a total of 96 1,000-channel KPiX chips would be connected from 8 front-end cables with 12 KPiX's each to one Level-1 Concentrator board. The number of Level 1 concentrator boards in the detector depends on the sub-system, e.g for the EMC Barrel there would be 821 L1C boards and 52 L2C boards (80k KPiX, 96 KPiX for each L1C board, 16 L1C boards for each L2C board)



Level 1 and Level 2 Concentrators



The Level 1 Concentrator boards are in turn connected via 3-Gbit/sec fibers to the Level-2 Concentrator boards. These are similar to the Level 1 Concentrator boards. They fan out and fan in signals to/from the Level 1 Concentrator boards. In addition the data-streams of sorted event data received from each Level 1 Concentrator board are merged and sorted before transmission to the off-detector processor boards. The Level 2 boards are either located inside the detector or outside, depending on the sub-system. E.g. for the EMC Barrel there are 36 of such boards inside the detector volume.

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Level 2 Concentrator boards are connected to ATCA modules



ATCA DAQ Modules







Rear Transition Module

Reconfigurable Cluster Element Module

Management Processor

Ethernet on Rear-Transition Board

- Front-end data sorted in Level 1 and Level 2 concentrator modules
- Two SLAC custom modules in ATCA with functionality described in the LOI
- Note that the event data is zero-suppressed in the sub-systems without the need for a global trigger system. All data produced in the front-ends above a programmable threshold is read out. For diagnostics and debugging, the DAQ includes the ability to assert calibration strobe and trigger signals, transmitted to the front-ends via the Level-2 and Level-1 Concentrator boards using the fibers shown in Figure 1. The fiber transports encoded command, clock, and synchronization to all the front-ends

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Power & Environmental Monitoring



- Power Conversion circuits on the Level 2 and Level 1 Concentrator boards supply the power to the front-ends, starting with 48V or higher voltages from off-detector supplies. Alternatively, serial powering architectures are also under consideration. The power supplies are located in several racks on or next to the detector.
- Environmental and health monitoring circuits are also included on the concentrator boards. In addition there may be additional monitoring boards in the detector, connected to RCE fiber interfaces. In addition there are crates of monitoring modules mounted in several racks on or next to the detector.