DIF Firmware

Real or Virtual?

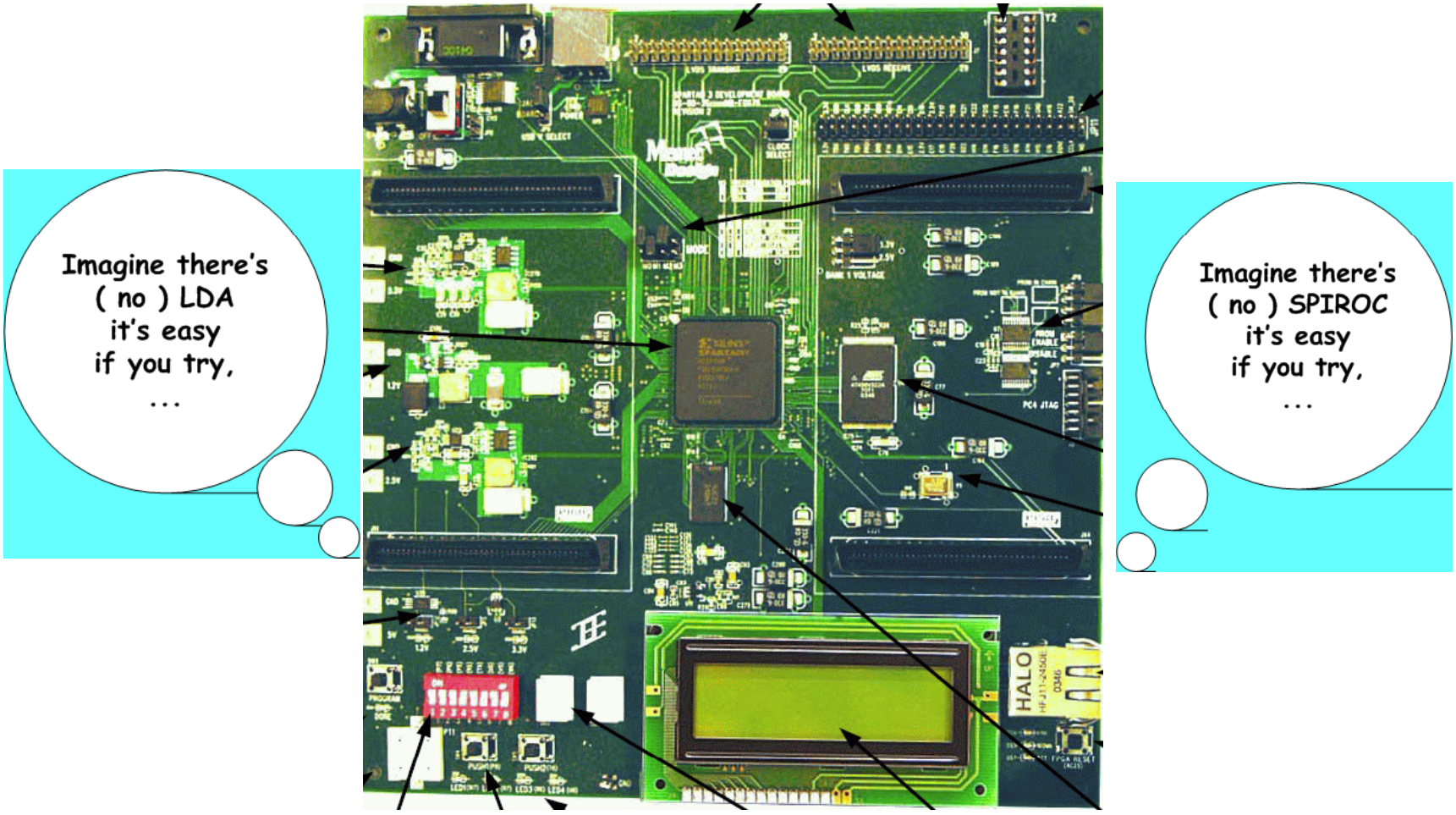
Status and Comments

Presented by Frantisek Krivan

DIF Documents

- DIF Commands Proposal - Mathias Reinecke
- DIF ASIC Timing diagrams - Mathias Reinecke
- DIF Development for ECAL, DCAL
- SPIROC I. and II. Technical Information – Omega Webpage
- Calice LDA Docs - Marc Kelly
- Format of the read-out data of the DIF – Remi Cornat
- E-mail discussions
- Spartan Docs, USB Docs, SPI Docs, …
- …

Virtual DIF and real world or vice-versa



Hardware Sandbox

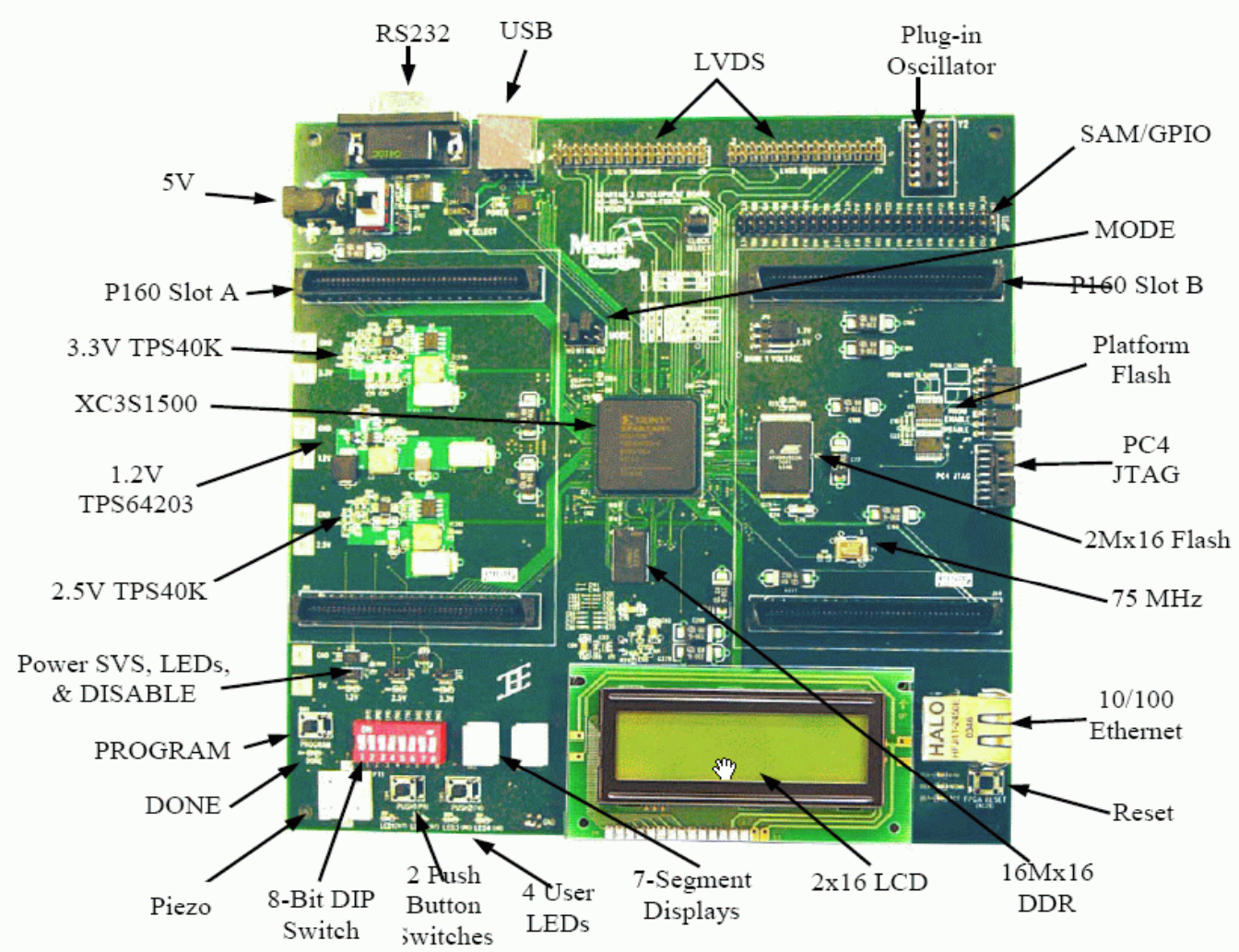
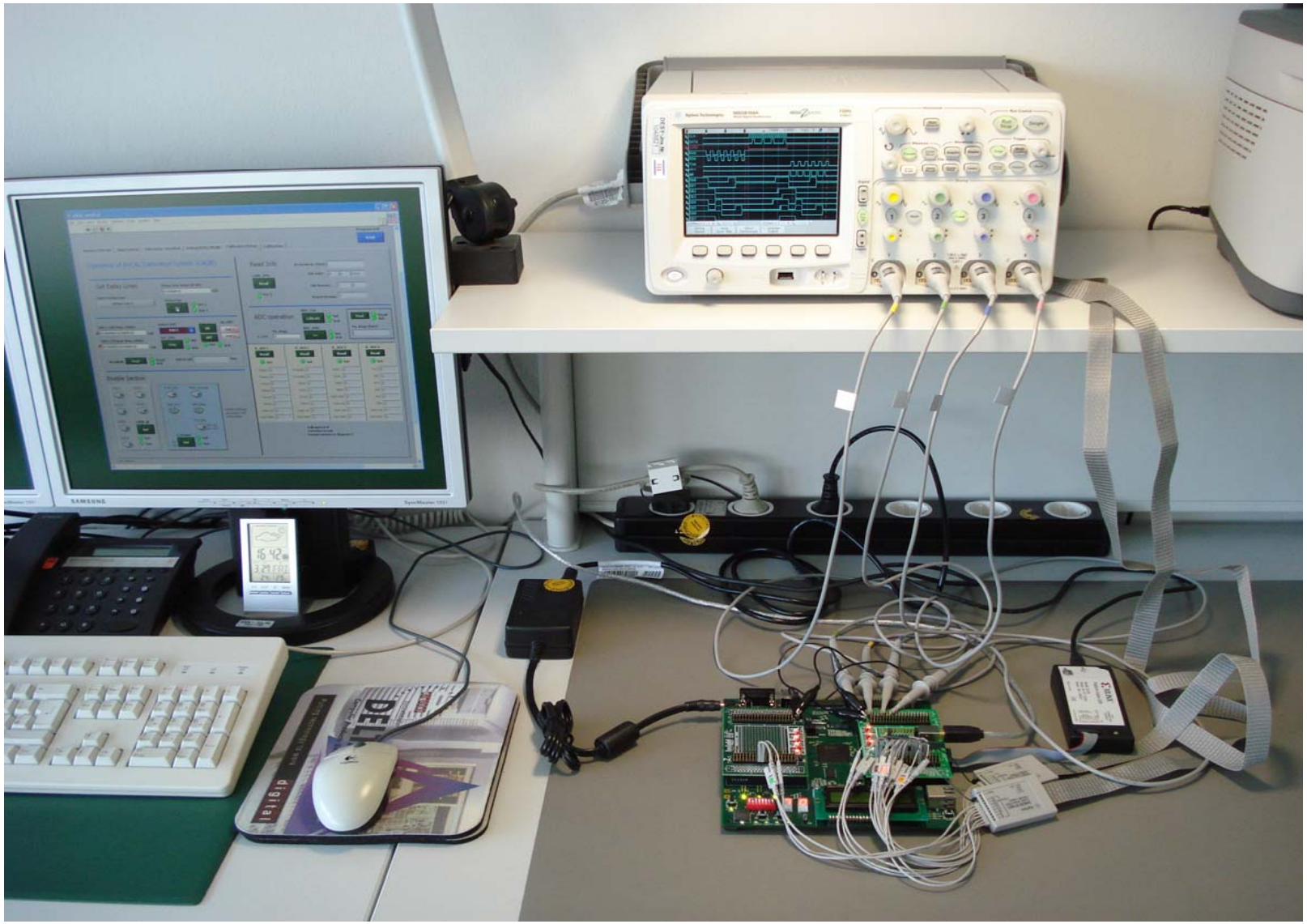
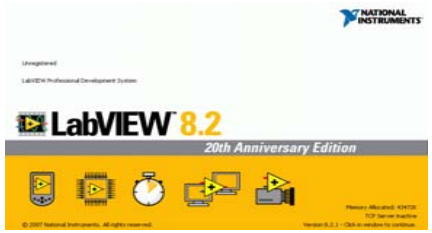


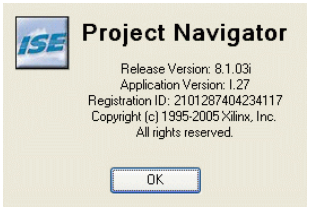
Figure 1 – Spartan-3 MB Development Board

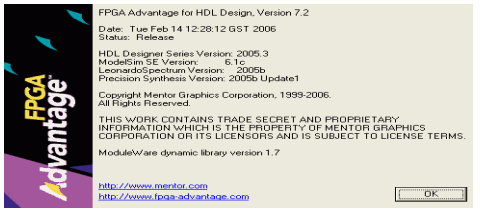
Hardware Sandbox

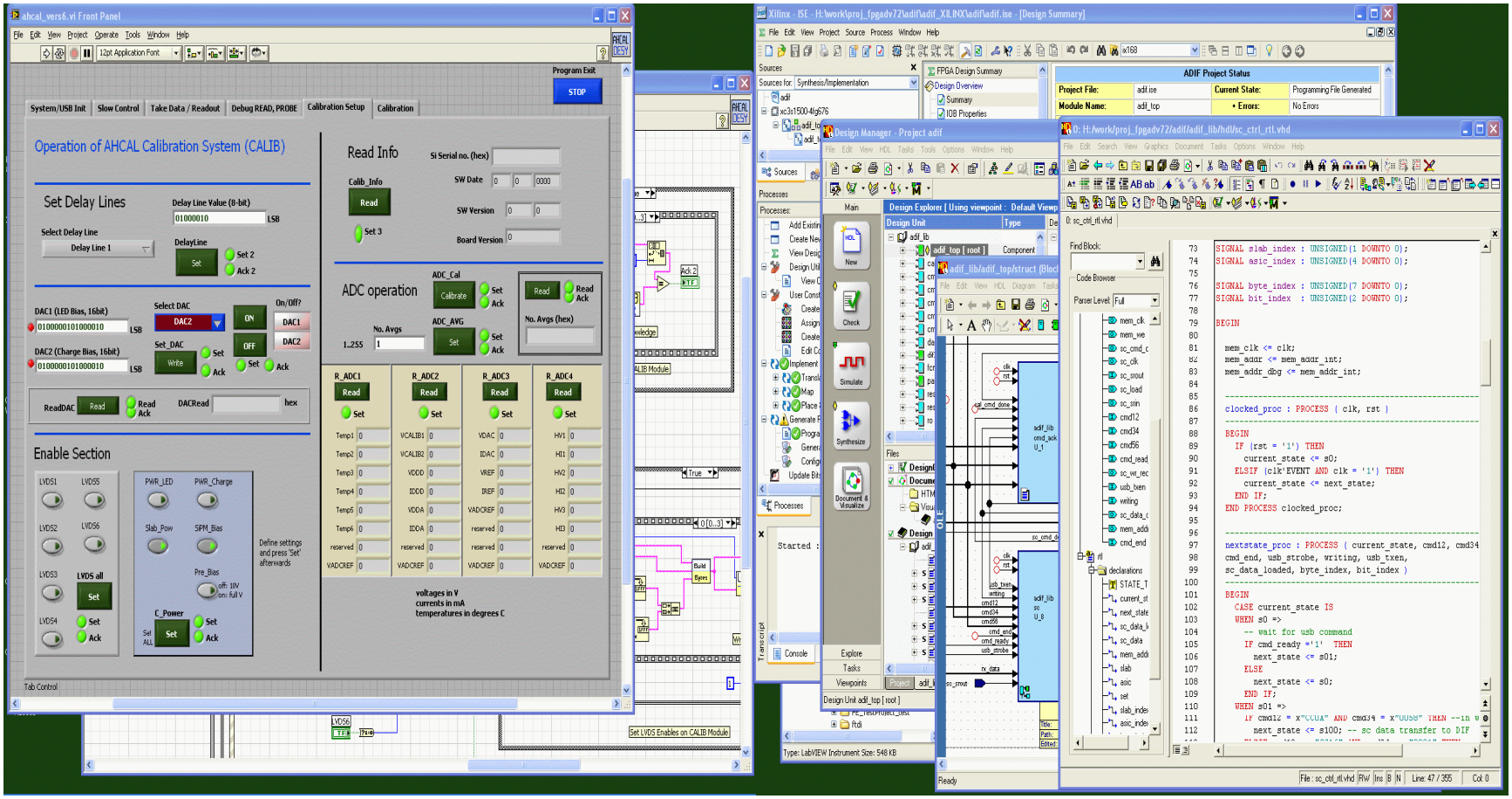


Software Environment

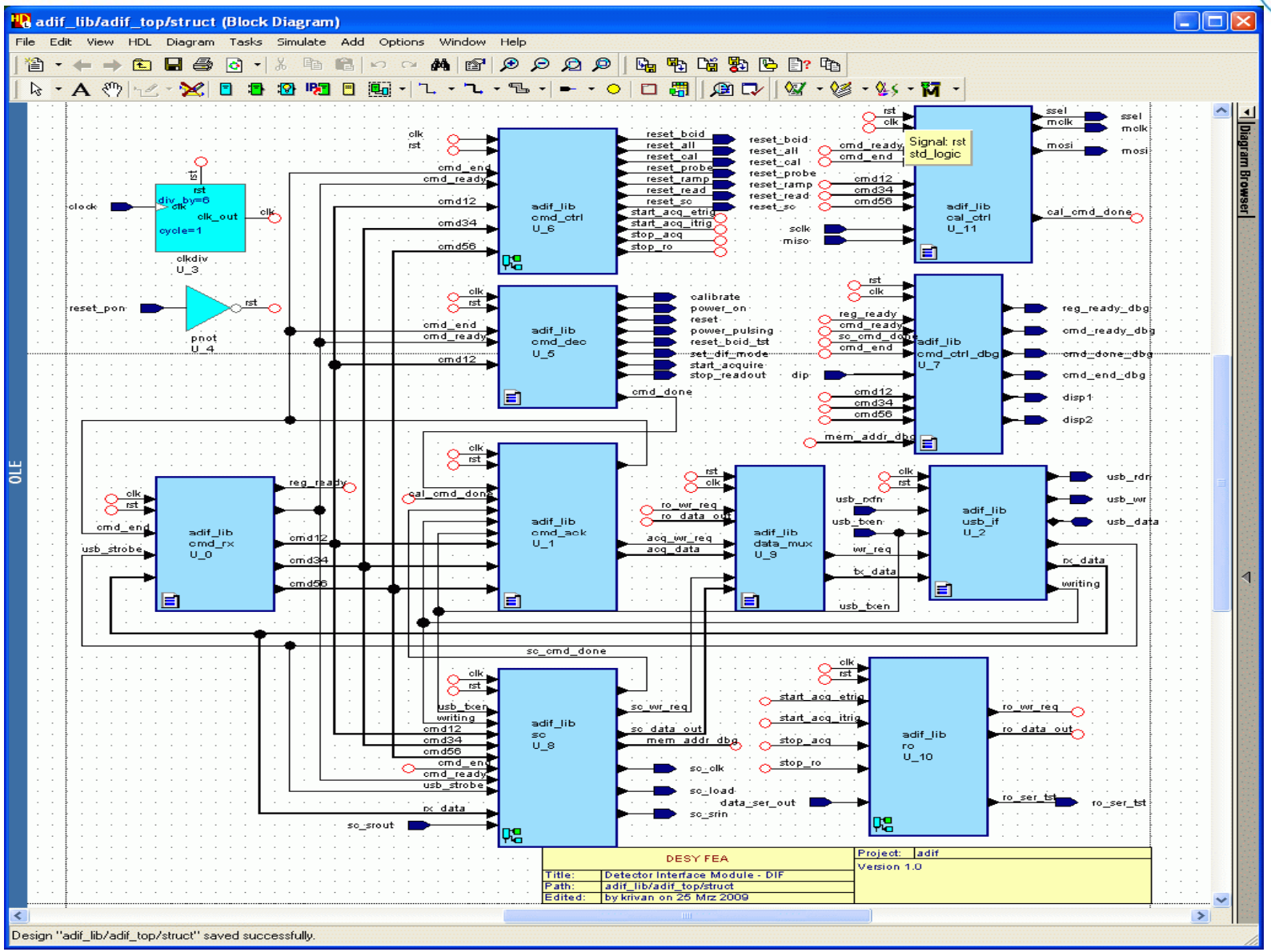








Block Diagram – Top Collection

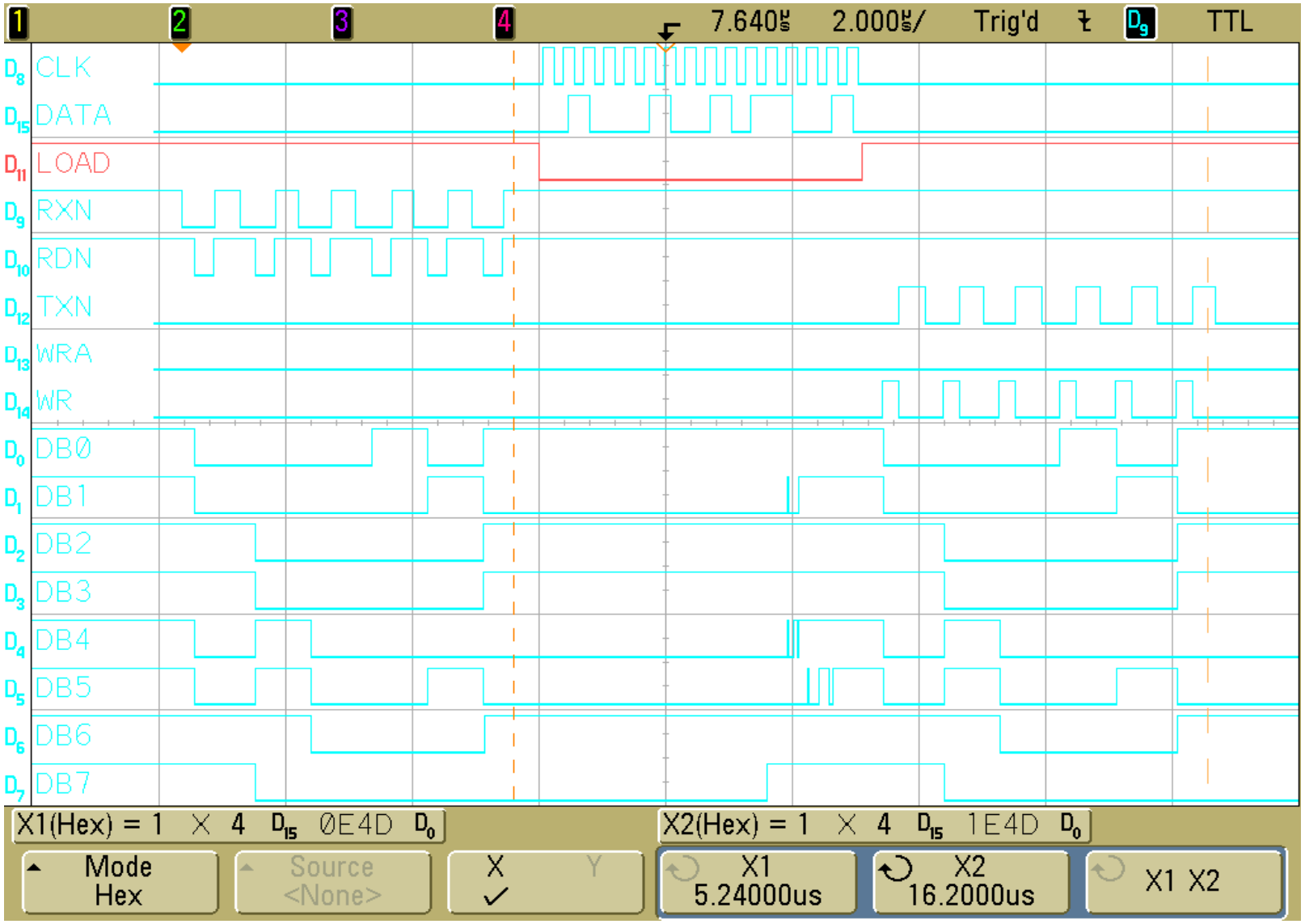


SPI Commands - LabView

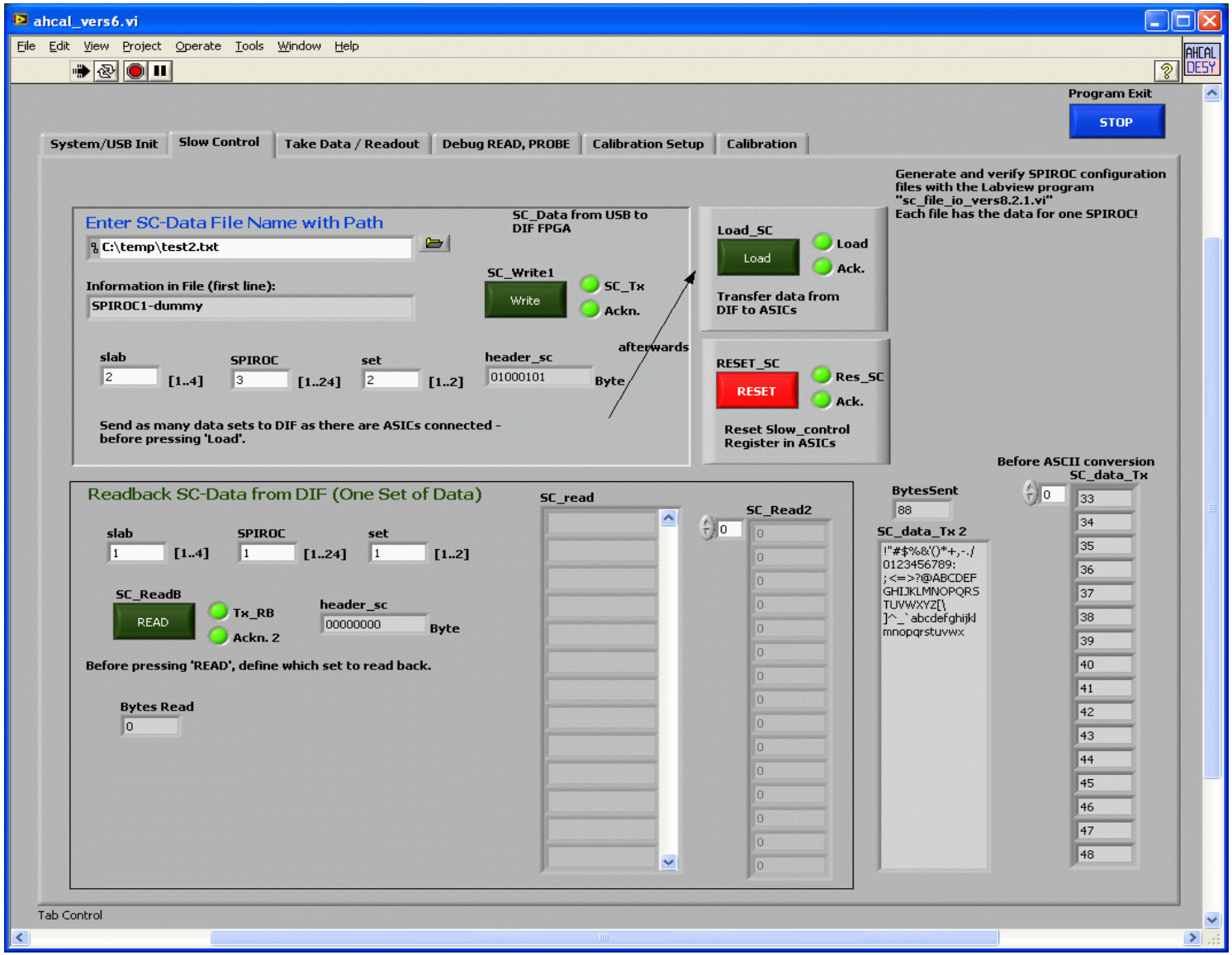
SPI Commands Table (Part)

SPI Commands for CALIB Board from DIF Board					
Command:	**Hex**	**Data**		**Return Value**	
	Group 1:		**System informationen**		
Read Silicon Serial Number	0x11	--	--	6 Byte	SiliconNumber
Read Software data	0x12	--	--	4 Byte	Datum: DD MM JJJJ
Read Software version	0x13	--	--	1 Byte	0.0 - 15.15 (0xFF)
Read Board version	0x14	--	--	1 Byte	0 - 31
	Group 2:		**Set Delay Line**		
Set DelayLine 1	0x21	1 Byte	0-255	--	--
Set DelayLine 2	0x22	1 Byte	0-255	--	--
Set DelayLine 3	0x23	1 Byte	0-255	--	--
	Group 3:		**Enable Transmitter and Power**		
Enable LVDS Repeat en_1	0x31	1 Byte	0 or 1	--	--
Enable LVDSTransm. en_2	0x32	1 Byte	0 or 1	--	--
Enable LVDSTransm. en_3	0x33	1 Byte	0 or 1	--	--

SPI Command Example



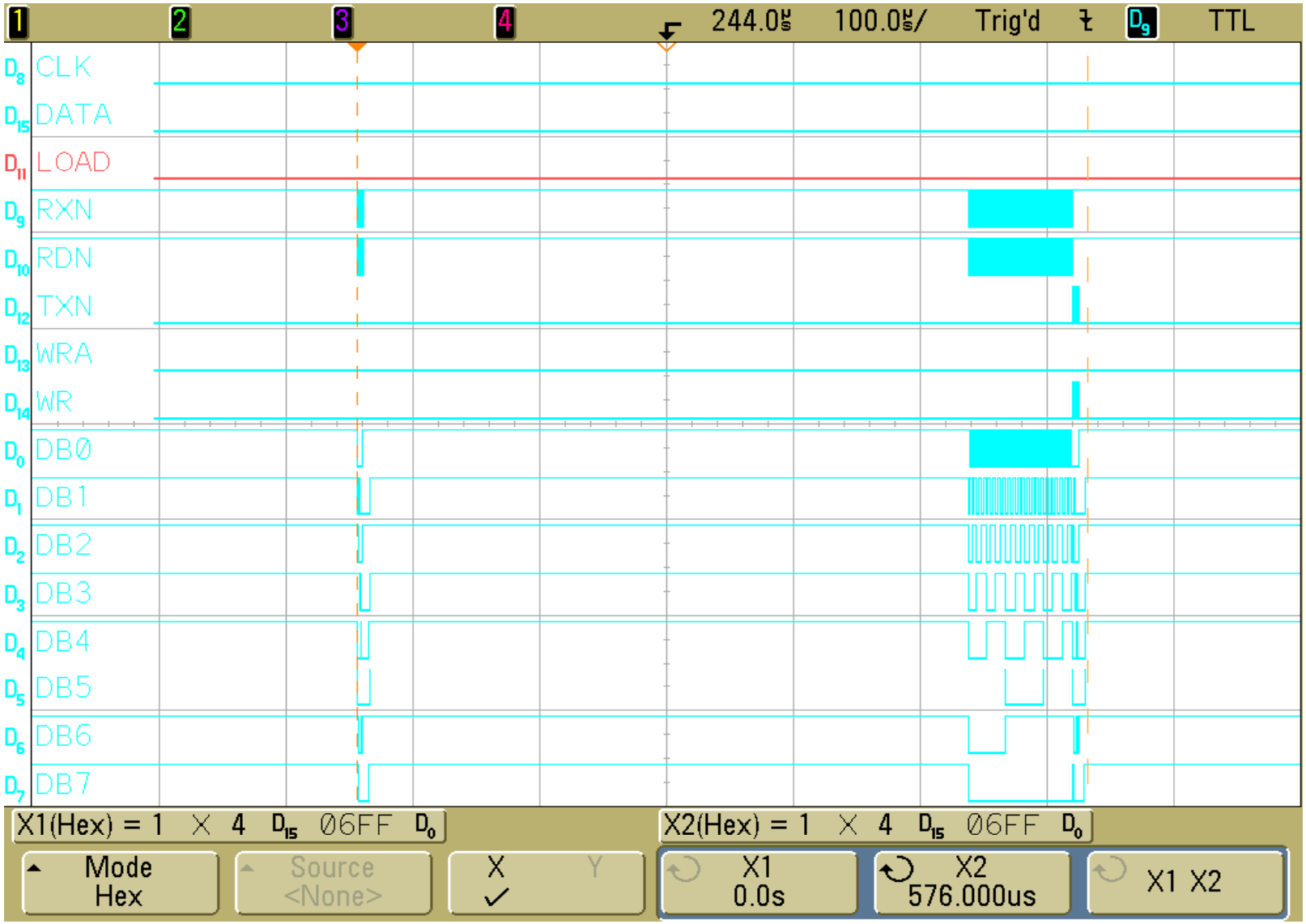
SC LabView


ahcal_vers6.vi
File Edit View Project Operate Tools Window Help
AHCAL DESY
Program Exit
STOP
System/USB Init
Slow Control
Take Data / Readout
Debug READ, PROBE
Calibration Setup
Calibration
Generate and verify SPIROC configuration files with the Labview program "sc_file_io_vers8.2.1.vi" Each file has the data for one SPIROC!
Enter SC-Data File Name with Path
C:\temp\test2.txt
SC_Data from USB to DIF FPGA
Information in File (first line):
SPIROC1-dummy
SC_Write1
Write
SC_Tx
Ackn.
afterwards
slab
2
[1..4]
SPIROC
3
[1..24]
set
2
[1..2]
header_sc
01000101
Byte
Send as many data sets to DIF as there are ASICs connected - before pressing 'Load'.
Load_SC
Load
Load
Ack.
Transfer data from DIF to ASICs
RESET_SC
RESET
Res_SC
Ack.
Reset Slow_control Register in ASICs
Before ASCII conversion
SC_data_Tx
Readback SC-Data from DIF (One Set of Data)
SC_read
SC_Read2
BytesSent
88
SC_data_Tx 2
slab
1
[1..4]
SPIROC
1
[1..24]
set
1
[1..2]
SC_ReadB
READ
Tx_RB
Ackn. 2
header_sc
00000000
Byte
Before pressing 'READ', define which set to read back.
Bytes Read
0
Tab Control

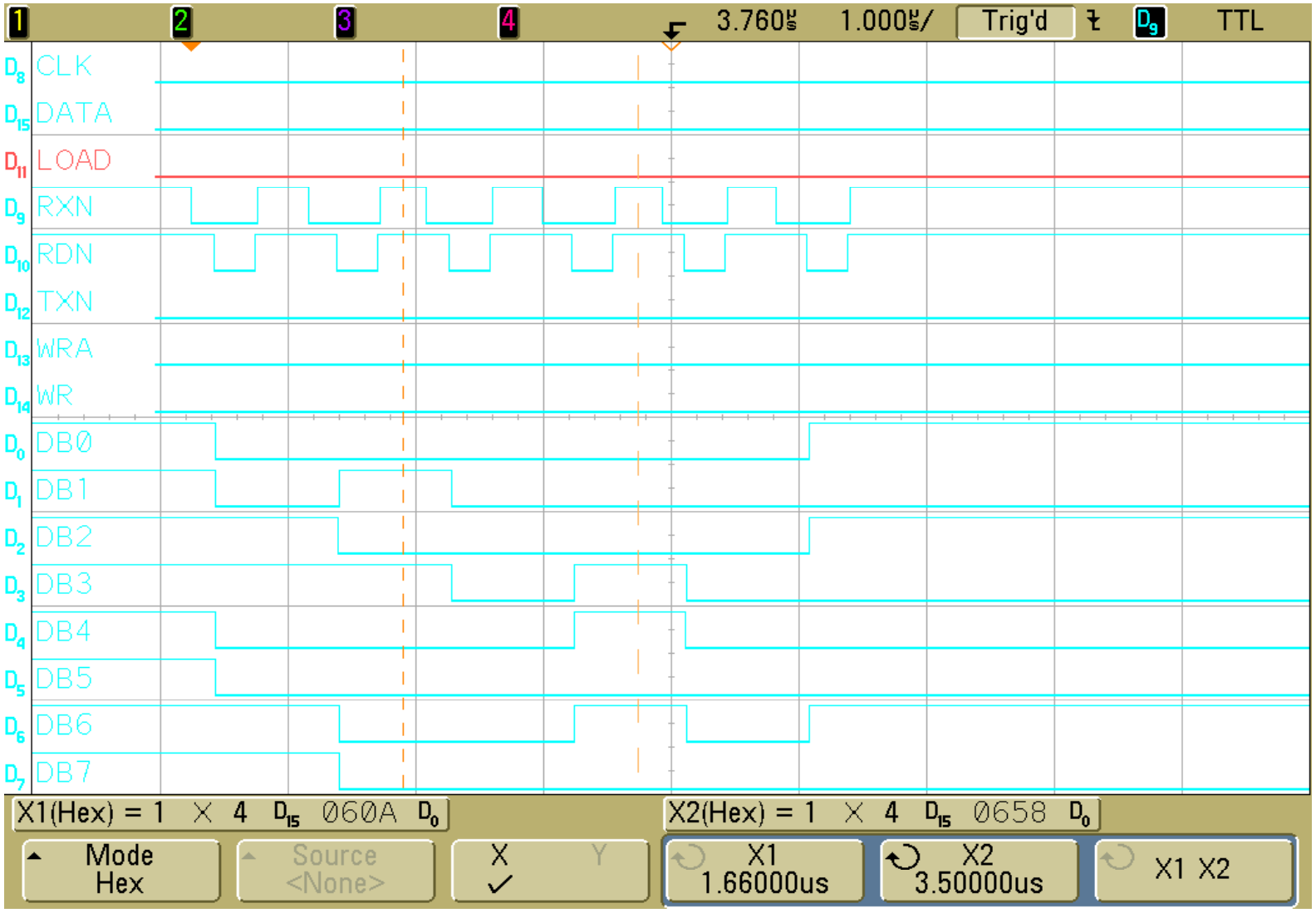
SC Memory Mapping

- Parameters Size
  - Chain 1 – 4
  - ASIC 1 – 24
  - Set 1 -2
- Alternate versus Continual Mapping
  - Alternate Set 1/2
  - Alternate Chain 1/2/3/4
- Block size 128 bytes – 88 used / 40 free
- 88 bytes – 704 bits
  – we skip 1 bit from 1 byte

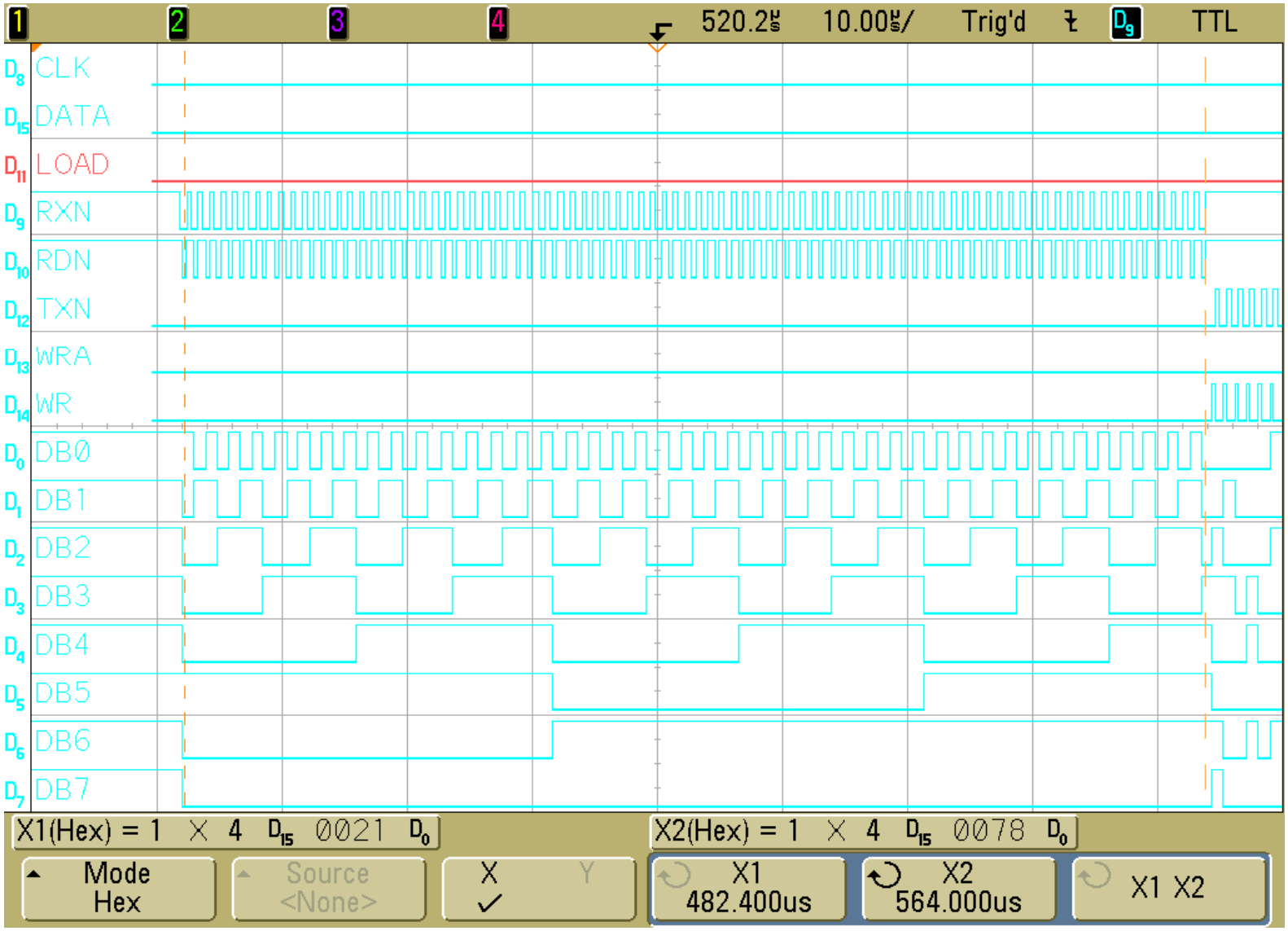
SC USB to DIF


1
2
3
4
244.0ns
100.0ns/
Trig'd
TTL
D8 CLK
D15 DATA
D11 LOAD
D9 RXN
D10 RDN
D12 TXN
D13 WRA
D14 WR
D0 DB0
D1 DB1
D2 DB2
D3 DB3
D4 DB4
D5 DB5
D6 DB6
D7 DB7
X1(Hex) = 1 X 4 D15 06FF D0
X2(Hex) = 1 X 4 D15 06FF D0
Mode
Hex
Source
<None>
X
Y
X1
0.0s
X2
576.000us
X1 X2

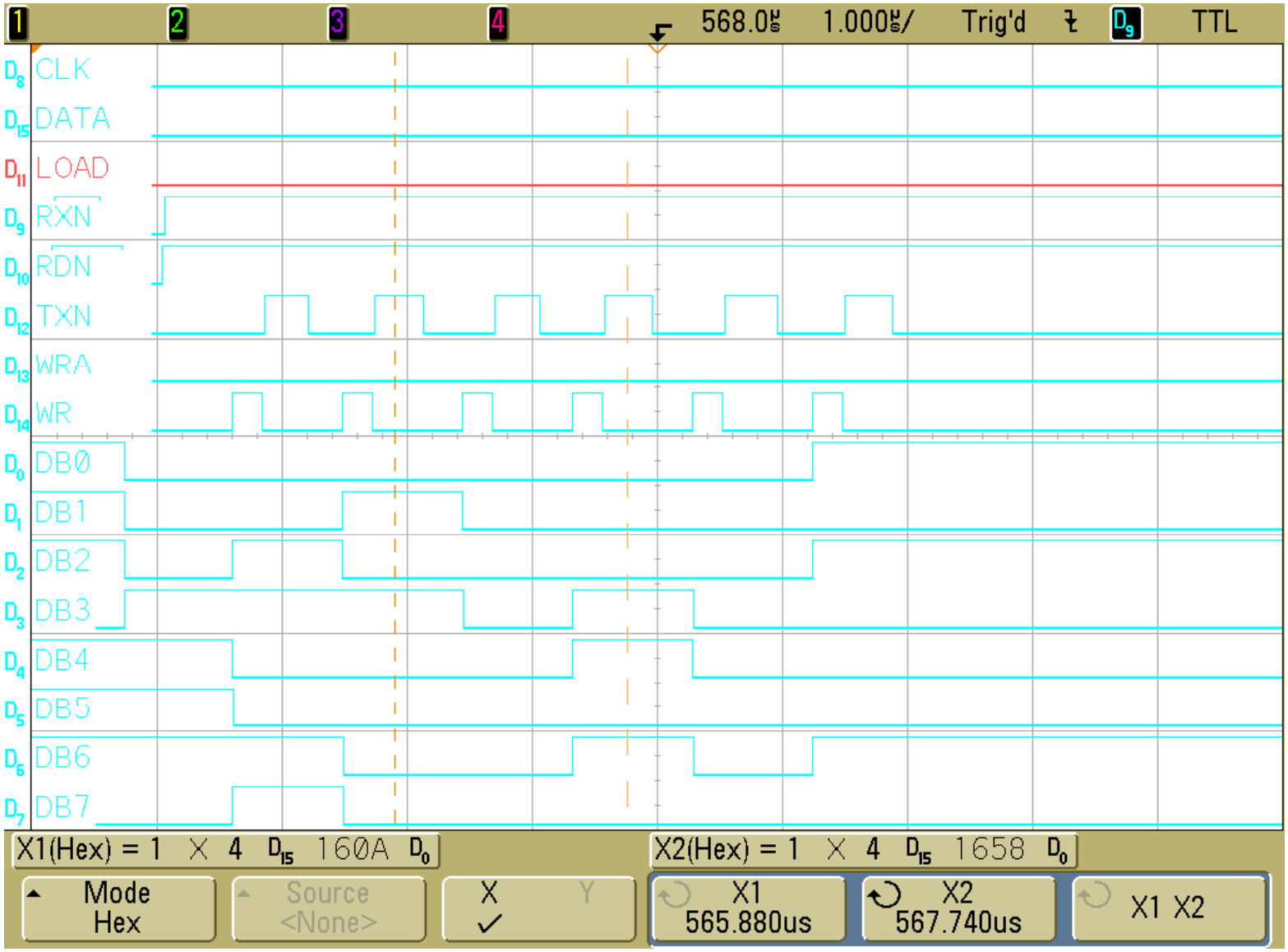
SC USB to DIF – Command Part



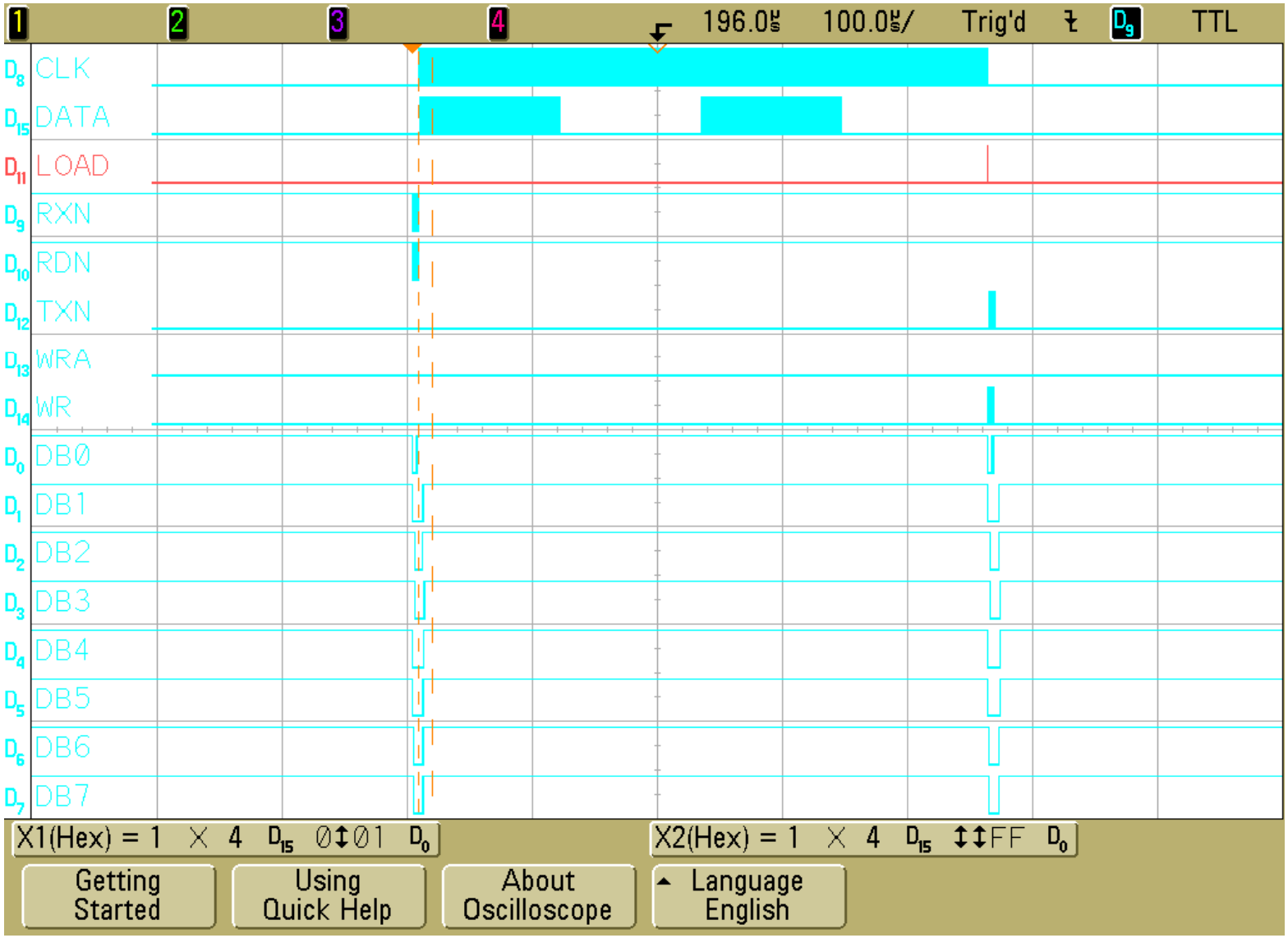
SC USB to DIF – Data Part



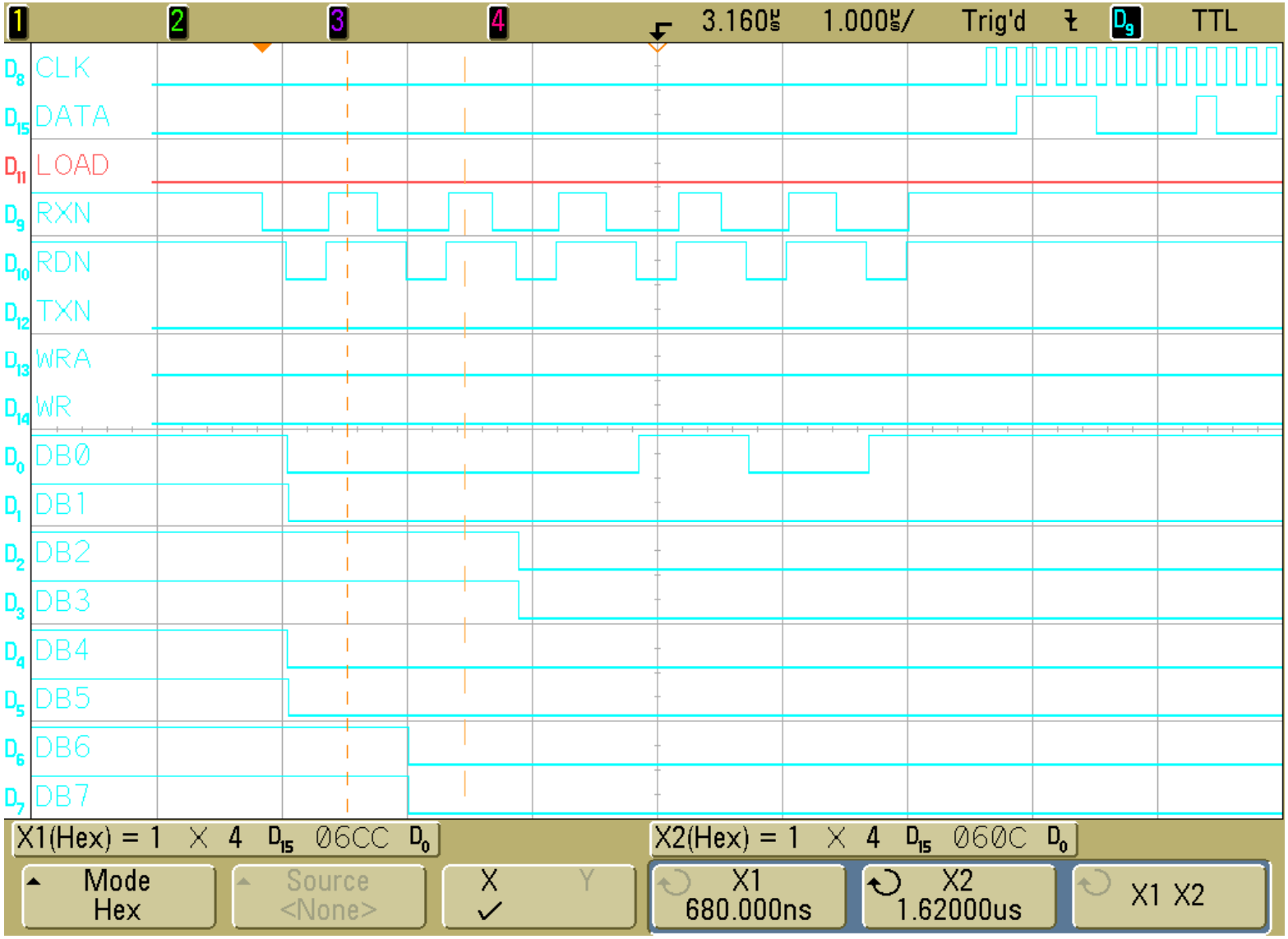
SC USB to DIF - Acknowledge Part



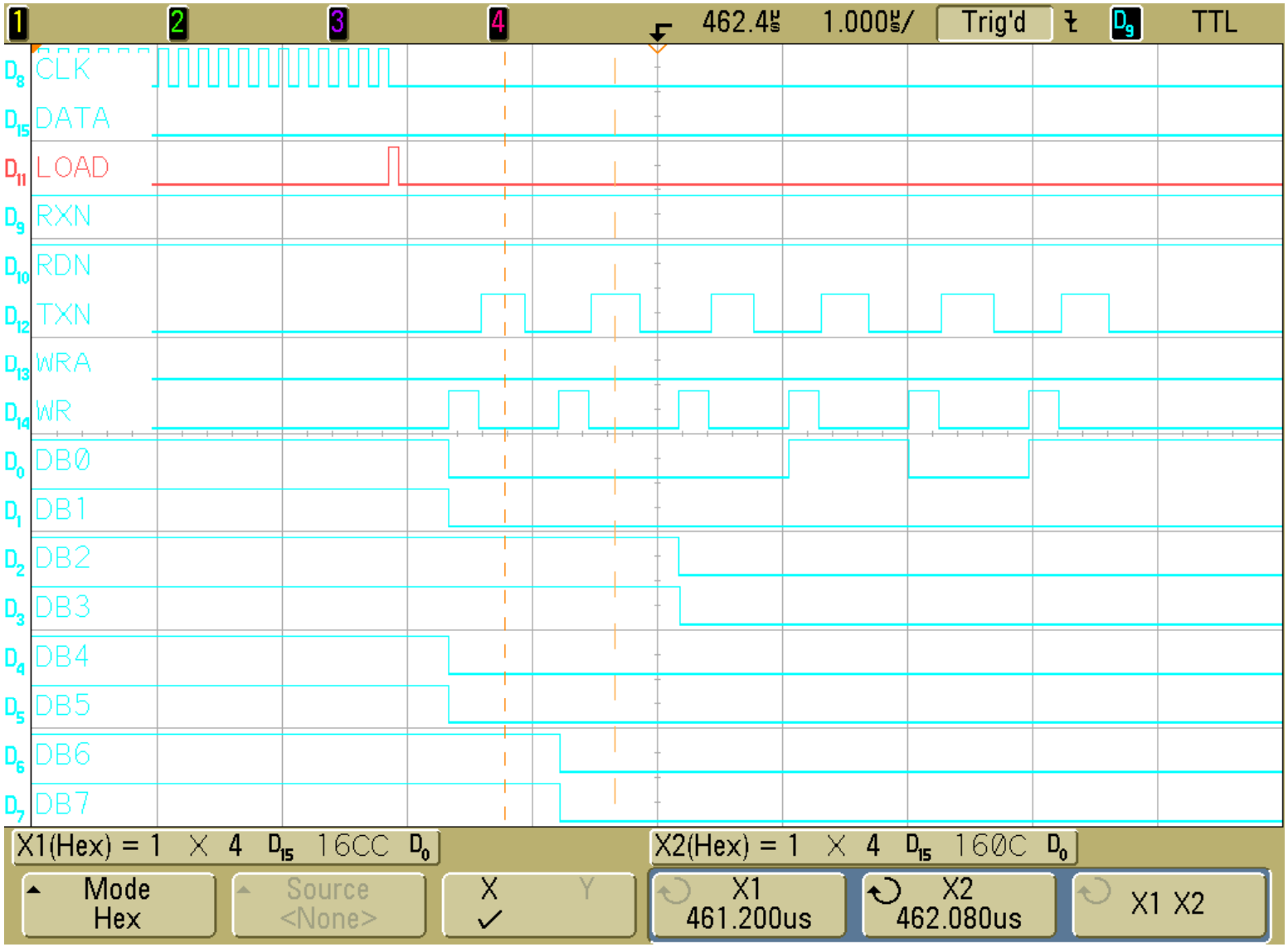
SC Load DIF to ASIC's



SC Load - Command Part



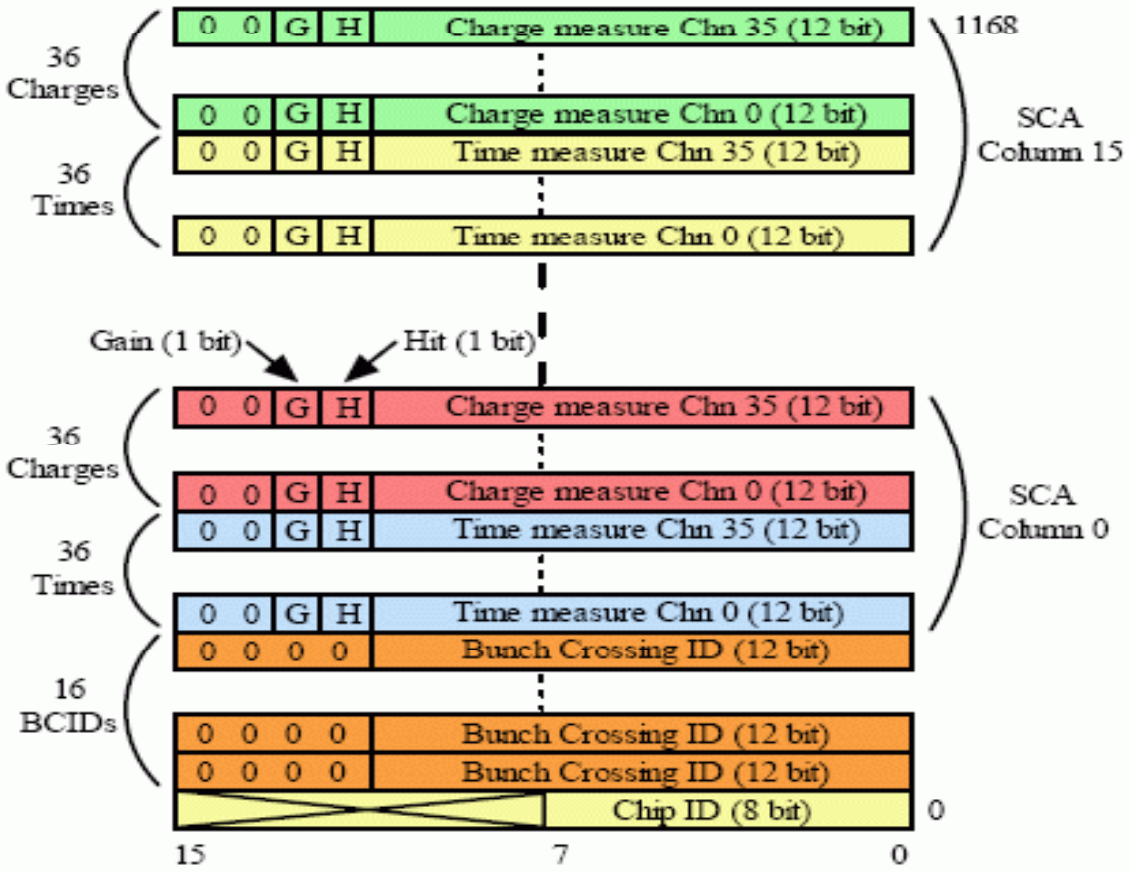
SC Load - Acknowledge Part



SPIROC RAM MAPPING

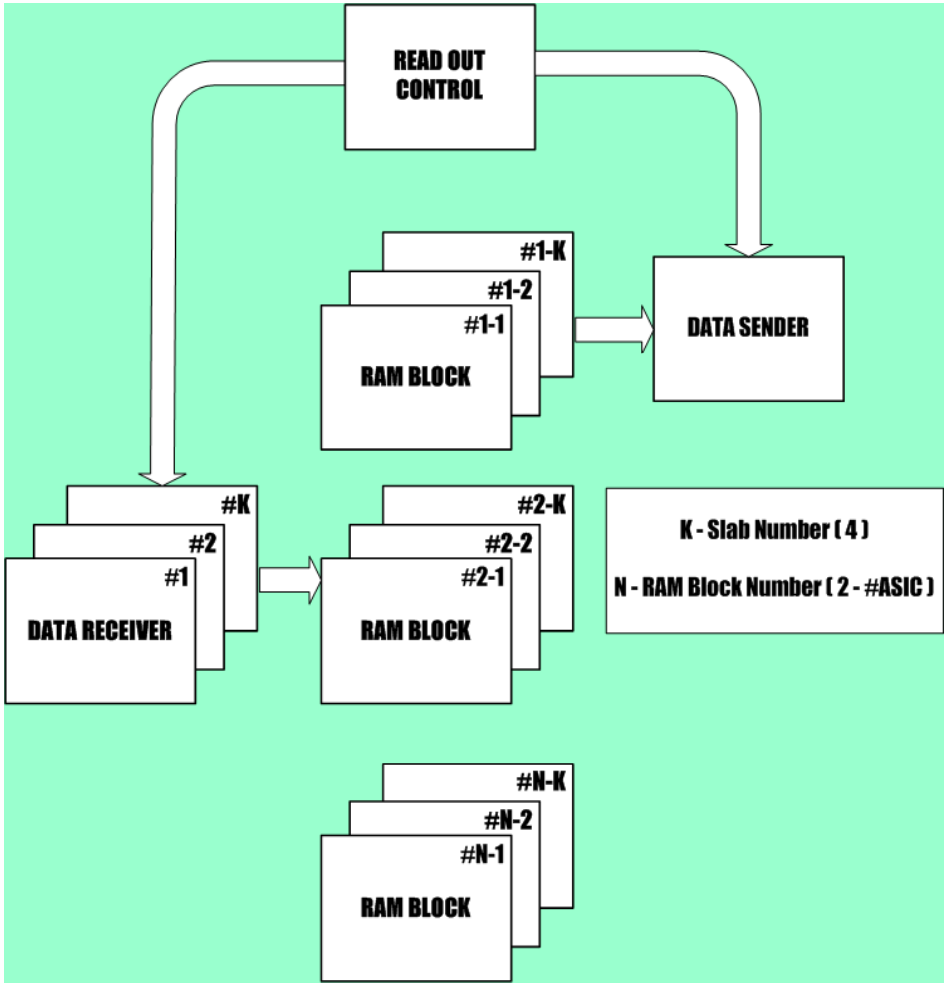
DATASHEET

12 Spiroc RAM mapping



Readout II.

- Dual Port Memory
  - More effective using of the memory space
- RAM Block FIFO
  - Data reordering
  - Data reduction (global cut, local cut, area cut)



Control Signals RO / Power

- Counter solution
  - Counter step definition (100us – 12bits, 1us – 18bits)
  - Synchronisation
  - Register definition (1 ON, 1 OFF, 1 default value)
  - Common counter for RO / Power Signals
- LUT solution
  - After table loading no more setup needed

Conclusions

- DIF Prototype Board connected to PC through USB
- Fast Command Decoder and Signal Generator ready for testing
- Simple Standard Command Decoder and Signal Generator ready for testing
- Slow Control Data transfer to DIF, loading to ASIC's and reading back ready for testing
- Simple SPI Command transfer ready for testing
- Data Readout in progress