

DIF Firmware

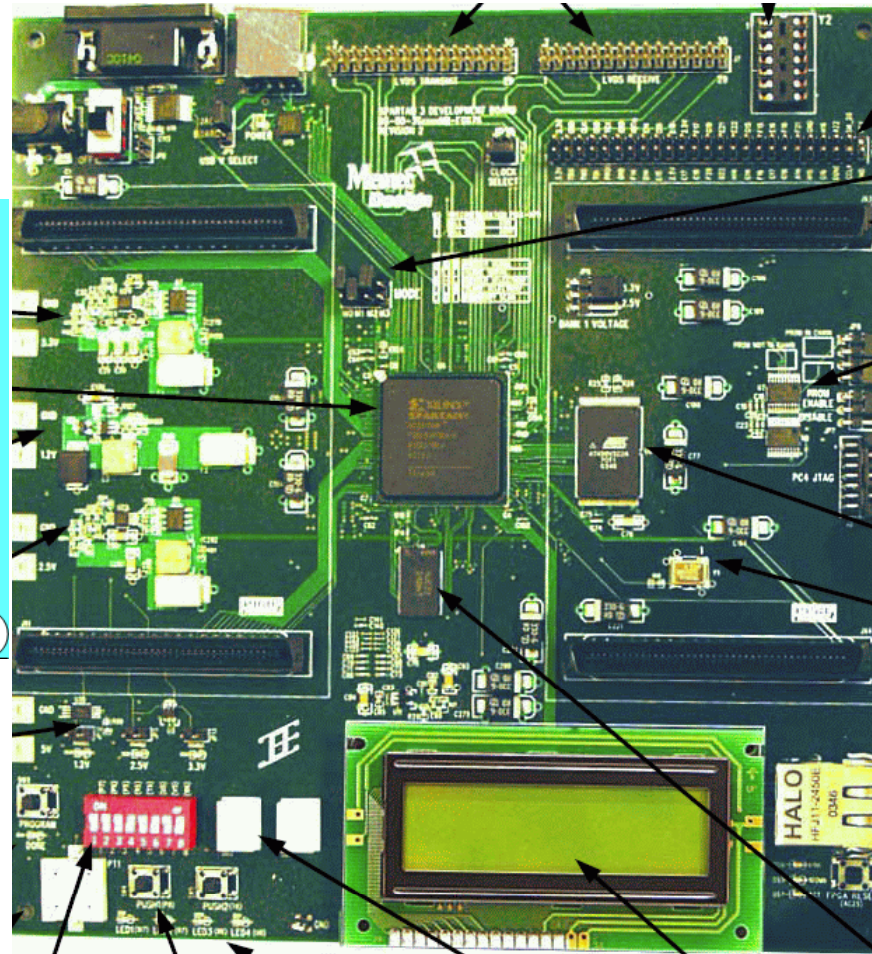
Real or Virtual?

Status and Comments

Presented by Frantisek Krivan



- DIF Commands Proposal - Mathias Reinecke
- DIF ASIC Timing diagrams - Mathias Reinecke
- DIF Development for ECAL, DCAL
- SPIROC I. and II. Technical Information - Omega Webpage
- Calice LDA Docs - Marc Kelly
- Format of the read-out data of the DIF - Remi Cornat
- E-mail discussions
- Spartan Docs, USB Docs, SPI Docs, ...
- ...



Imagine there's
(no) LDA
it's easy
if you try,
...

Imagine there's
(no) SPIROC
it's easy
if you try,
...

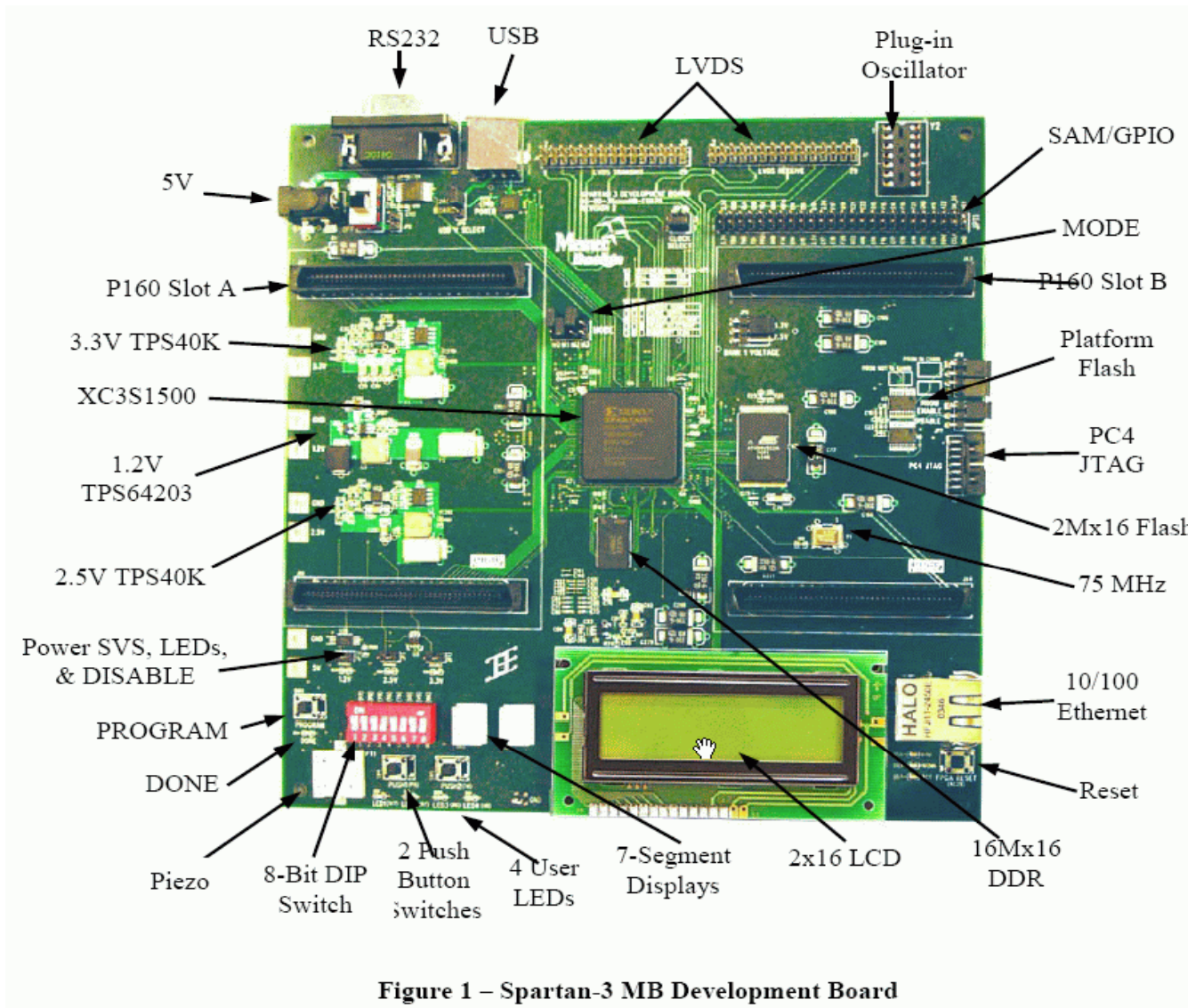
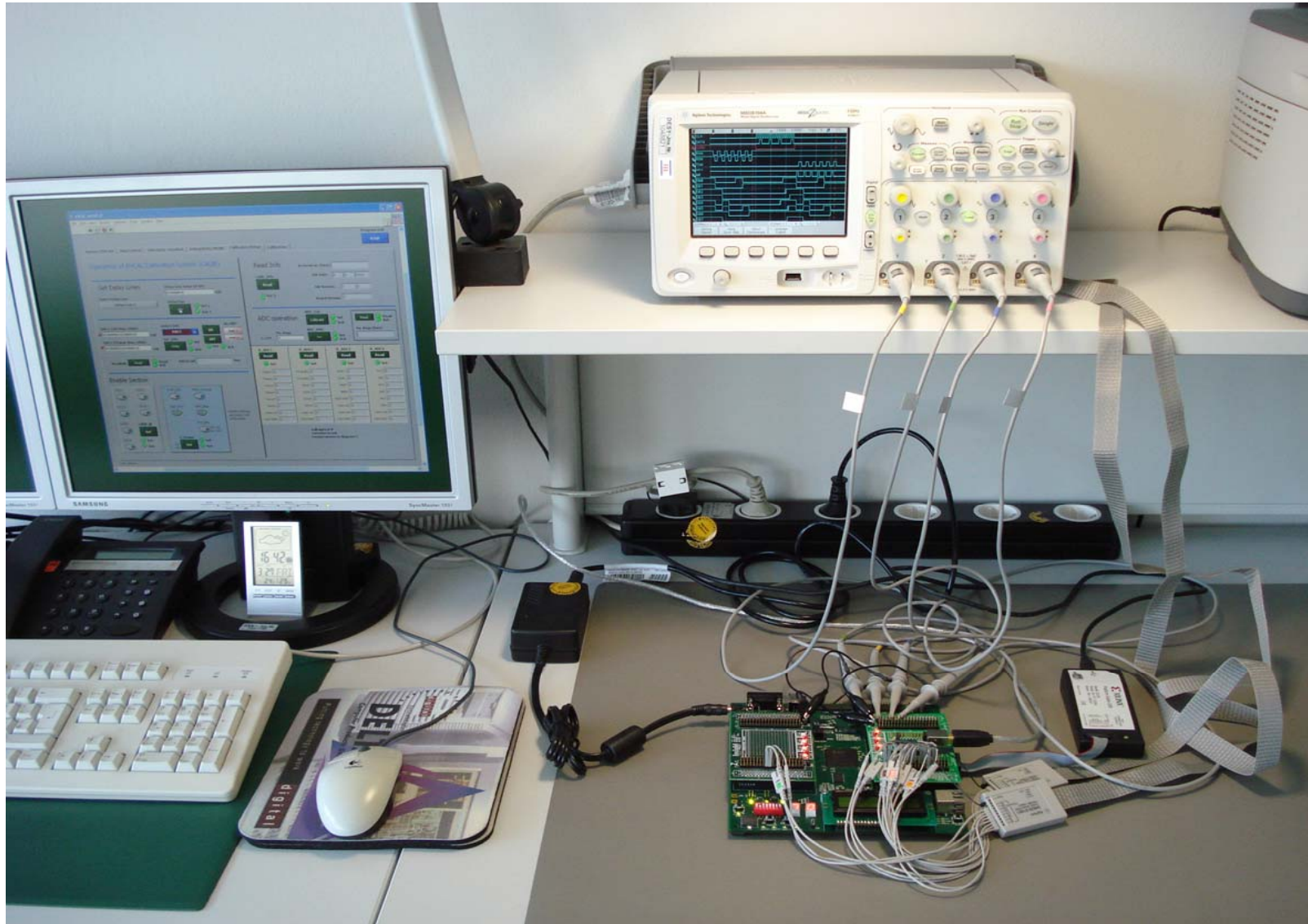
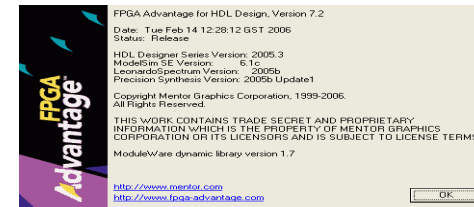
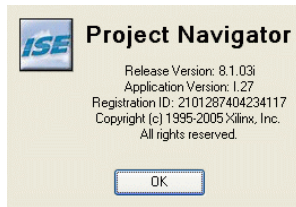


Figure 1 – Spartan-3 MB Development Board



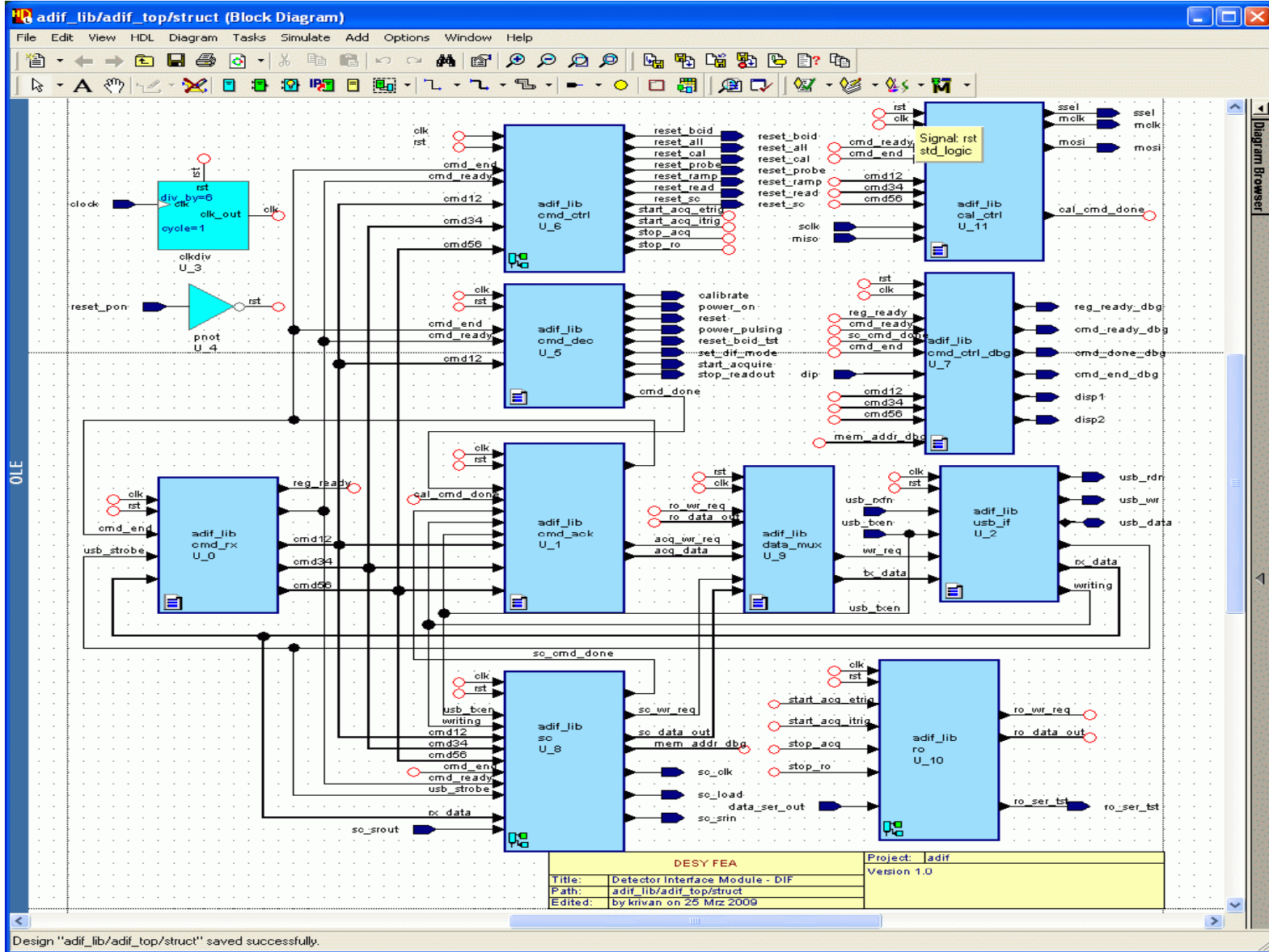


The screenshot displays a multi-window software environment. On the left, a LabVIEW front panel titled "Operation of AHCAL Calibration System (CALIB)" is visible, featuring various control elements like "Set Delay Lines", "ADC operation", and "Enable Section". In the center, the ISE Project Navigator window shows the project structure for "adif". On the right, the Xilinx ISE Design Explorer window is open, displaying a logic diagram and a code browser with VHDL code for a state machine.

```

73 SIGNAL slab_index : UNSIGNED(1 DOWNTO 0);
74 SIGNAL asic_index : UNSIGNED(4 DOWNTO 0);
75
76 SIGNAL byte_index : UNSIGNED(7 DOWNTO 0);
77 SIGNAL bit_index : UNSIGNED(2 DOWNTO 0);
78
79 BEGIN
80   mem_clk <= clk;
81   mem_addr <= mem_addr_int;
82   mem_addr_dbg <= mem_addr_int;
83   mem_data <= mem_data_int;
84   mem_data_dbg <= mem_data_int;
85   mem_data_loaded <= mem_data_loaded_int;
86   mem_data_loaded_dbg <= mem_data_loaded_int;
87   mem_data_loaded_int <= mem_data_loaded_int;
88   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
89   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
90   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
91   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
92   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
93   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
94   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
95   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
96   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
97   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
98   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
99   mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
100  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
101  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
102  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
103  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
104  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
105  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
106  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
107  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
108  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
109  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
110  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
111  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;
112  mem_data_loaded_int_dbg <= mem_data_loaded_int_dbg;

```



ahcal_vers6.vi

File Edit View Project Operate Tools Window Help

System/USB Init Slow Control Take Data / Readout Debug READ, PROBE Calibration Setup Calibration

Operation of AHCAL Calibration System (CALIB)

Set Delay Lines

Delay Line Value (8-bit) 01001101 LSB

Select Delay Line Delay Line 2

DelayLine Set Set 2 Ack 2

DAC1 (LED Bias, 16bit) 0100000101000010 LSB

DAC2 (Charge Bias, 16bit) 0100000101000010 LSB

Select DAC DAC2 ON OFF DAC1 DAC2

Set_DAC Write Set Ack Set Ack

ReadDAC Read Read Ack DACRead hex

Enable Section

LVDS1 LVDS5 PWR_LED PWR_Charge

LVDS2 LVDS6 Slab_Pow SIPM_Bias

LVDS3 LVDS all Set

LVDS4 Set Ack

Pre_Bias off: 10V on: full V

C_Power Set ALL Set Ack

Define settings and press 'Set' afterwards

Read Info

Si Serial no. (hex)

SW Date 0 0 0000

SW Version 0 0

Board Version 0

ADC operation

ADC_Cal Calibrate Set Ack Read Read Ack

ADC_AVG No. Avgs 1.255 1 Set Set Ack

R_ADC1	R_ADC2	R_ADC3	R_ADC4
Temp1 0	VCALIB1 0	VDAC 0	HV1 0
Temp2 0	VCALIB2 0	IDAC 0	HI1 0
Temp3 0	VDDD 0	VREF 0	HV2 0
Temp4 0	IDDD 0	IREF 0	HI2 0
Temp5 0	VDDA 0	VADCREf 0	HV3 0
Temp6 0	IDDA 0	reserved 0	HI3 0
reserved 0	reserved 0	reserved 0	reserved 0
VADCREf 0	VADCREf 0	VADCREf 0	VADCREf 0

voltages in V
currents in mA
temperatures in degrees C

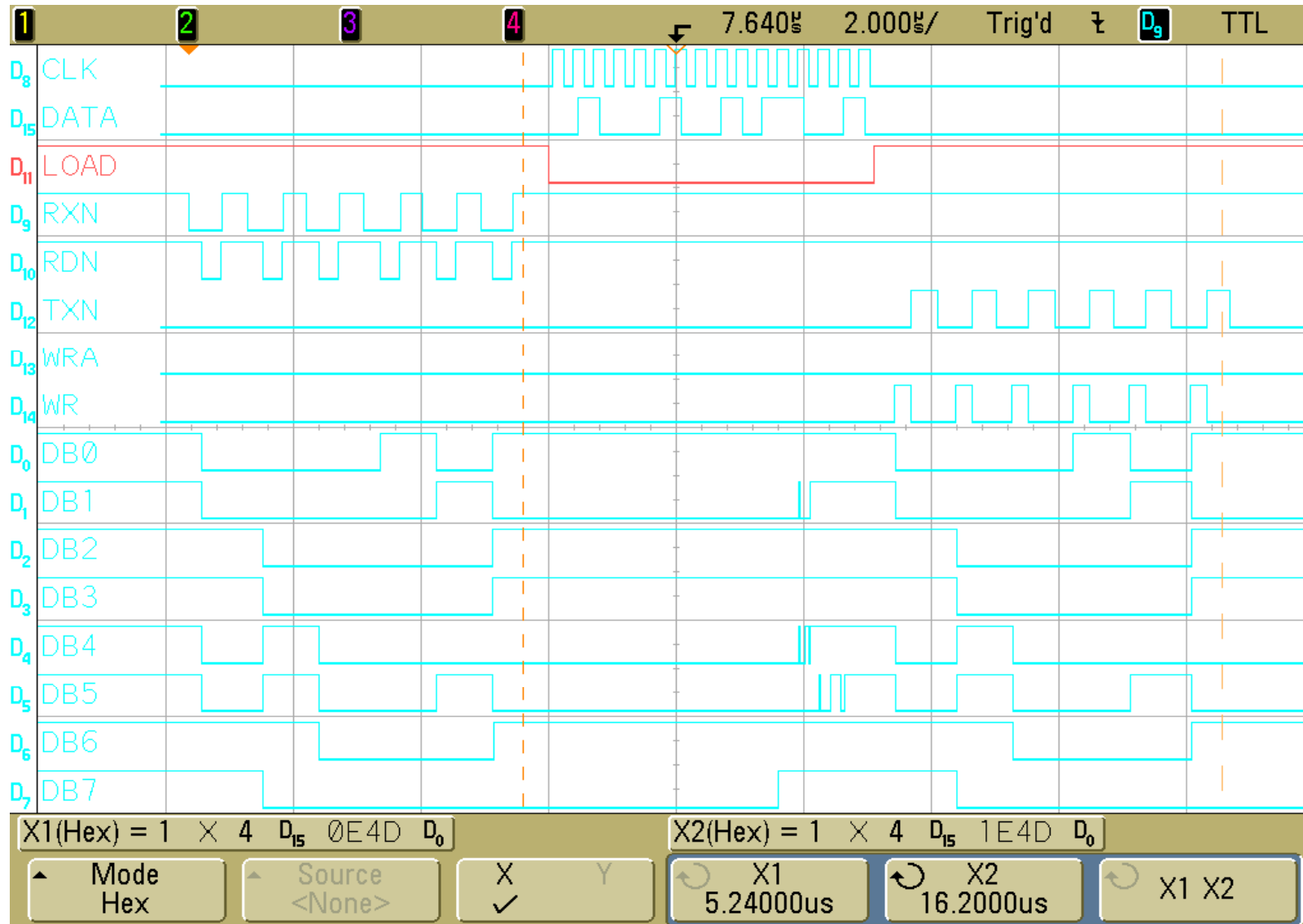
Tab Control

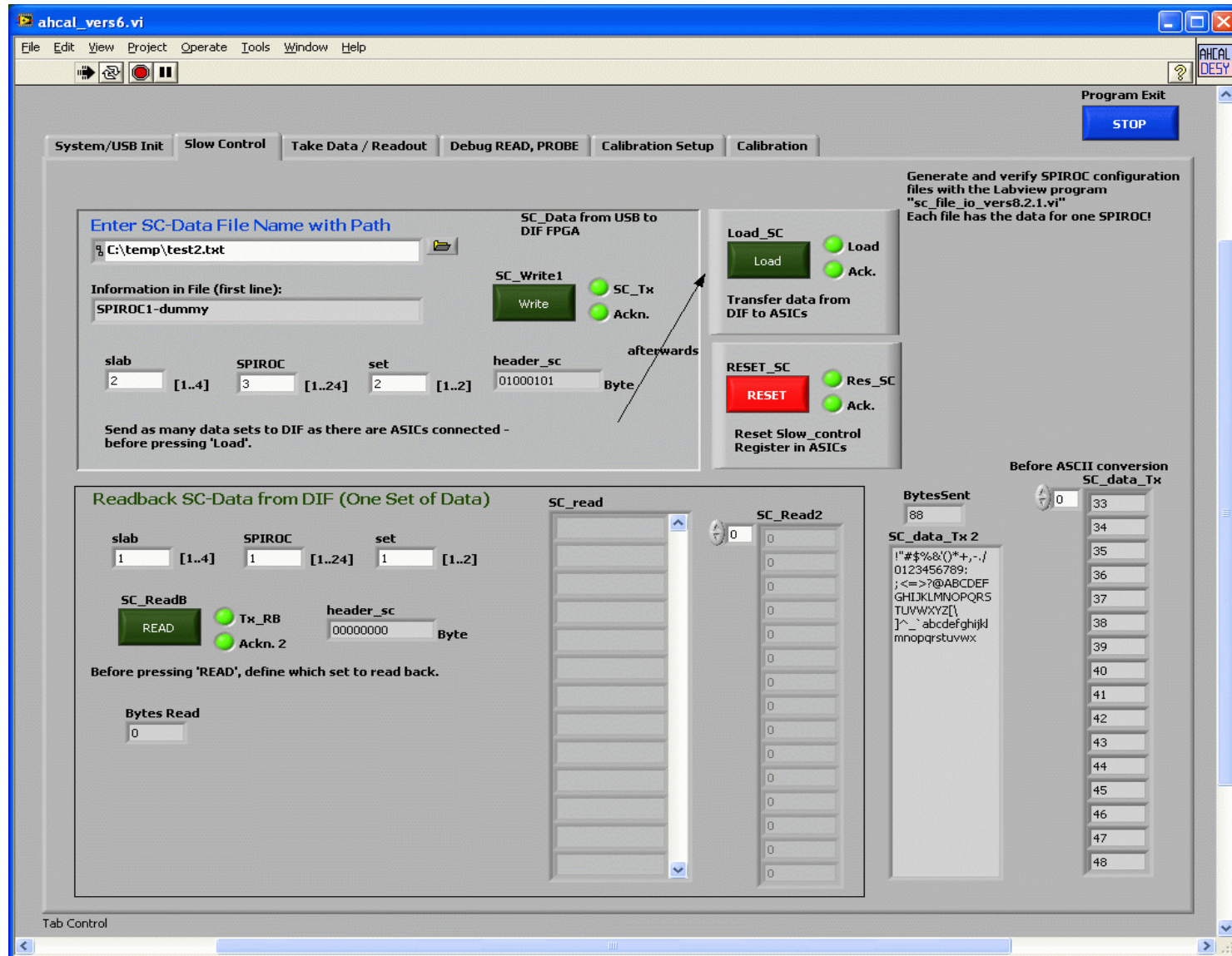
SPI Commands Table (Part)



SPI Commands for CALIB Board from DIF Board					
Command:	Hex	Data		Return Value	
Group 1:			System informationen		
Read Silicon Serial Number	0x11	--	--	6 Byte	SiliconNumber
Read Software data	0x12	--	--	4 Byte	Datum: DD MM JJJJ
Read Software version	0x13	--	--	1 Byte	0.0 - 15.15 (0xFF)
Read Board version	0x14	--	--	1 Byte	0 - 31
Group 2:			Set Delay Line		
Set DelayLine 1	0x21	1 Byte	0-255	--	--
Set DelayLine 2	0x22	1 Byte	0-255	--	--
Set DelayLine 3	0x23	1 Byte	0-255	--	--
Group 3:			Enable Transmitter and Power		
Enable LVDS Repeat en_1	0x31	1 Byte	0 or 1	--	--
Enable LVDSTransm. en_2	0x32	1 Byte	0 or 1	--	--
Enable LVDSTransm. en_3	0x33	1 Byte	0 or 1	--	--

SPI Command Example

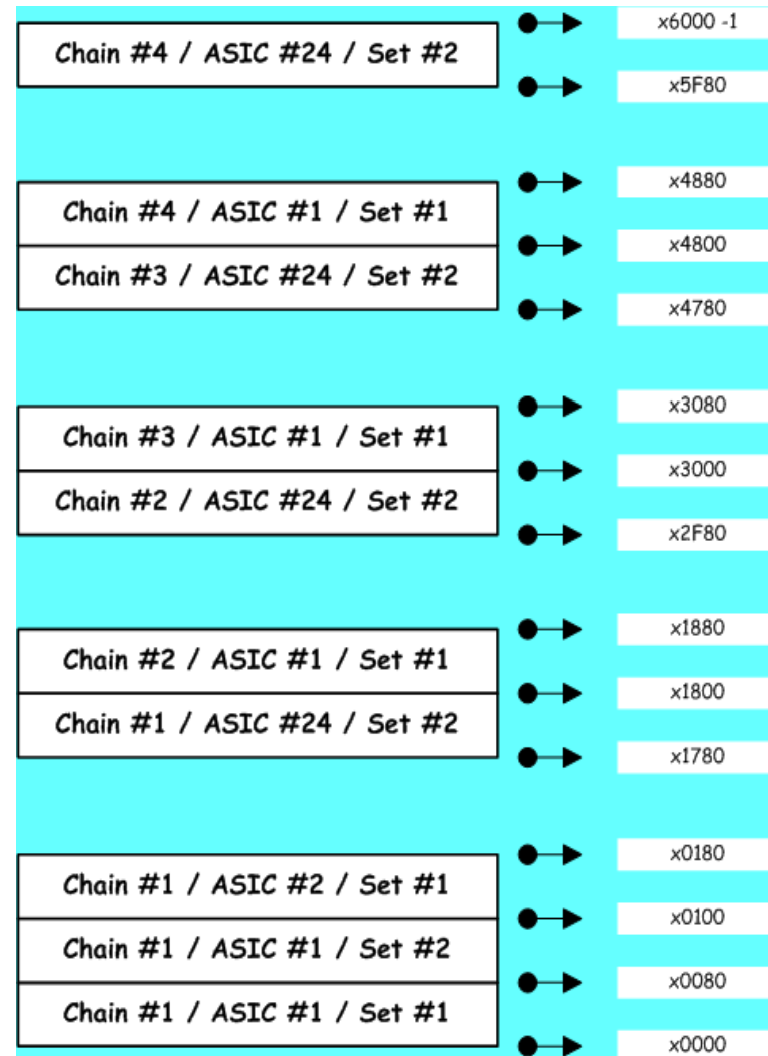




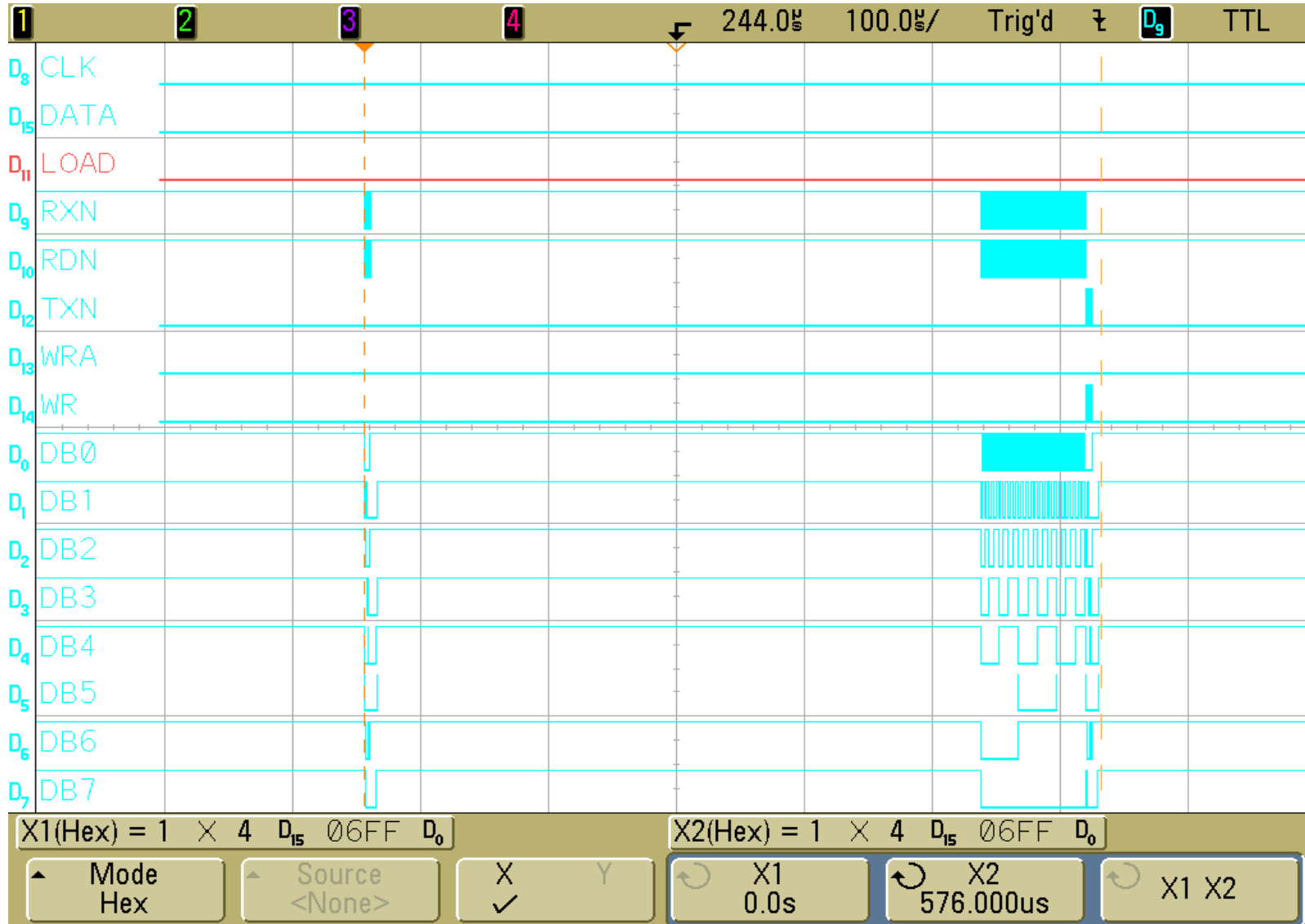
The screenshot shows the LabView interface for 'ahcal_vers6.vi'. It features a menu bar (File, Edit, View, Project, Operate, Tools, Window, Help) and a toolbar with icons for Run, Stop, and Help. The main interface is divided into several functional areas:

- System/USB Init**: A tab at the top left.
- Slow Control**: A tab at the top left.
- Take Data / Readout**: A tab at the top left.
- Debug READ, PROBE**: A tab at the top left.
- Calibration Setup**: A tab at the top left.
- Calibration**: A tab at the top left.
- Program Exit**: A button with a 'STOP' label.
- Enter SC-Data File Name with Path**: A text input field containing 'C:\temp\test2.txt'.
- Information in File (first line):**: A text input field containing 'SPIROC1-dummy'.
- slab**: A numeric input field with '2' and a range of '[1..4]'.
- SPIROC**: A numeric input field with '3' and a range of '[1..24]'.
- set**: A numeric input field with '2' and a range of '[1..2]'.
- header_sc**: A text input field with '01000101' and a unit of 'Byte'.
- SC_Write1**: A 'Write' button with 'SC_Tx' and 'Ackn.' indicators.
- Load_SC**: A 'Load' button with 'Load' and 'Ack.' indicators.
- RESET_SC**: A 'RESET' button with 'Res_SC' and 'Ack.' indicators.
- Transfer data from DIF to ASICs**: Text label for the Load_SC section.
- Reset Slow_control Register in ASICs**: Text label for the RESET_SC section.
- Generate and verify SPIROC configuration files with the Labview program "sc_file_io_vers8.2.1.vi"**: Text label for the Load_SC section.
- Each file has the data for one SPIROC!**: Text label for the Load_SC section.
- Readback SC-Data from DIF (One Set of Data)**: A section with its own 'slab', 'SPIROC', and 'set' inputs, a 'SC_ReadB' 'READ' button, and 'Tx_RB' and 'Ackn. 2' indicators.
- header_sc**: A text input field with '00000000' and a unit of 'Byte'.
- Bytes Read**: A numeric input field with '0'.
- Before pressing 'READ', define which set to read back.**: Text label for the Readback section.
- SC_read**: A vertical list of 10 numeric input fields, all set to '0'.
- SC_Read2**: A vertical list of 10 numeric input fields, all set to '0'.
- BytesSent**: A numeric input field with '88'.
- Before ASCII conversion SC_data_Tx**: A vertical list of 16 numeric input fields, numbered 33 to 48.
- SC_data_Tx 2**: A text area containing a string of characters: '!"#%&()*+,-./0123456789:;<=>@ABCDEF GHIJKLMNOPSRTUVWXYZ[]^_`abcdefghijklmnopqrstuvwxyz'.

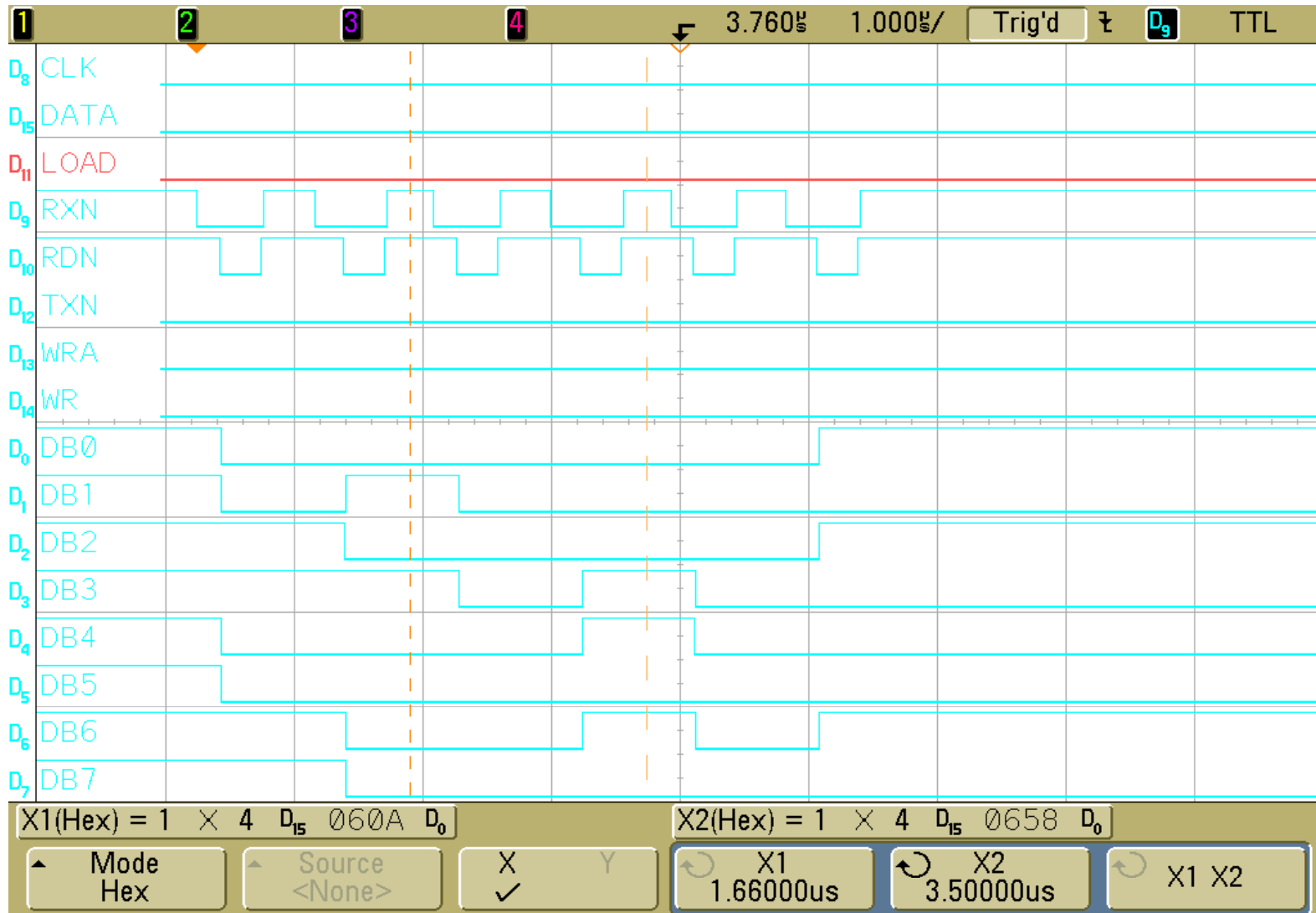
- ❑ Parameters Size
 - ❑ Chain 1 - 4
 - ❑ ASIC 1 - 24
 - ❑ Set 1 -2
- ❑ Alternate versus Continual Mapping
 - ❑ Alternate Set 1/2
 - ❑ Alternate Chain 1/2/3/4
- ❑ Block size 128 bytes - 88 used / 40 free
- ❑ 88 bytes - 704 bits
 - we skip 1 bit from 1 byte



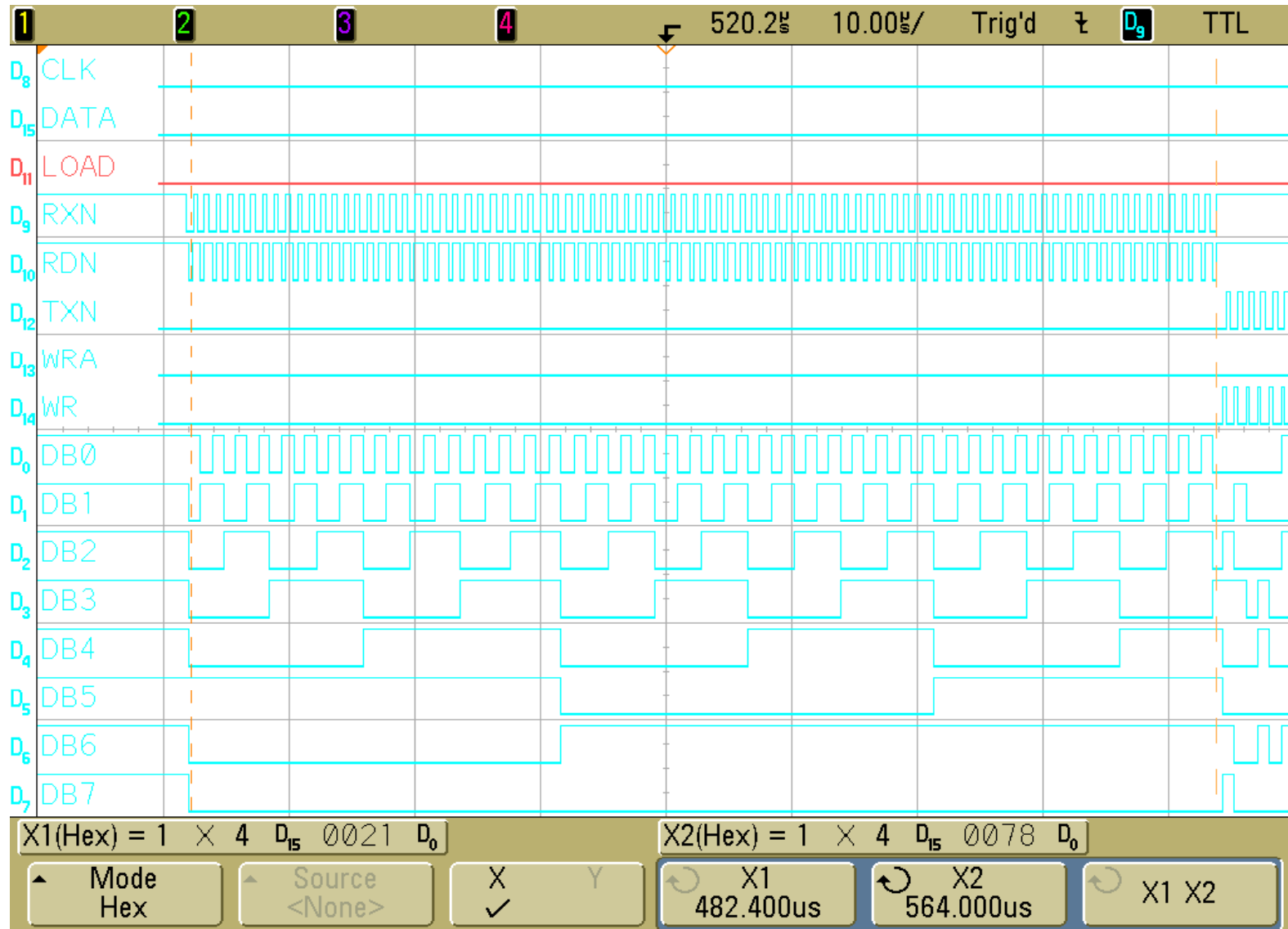
SC USB to DIF



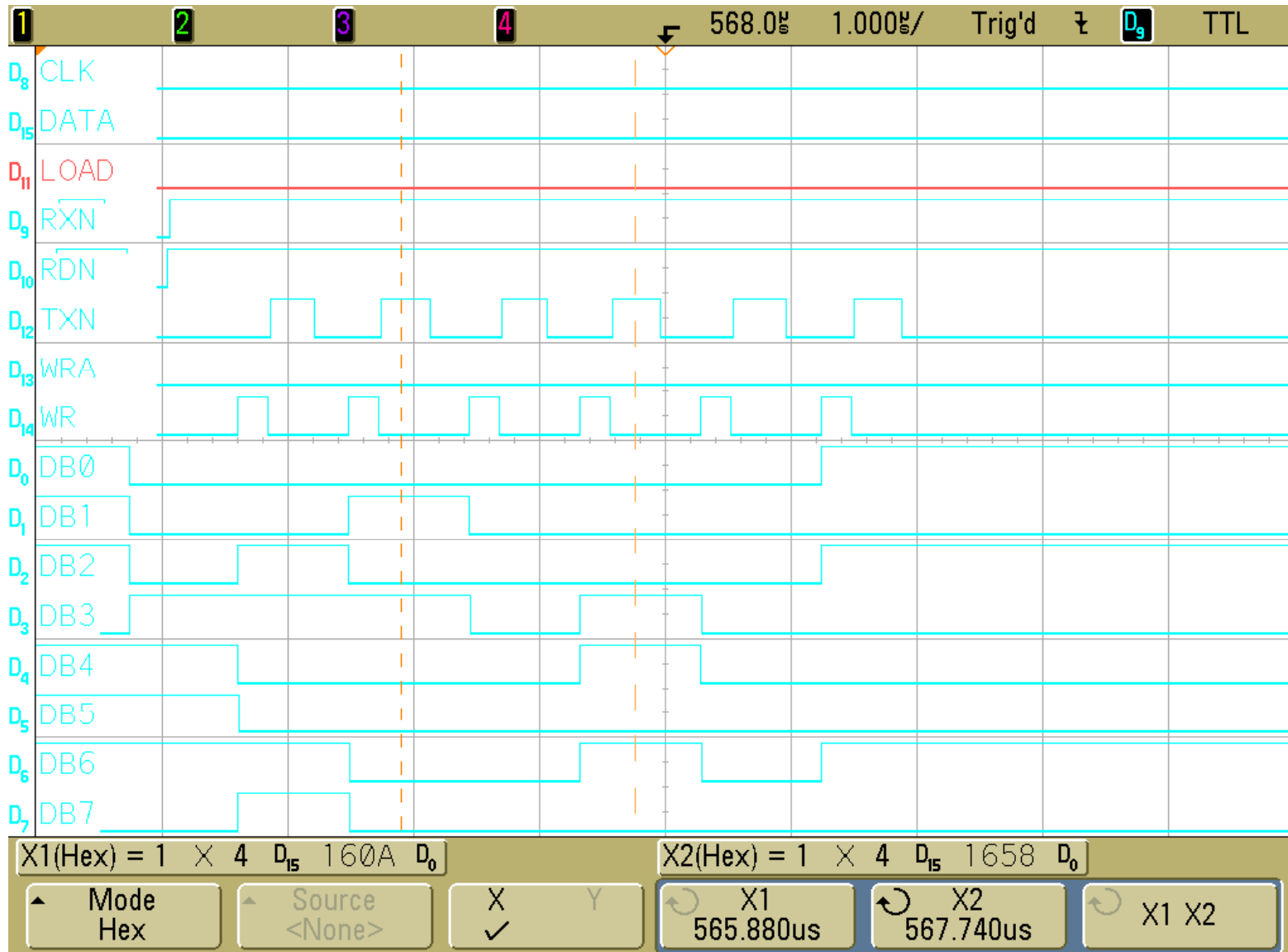
SC USB to DIF – Command Part



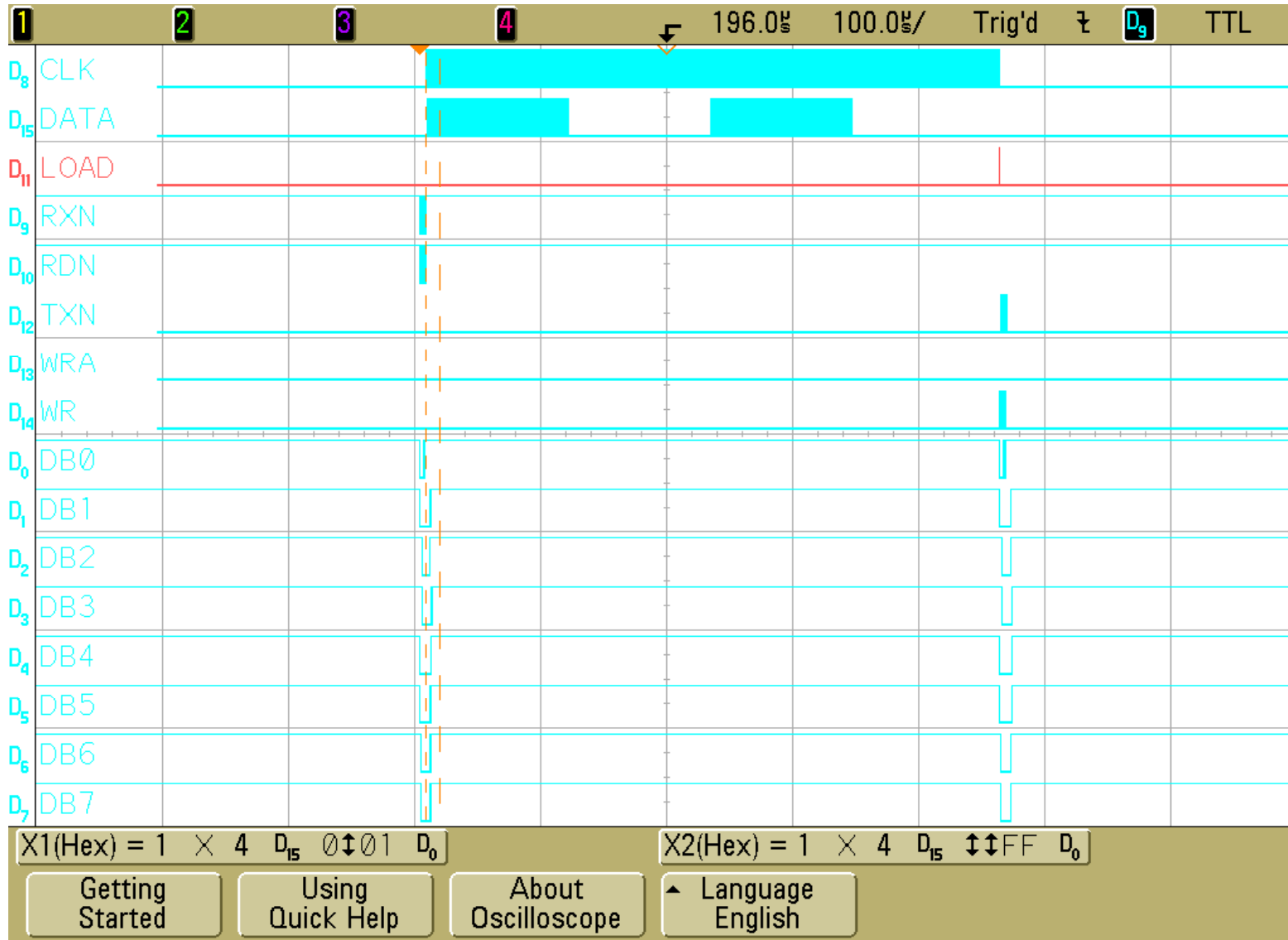
SC USB to DIF - Data Part



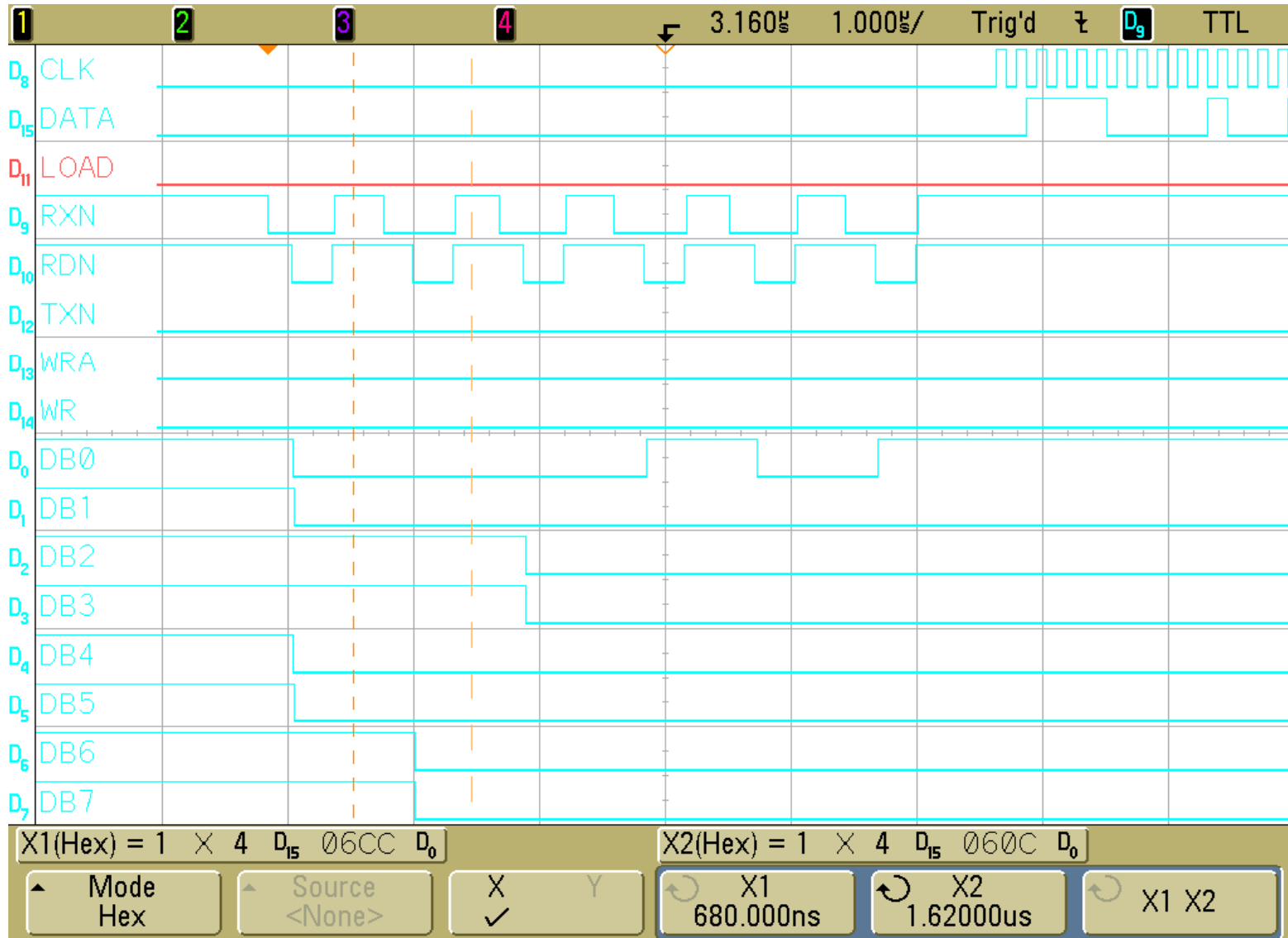
SC USB to DIF - Acknowledge Part



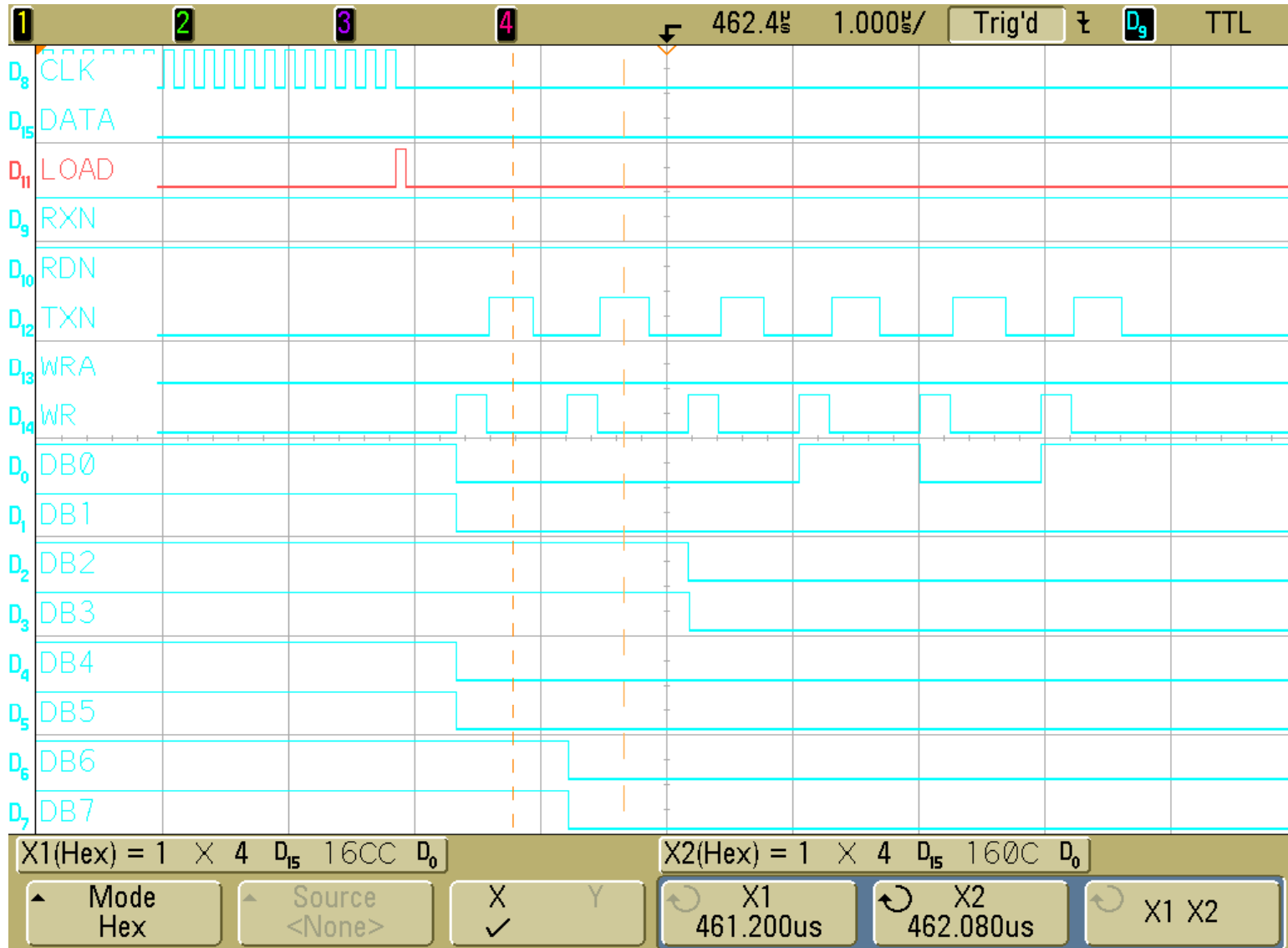
SC Load DIF to ASIC's



SC Load - Command Part



SC Load - Acknowledge Part



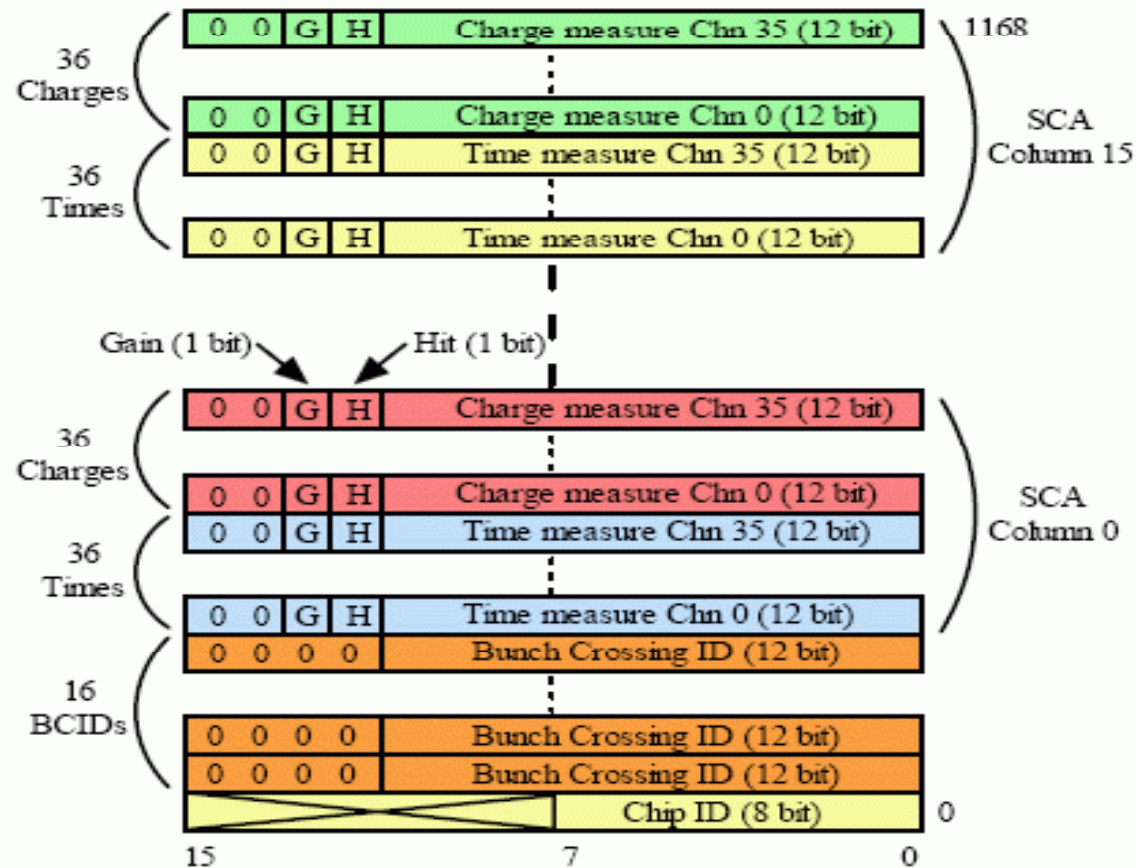
SPIROC RAM MAPPING



DATASHEET

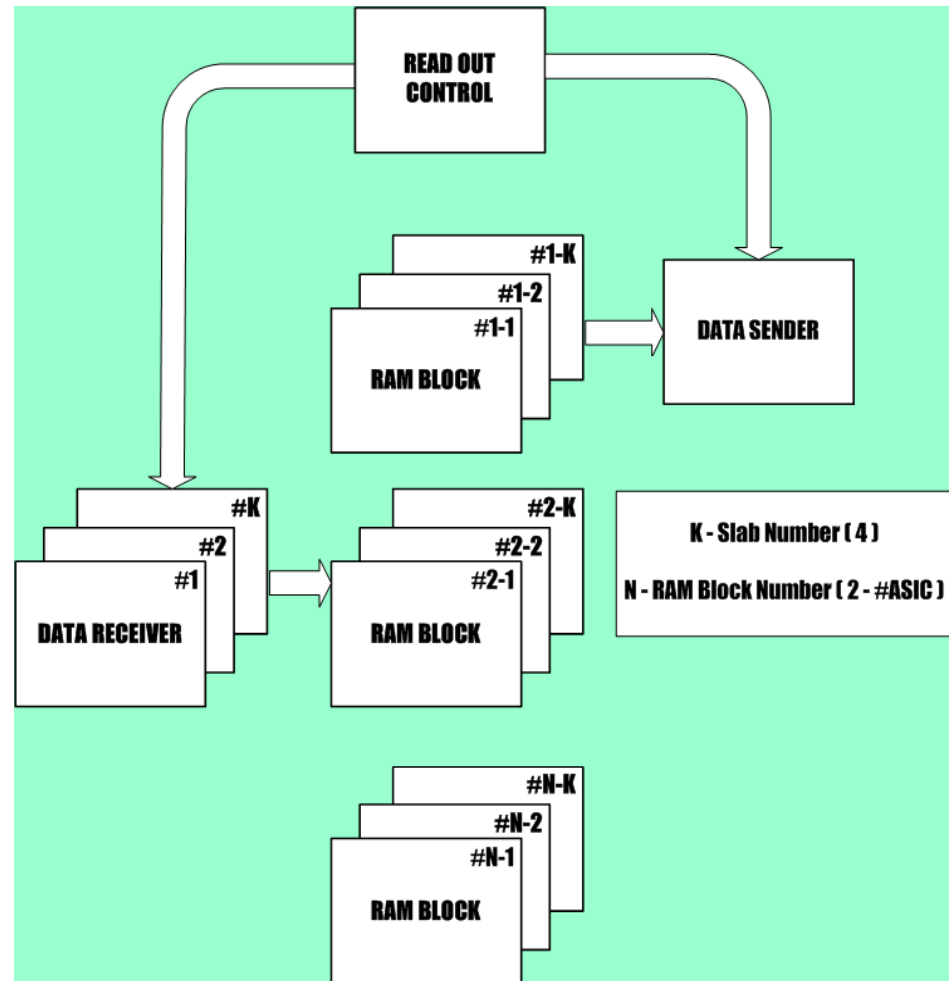


12 Spiroc RAM mapping



- ❑ Dual Port Memory
 - ❑ More effective using of the memory space

- ❑ RAM Block FIFO
 - ❑ Data reordering
 - ❑ Data reduction (global cut, local cut, area cut)



- ❑ Counter solution
 - ❑ Counter step definition (100us - 12bits, 1us - 18bits)
 - ❑ Synchronisation
 - ❑ Register definition (1 ON, 1 OFF, 1 default value)
 - ❑ Common counter for RO / Power Signals
- ❑ LUT solution
 - ❑ After table loading no more setup needed

- ❑ DIF Prototype Board connected to PC through USB
- ❑ Fast Command Decoder and Signal Generator ready for testing
- ❑ Simple Standard Command Decoder and Signal Generator ready for testing
- ❑ Slow Control Data transfer to DIF, loading to ASIC's and reading back ready for testing
- ❑ Simple SPI Command transfer ready for testing
- ❑ Data Readout in progress