DEPFET technology for the ILC: Achievements, latest results and future plans

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On behalf of the DEPFET Collaboration
(www.depfet.org)

DEPFET Collaboration

❖ DEPFET is not only a technology but a Collaboration

- **University of Barcelona**
- **Ramon Llull University**
- **Bonn University**
- **Heidelberg University**
- **Goettingen University**
- **Karlsruhe University**
- **IFJ PAN, Krakow**
- **MPI Munich**
- **Charles University, Prague**
- **IGFAE, Santiago de Compostela University**
- **IFIC, CSIC-UVEG, Valencia**
- **University of Giessen**

www.depfet.org

Outline

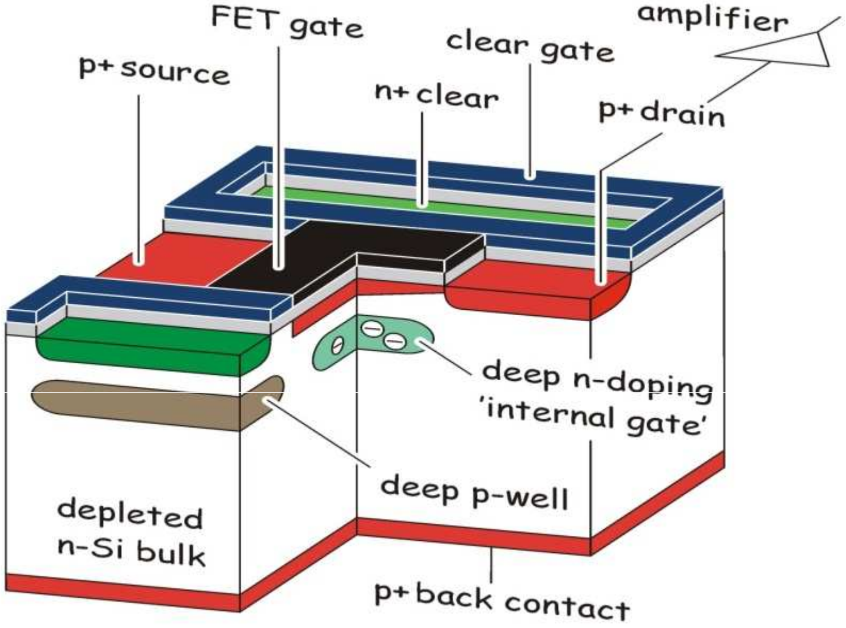
- What is a DEPFET?
- Elements. What’s new?
- Thinning, irradiation, bonding…
- Test Beam campaigns 2008 and 2009
- Conection ILC - Belle-II
- Summary and Conclusions

DEPFET – DEpleted P-channel Field Effect Transistor

- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)

- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 600 pA/e^-$)
- Accumulated charge can be removed by a clear contact

- Internal amplification
- Low power consumption: Readout on demand (Sensitive all the time, even in OFF state)



GOAL

- o Small pixel size ~25µm
- o r/o per row ~50ns (20MHz) (drain)→Fully depleted bulk
- o Noise≈40e^- at high bandwith→Small capacitance and first in-pixel amplification
- o Thin Detectors≈50µm

ILC S3b prototype system

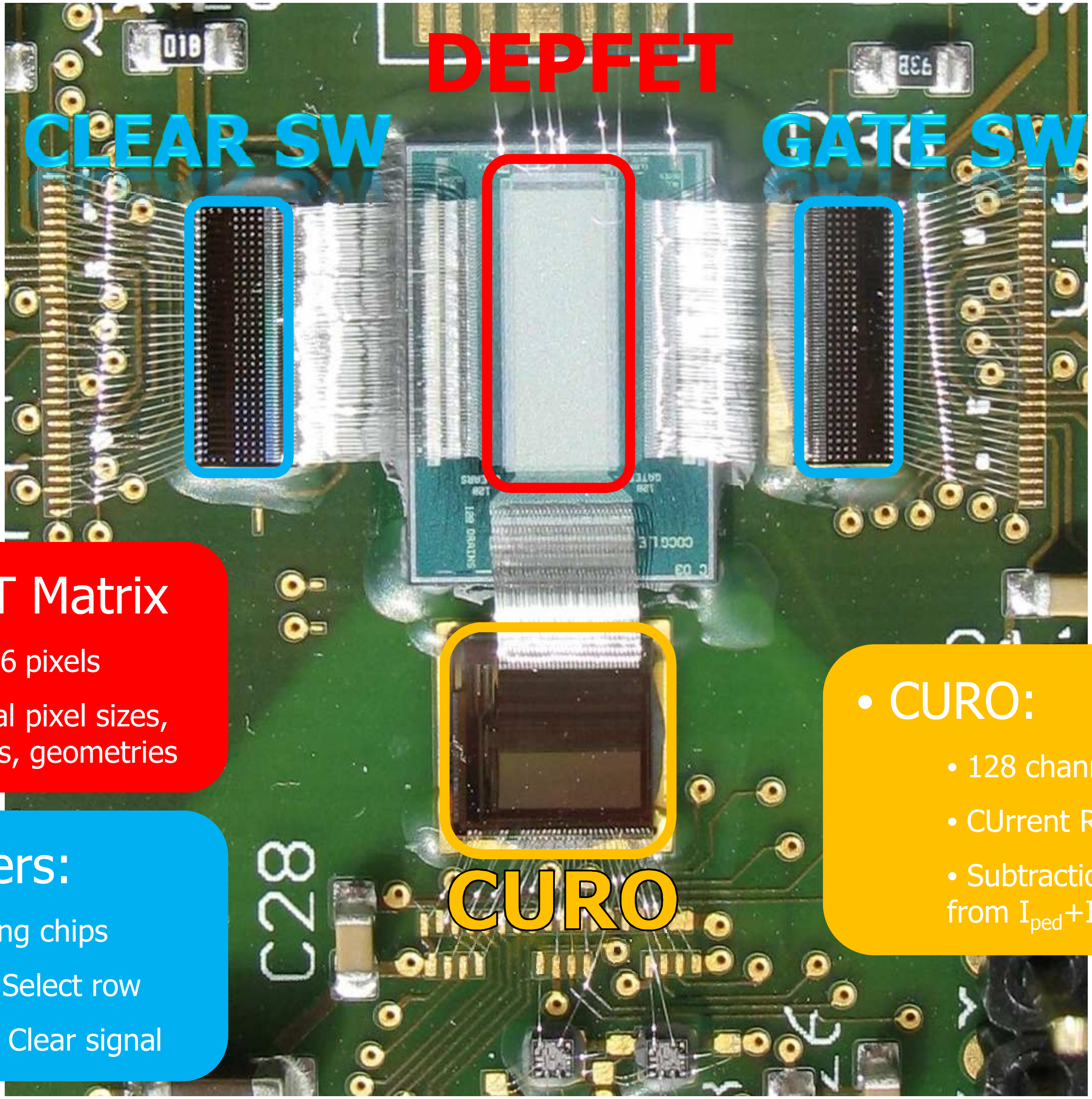
•Hybrid Board

- DEPFET 64x256 matrix
- Readout chip (CURO)
- Steering chips (Switchers)

•S3b Readout Board

- ADCs→Digitization
- FPGA→Chip config. and synchronization during DAQ
- RAM→Data storage
- USB 2.0 board→PC comm.

Hybrid board

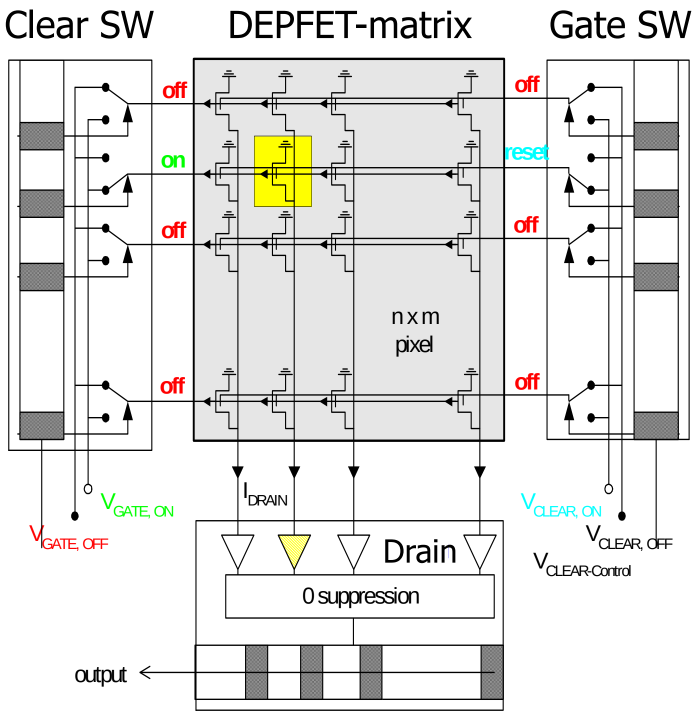


- DEPFET Matrix
  - 64x256 pixels
  - Several pixel sizes, implants, geometries

- Switchers:
  - Steering chips
  - Gate: Select row
  - Clear: Clear signal

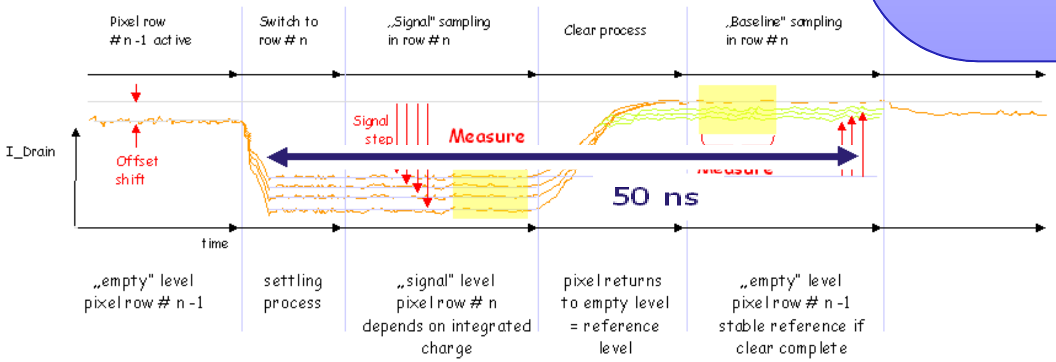
- CURO:
  - 128 channels
  - CUrrent Read Out
  - Subtraction of I_{ped} from $I_{ped}+I_{sig}$

Operation mode: Row wise readout



Row wise r/o (*Rolling Shutter*)

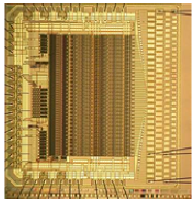
- Select row with external gate, read current, clear DEPFET, read current again → The difference is the signal
- Low power consumption: Only one row active at a time; Readout on demand (Sensitive all the time, even in OFF state)
- Two different auxiliary chips needed (Switchers)
- Limited frame rate



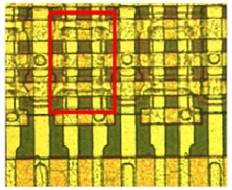
Enable row – Read current (I_{sig} + I_{ped}) – Clear – Read current (I_{ped}), Subtract – Move to next row

The next steps....

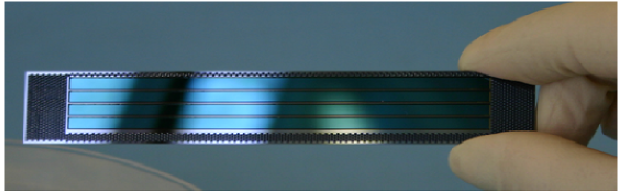
✓ steering chips Switcher

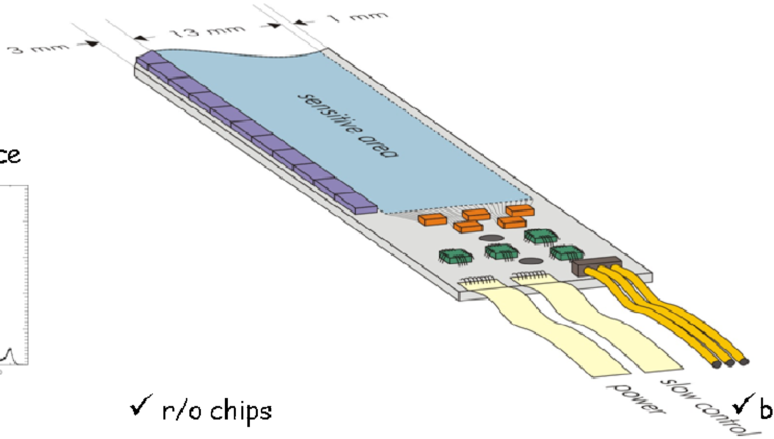


✓ sensor development

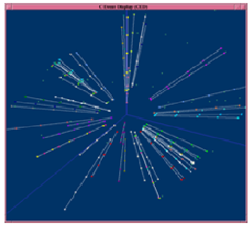


✓ thinning technology

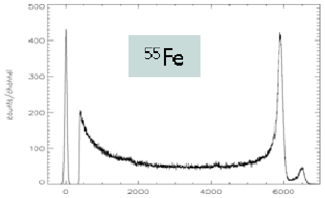




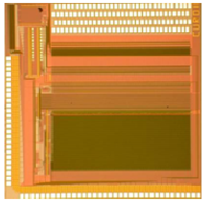
✓ Simulation



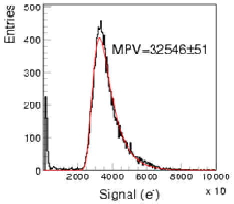
✓ radiation tolerance



✓ r/o chips



✓ beam test

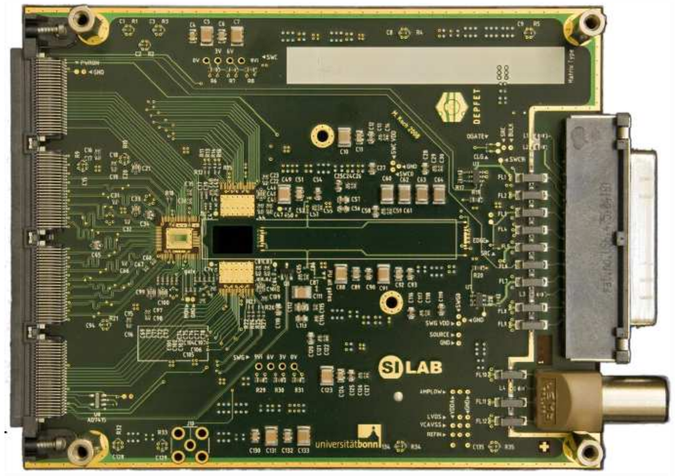


See DEPFET Backup Document at *www.depfet.org*

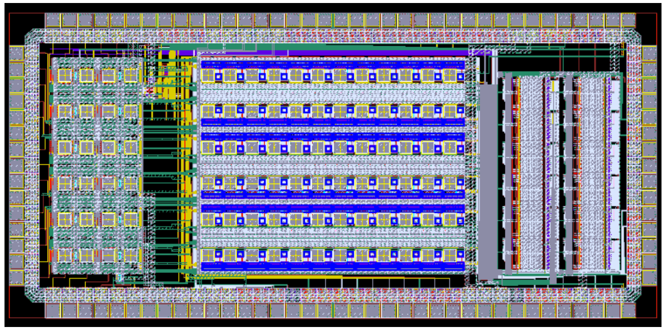
Many years of R&D for the ILC VXD (see review fall 2007)

→The DEPFET is ready to be used in precision vertex detectors

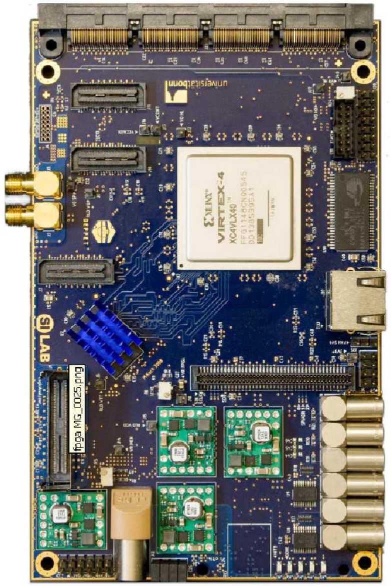
A new r/o chip – DCD (Drain Current Digitizer)



Test chip DCD2: 6X12 channels

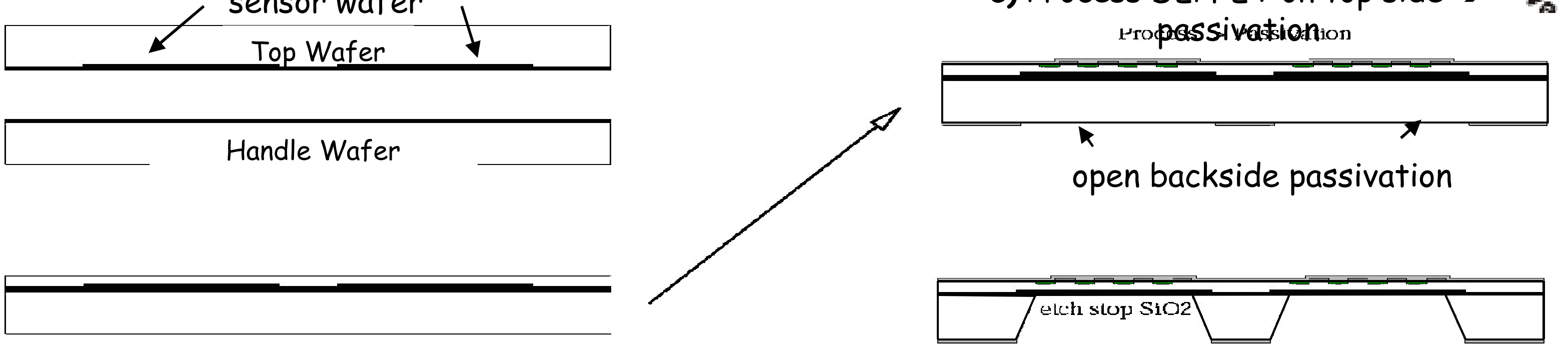


- ➢ Improved input cascode (regulated) and current memory cells
- ➢ Integrated 8bit current based ADC per channel
- ➢ Designed for 40 pF load at the input (5cm Drain line)
- ➢ Layout for bump bonding, radiation hard design
- ➢ Power consumption per channel 2.0 mW (Analog) + 0.8 mW (Digital)
- ➢ Digital hit processing done with second digital chip (DHP)



Thinning technology

a) Oxidation and back side implant on sensor wafer



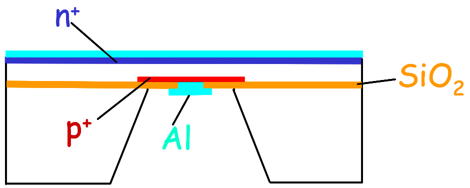
b) Wafer bonding and grinding/polishing of top wafer. Thin sensor side to desired thickness

c) Process DEPFET on top side ➔ passivation

open backside passivation

d) Anisotropic deep etching opens "windows" in handle wafer. Structure resist, etch backside up to oxide/implant

Implants like DEPFET config.



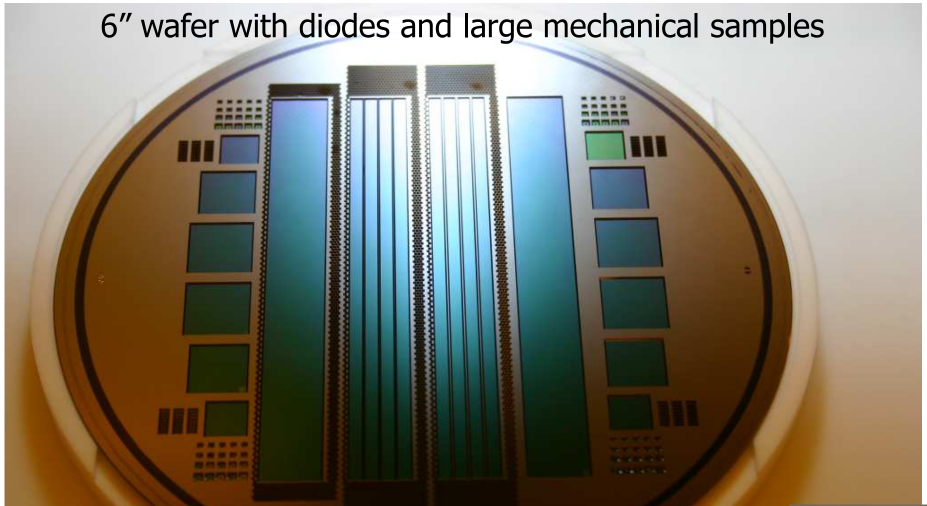
unstructured n+ on top
structured p+ in bond region

- Sensor wafer: high resistivity d=150mm wafer.
- Bonded on low resistivity "handle" wafer".
- 50 μm thickness produced
- Rigid frame for handling and mechanical stiffness

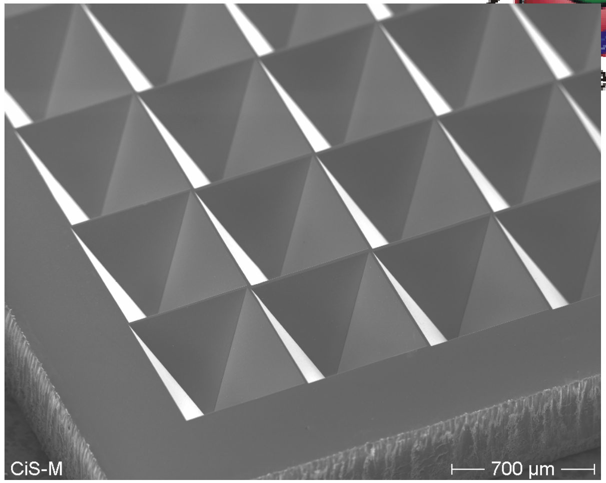
Mature technique (~7 years old):

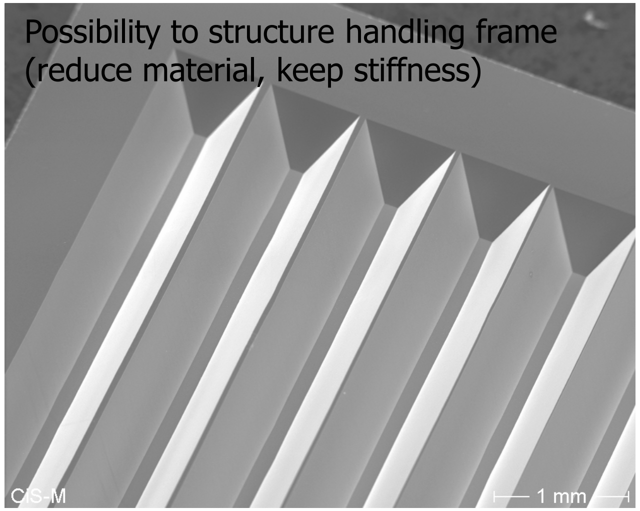
- ILC:
  - ✓ Mechanical samples
- sLHC
  - ✓ Thin (75 and 150 μm) ATLAS pixel sensors
- Tested on diodes with excellent results (low leakage current maintained after thinning)

Thinning : mechanical samples

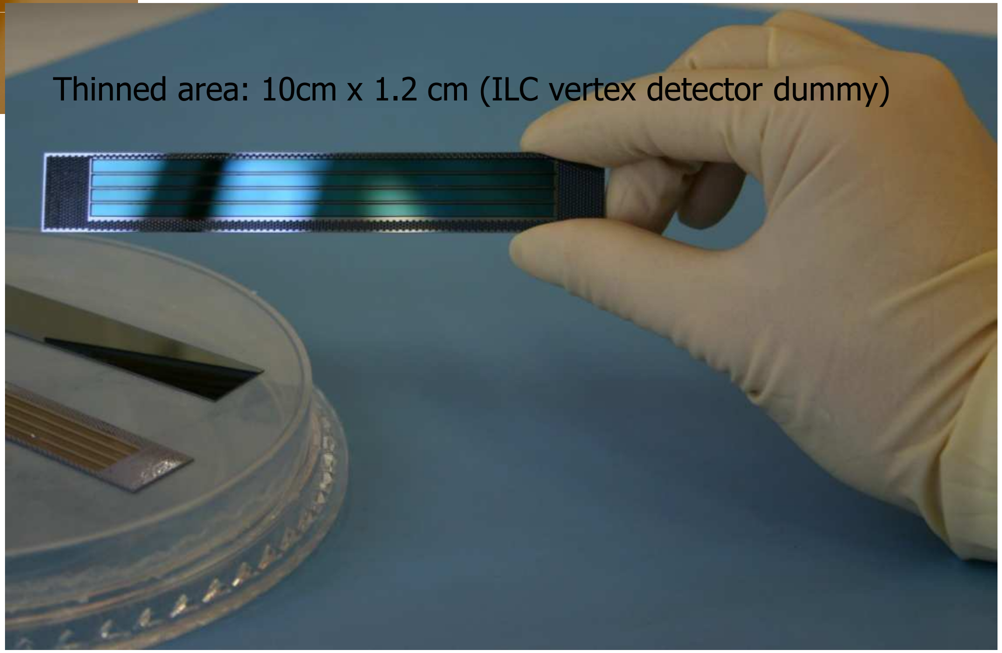


6” wafer with diodes and large mechanical samples



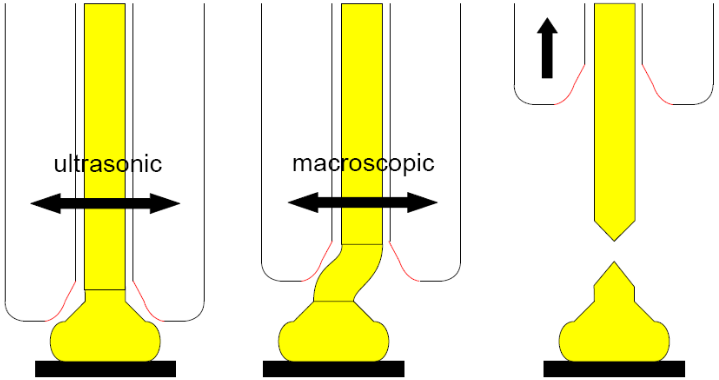


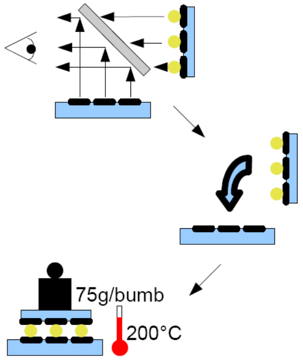
Possibility to structure handling frame
(reduce material, keep stiffness)



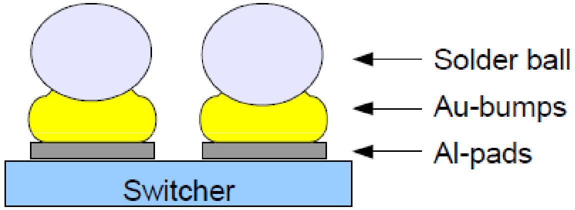
Thinned area: 10cm x 1.2 cm (ILC vertex detector dummy)

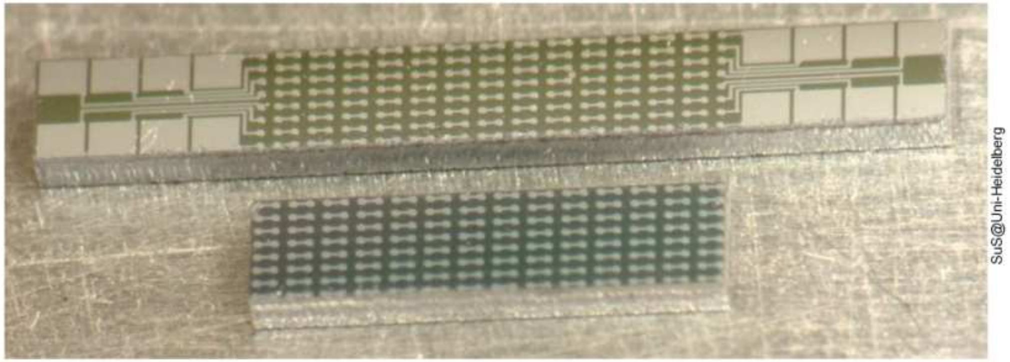
Baseline: Gold Stud Bump Bonding





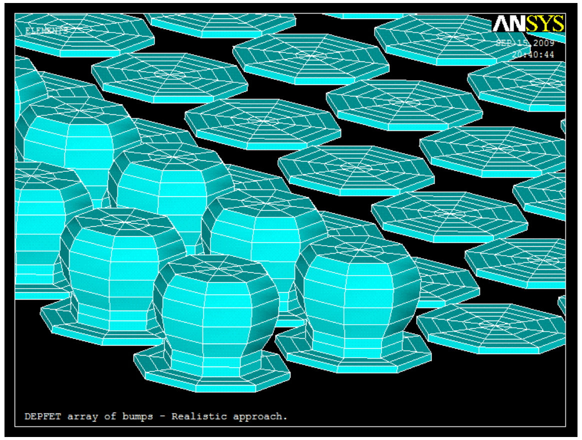
- Capillary presses ball onto Al-bondpad and forms bump
- Ultrasonic to get Au-Al interconnection
- Weakening of wire for break point near the bump
- Pull up capillary, clamp and rip off wire to get tail for next flame-off





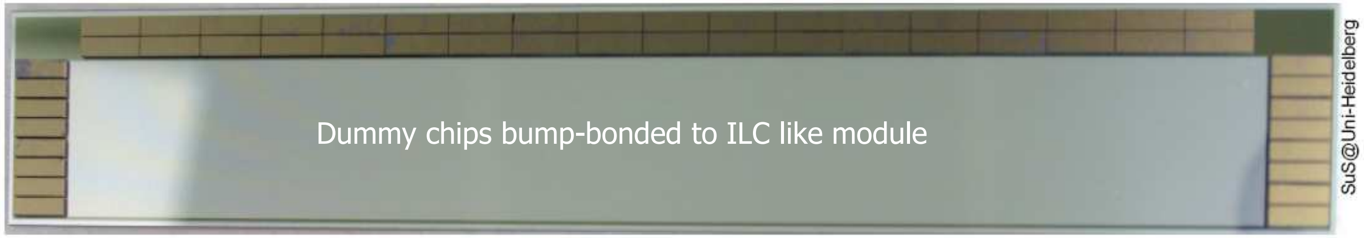
SuS@Uni-Heidelberg

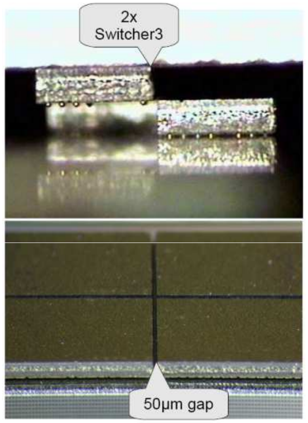
DCD dummy chip and substrate
224 pads



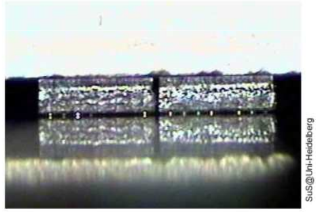
DEPFET array of bumps - Realistic approach.

Baseline: Gold Stud Bump Bonding

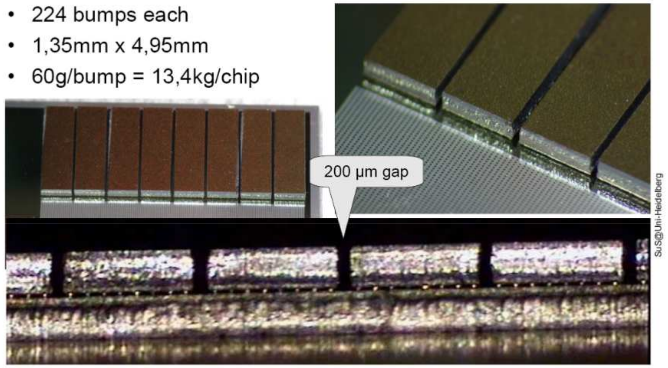

Dummy chips bump-bonded to ILC like module



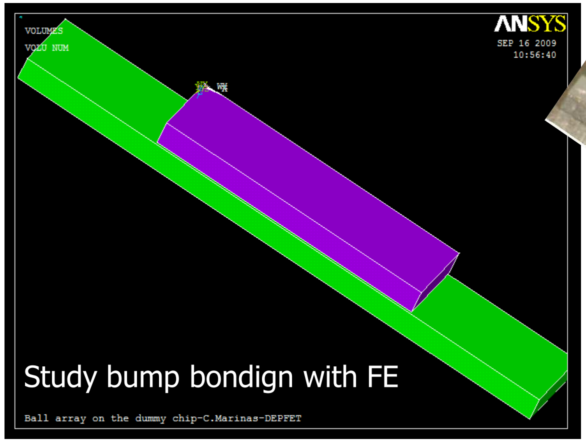
- 36 Switcher3 successfully flipped
- 164 bumps each
- 60g/bump = 9,8kg/chip
- 1,4mm x 5,8mm



- 16 DCD successfully flipped
- 224 bumps each
- 1,35mm x 4,95mm
- 60g/bump = 13,4kg/chip

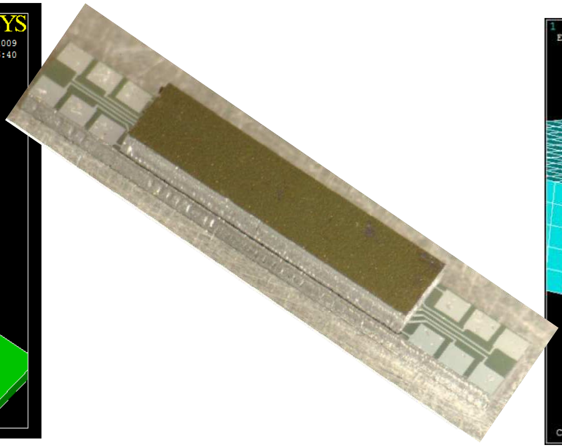


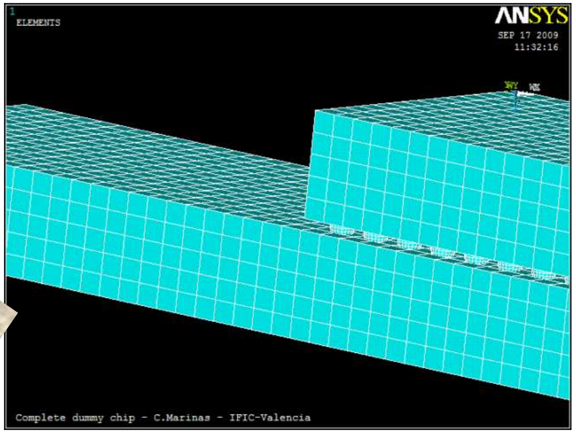
6 of 8 DCDs on the short balcony of one end of the ILC module



Study bump bondign with FE

Ball array on the dummy chip-C.Marinas-DEPFET





Complete dummy chip - C.Marinas - IFIC-Valencia

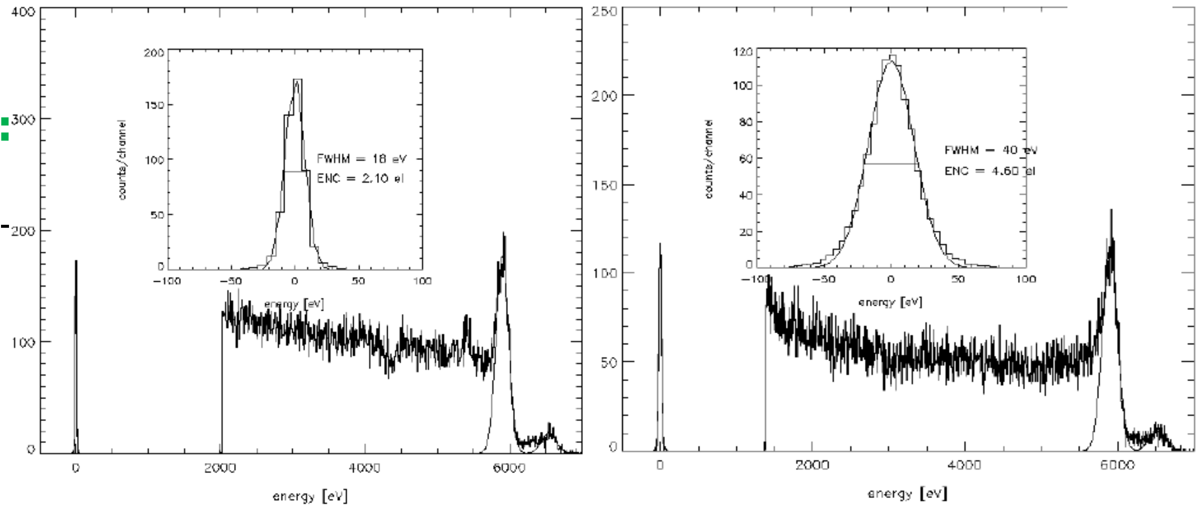
Irradiations

✓ Non ionizing Energy Loss (NIEL)
  - Leakage current increase -> shot noise
  - Trapping not critical

✓ Ionizing radiation – Total Ionizing dose (TID)
  - 2 MOS gates (Gate, Clear Gate) susceptible to be damaged
  - Fixed oxide positive charge -> ΔV_T
  - Interface trap density
    - ➢ Reduced mobility (g_m)
    - ➢ Higher 1/f noise

$$ENC = \sqrt{\underbrace{\alpha \frac{8kTg_m}{3g_q^2}\frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2}_{1/f} + \underbrace{qI_{Leak}\tau}_{I_L}}$$

Unirradiated:
τ=10μs T=RT
ENC_{noi} = 2.1e$^-$



4 MRad X-Ray
τ=10μs T=RT
ENC_{noi} = 4.6e$^-$

- DEPFET will work well for ILC doses

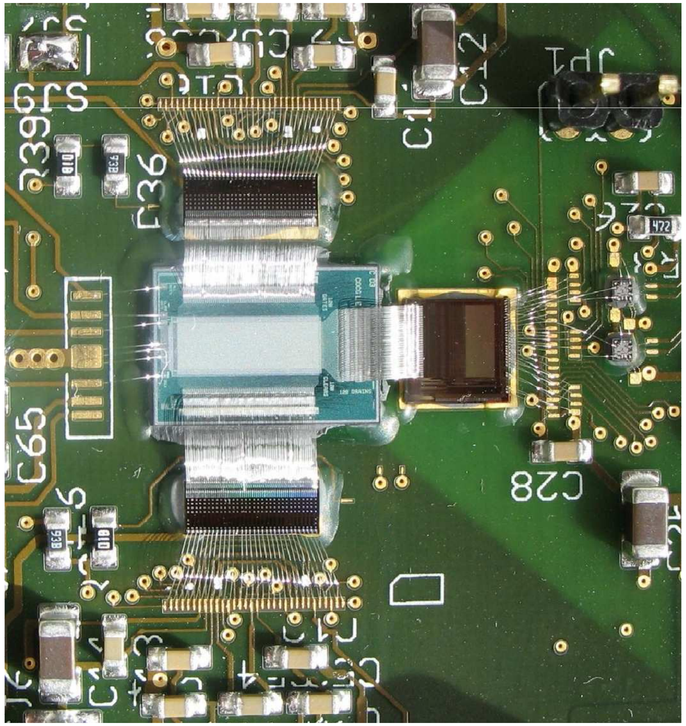
The latest DEPFET Generation ‘PXD5’

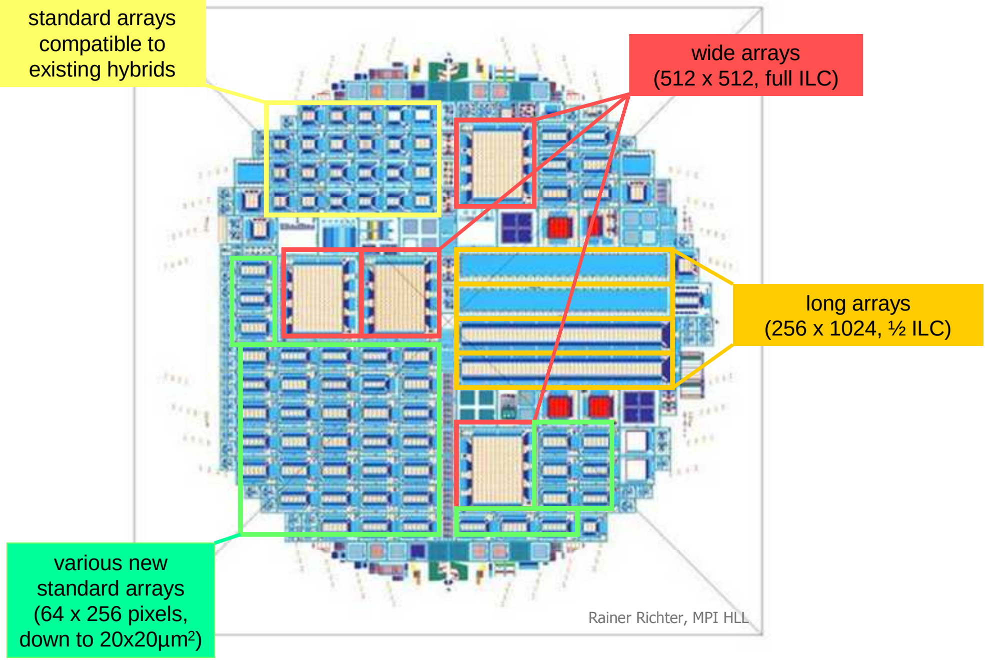
❑ Longer matrices (256x64 pixels)

❑ New DEPFET variants:

→ **Test Beam 2009 at CERN**

- ✓ Very small pixels (20µm x 20µm)
- ✓ Capacitively Coupled Clear Gate (C3G) → New step forward in gain
- ✓ Shorter Gate lengths → Increased internal amplification g_q, (6µm in PXD4; 5 µm in PXD5 → Factor 2 better expected)





standard arrays compatible to existing hybrids

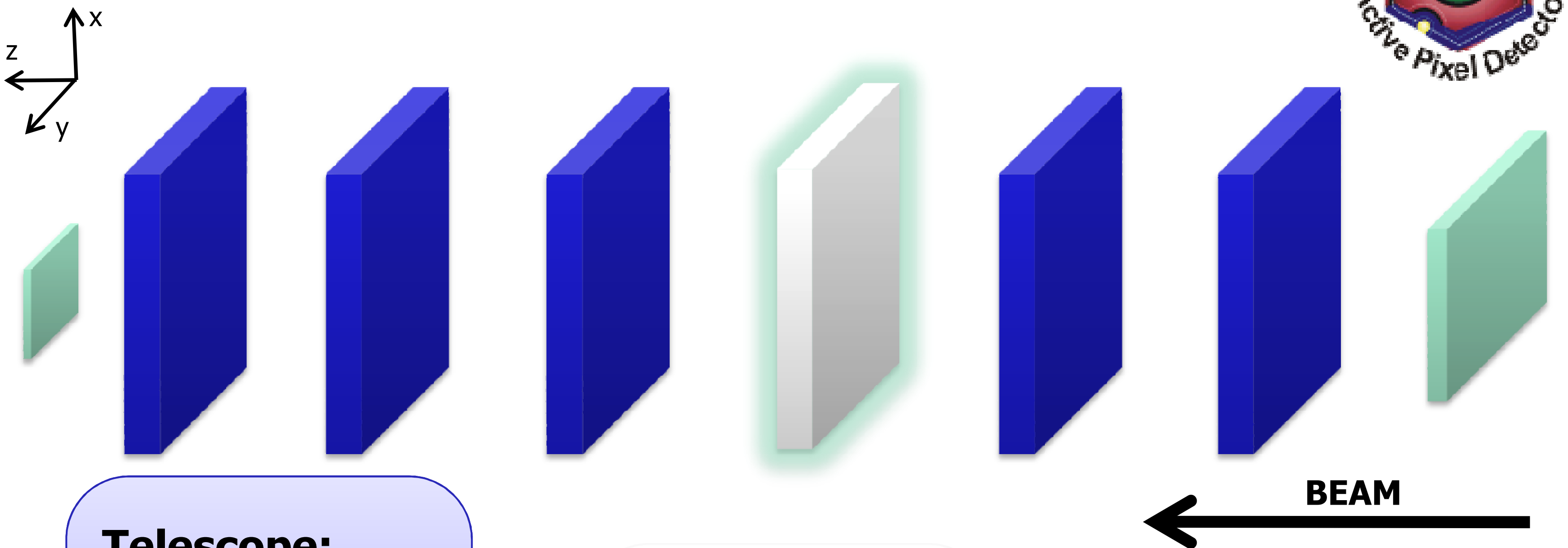
wide arrays (512 x 512, full ILC)

long arrays (256 x 1024, ½ ILC)

various new standard arrays (64 x 256 pixels, down to 20x20µm²)

Rainer Richter, MPI HLL

Test Beam setup



Telescope:

- 5 DEPFET planes
- 32x24μm^2
- CCG
- 450 μm thick

DUT:

- 1 DEPFET modules
- Various pixel sizes, gate lengths, Clear mechanisms
- 450 μm thick

Scintillators:

- 1 Big "Beam finder"
- 1 Finger "Beam allignment"
- Triggering

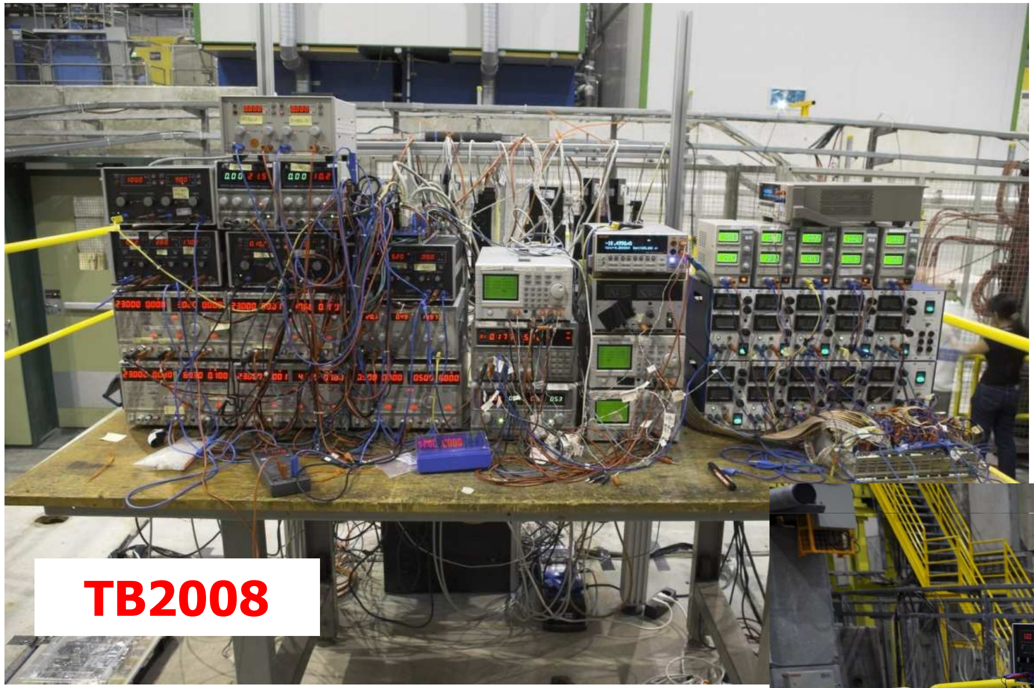
Trigger Synchronization
via TLU (Trigger Logic Unit)

All the modules electrically precharacterized using gamma sources and lasers

Test Beam set-up 2009

✓ Complete measurement programme in the H6 (SPS) line at CERN during 2008 and 2009 campaigns.
✓ EUDET DUT

Test Beam set-up 2009



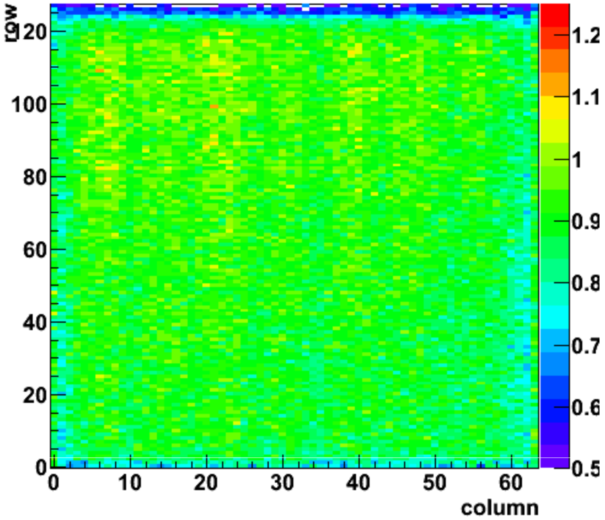
- Dedicated DEPFET Power Supplies, one per module

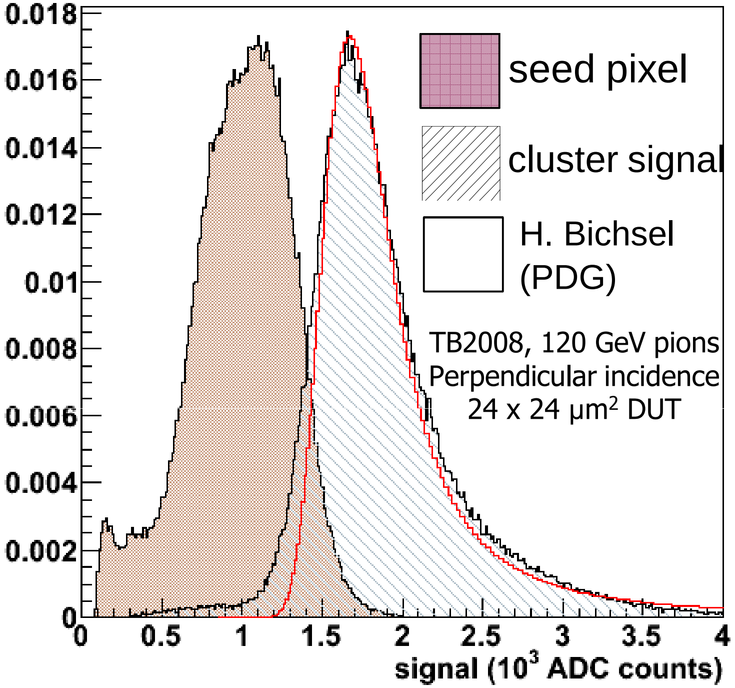
- The complex powering scheme is software controlled

→ Plug-and-play telescope

TB 2008 and 2009 results

Gain map: Deviation from average seed signal





- 64x128, 24x24 μm² Common Cleargate (TB2008)
  MPV=1715 ADC counts
  g_q=363pA/e^-

- 64x256, 32x24 μm² Capacitative Coupled Cleargate (TB2009)
  MPV~2400 ADC counts
  g_q~500pA/e^-

- 64x256, 20x20 μm² Common Cleargate, $\text{Length}_{\text{Gate}}$=5μm (TB2009)
  MPV~3100 ADC counts
  g_q~650pA/e^- (2x previous g_q, as expected)

TB 2008: Resolution

We cannot ignore multiple scattering (even at 120 GeV) or telescope resolution. DUT resolution measurement obtained by plugging in a theoretical expectation for the Multiple Scattering (either by simulating the setup in GEANT4) and error from tracking fit (P. Kvasnicka).

Module #	0	1	2	3	4	5
X Residual (μm)	2.9	2.2	2.3	2.0	3.1	3.4
Y Residual (μm)	2.3	1.7	1.7	1.7	2.2	2.6
X Resolution (μm)	2.1	1.6	1.9	1.3	2.6	2.4
Y Resolution (μm)	1.5	1.3	1.2	1.2	1.8	1.7

120 GeV pions, perpendicular incidence, 32x24 μm^2 telescope + 24x24 μm^2 DUT (3)

Energy scan is a useful cross-check to disentangle intrinsic resolution-MS correctly.

Belle-II - Super-B Factory at KEK

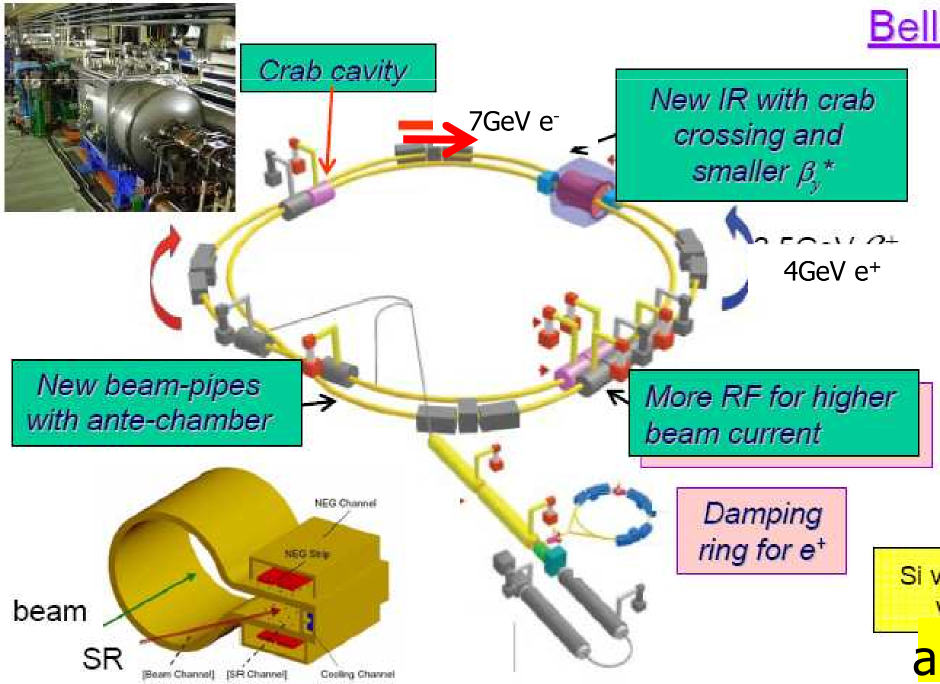
(Masa Yamauchi, Spring 2008)

KEKB Upgrade Plan : Super-B Factory at KEK

- *Asymmetric energy e^+e^- collider at $E_{CM}=m(\Upsilon(4S))$ to be realized by upgrading the existing KEKB collider.*

~2012
- *Initial target: 10 × higher luminosity* $\cong 2\times10^{35}$/cm^2/sec
  $\rightarrow 2\times10^{9}$ *BB and $\tau^+\tau^-$ per yr.*

~202X
- *Final goal: $L=8\times10^{35}$/cm^2/sec and $\int L\,dt = 50$ ab^{-1}*



Crab cavity

7GeV e⁻

New IR with crab crossing and smaller β_y^*

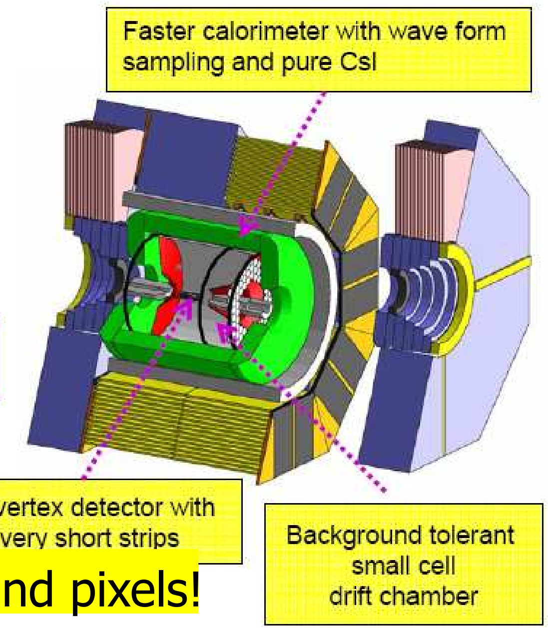
4GeV e⁺

New beam-pipes with ante-chamber

More RF for higher beam current

Damping ring for e⁺

Belle with improved rate immunity



Faster calorimeter with wave form sampling and pure CsI

Si vertex detector with very short strips

and pixels!

Background tolerant small cell drift chamber

Belle-II PXD group has decided on DEPFET as baseline

From ILC to Belle-II

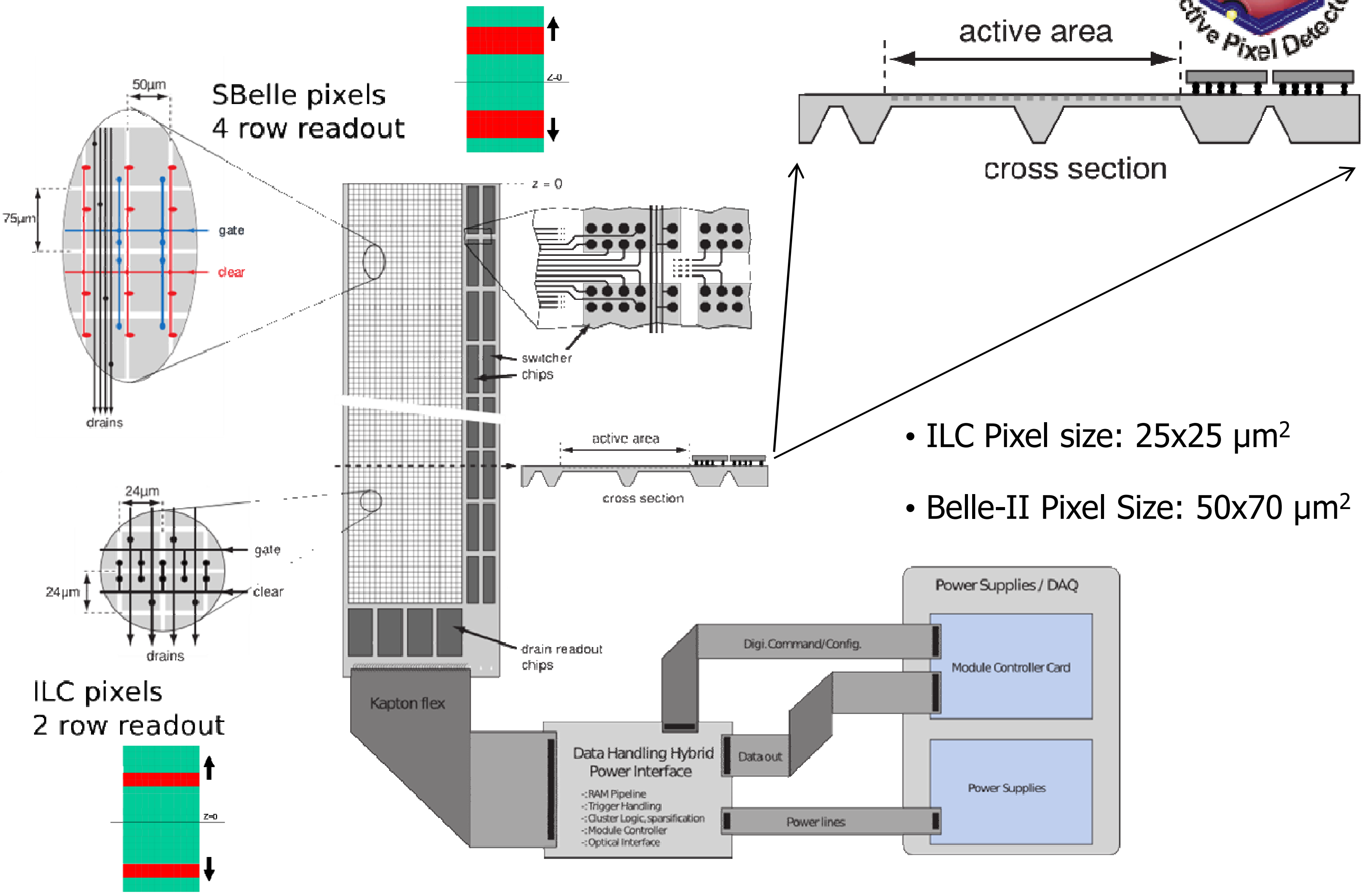
- Belle-II is more challenging rather than ILC in some points

	ILC	Belle-II
Occupancy	0.13 hits/mm^2/s	0.4 hits/mm^2/s
Radiation	< 100 krad/year	> 1Mrad/year
Duty cycle	1/200	1
Frame time	25-100 µs	10 µs
Momentum range	All momenta	Low momentum (< 1 GeV)
Acceptance	6º-174º	17º-150º

- ILC
  - Excellent single point resolution (3-5 µm) → Small pixel size 25µm^2
  - Low material budget (0.12%X_0/layer)

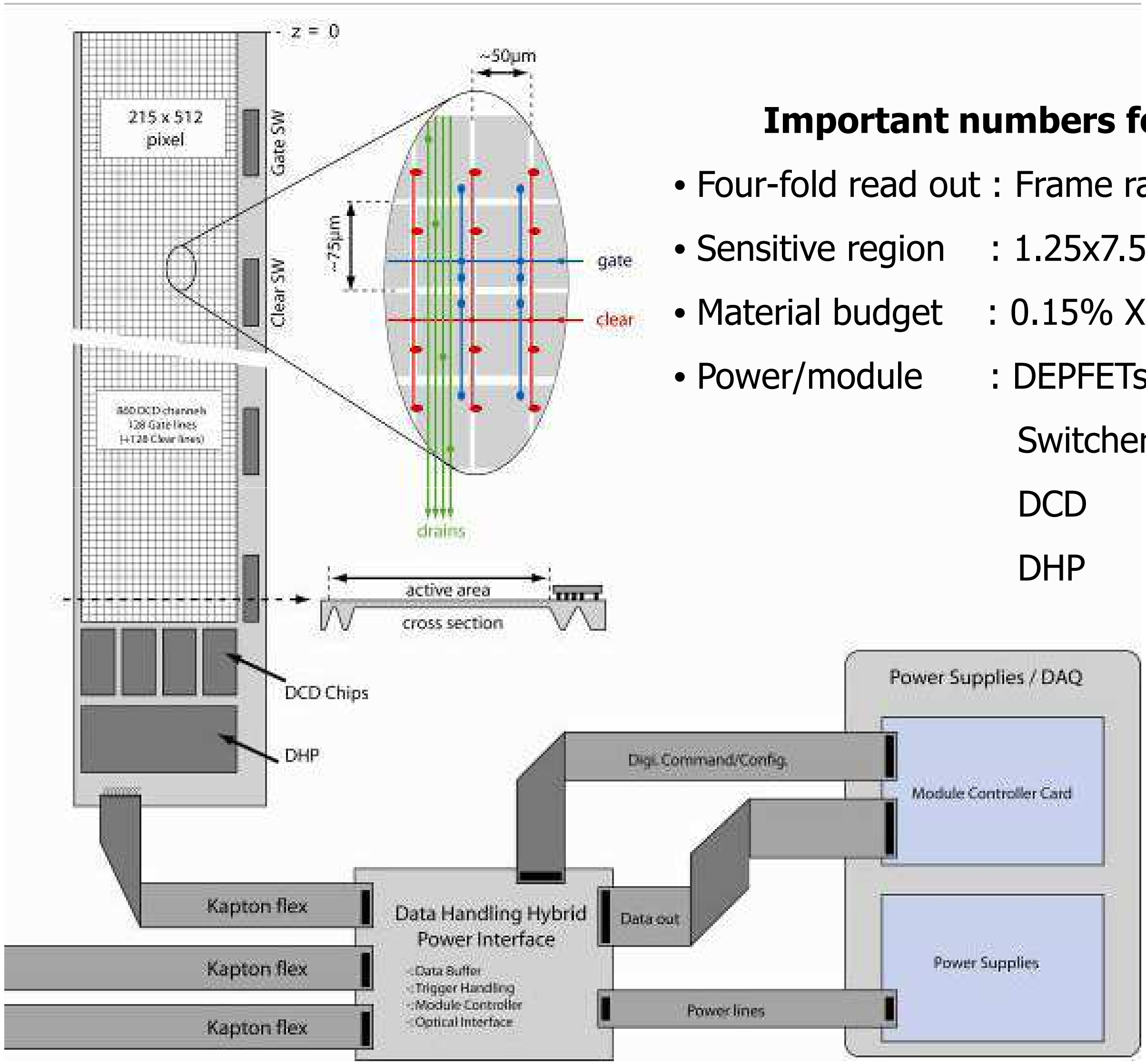
- Belle II
  - Modest spatial resolution (10µm) → Moderate pixel size (50 x 75 µm^2)
  - Few 100 MeV momenta → Lowest possible material budget (0.15% X_0/layer)

The half ILC/Belle-II module



- ILC Pixel size: 25x25 µm^2
- Belle-II Pixel Size: 50x70 µm^2

Belle-II PXD



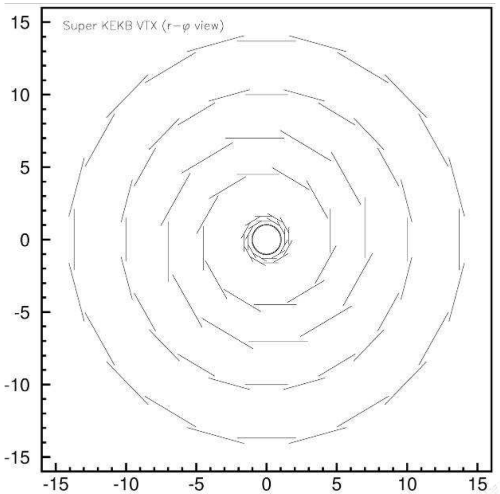
Important numbers for the baseline layout:

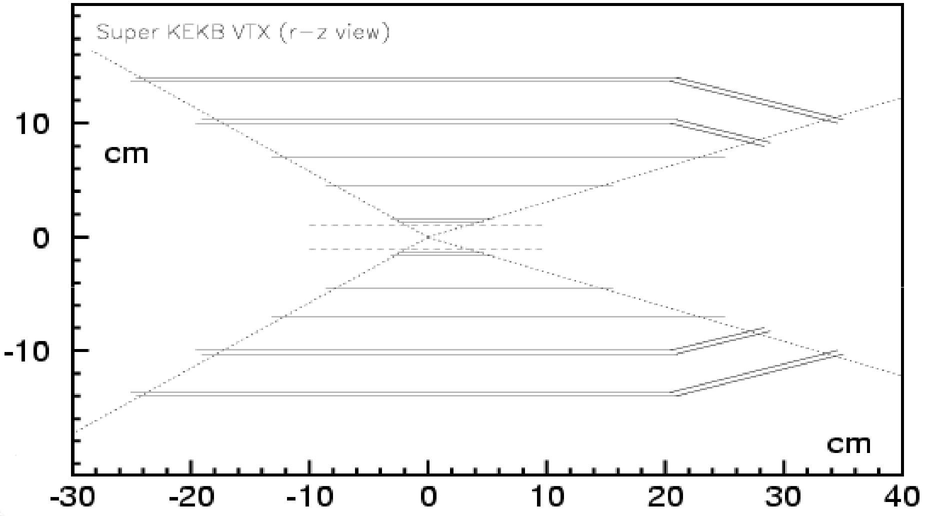
- Four-fold read out : Frame rate 100 kHz, 80ns/row
- Sensitive region : 1.25x7.5 cm^2 (L1), 1.25x11.7 cm^2 (L2)
- Material budget : 0.15% X_0 (incl. frame, chips, bumps)
- Power/module : DEPFETs ~ 0.5 W half module

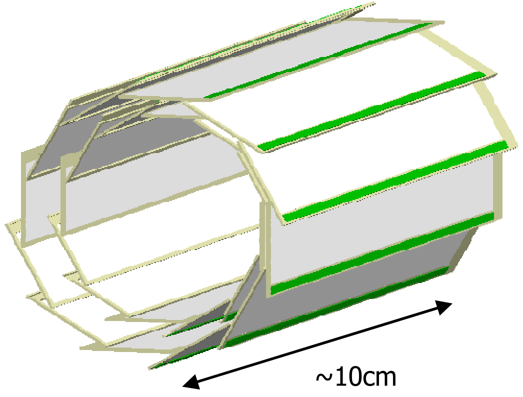
Switcher	~ 0.1 W	
DCD	~ 5	W on each ladder end
DHP	~ 2	W on each ladder end

Belle-II PXD

- 2 thin pixel layers at 1.3 cm and 2.2 cm (subject to optimization)
- 4 layers with double sided Si-strip detectors
- Angular coverage 17°<θ < 150°, slanted at the end







Conclusions

✓ The DEPFET Collaboration is developing pixel sensors with integrated amplification.

- Good spatial resolution, low material budget and low power consumption

✓ Building the system

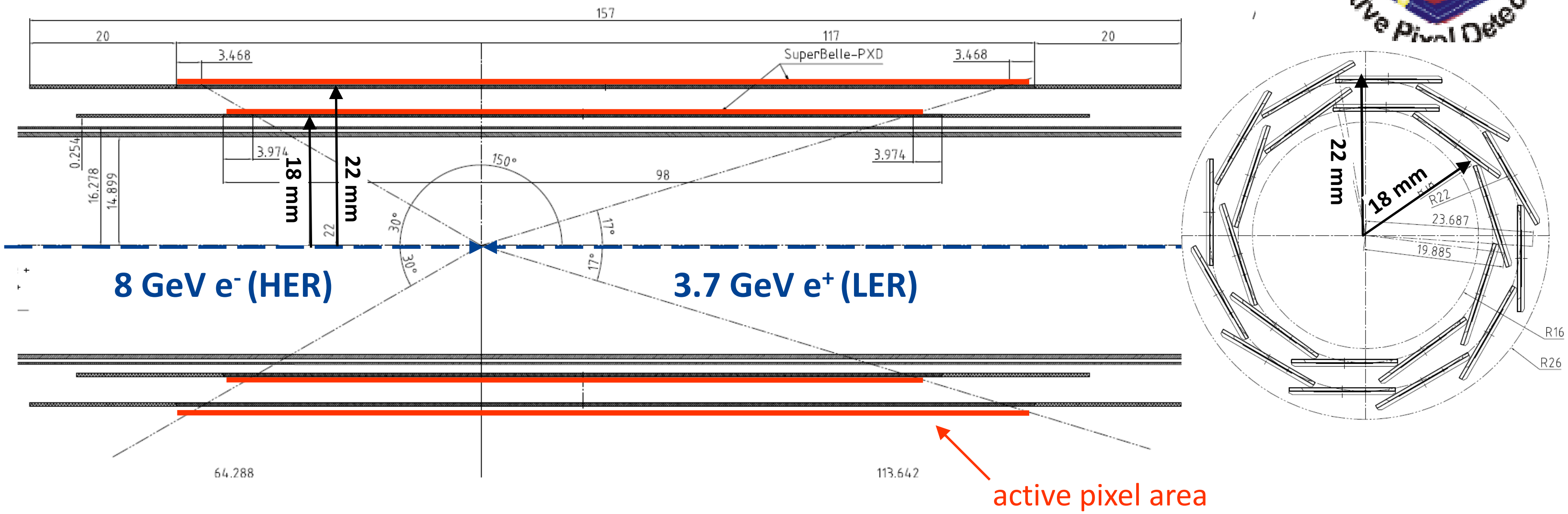
- Auxiliary electronics, bump bonding, cooling, mechanics

✓ Sensors with small pixel size and new features (C3G and shorter gate length) have been characterized in Test Beam 2009

- Better results than standard 2008 sensors: Up to 80% higher g_q
- Spatial resolutions of 1.4 µm on 24x24 µm^2 CCG pixel (2008)

✓ The DEPFET is ready to be used as transparent and high precision vertex detector at Belle-II. **This Project has boosted the R&D for ILC DEPFETs**.

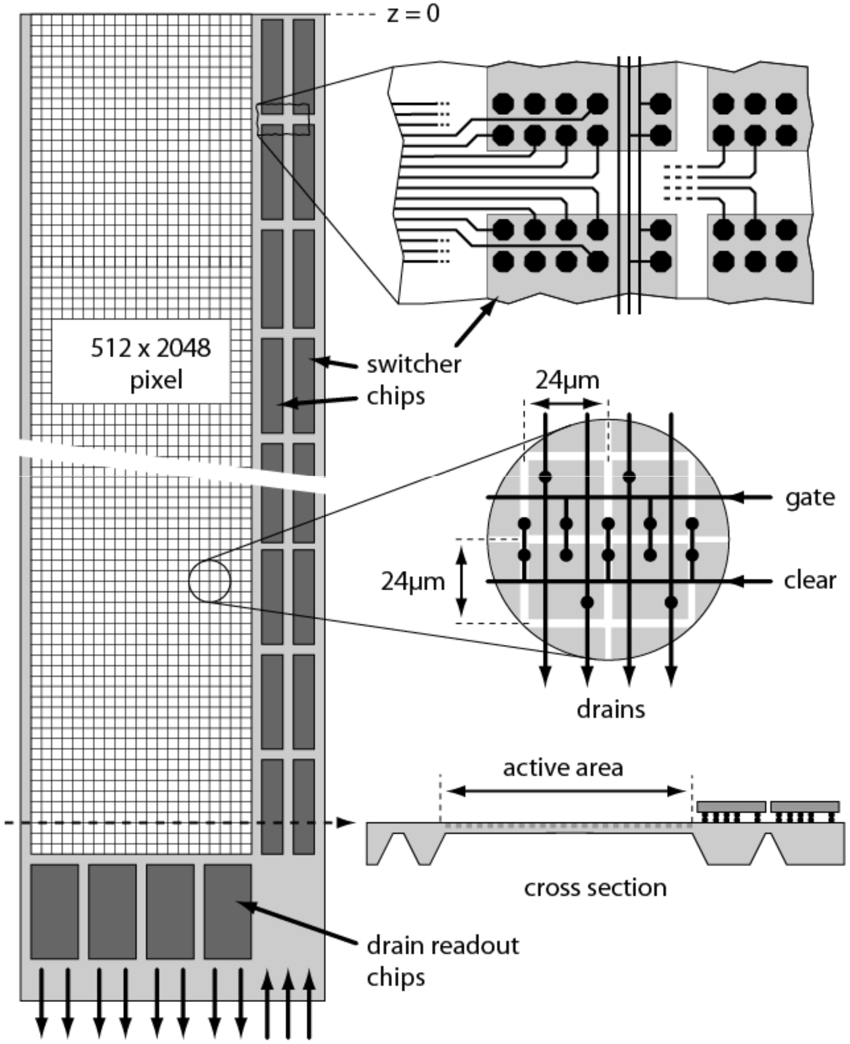
Thank you very much!



- occupancy: ~0.2 hits/µm^2/s (estimated for 1x10^{35} cm^{2}sec^{-1}, @ 1.8cm radius)
- spatial resolution : < 10 µm (r-phi**)** (can be less in z)
- pixel size: 50 µm (r-phi) x ~90 µm (z-axis)
- material budget < **0.15 % X_0** per layer
- **read-out time: 10 µs**
- radiation level: ~**1 Mrad per year**

- 17° - 150° acceptance (η = [0.55 .. 0.3])
- optional layer 0 at 1.3 cm radius with beam pipe up
- half-module active area: 4.9 cm x 1.2 cm (layer1)
- #pixels: 240 x 512
- r/o channels: 960 x 128 (4-fold parallel)
- **sample (row) rate: 12 MHz**

ILC VXD baseline design



Just as a starting point for the R&D!

- 5 layer, old TESLA layout
- 10 and 25 cm long ladders read out at the ends
- 24 micron pixel
- design goal 0.1% X_0 per layer in the sens. region

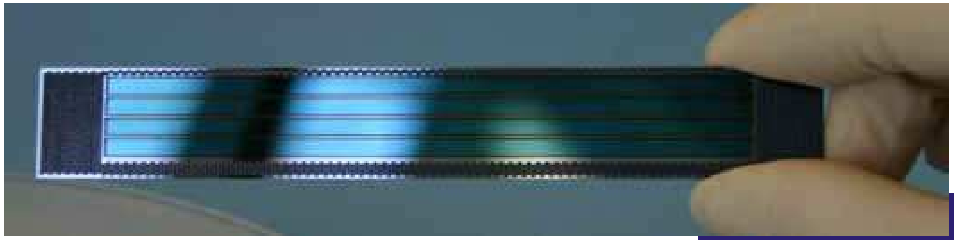
Strategy to cope with the background:

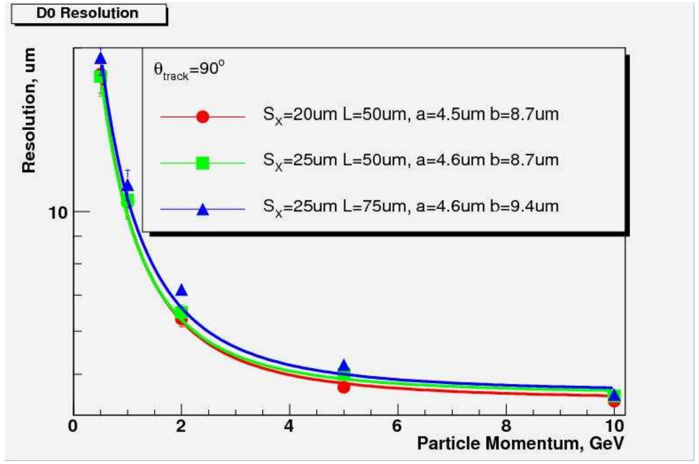
- read ~20 times per train
- store data on ladder
- transfer the data off ladder in the train pause

  → row rate of 40 MHz
- read two rows in parallel, doubles # r/o channels but:

  → row rate 20 MHz ☺

Achievements and status

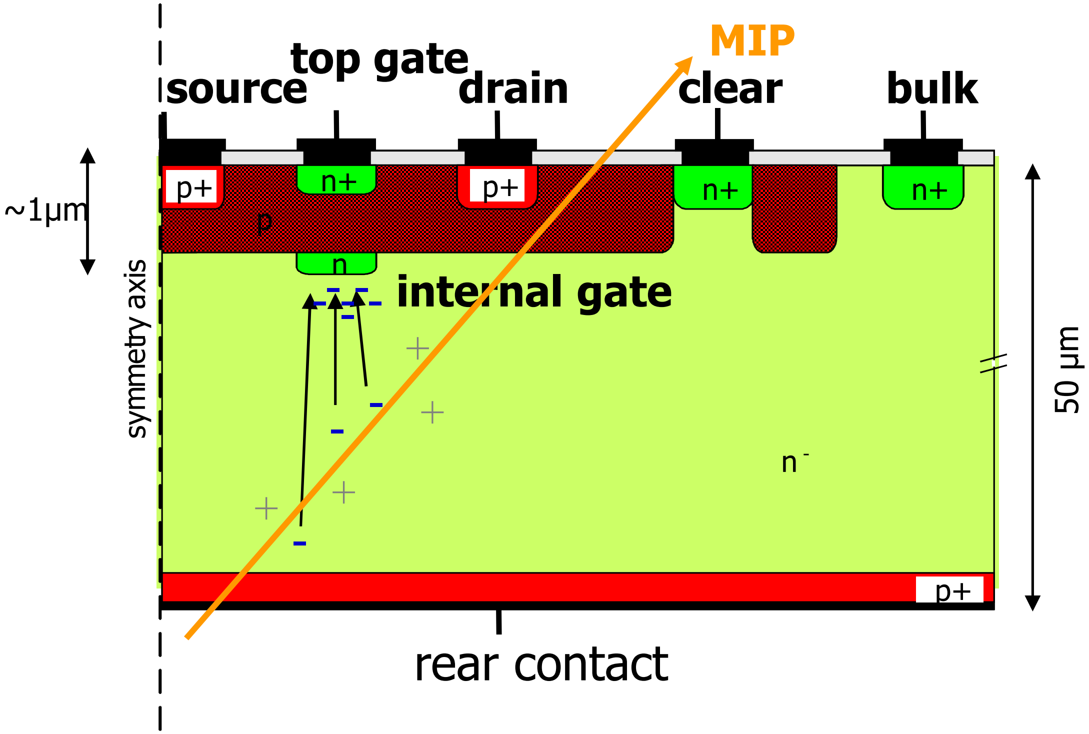




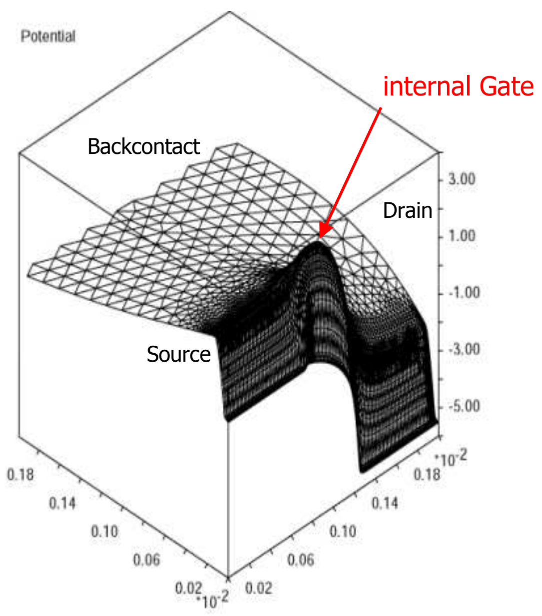
- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ test beam @ CERN:
  - ✓ S/N≈110 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. 1.3 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2
- ✓ Simulations show that the present DEPFET concept can meet the challenging requirements at the ILC VXD.

- ✓ New rad. hard Switcher3 chips tested and functional
- ✓ Production of 2nd iteration of DEPFETs under test
- ✓ New r/o chips DCD designed for read-out of large matrices are under test

DEPFET-Principle of Operation



Potential distribution:



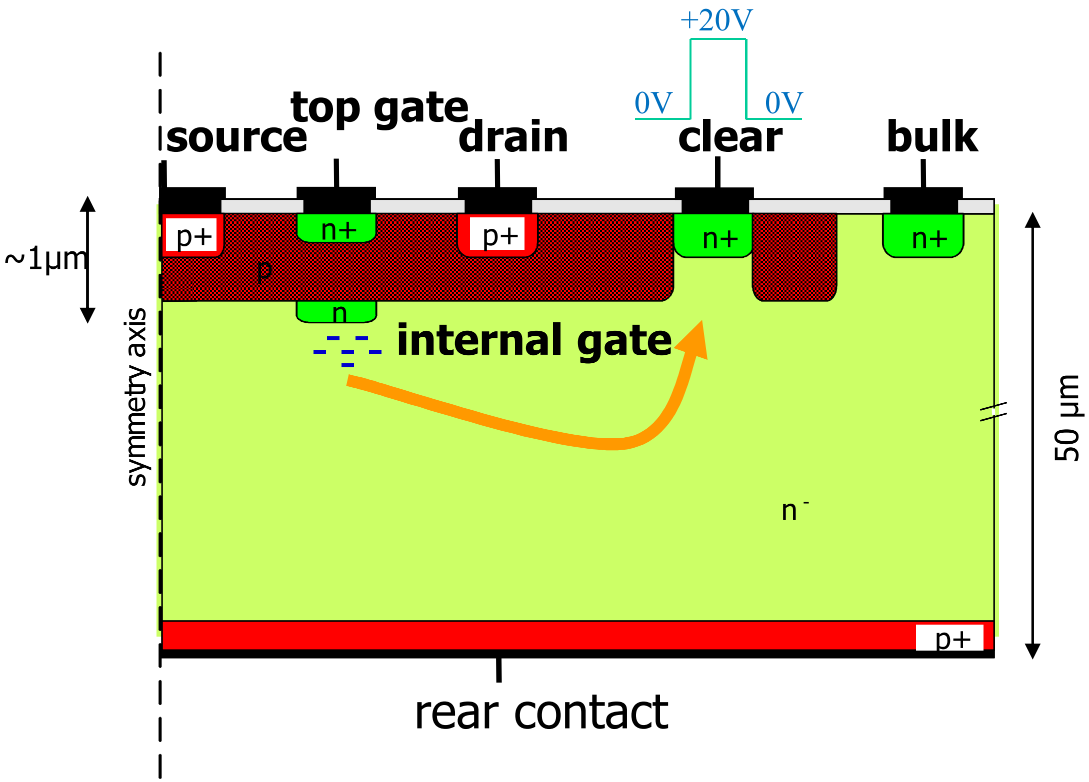
[TeSCA-Simulation]

FET-Transistor integrated in every pixel (first amplification)

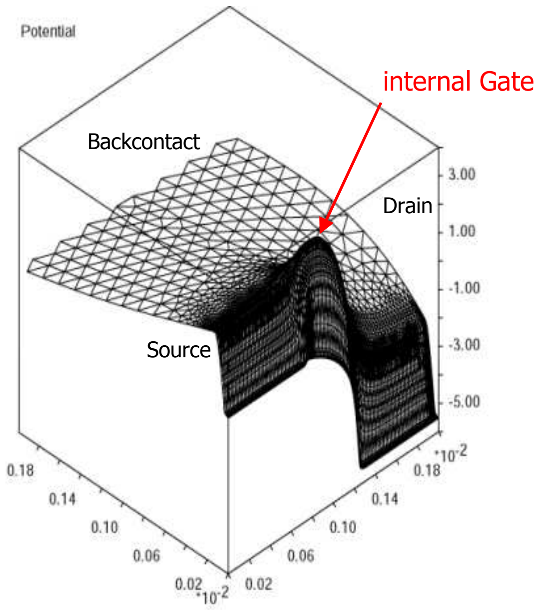
Electrons are collected in „internal gate" and modulate the transistor-current

Signal charge removed via clear contact

DEPFET-Principle of Operation



Potential distribution:



[TeSCA-Simulation]

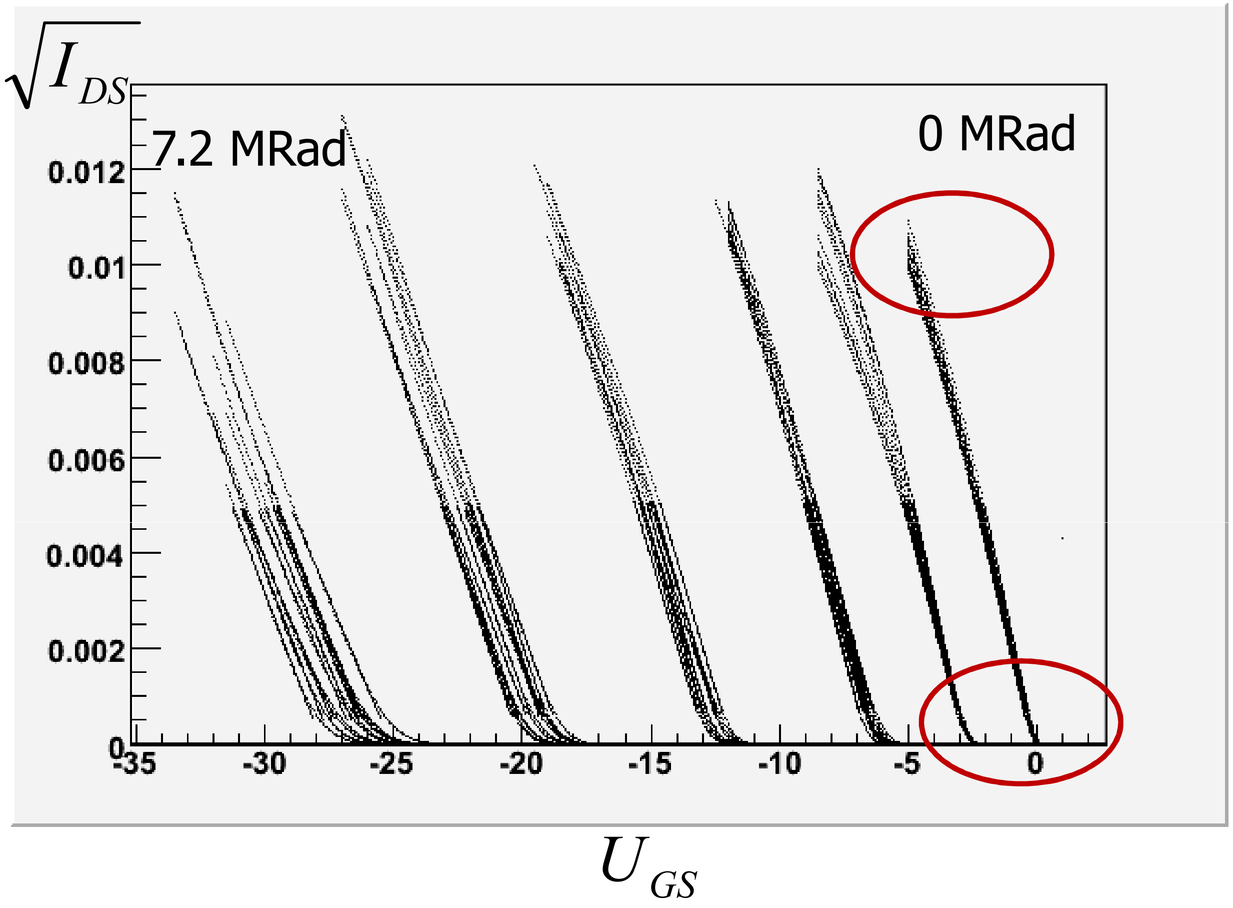
FET-Transistor integrated in every pixel (first amplification)

Electrons are collected in „internal gate“ and modulate the transistor-current

Signal charge removed via clear contact

→ Correlated Double Sample

Results – thresholdvoltage shift dispersion

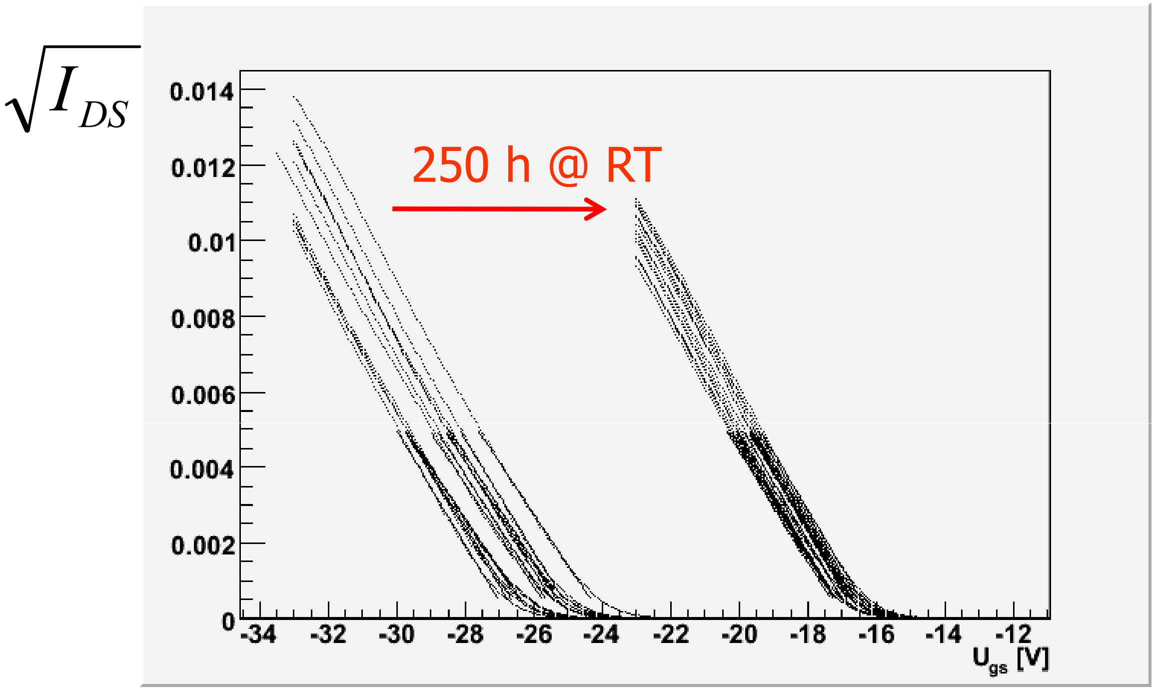


$$I_{ds} \propto \frac{W}{L}(U_{GS} - U_{THR})^2$$

$$\sqrt{I_{ds}} \propto \sqrt{\frac{W}{L}}(U_{GS} - U_{THR})$$

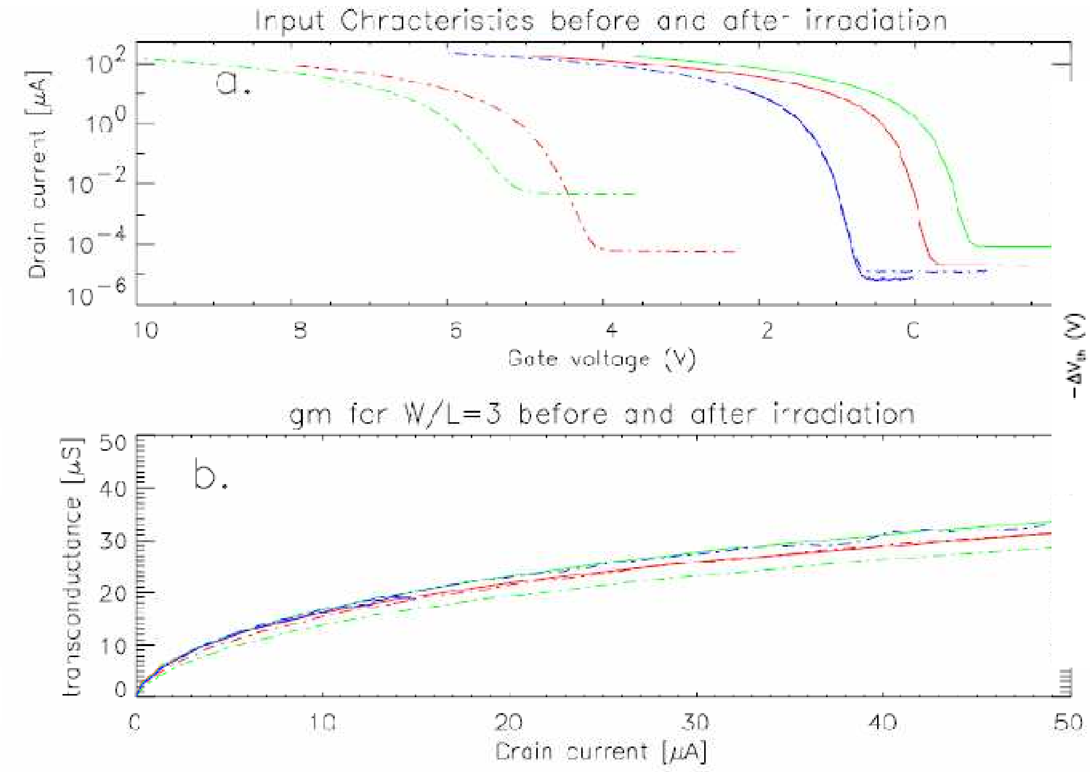
- Evidently a spread in the thresholdvoltages visible

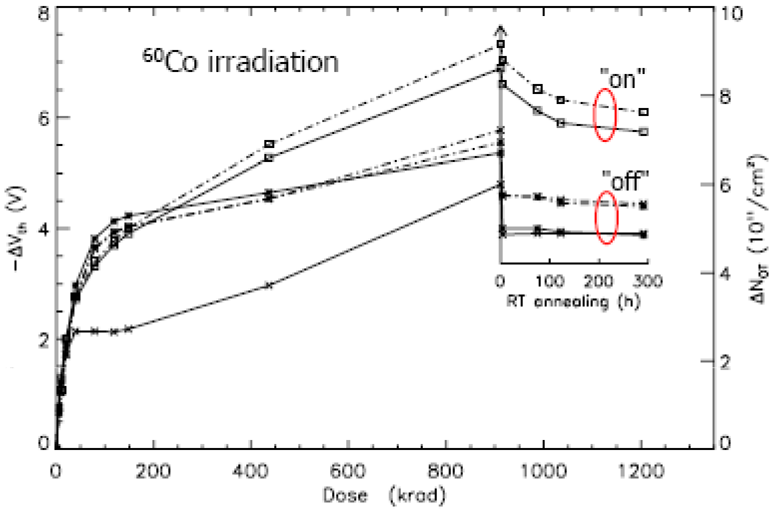
The way back - RT annealing



- Dispersion is reduced from 2.8V to ~ 0.8V
- Current variation @ ~100µA reduced from 90% to 40%

Electrical characteristics



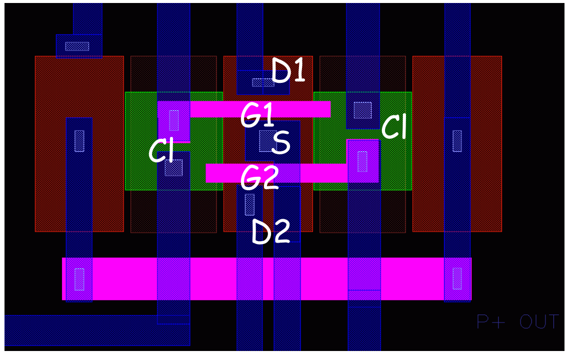


irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT$^{(*)}$
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4×10^{11} n/cm^2	~ 0	unchanged	1.4 pA
proton	283krad / 3×10^{12} n/cm^2	~-5V	~ -15%	26 pA

(*) 5..22 fA non irrad.

Irradiations – What happened in the past…

- **Single pixel structures**
- Electrical characteristics:
  - Threshold voltage shift
  - Subthreshold slope
  - G_m, G_q
  - Low frequency noise
- Leakage current
- Spectroscopic performance



	PXD4-10 MO2	PXD4-5 M05	PXD4-2 J14
Type	Protons, 30MeV	Neutrons, 1-20MeV	Gammas - ^{60}Co
Fluence / Dose	$1.2 \cdot 10^{12}$ p/cm²	$1.6 \cdot 10^{11}$ n/cm²	913kRad
1MeV n equivalent	$3 \cdot 10^{12}$ n_{eq}/cm²	$2.4 \cdot 10^{11}$ n_{eq}/cm²	n/a

LBNL Cyclotron

GSF Munich

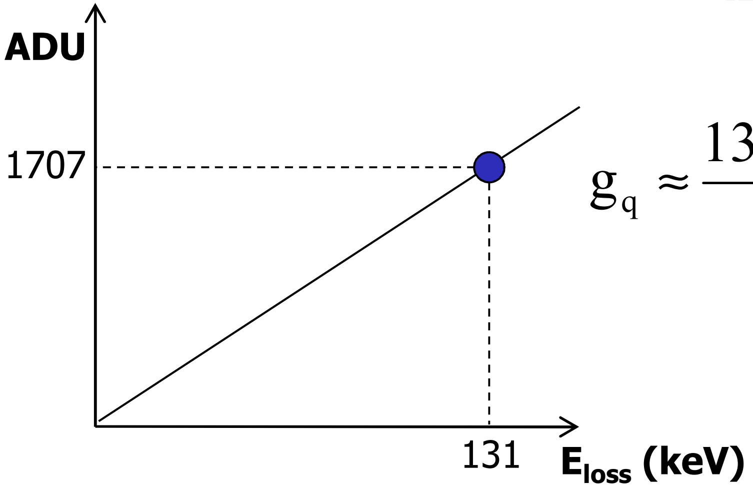
Gain and noise

- The most probably energy loss for a MIP in 450µm of Silicon is[1]:

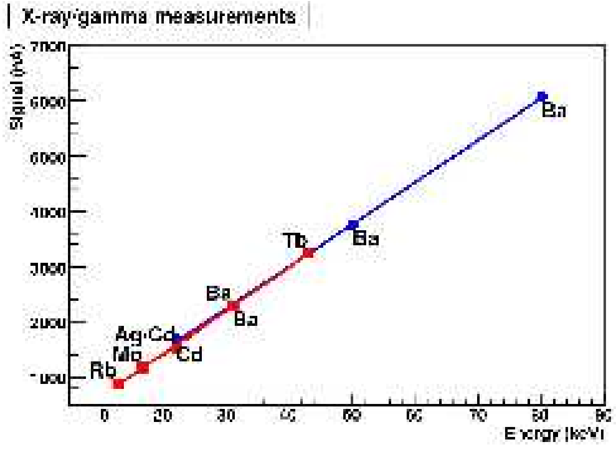
$$\Delta_{\mathrm{mp}} = \underbrace{450\mu m}_{\text{DEPFET Thickness}} \cdot \underbrace{0.75}_{\text{Scale factor}} \cdot \underbrace{388\,eV/\mu m}_{\text{Mean loss per }\mu\text{m}} = 35700e^- = 131keV$$

FIT → y=a+bx → Slope=Gain

b=13.0 ADU/keV



$$g_q \approx \frac{13.0ADU}{keV} \cdot \frac{7.7nA}{1ADU} \cdot \frac{3.6 \cdot 10^{-3}keV}{1e^-} \approx 0.360\,nA/e^-$$



$$\mathrm{ENC} = \underbrace{12.5\mathrm{ADU}}_{\text{Noise in ADU}} \cdot \underbrace{\frac{1\mathrm{keV}}{13.0\mathrm{ADU}}}_{\text{Gain}} \cdot \underbrace{\frac{1\mathrm{e^-h}}{3.6 \cdot 10^{-3}\mathrm{keV}}}_{\text{Energy to create e}^-\text{h}} \approx 267\mathrm{e^-}$$

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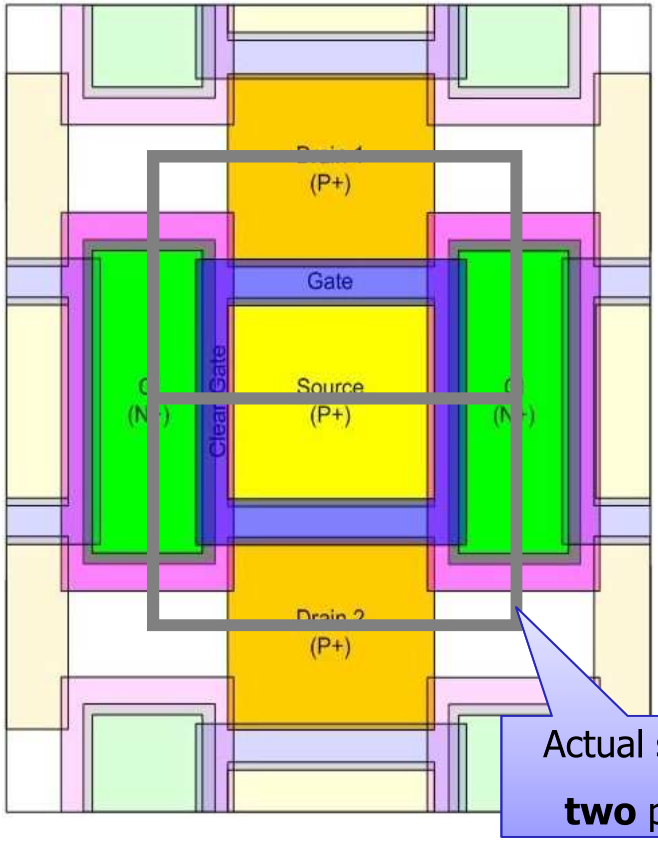
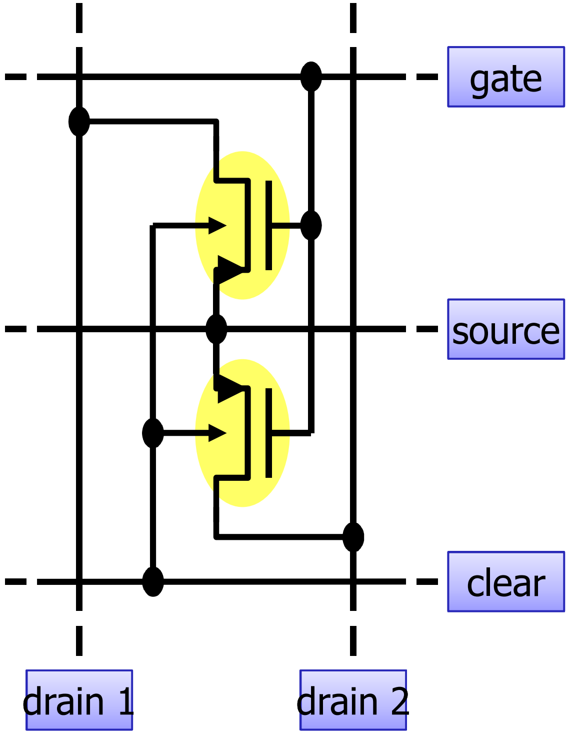
[1] http://pdg.lbl.gov/2008/reviews/passagerpp.pdf

Double pixel structure

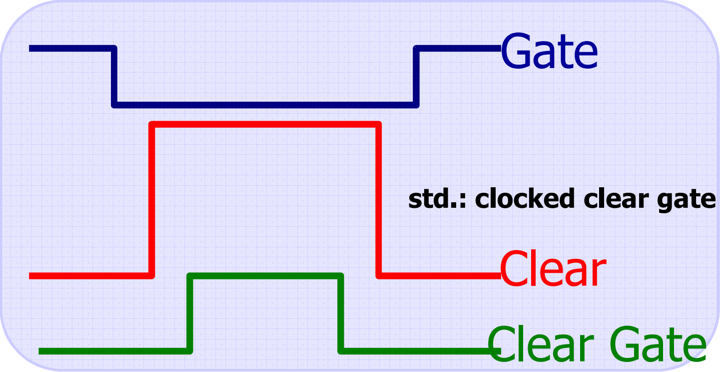


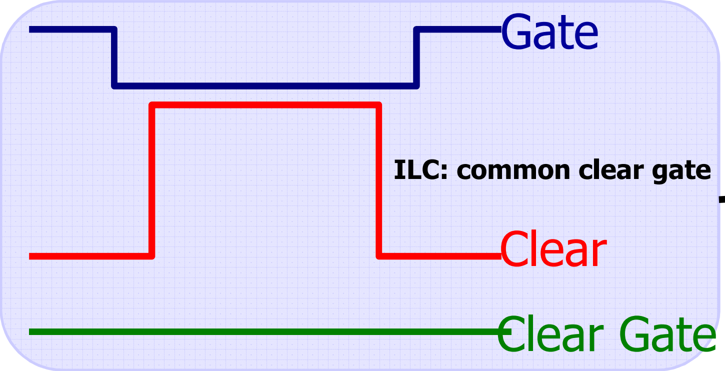
Actual size of **two** pixels

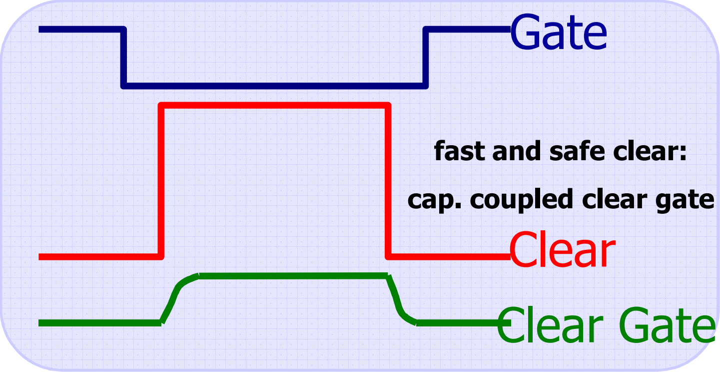
Merging two pixels (common source) for reduce the size

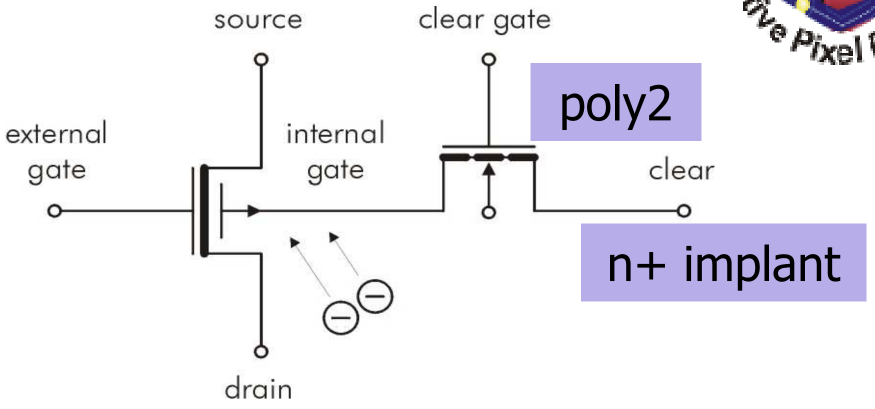


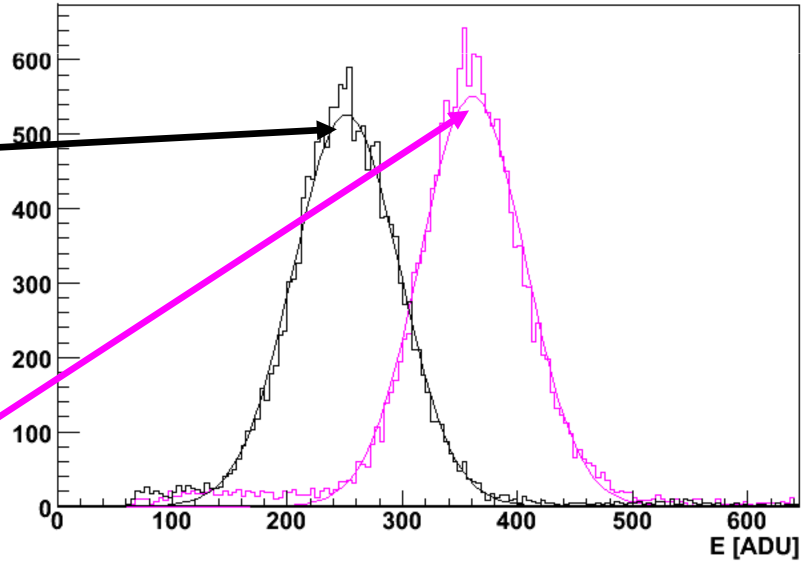
Capacitively Coupled Common Clear Gate











^{109}Cd spectrum (22keV, 6000 e$^-$)

taken with 128x64 matrix

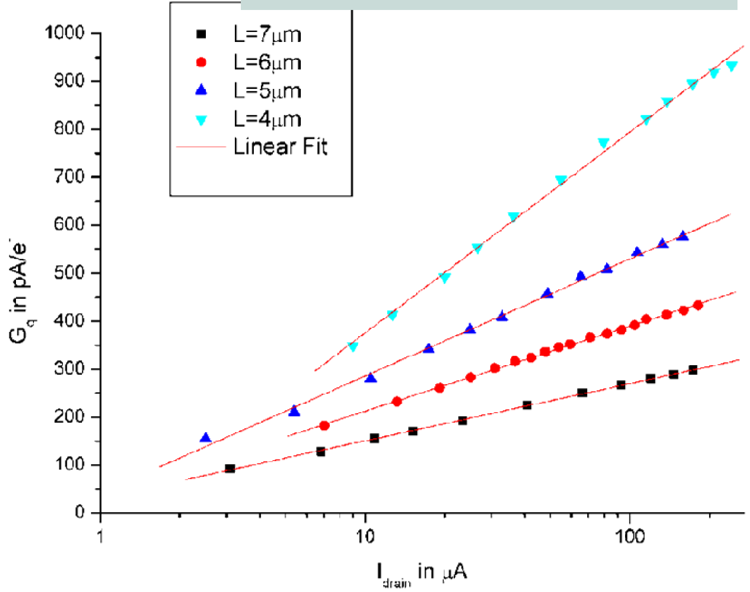
Internal Amplification

- ✔ The internal amplification measures the change in drain current in the presence of charge in the internal gate:

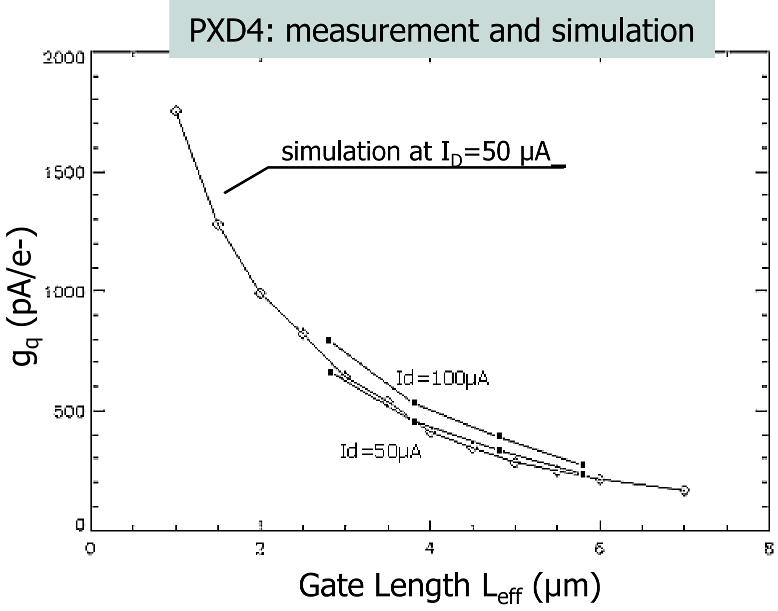
$$g_q = \frac{dI_{ds}}{dQ_{int}} \sim \frac{\sqrt{I_{ds}}}{\sqrt{W L^{\frac{3}{2}}}}$$

- ✔ Increasing g_q increases SNR
- ✔ Playing with channel length we can achieve up to g_q ~ 1 nA/e^-
- ✔ PXD4 has L=6μm, some matrices in PXD5 have now L=4μm → Expect factor 2 better S/N

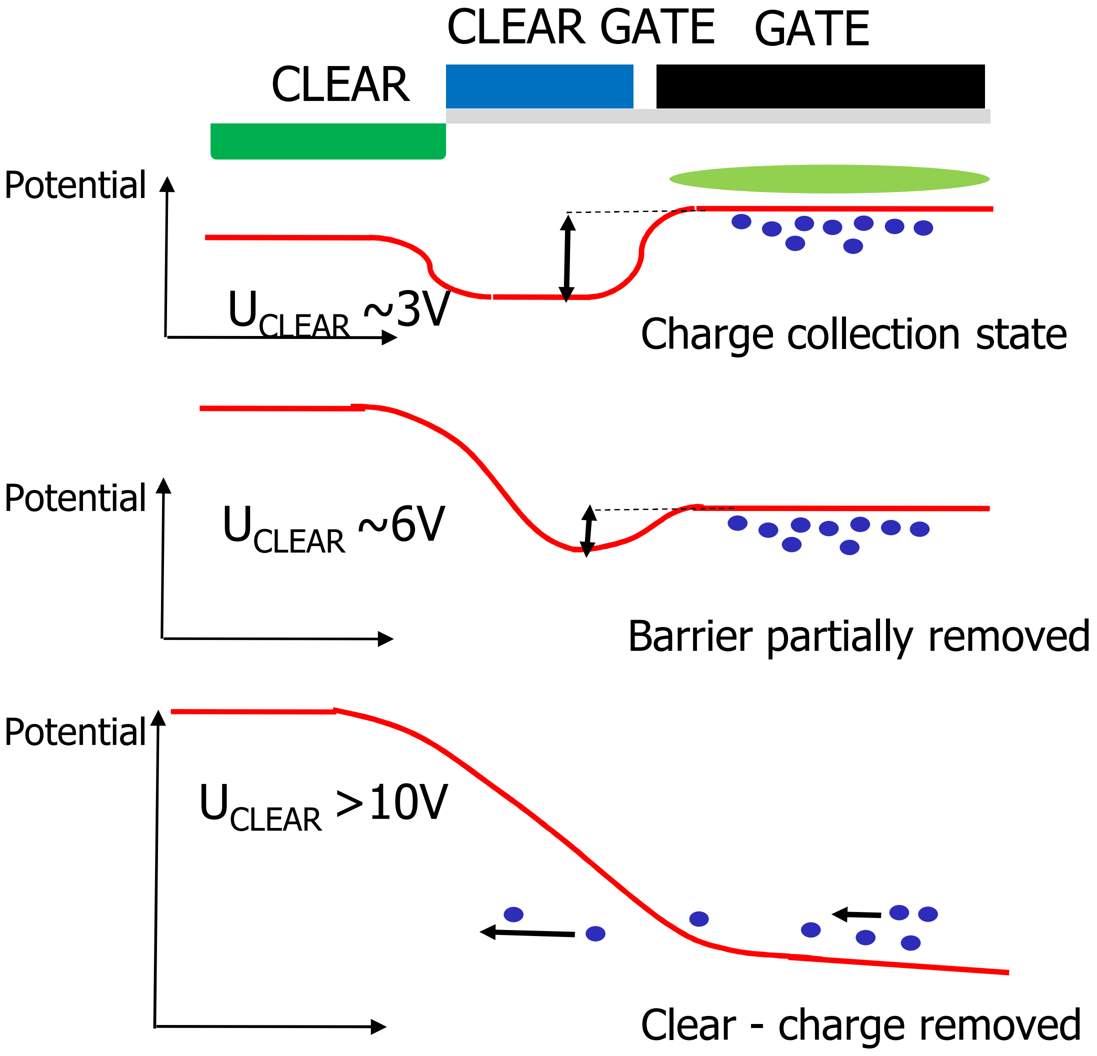
PXD5: single pixel measurement



PXD4: measurement and simulation



The Clear mechanism



CLEAR GATE GATE

CLEAR

Potential

U_{CLEAR} ~3V

Charge collection state

Potential

U_{CLEAR} ~6V

Barrier partially removed

Potential

U_{CLEAR} >10V

Clear - charge removed