Development of Readout ASIC for FPCCD Vertex Detector

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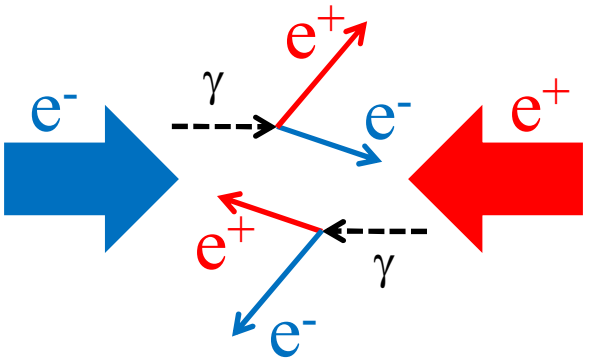
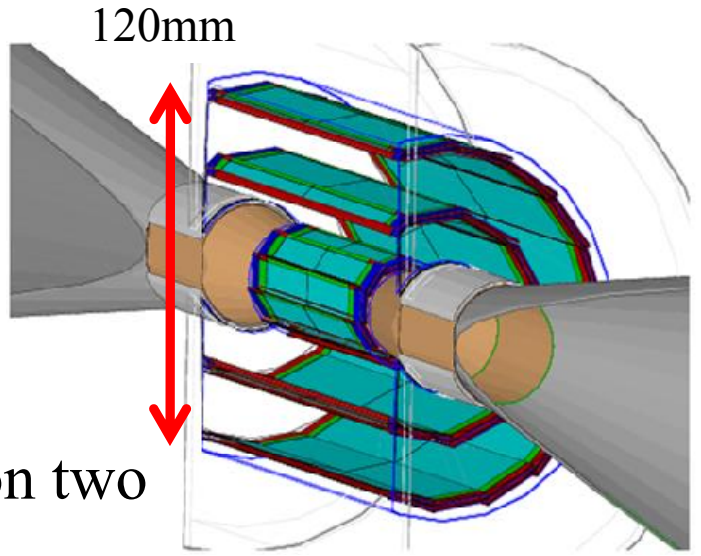
FPCCD Vertex Detector

- Large amounts of $e^+ \cdot e^-$ pair background is generated at beam collision.

⇨ For low pixel occupancy, we develop Vertex Detector adopt fine pixel CCD sensor.

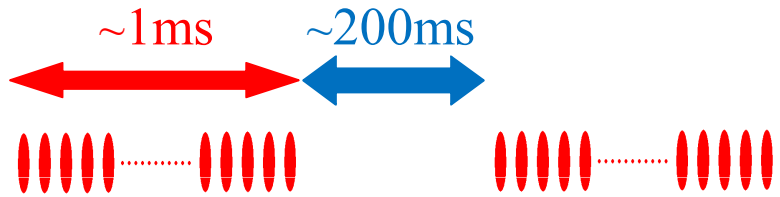


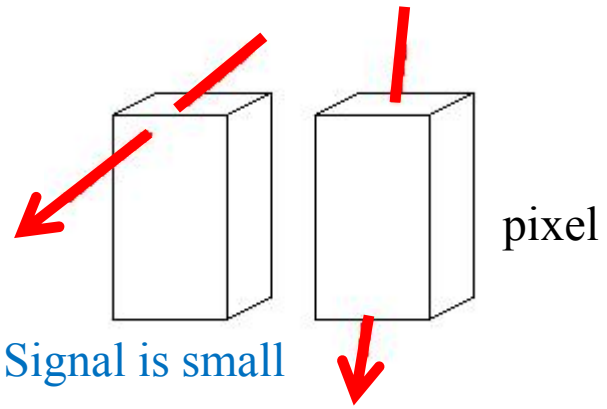
- <u>FPCCD Vertex Detector</u>
  - Fine Pixel CCD
    - Pixel size : 5μm × 5μm
    - Epitaxial layer thickness : 15μm
  - 20,000 × 128 pix/ch
  - # of channels ~ 6,000ch
  - Double layers : CCDs are attached on two sides of the ladders.
  - Readout ASIC for FPCCD is developed.



Requirements to readout ASIC

- Power consumption < 6 mW/ch
  - Setting in a cryostat
  - Total power consumption < 100W
- Readout rate > 10 Mpix/sec
  - Read out in the inter-train time
  - 20,000 × 128 pix / 200 ms
- Noise level < 30 electrons
  - Signal becomes small for particles penetrating with large angle.

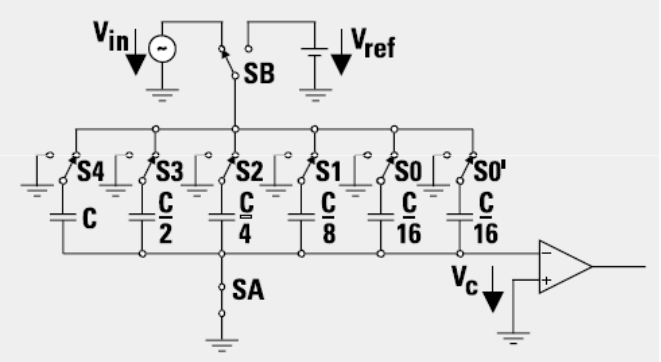




⇨ Readout ASIC was designed to satisfy these requirement.

Solution of Requirements

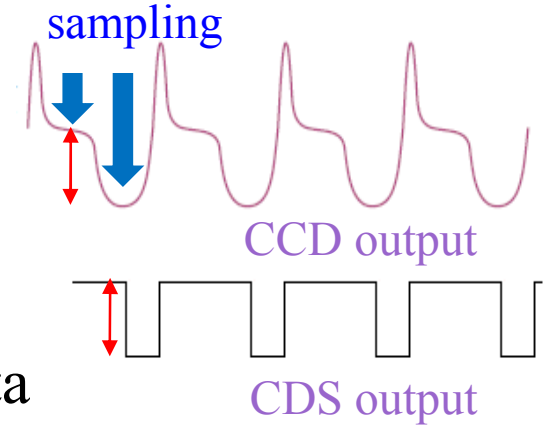
- Power consumption < 6 mW/ch
  - ➢ ADC is the main power consumption source.
  - ⇨ For suppressing power consumption at ADC, charge sharing ADC is used.
  - Signal is converted by comparing the reference voltage with a capacitor.
  - ⇨ Power consumption of ADC < 10μW/ch

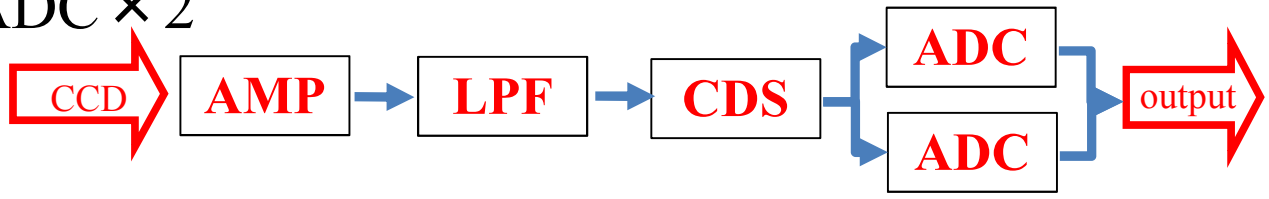


- Readout rate > 10 Mpix/sec
  - ➢ It is difficult to operate charge sharing ADC with high-speed
  - ⇨ Two 5MHzADC are used alternatively.
  - → 10Mpix/sec
- Estimated noise level < 30e

Test sample of readout ASIC

- Design of prototype ASIC
  - Amplifier
  - Low pass filter (LPF)
  - Correlated double sampling (CDS)
    - ➢ sample backward and forward of pixel data
    - ➢ output voltage difference at sampling points
  - Charge sharing ADC × 2
    - ➢ Serial output





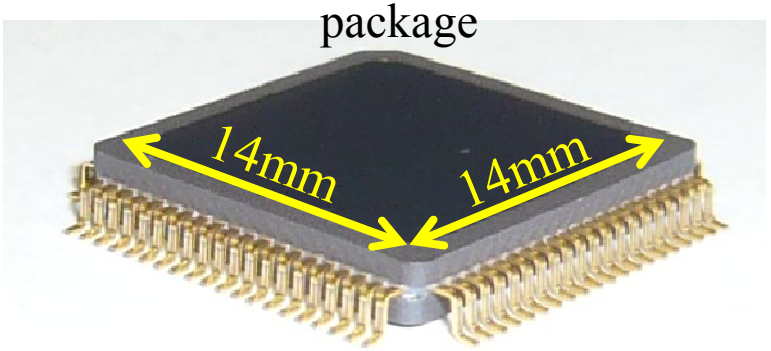
- Test sample

  0.35μm TSMC process

  Chip size : 2.85 mm × 2.85 mm

  # of channels : 8

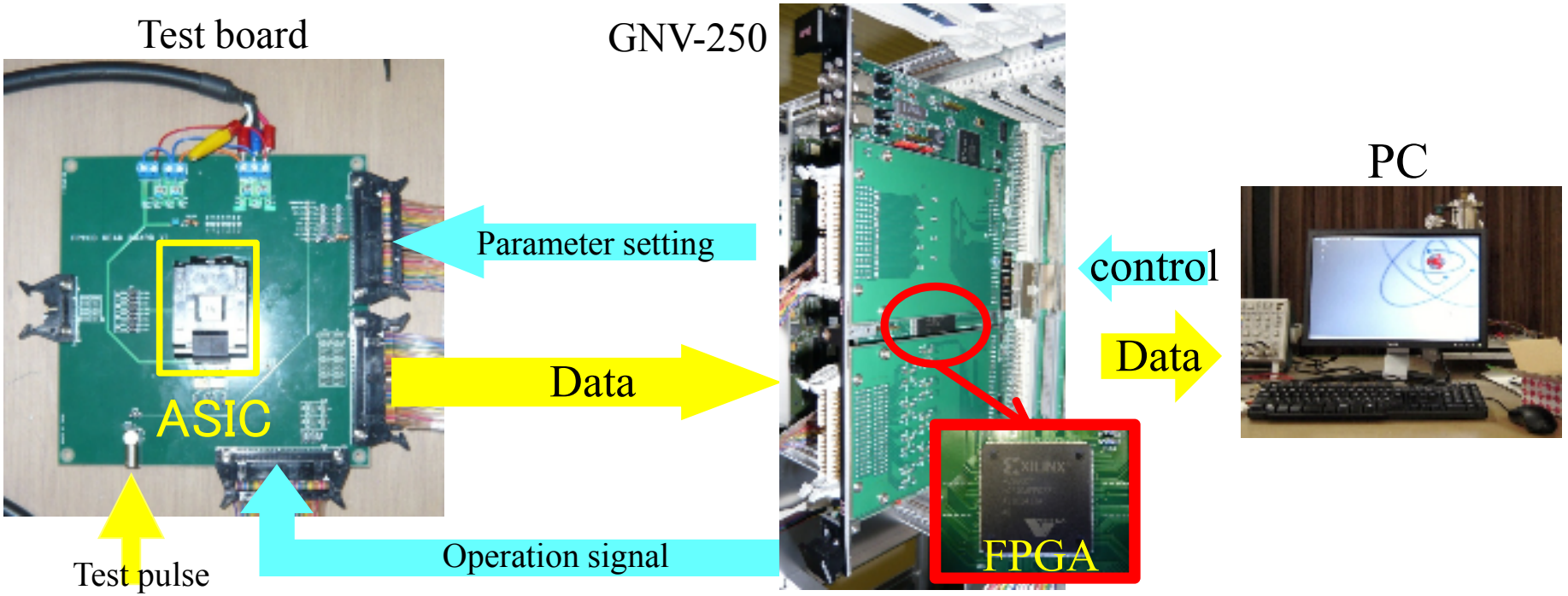
  Package : QFP-80 pin



⇨ The performance of a test sample was checked

Test bench

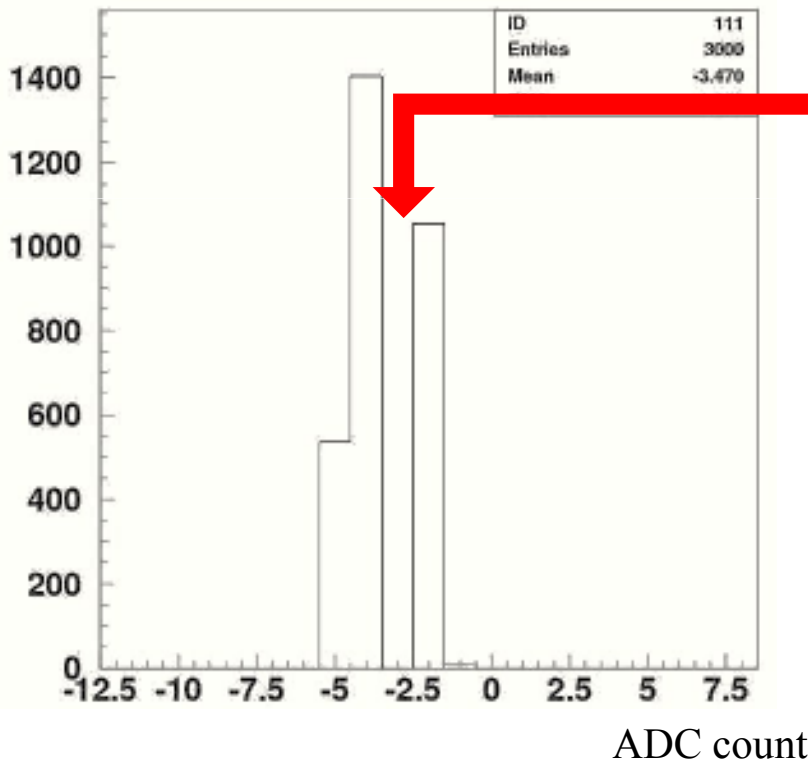
- Data acquisition and circuit control are done by a VME module.
  - GNV-250 module
    - ➢The control logic was implemented into FPGA.
  - The test job and parameter setting are controlled by PC.
  - ADC output is stored on FIFO embedded in FPGA, and sent to PC.



Pedestal distribution

- Pedestal distribution was checked
  - Conversion rate ~1.5 Mpix/sec

Pedestal distribution



- Some ADC counts are not output.

⇨ The reason was investigated.

⇨ Next slide

- Noise level

RMS = 1.1

Equivalent noise charge at sensor input

⇒ ~45e (Requirement:30e)

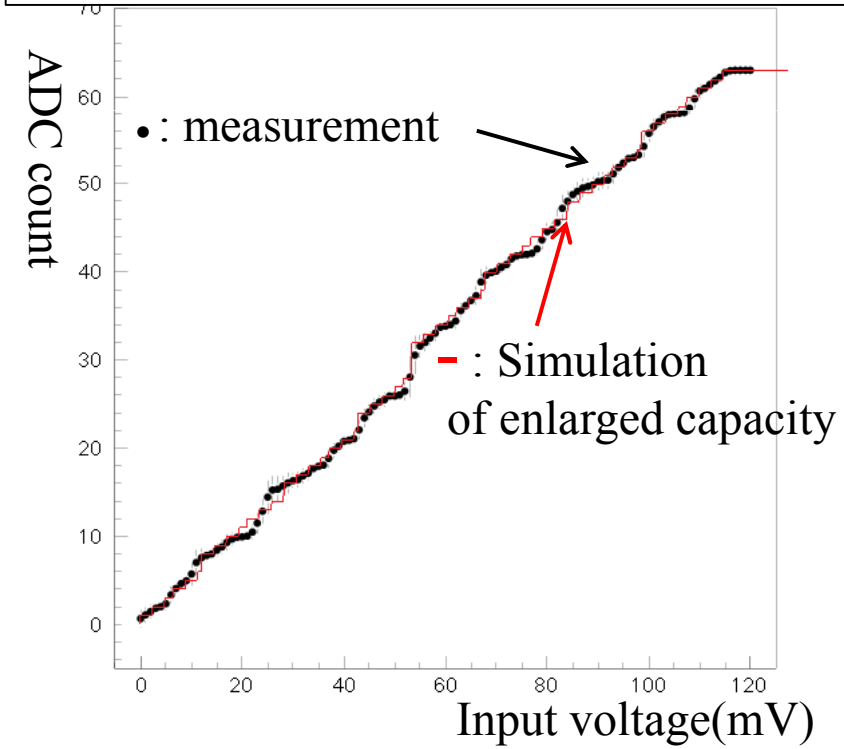
⇨ Temperature dependency was checked.

⇨ After the next slide

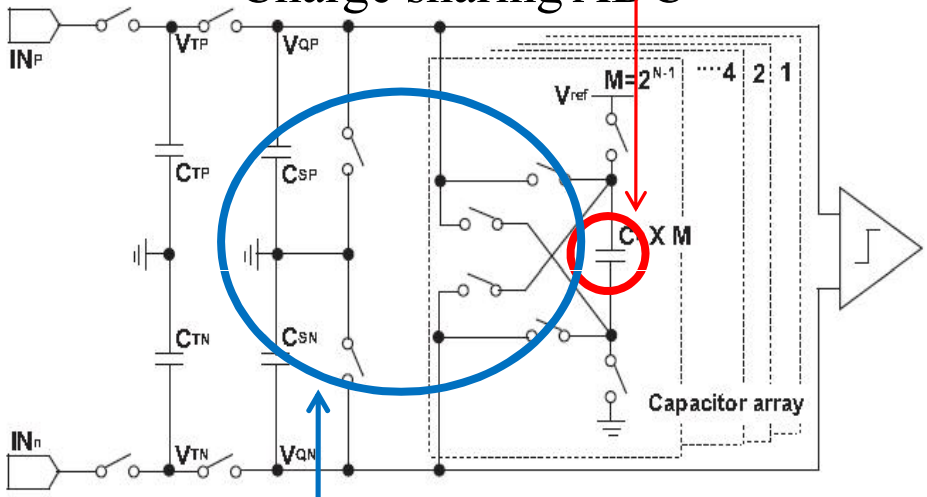
Problem of ADC design

- ADC output was simulated by MATLAB.
- Simulation result of enlarged capacity of ADC capacitor is consistent with measurement.

Test chip measurement and simulation



Charge sharing ADC

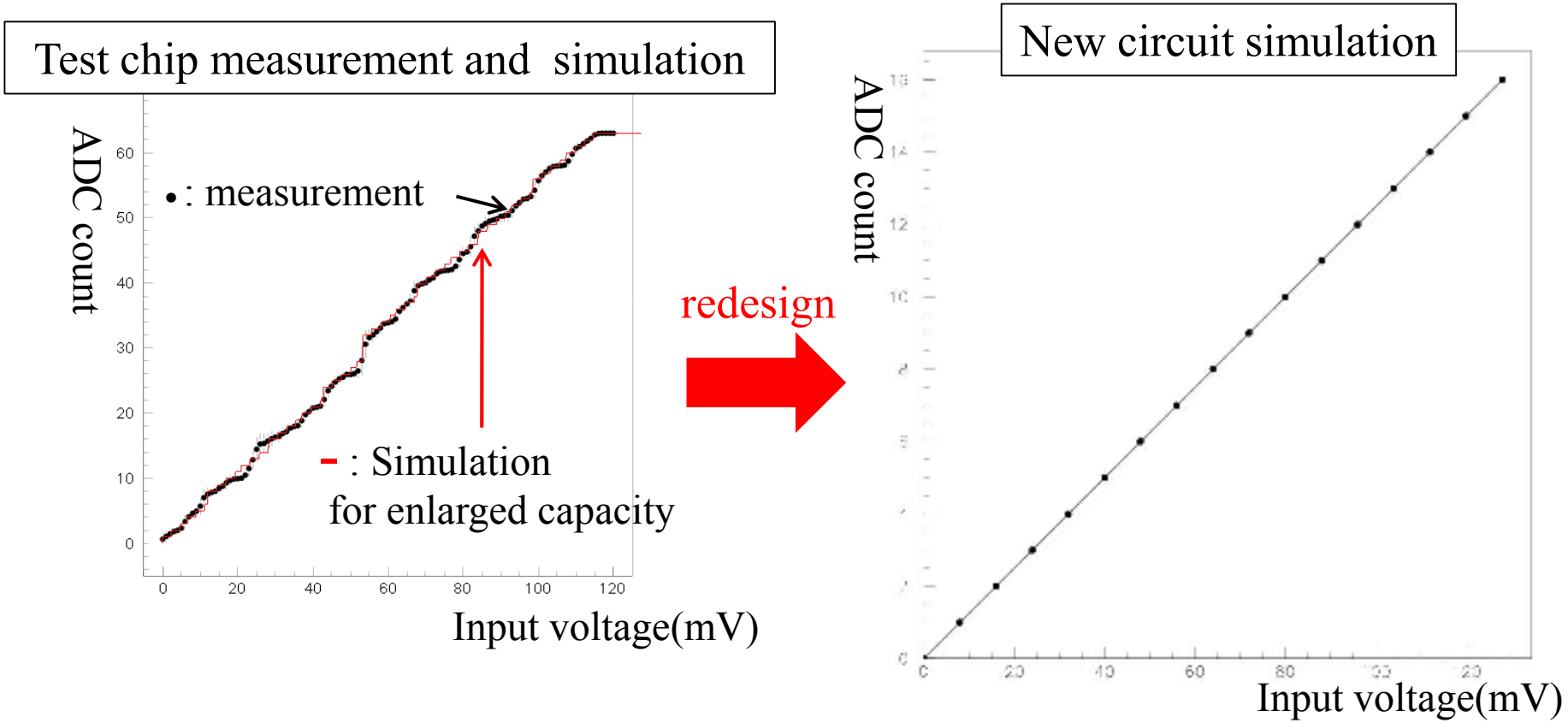


• The floating capacitance at the switching circuit in the ADC unbalanced the ADC capacitor ratio.

⇨ The switching circuit was designed again.

New circuit

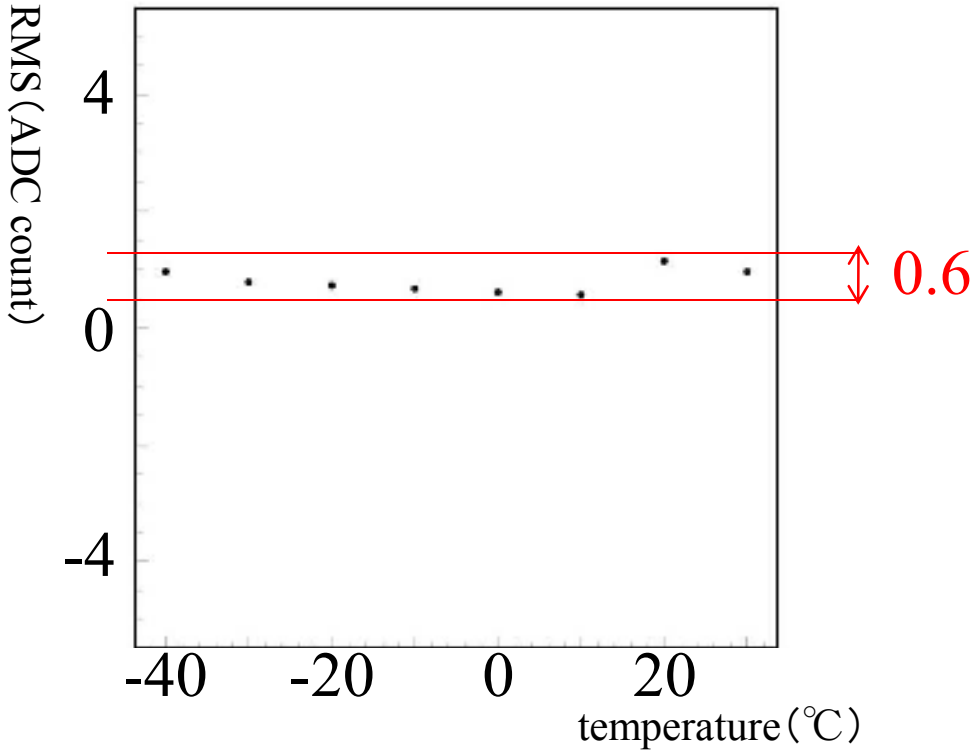
- ADC output was checked by simulation with new switching circuit.



➪ New circuit has no problem, and is adopted to the next sample.

Temperature dependency of Pedestal

- The pedestal distribution was measured for various temperature.

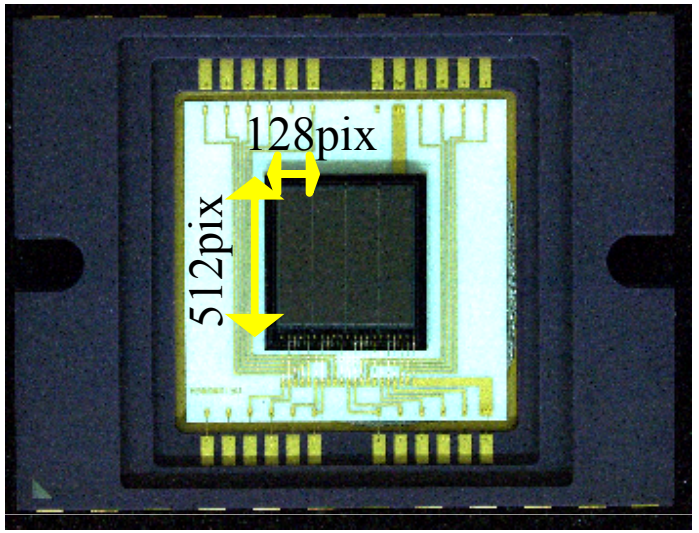


- The main fluctuation of RMS comes from effect of the missing ADC counts.
- The temperature dependency is smaller than the RMS fluctuation.

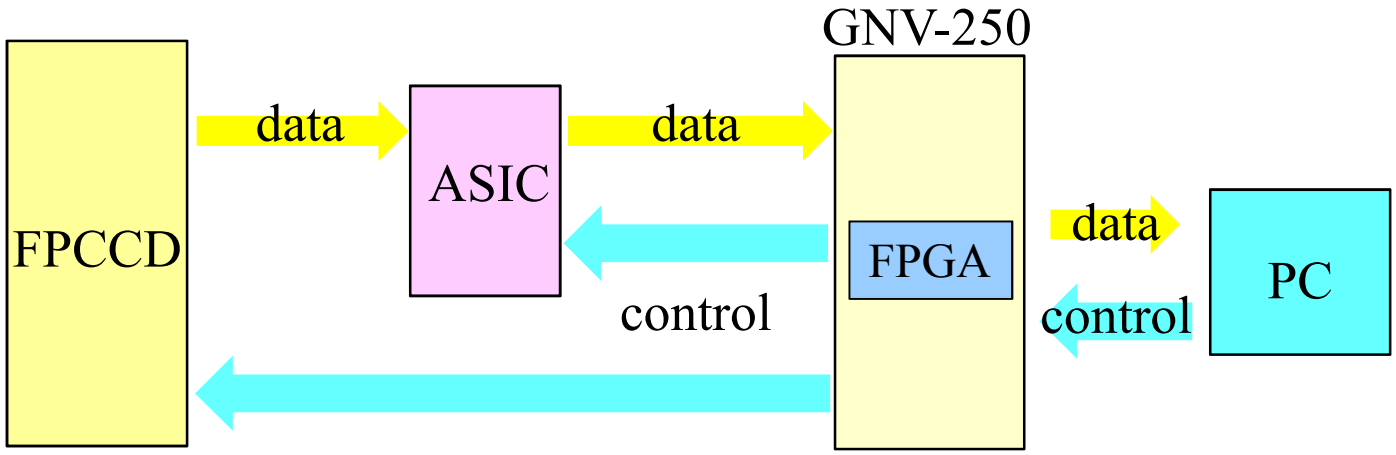
⇨ The temperature dependency will be studied with the next sample.

Fine Pixel CCD sample

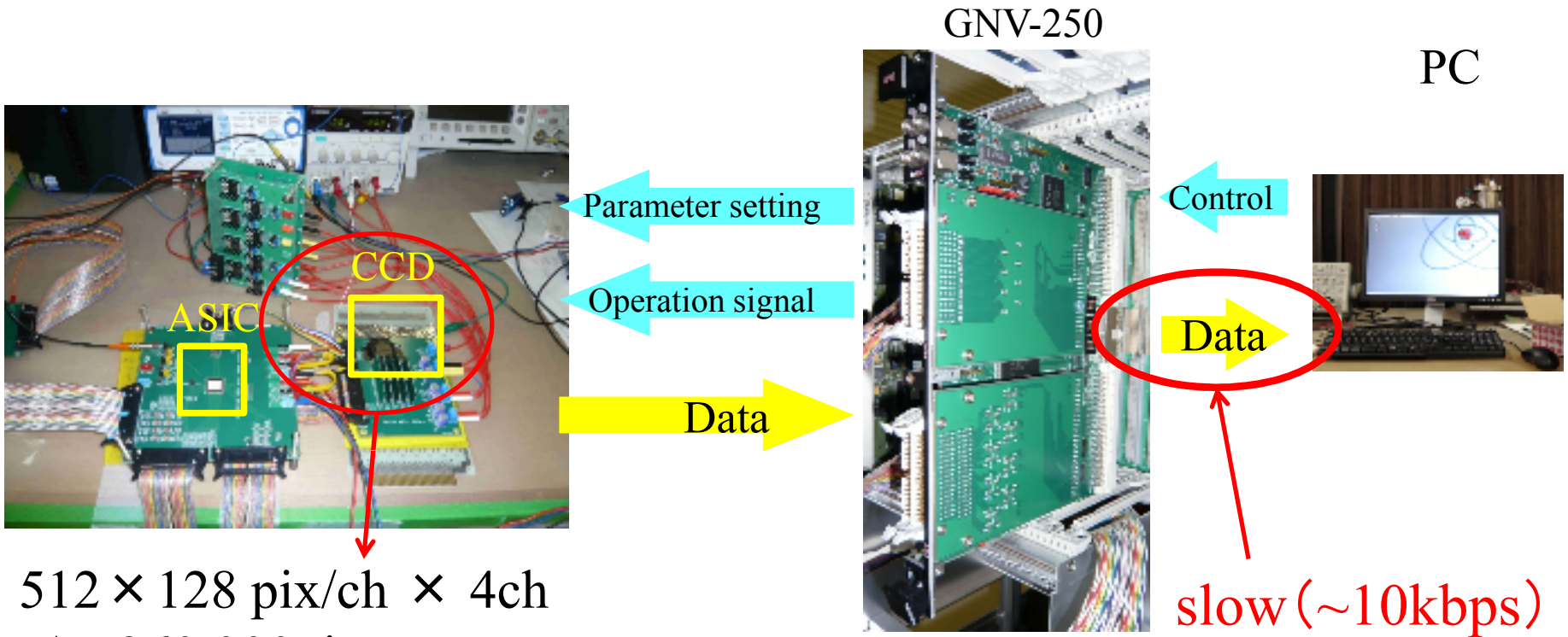
- Test sample to establish technology
  - Pixel size : 12μm × 12μm
  - Epitaxial layer thickness : 15μm
  - # of readout channels : 4ch
    - ➢512 × 128 pix/ch



- FPCCD and readout ASIC were connected.
  - The control logic for CCD was also implemented on FPGA.



FPCCD readout



512 × 128 pix/ch × 4ch
⇒ ~260,000pix

- Speed transmission of VME module to PC is slow.
- ADC output is temporarily stored in FIFO.
- By limit of FPGA capacity, all the data cannot be stored.

⇨ ADC data were converted to 1bit.

– Threshold : 30

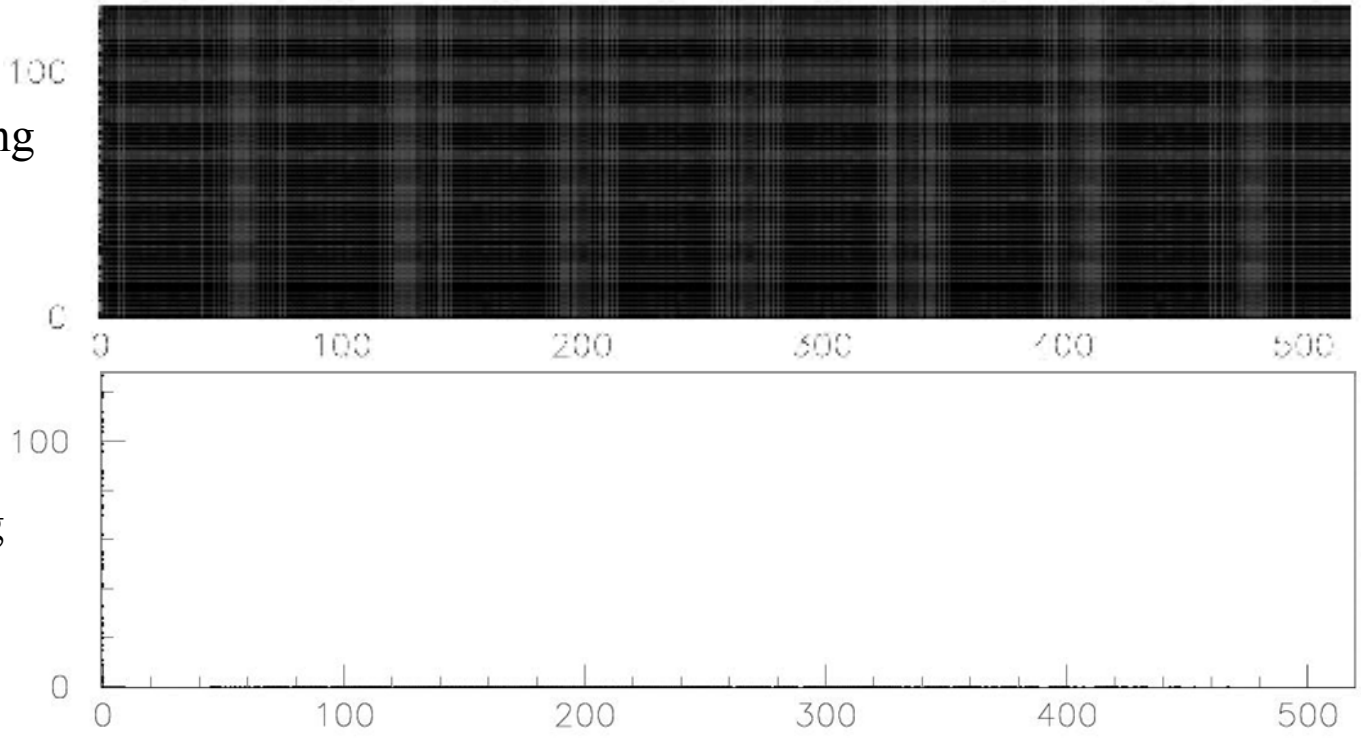
FPCCD reaction for light

- Response of FPCCD to the light was checked.

Black : do not react
White : react

Light shielding

No shielding



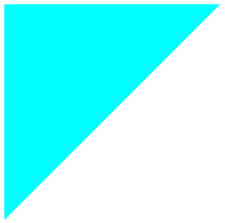
- 1channel(512 × 128 pixel)

⇨ Response of FPCCD to the light emission can be observed.

⇨ The image will be read as the next step.

Summary

- We developed FPCCD vertex detector
  - ➢ Requirement for readout ASIC
    - ◆ Power consumption < 6mW/ch
    - ◆ Readout rate > 10Mpix/sec
    - ◆ Noise level < 30e
- Pedestal check for readout ASIC sample
  - ➢ Noise level ～ 45e
  - ➢ Some ADC count are not output.
  - ⇨ switching circuit was designed again.
  - ➢ Temperature dependency of ASIC cannot be observed because of missing ADC.
  - ⇨ examined next sample
- FPCCD sample readout
  - ➢ By limit of FPGA capacity, all pixel cannot read out.
  - ⇨ ADC data were converted 1bit.
  - ➢ Readout ASIC can read out FPCCD data
  - ⇨ Next step is readout image
  - ➢ Readout board can read out all pixel is developed and tested.



Buck up

Power consumption of LVDS

- Differential voltage : 350mV
- Resistor : 100Ω
- Power consumption : $(350mV)^2$ / 100Ω = 1.2mW
- Below 6mV