CMOS pixels with Charge Storage : ISIS2

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and LCFI collaboration

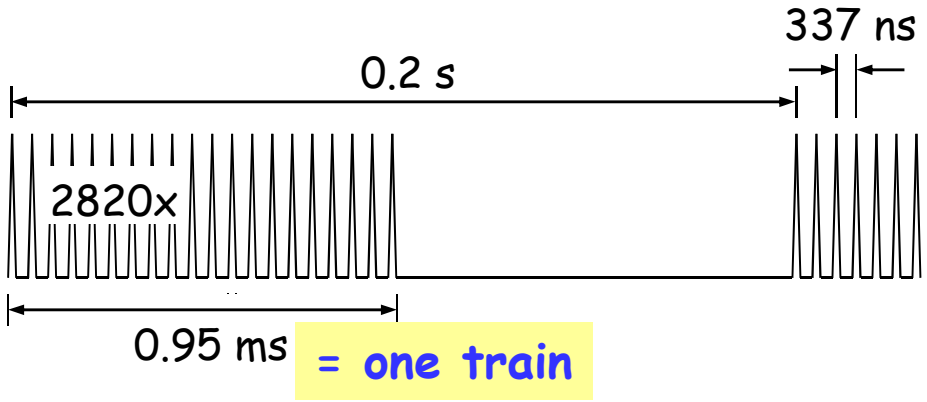
ALCPG09, 30 September 2009

Outline

- ISIS introduction
- ISIS1
- ISIS2 Test structure
- ISIS2 Full array

- Summary

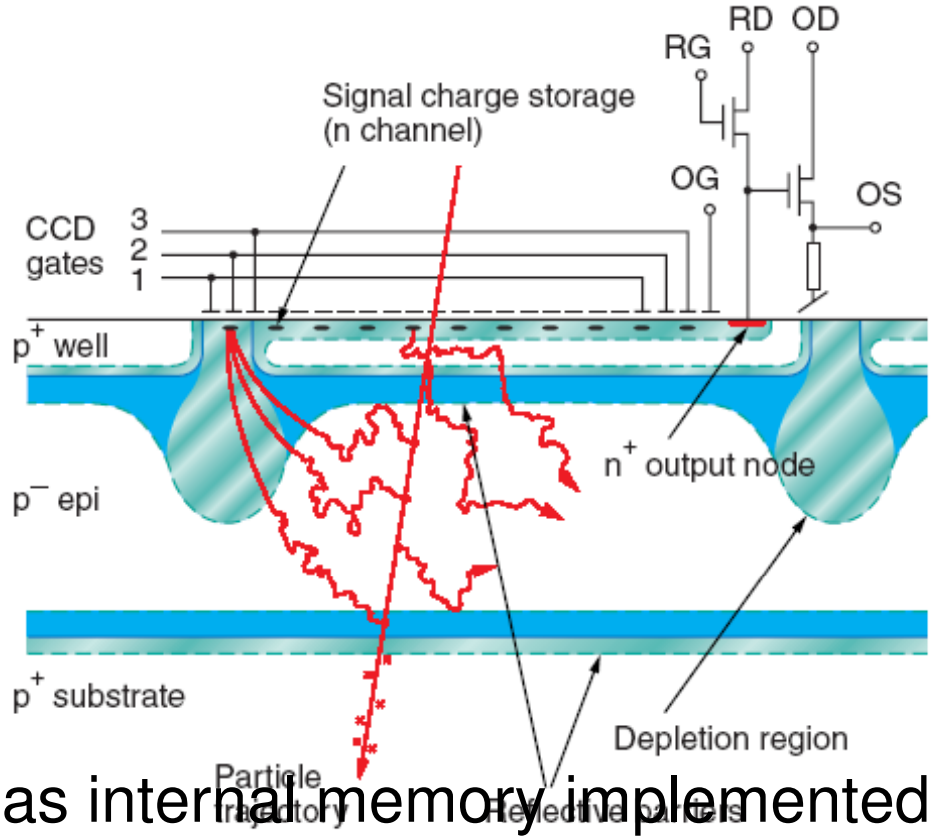
Two Approaches to Time Slicing



- Large bkg → need 20 time slices in one bunch train
- Can do
  - Fast readout → CPCCD, MAPS, DEPFET, …
  - In pixel storage → ISIS

- In pixel storage does not need power cycling – mechanical implications

ISIS – In-Situ Storage Image Sensor



- Each pixel has internal memory implemented as CCD register
  - Charge collected under a photogate
  - Charge is transferred to 20-pixel storage CCD in situ during collisions
  - Conversion to voltage and readout in the 200 ms-long quiet period after collisions

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ISIS as Imaging Sensor

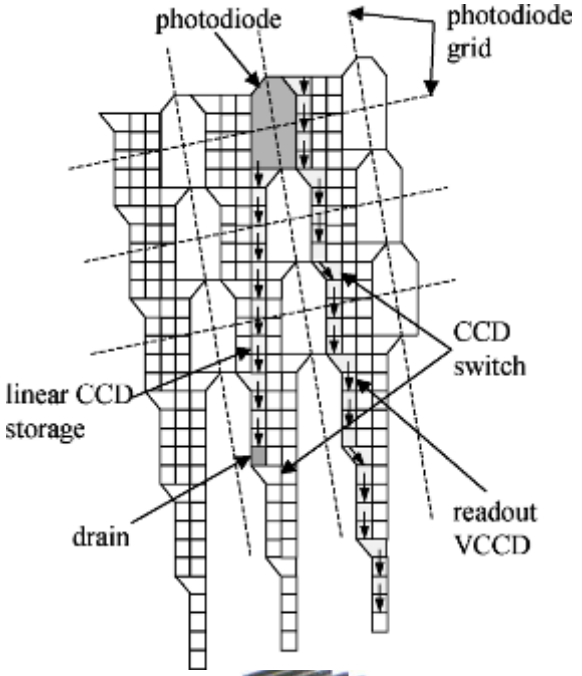
- First proposed for visible light

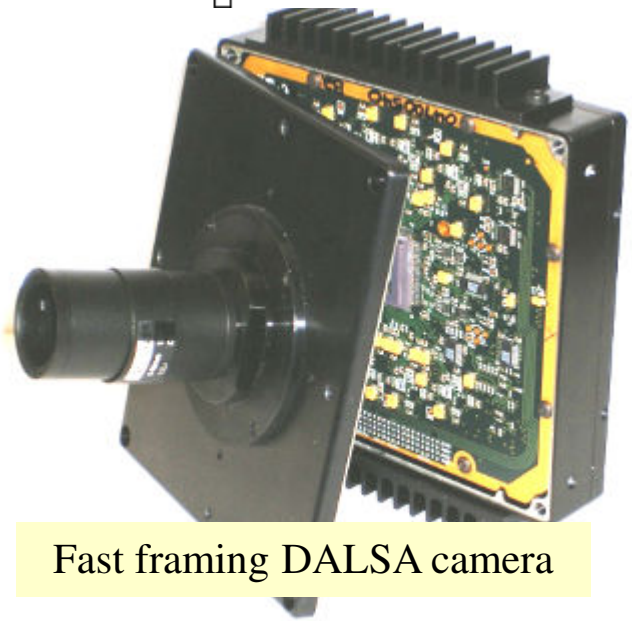
  ETOH *et al.* IEEETRANS ELECTRON DEVICES, 50, (2003) pp 144-151

  – 103 sequential images at 312x260 resolution
  – Max frame rate: 1 MHz

- CCD camera by DALSA
  – 16 sequential images at 64x64 resolution
  – Pixel : 100 x 100 μm^2
  – Max frame rate 100 MHz (!)
  – Used for Imaging Mass Spectroscopy

- Interest for fast X-ray detection at light sources (XFEL)

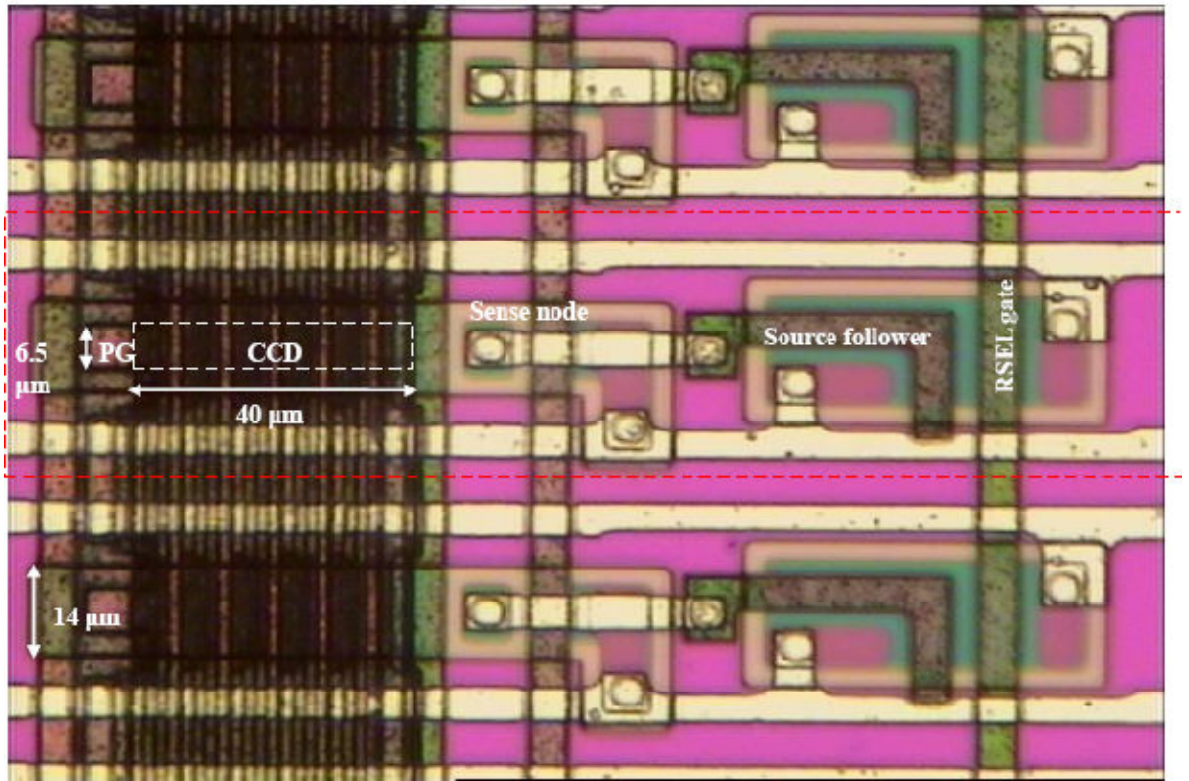


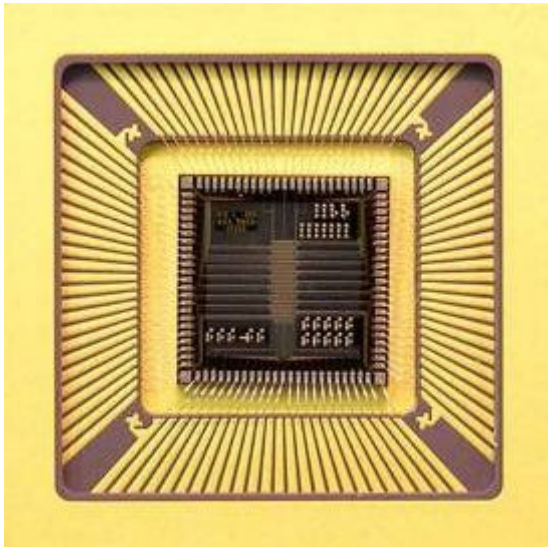


Fast framing DALSA camera

ISIS1

- e2V CCD ~2 μm process
- pixel 160 x 40 μm; 5 storage cells
- Two variations : with and without p-well





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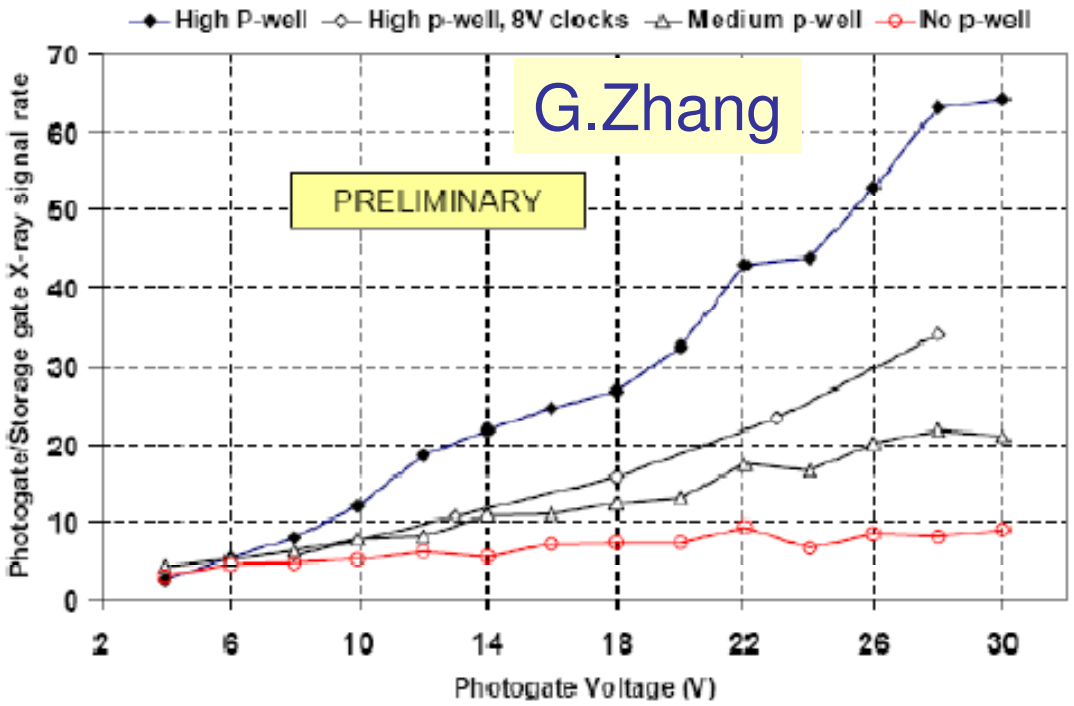
ISIS1 Results

- Tested with ^{55}Fe
- High p-well doping protect storage register
- Look at ratio of charge collected at photogate to charge collected at storage pixel
  - If increase clock voltage, get punch through under in-pixel CCD, R drops
  - Lower p-well doping, charge reflection decreases



ISIS1 publications:

Zhang *et al* Nucl.Instr.Meth. A607 (2009) 538

Testbeam results

J.J.Velthuis *et al*. Nucl.Instr.Meth..A599 (2009) 161
D. Cussans *et al*. Nucl.Instr.Meth. A604 (2009) 393

- 2008: ISIS Proof of Principle as particle detector

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ISIS2

Next generation ISIS: ISIS2

- Received ISIS2 from Jazz Semiconductor in Oct 2008
  - Process: 0.18 μm with dual gate oxide
  - Developed special process: buried channel and deep p+ implant
- First time ever CCD buried channel in a CMOS process

- Two independent sections of 32x128 pixels
  - Pixel size 80x10 um^2
  - Section area 3 mm^2
- A, B, C, D have different layout of deep p+ implant
- Rolling shutter readout of 32 columns

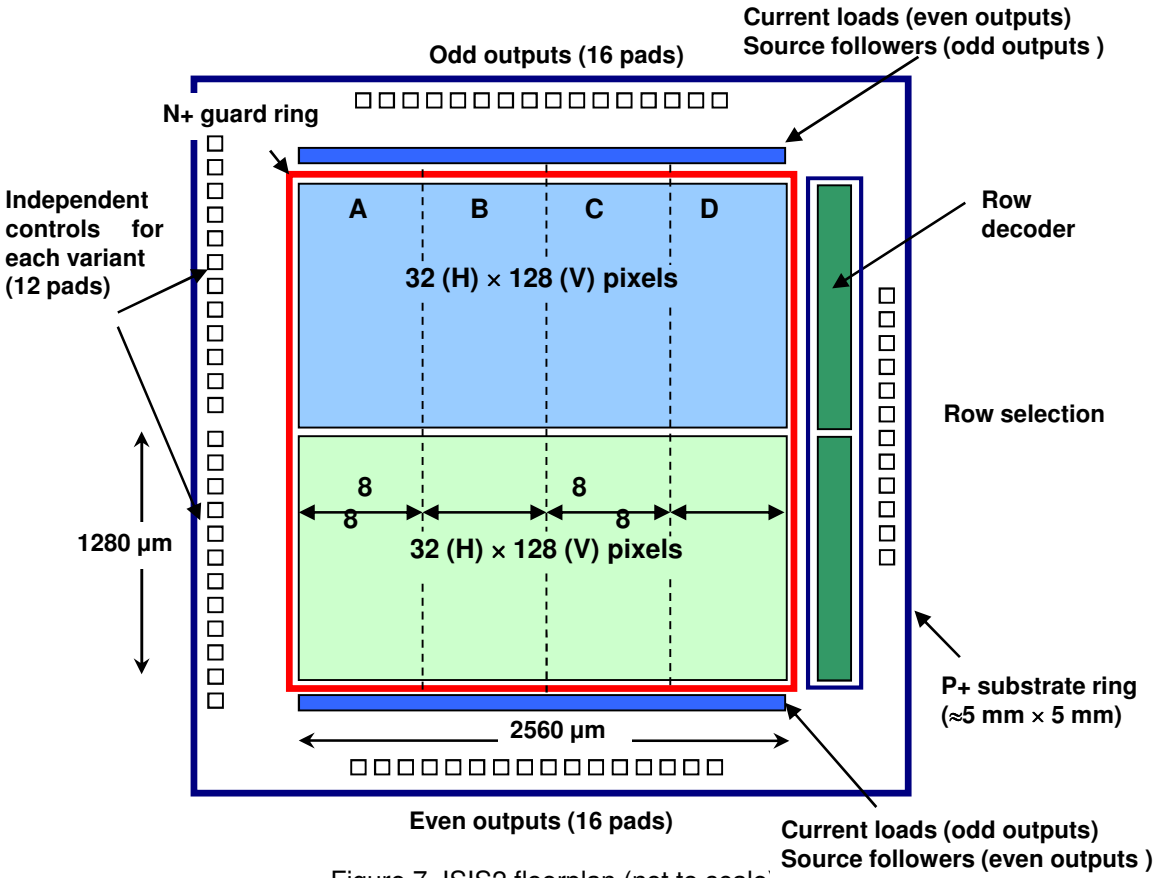
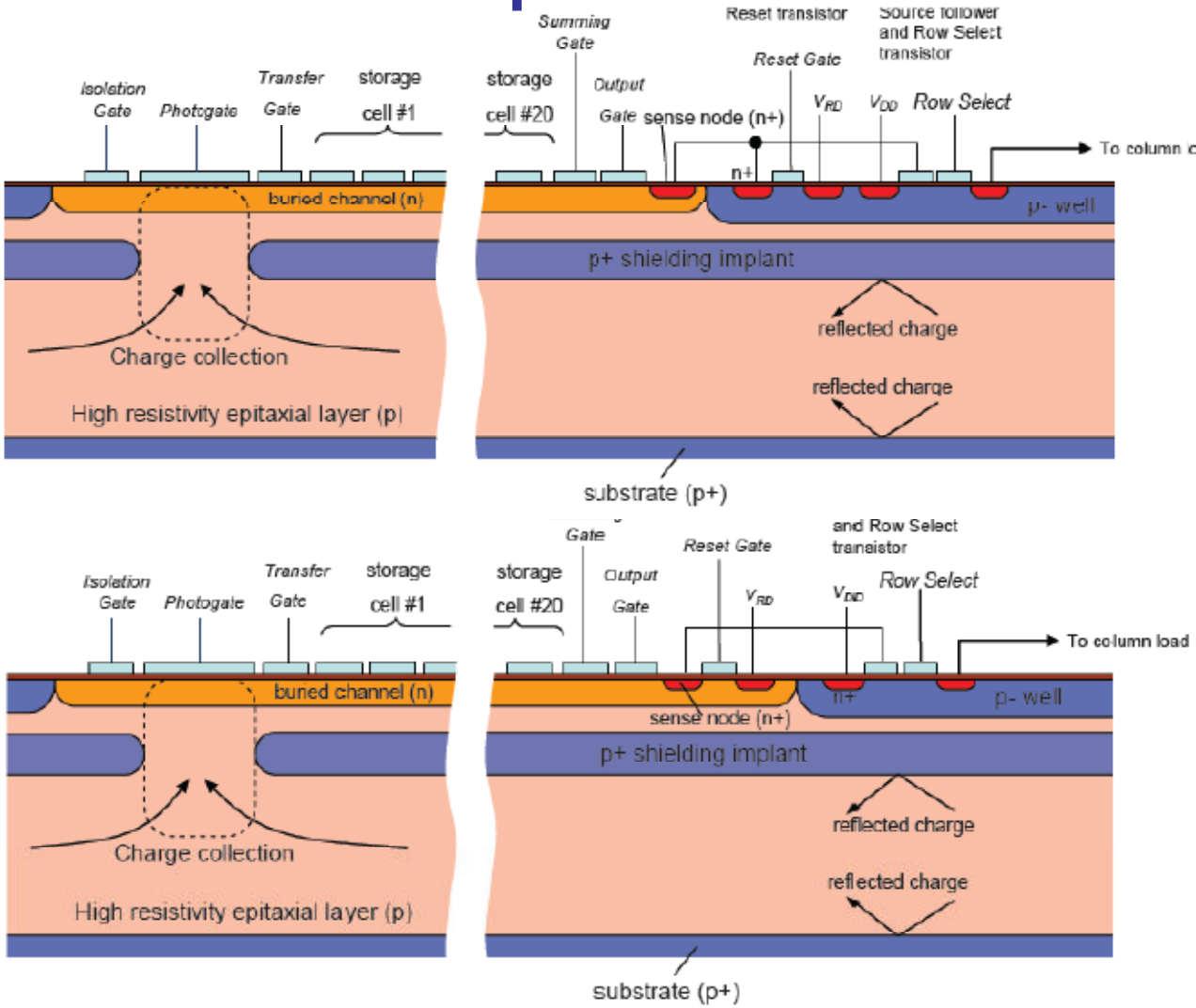


Figure 7. ISIS2 floorplan (not to scale).

ISIS2 Process Splits

- Reset transistor
  - Surface channel
  - Buried channel
- Other splits
  - CCD gate width
  - With and without deep p+
  - With deep p+ but no charge collection hole
  - Changes in dopant concentrations of ~20%



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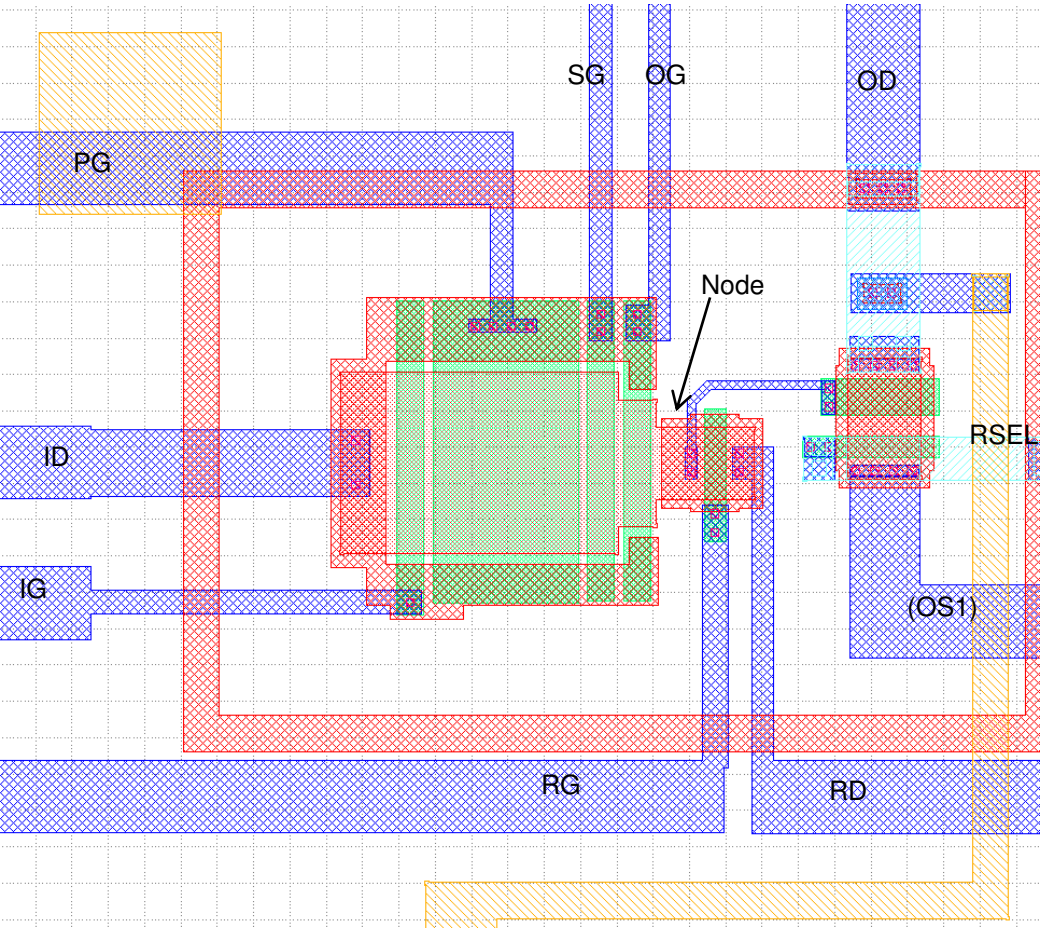
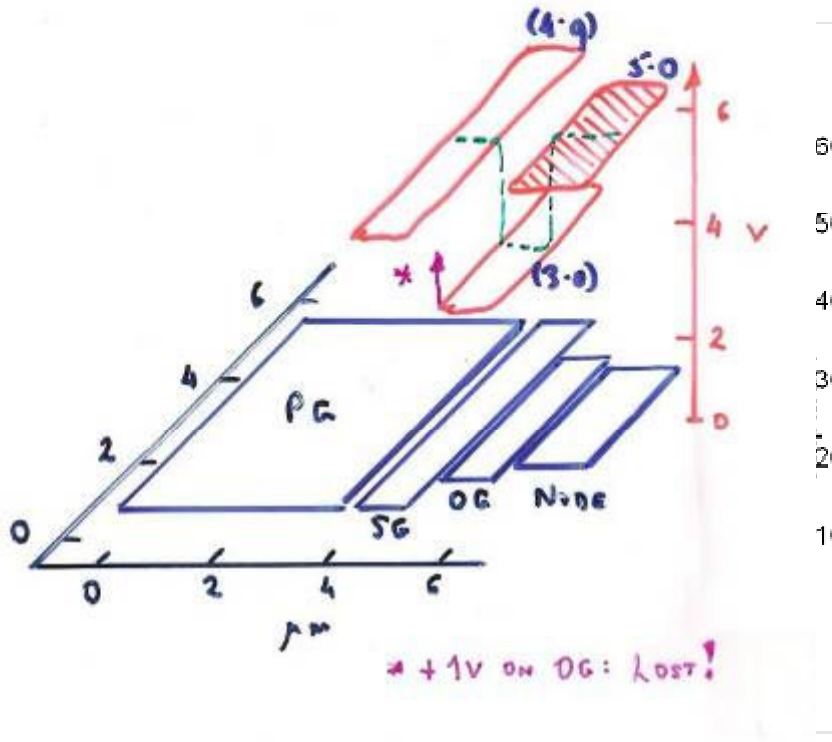
ISIS2 Test Results

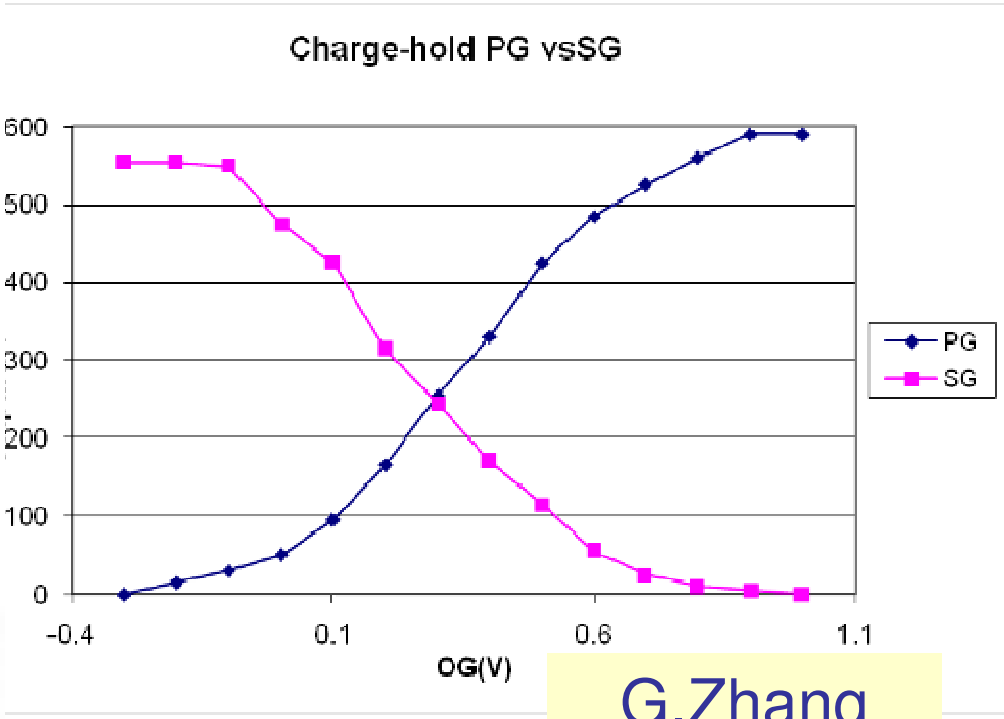
Test Structure



- Same as full array but no CCD transfer gates
  - Custom made 4T structure
- Allowed to establish operating conditions
  - Note tapered transition from Output/Summing gates to Output node
- Small feature size
  - Small capacitance of output node → expect excellent noise performance
  - Edge effects and 3D fringe fields are very important

ISIS2 Fringe Effect



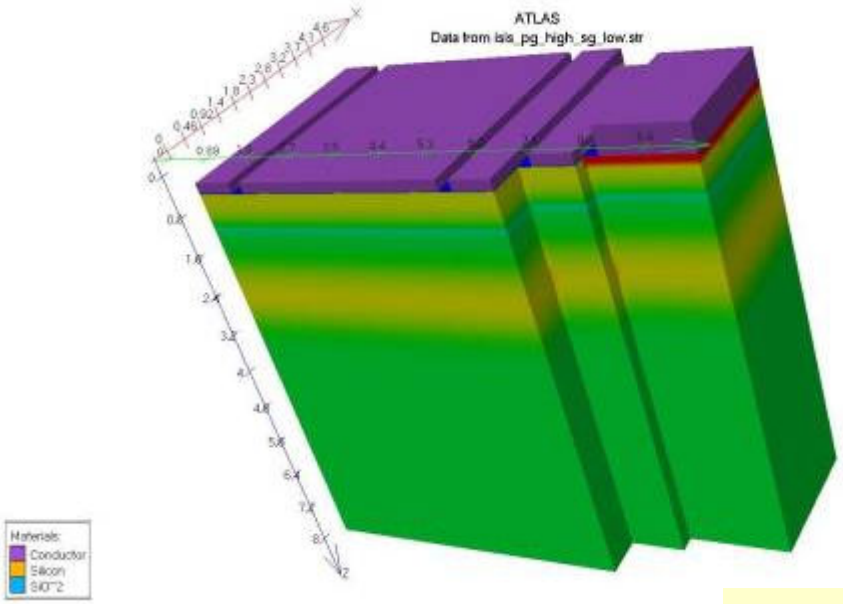


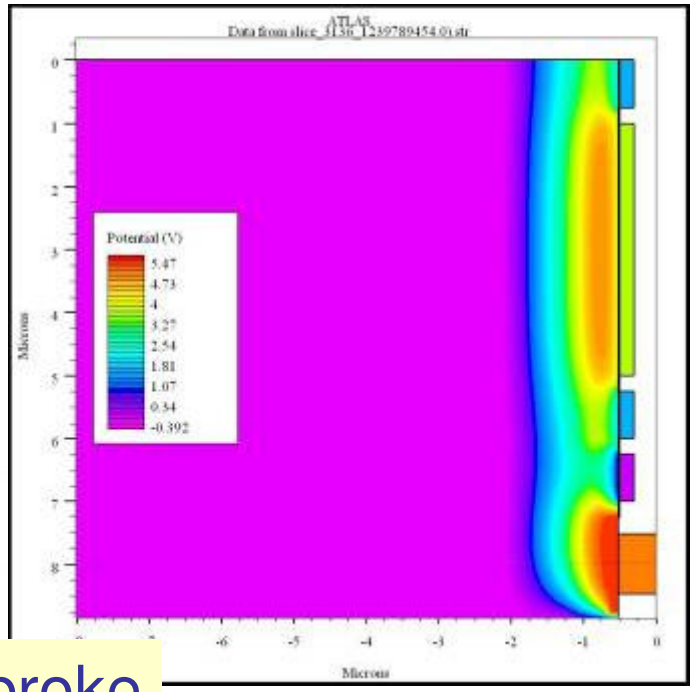
G.Zhang
Ch.Damerell

- Potential under the output gate pulled up by output node at 5V
  - Charge leaked to output node directly from photo gate

TCAD Simulations

- 3D simulations confirmed large fringe effects
  - Silvaco TCAD
  - Used 2D simulation before





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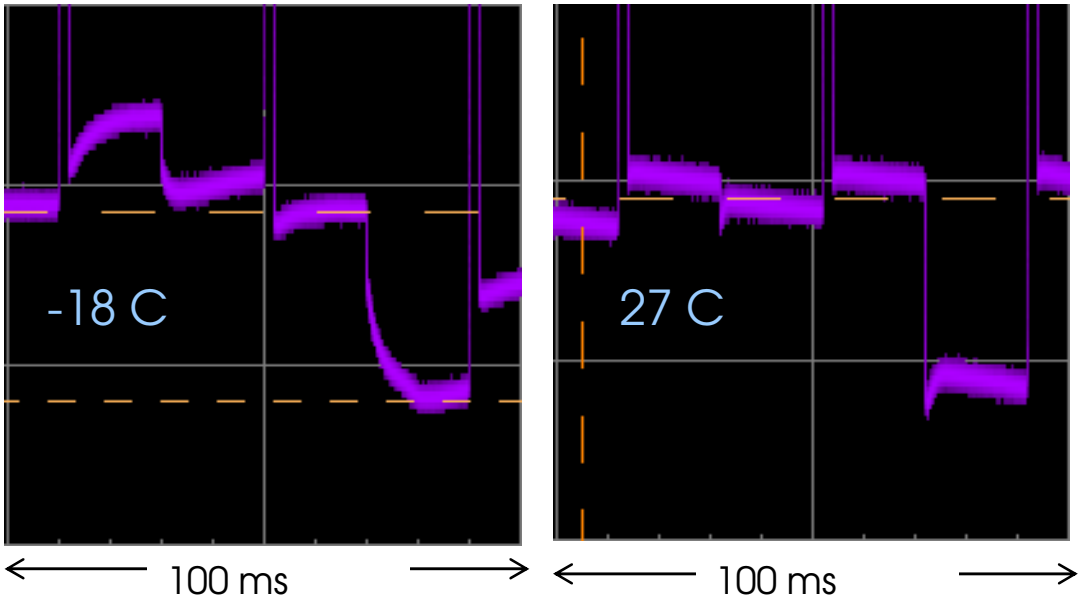
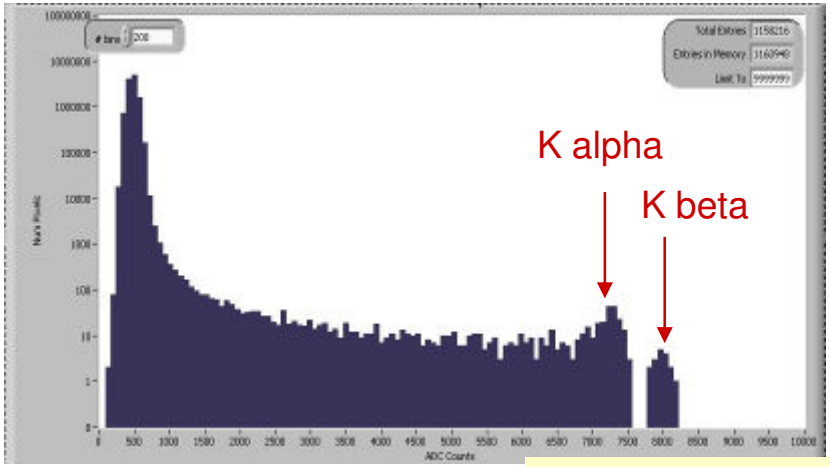
Readout Rate



- Processing/design flaw: large resistance of polysilicon gates
  - Gates are not doped
- It takes ~ a few ms for one transfer between two neighbouring gates
  - This means large dark current accumulated.
- Low temperature reduces dark current but also further increases the gate resistance
- Slow clock but anyway have efficient charge transfer

X-ray Calibration

- Calibration with Fe55 (1620e- and 1780e- lines)
  - Hits on output node (unclocked)
  - Hits transferred from photo gate
- Measured CTE, noise at different T
  - Sensitivity 24 μV/e-
  - Noise 6 e- achieved for optimum CDS timing

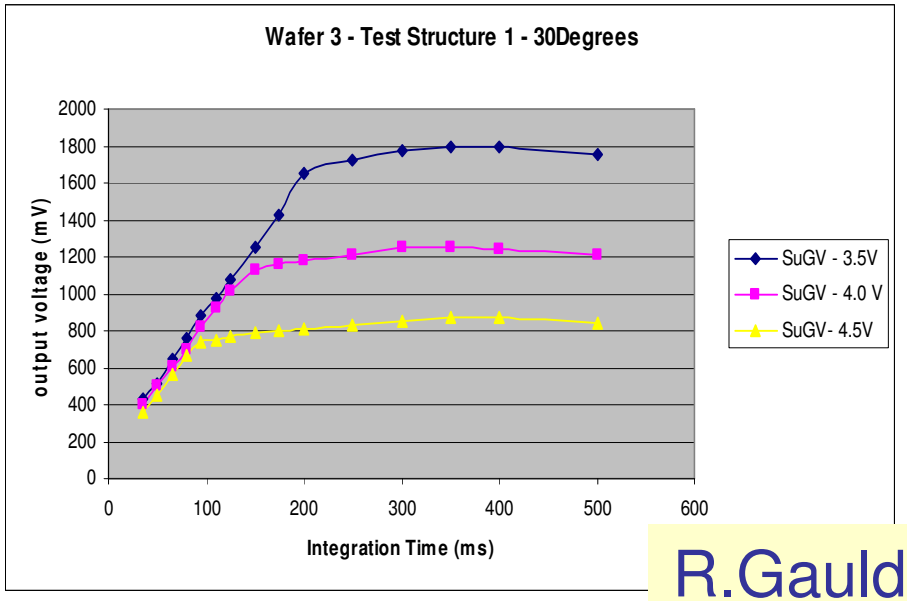


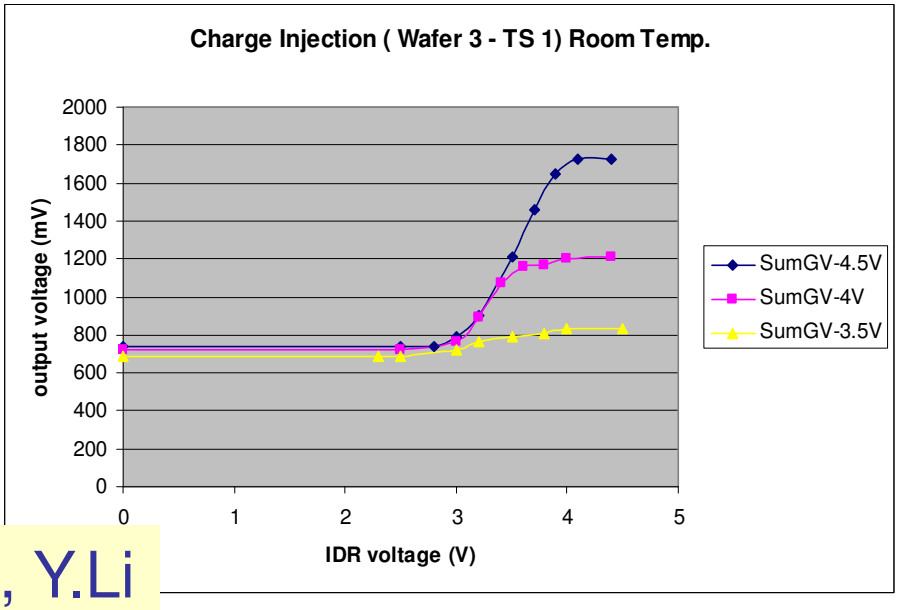
Fe55 calibration on OD

Signal-pedestal peak separation	-10C	31C
CTE	94.2%	94.5%
OD noise	20 e-	14 e-
PG noise	27 e-	66 e-

Y.Li, J.J.John, R.Gao

Charge Transfer Studies





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Leakage current

IDR: charge injection

- Can exercise by transferring charge from dark current, charge injection or LED
  - Good linearity
- Well capacity dependent on Summing Gate bias
  - 5-10ke for 1x5 μm PhotoGate

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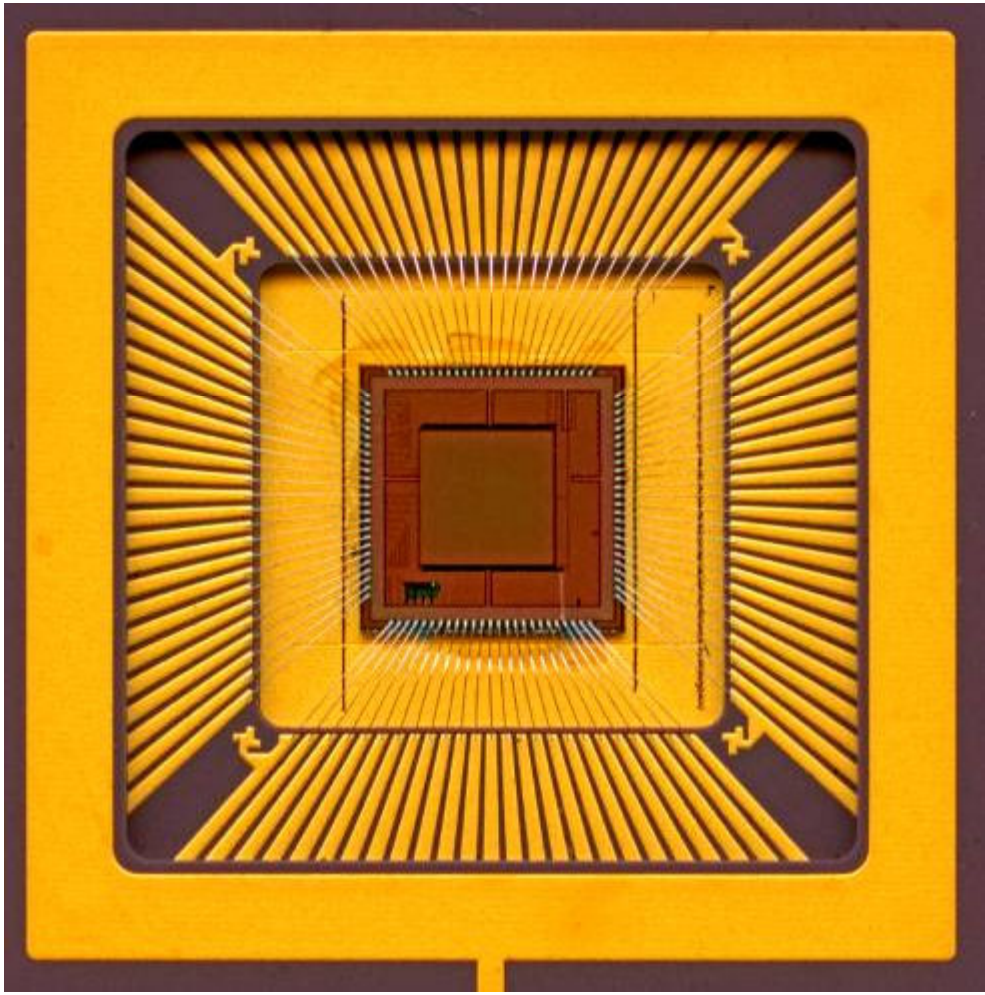
ISIS2 Main Array

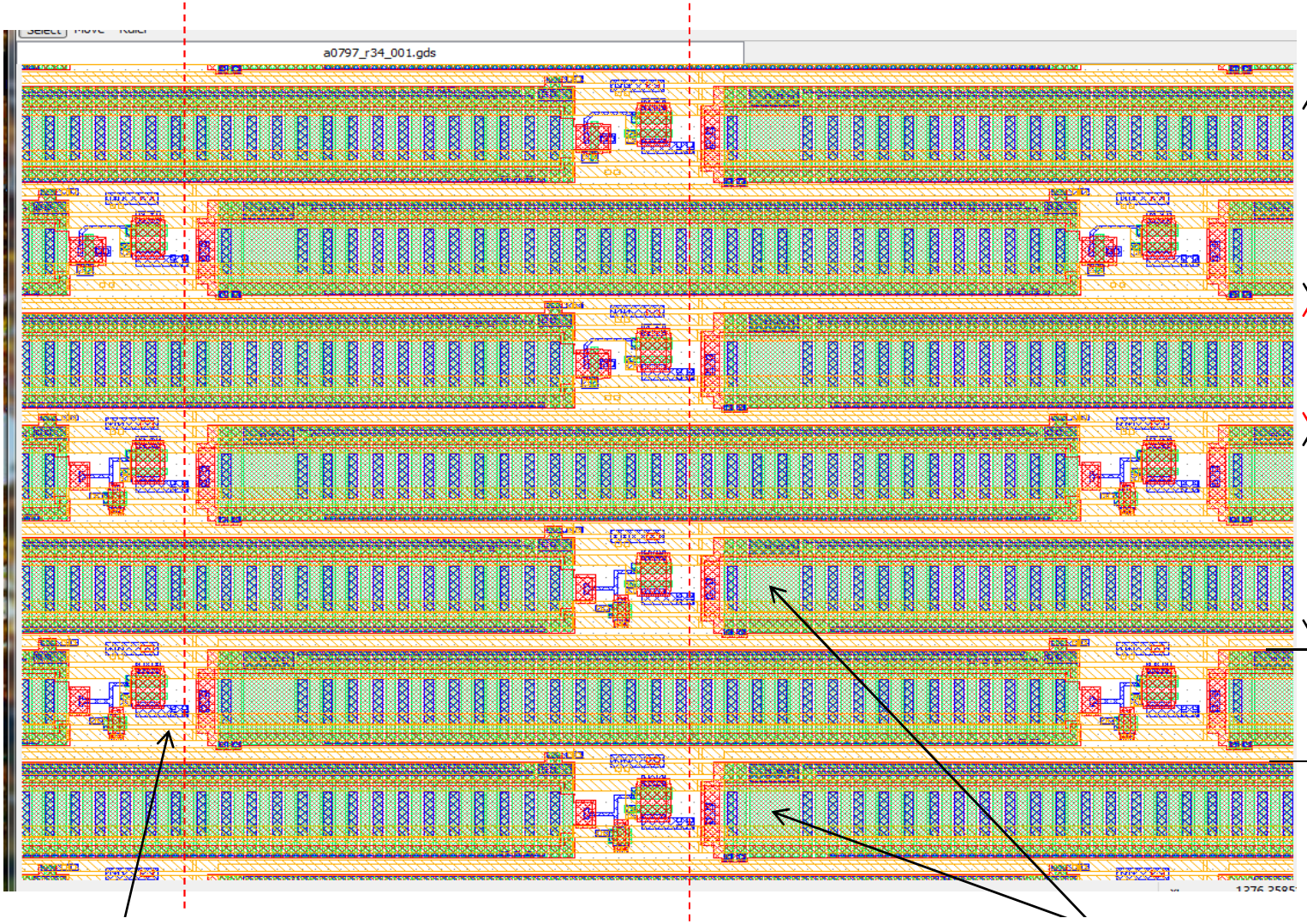
ISIS2 main array

- 256X32 pixels
- Pixel size 80x10 μm^2
- 20 storage cells

- Imaging pixel 40x20 μm^2



ISIS2 Pixel Layout



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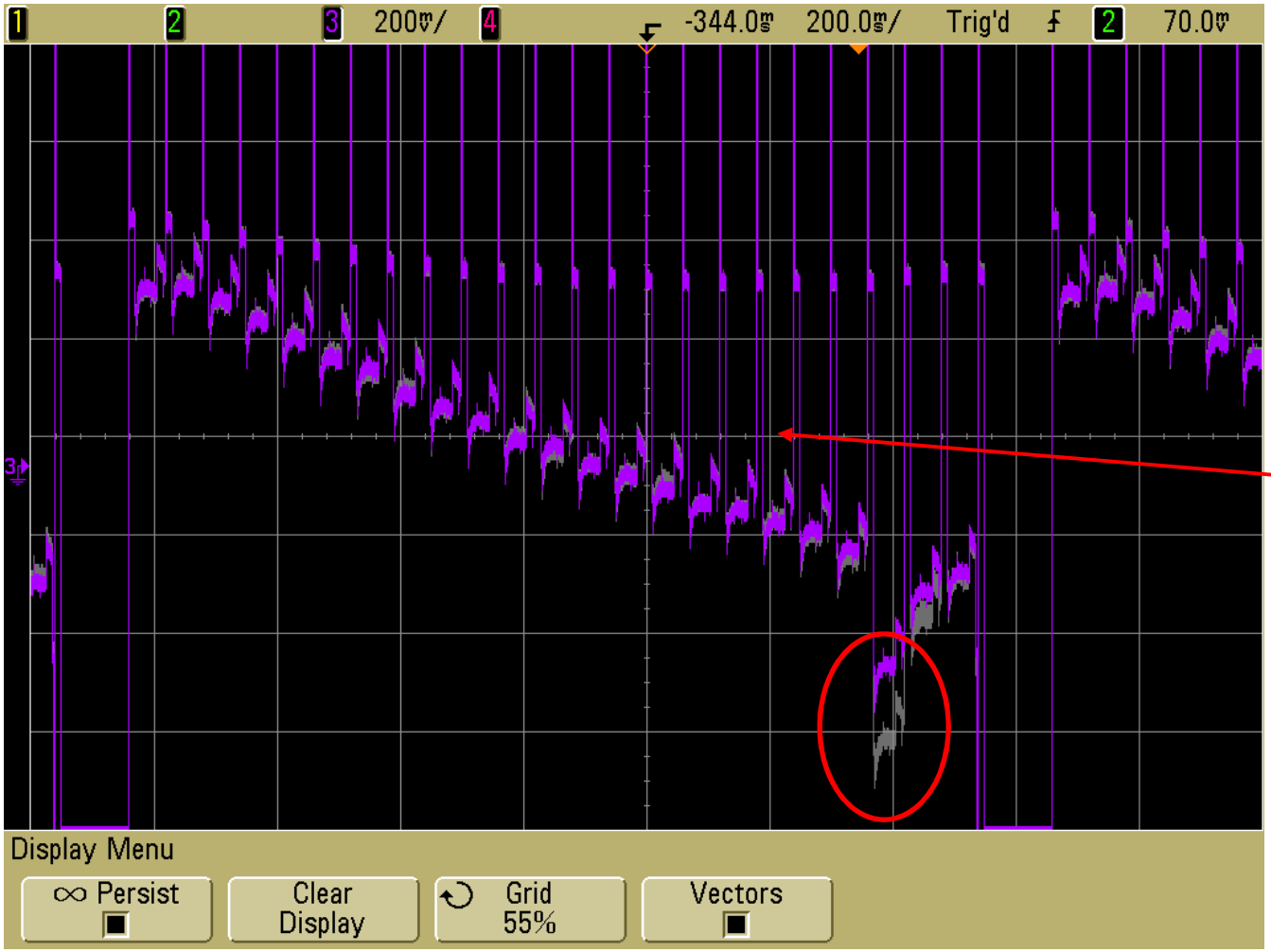
First successful charge transfer in main array on 21 July 2009!



The linear shape indicates leakage current accumulation.

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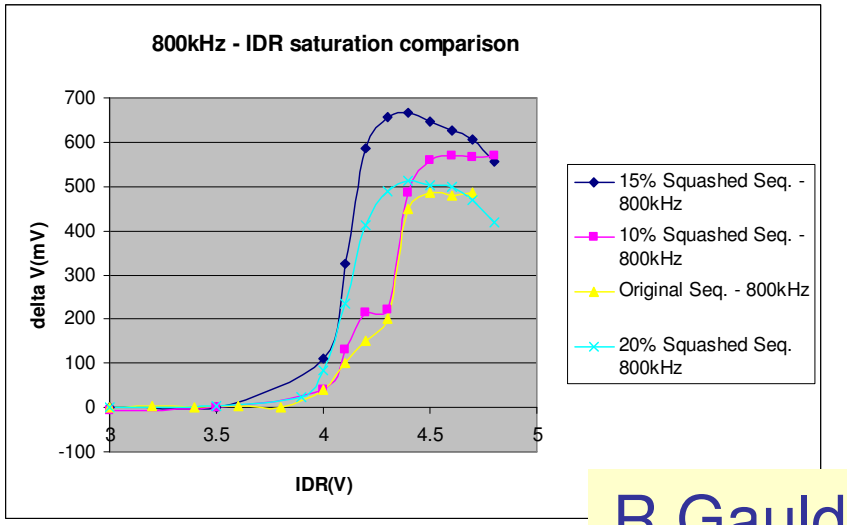
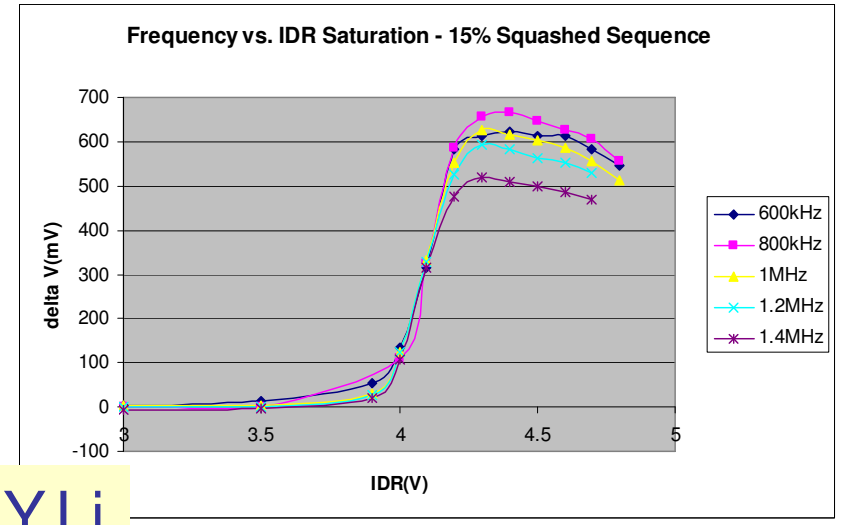
Readout Time Minimization





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Optimization of time sequence

- Reducing time for transfer gates, 85% of SG time
- Run at highest clock frequency

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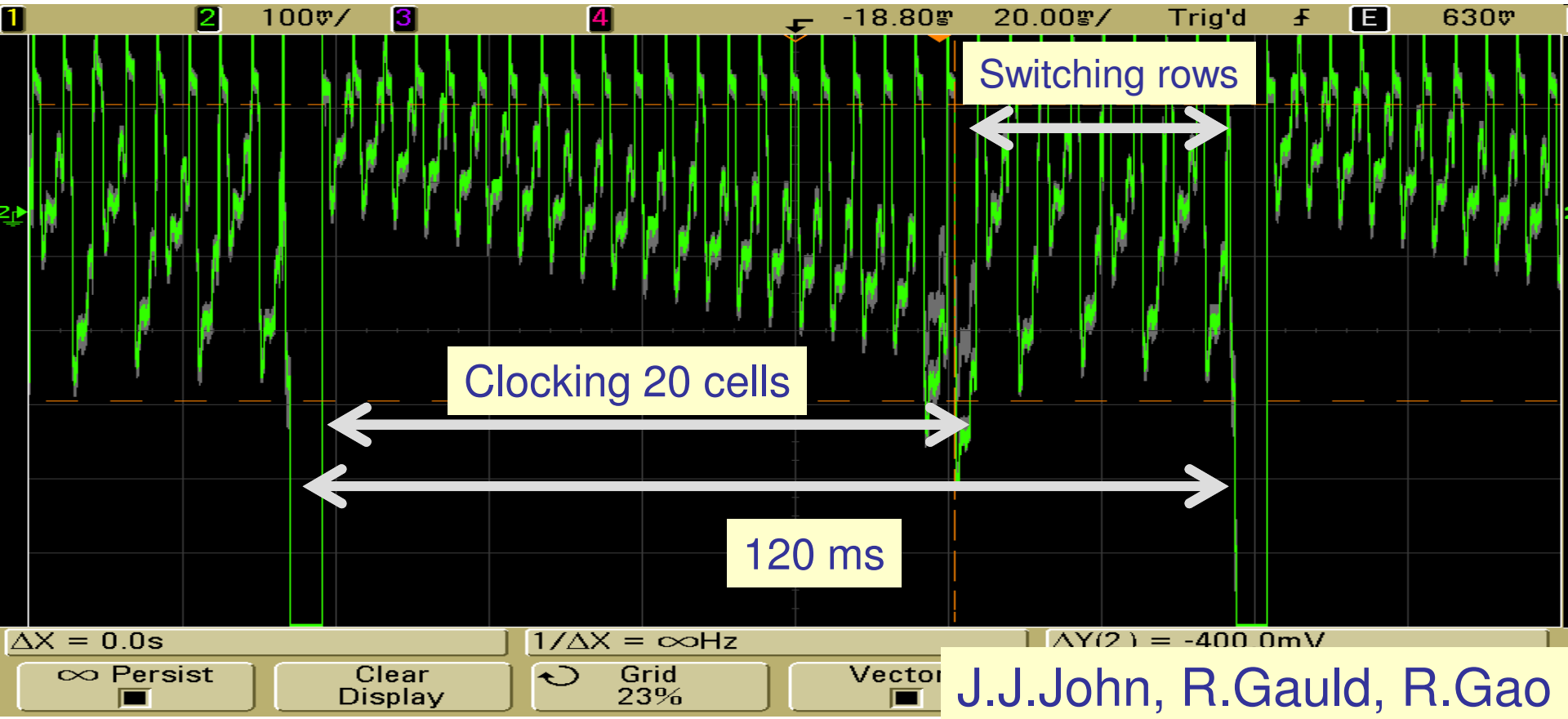
Max Readout Speed

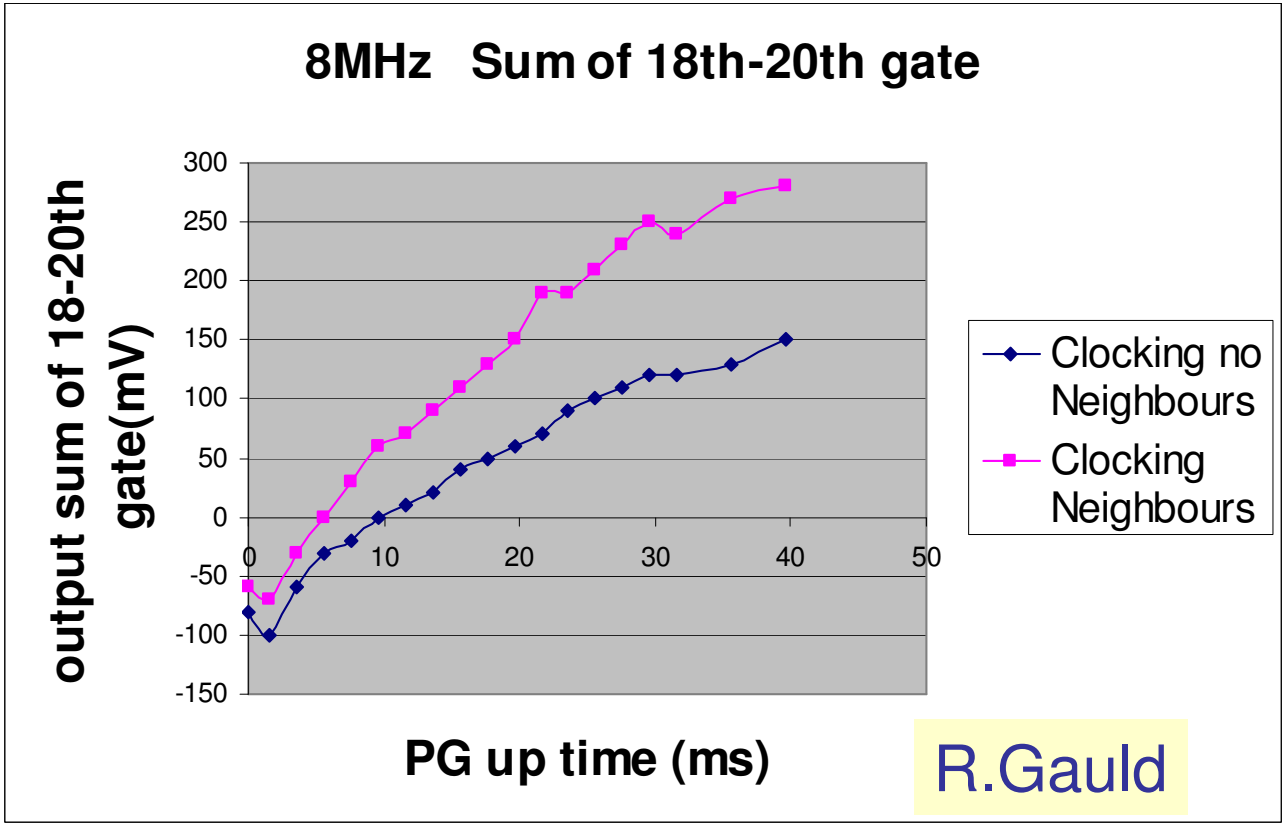
- 8 Hz for 5 rows
  - Achieved at room T
  - Each additional row adds ~few ms



J.J.John, R.Gauld, R.Gao

Clocking Neighbours

- Clears charge from neighbouring PGs
- Reduce leakage current in row under test



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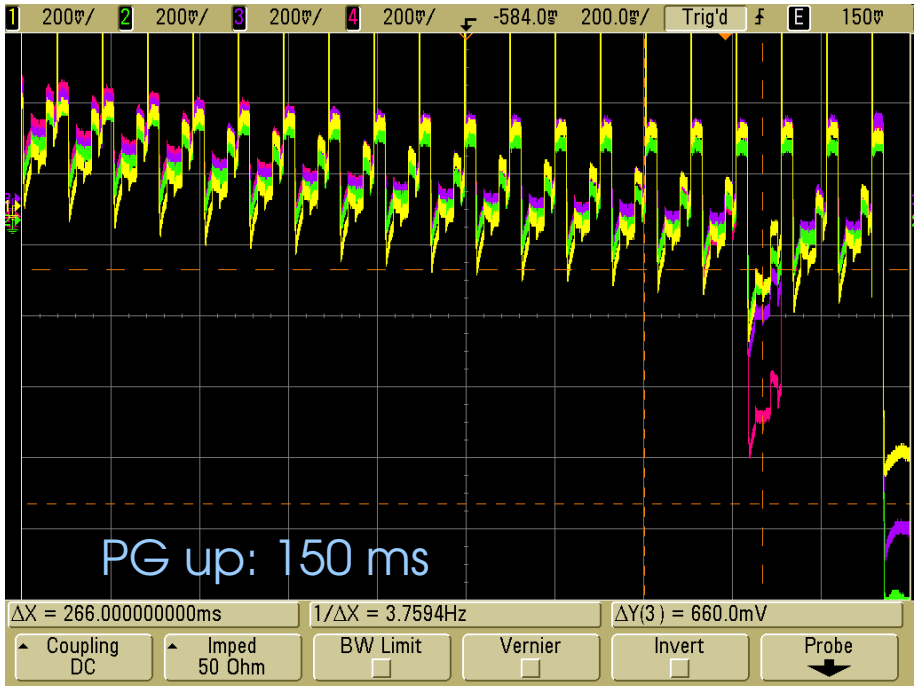
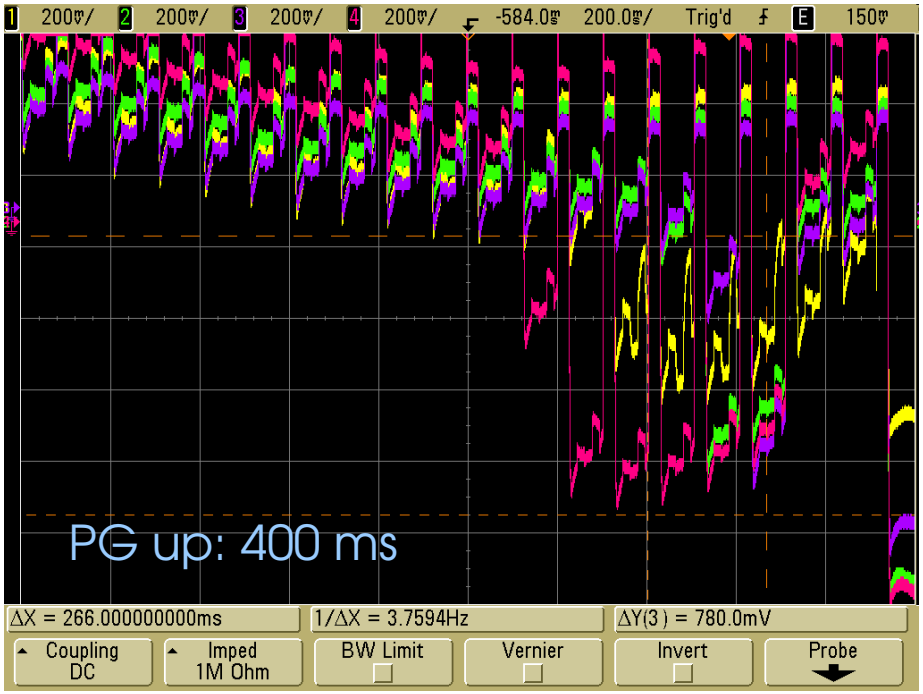
Comparison of deep p+ splits

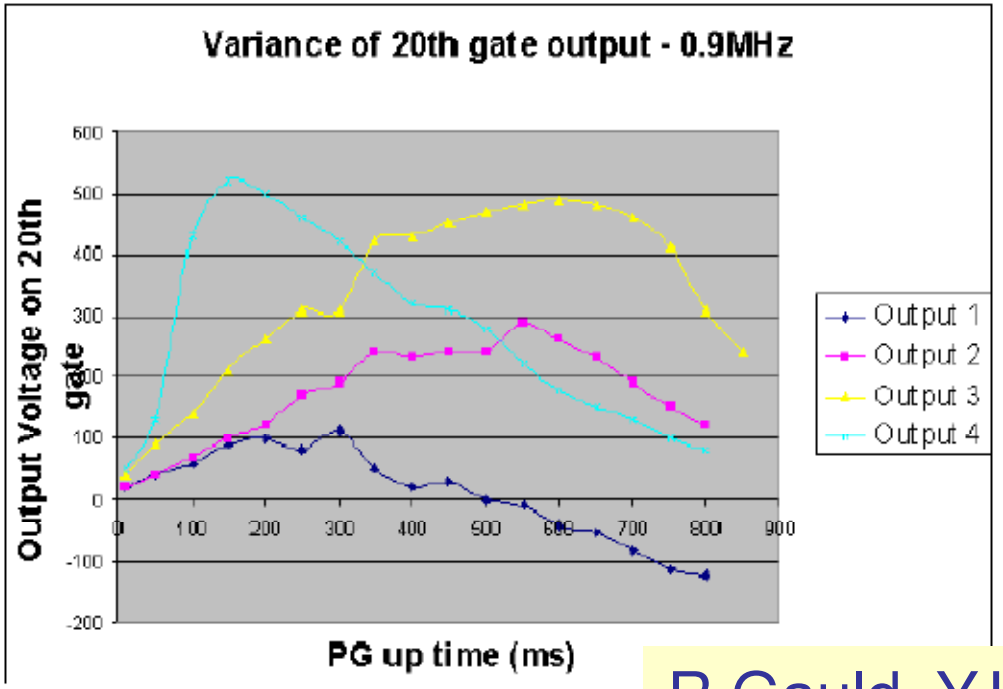




1: No deep p+ shield (YELLOW)
2: Deep p+ equal to PG over lap over buried channel (GREEN)
3: Same as 2 with extra 0.25um on all sides (PURPLE)
4: Deep p+ shield without aperture (PINK)

Dark Current Comparison

- Different dark current for different p+ splits



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Channel 1 (No deep p+)

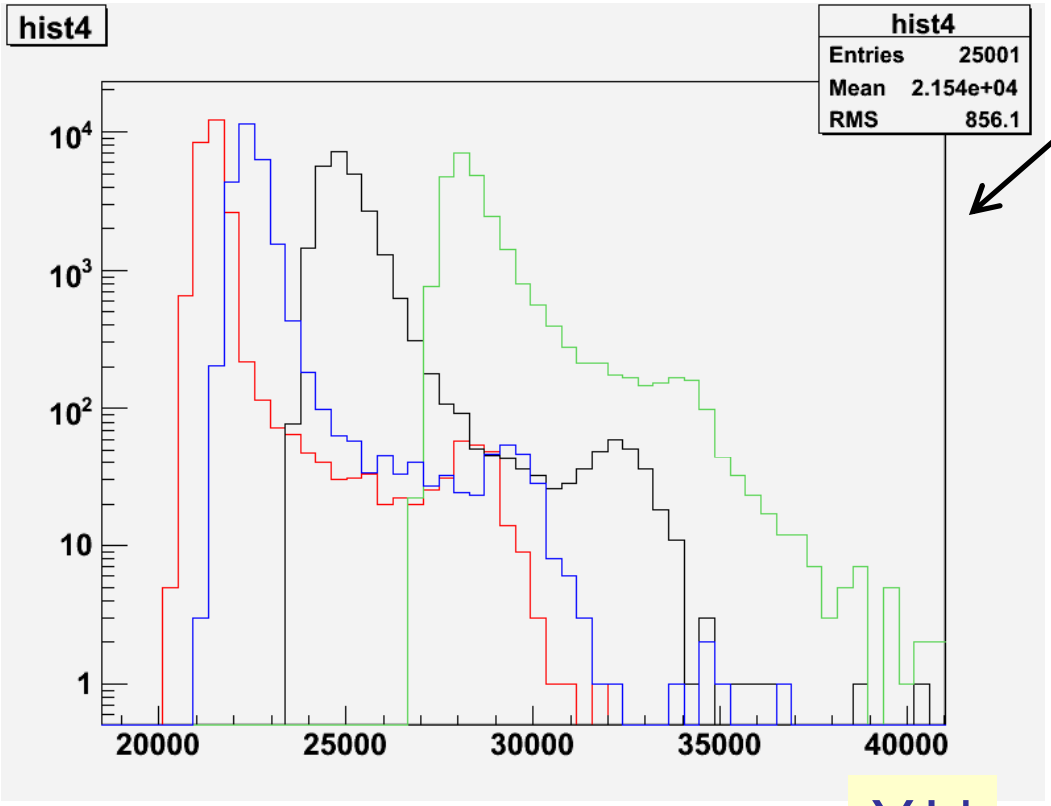
Channel 2 (Deep p+ with aperture = PG)

Channel 3 (Deep p+ with wider aperture)

Channel 4 (Deep p+ without aperture)

^{55}Fe Calibration

Temperature: -6 C; PG held up for 10 ms. The whole sequence is ~2.5 s so it is unclear how many hits were collected at photo gate.



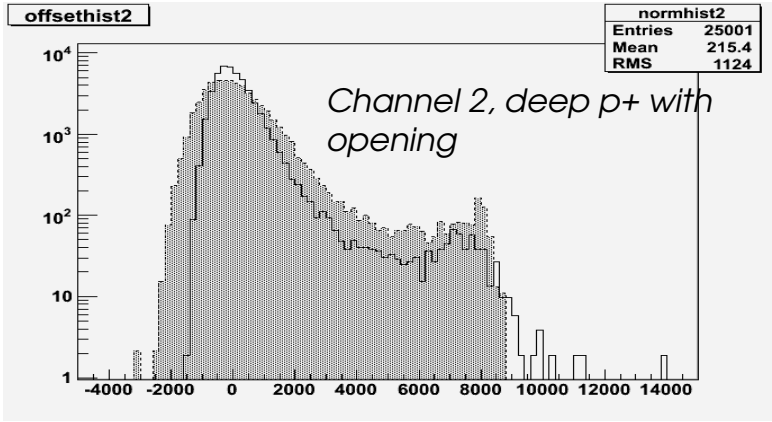
Y.Li

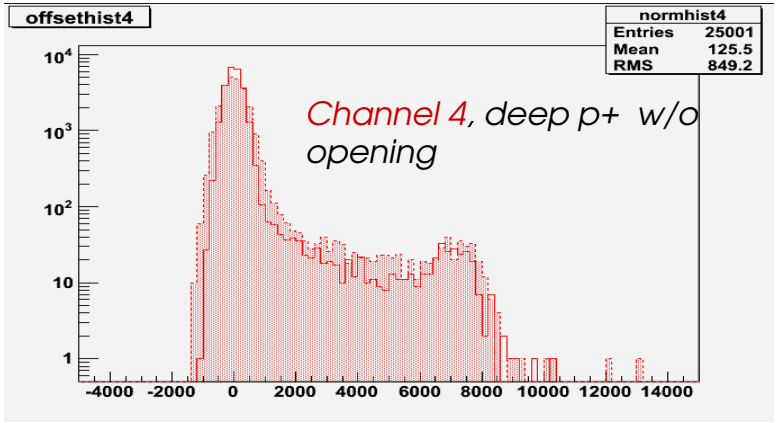
Blue: Channel 1 (No deep p+)

Black: Channel 2 (Deep p+ with aperture = PG)

Green: Channel 3 (Deep p+ with wider aperture)

Red: Channel 4 (Deep p+ without aperture)





Solid line: PG up 10 ms;

Filled area: PG up 50 ms.

Future plans

- Clearly already achieved more than could have hoped with just one sensor iteration!

Next

- Running of full array: 32 columns x 128 rows
  - Currently at 4 columns x 5 rows
- Do laser scans to map CCE and beam test to see charged particles

- Currently ISIS sensors are not funded in the UK due to STFC crisis and we are looking for ways to produce next sensor, ISIS2.1 or ISIS3

Summary

- ISIS2 successfully demonstrated feasibility of multiple charge storage and transfer in CMOS process
  - First implementation of CCD in CMOS process
  - 10 x 80 um pixel with 20 cells
  - Low noise
  - Efficient charge transfer

  - Slow rate understood, can be easily fixed

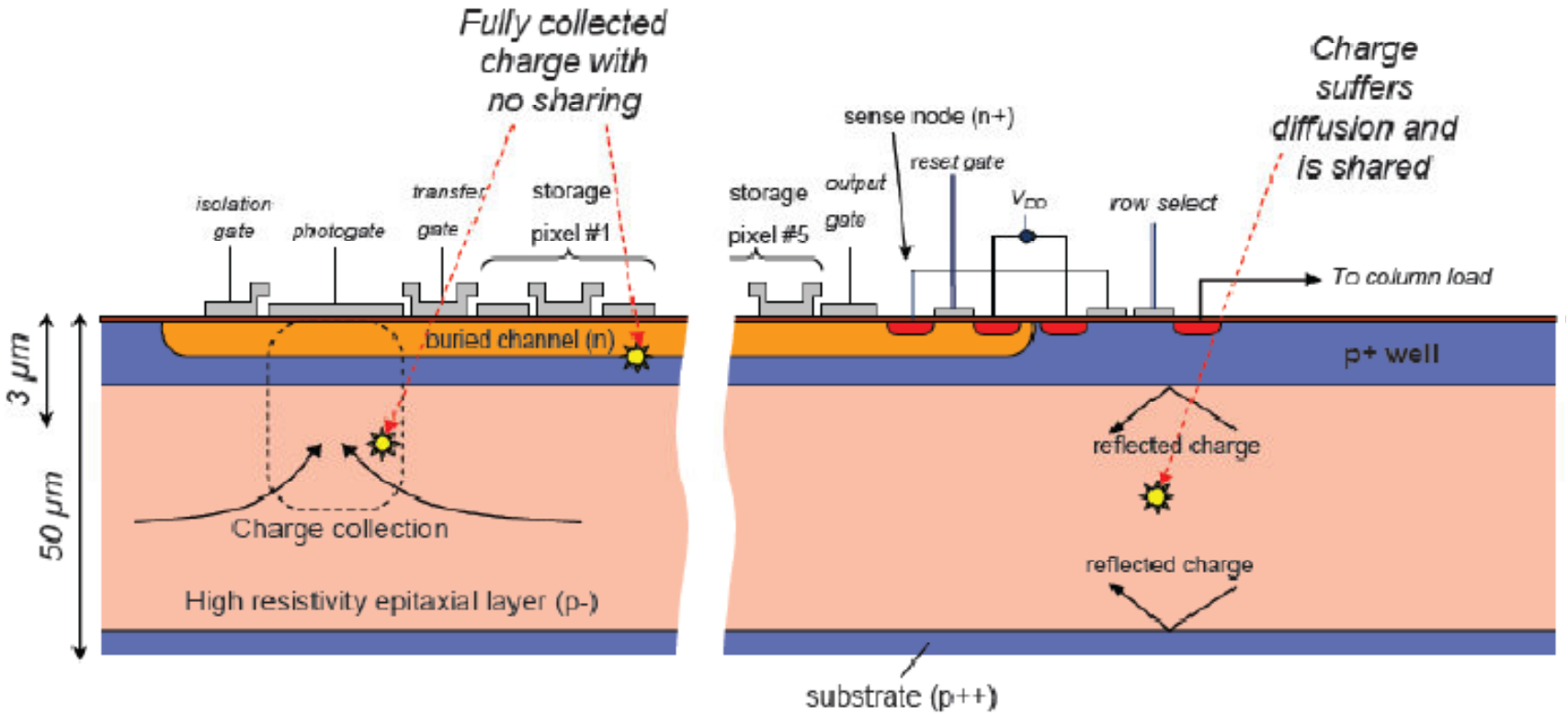
- Next: Laser testing & testbeam

Need to keep this promising approach to LC vertexing alive!

Backups

ISIS1 Charge Collection

- Tested with 55Fe



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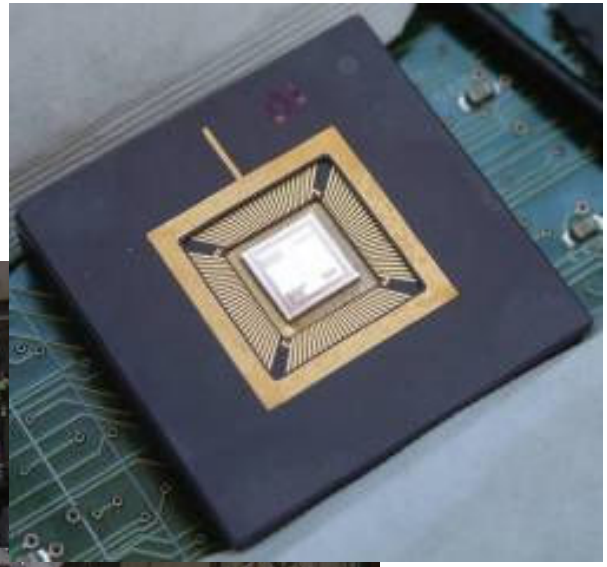
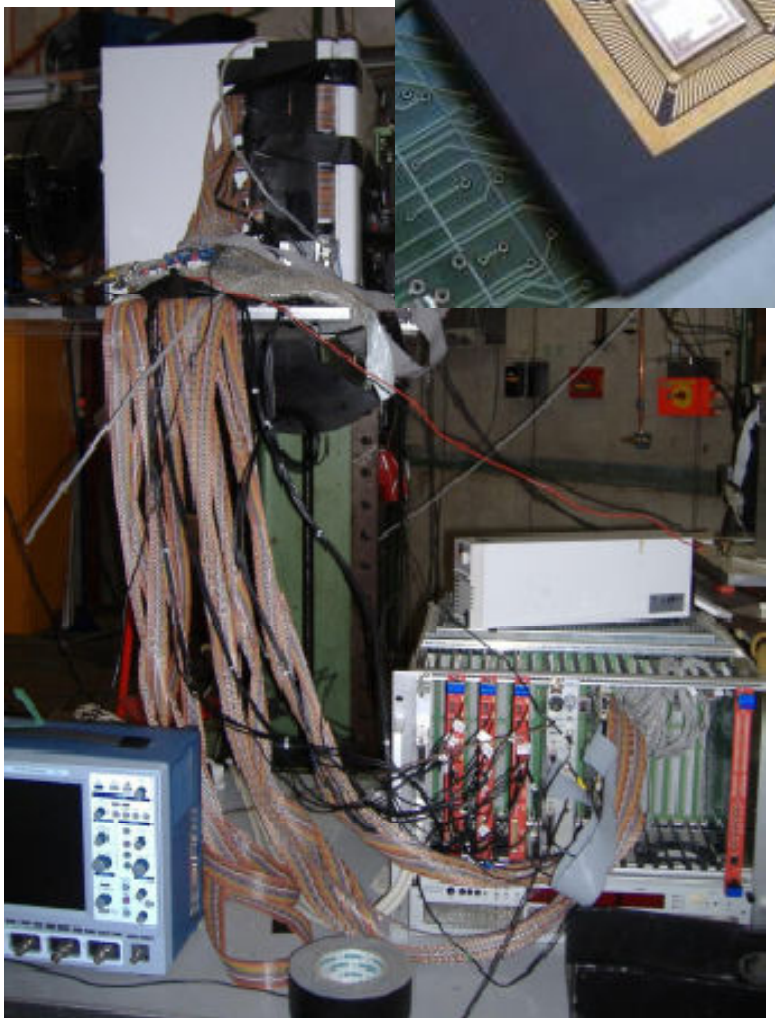
ISIS1 Test Beam 2007

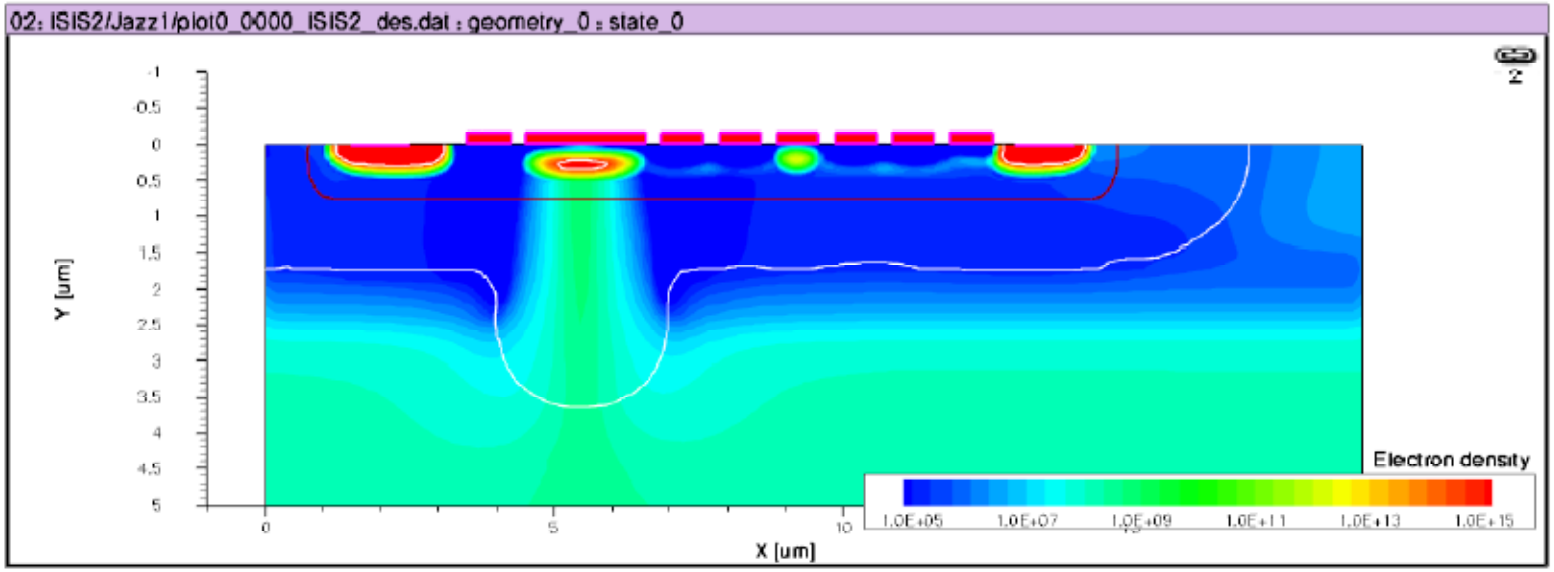
- S/N = 37
- Position resolution in x-direction 10.8 μm
  - 60 μm → some charge sharing
  - Sqrt(60 μm) = 17.3 μm
  - Included large multiple scattering
- Little charge sharing in y-direction (140 μm across pixel)





ISIS2 Charge Collection

- Simulated charge collection 2D TCAD



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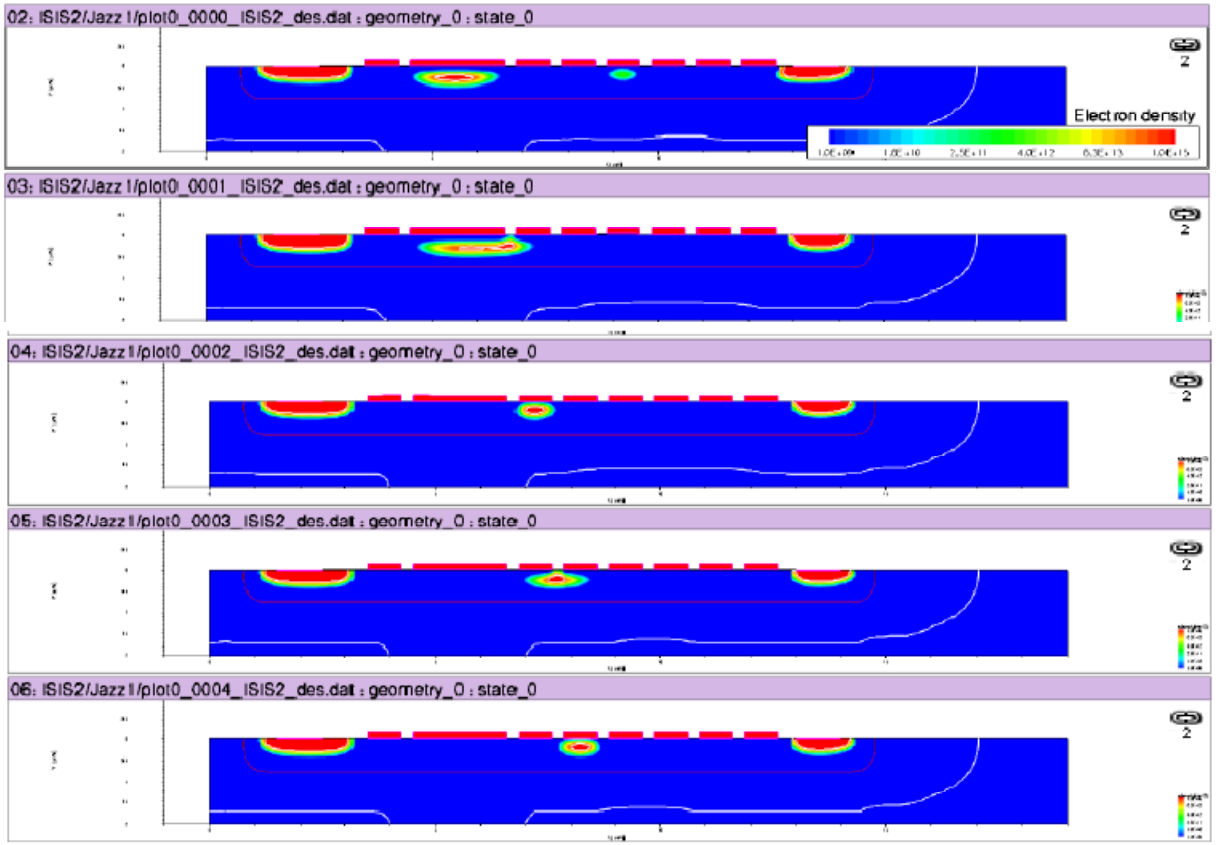
ISIS2 Charge transfer

- Simulated charge transfer to photogate and to storage cells in 2D TCAD – all function with high efficiency



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ISIS2 PhotoGate

- Cross section under photogate