# ILD Meeting at ALCPG09

## Current status, Key Issues, Plan & Timeline for the ILD Silicon tracking system

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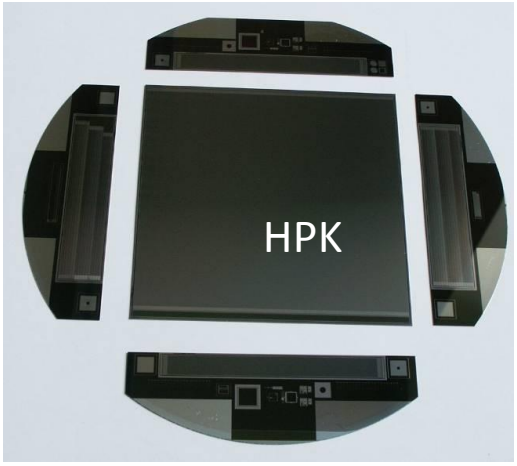
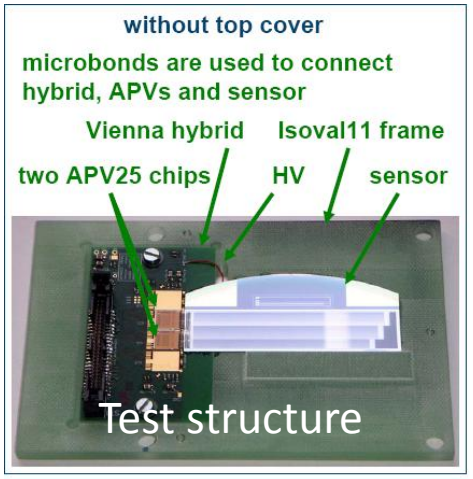
# Items to develop the ILD Si tracking system

- Sensors
- FE Electronics
- FEE & sensor connection, cabling related DAQ
- Mechanics & Detector Integration issues
- Combined test beams and simulation studies
- Plan and Timeline for the 2012 horizon

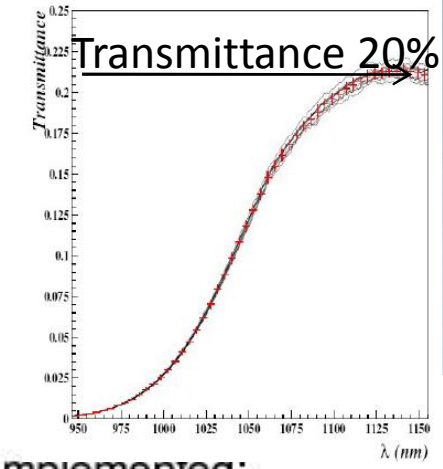
# Silicon Sensors

- **Baseline**: strip sensors, 8'', 200 µm thick, 50 µm pitch, alignment friendly (a.f.) with 70% transmittance & active edge options.
- **Present status**: 6'', 320 m thick, 9.15x9.15 cm$^2$, 50  pitch (HPK) and very preliminary A.F. option (20% measured transmittance)

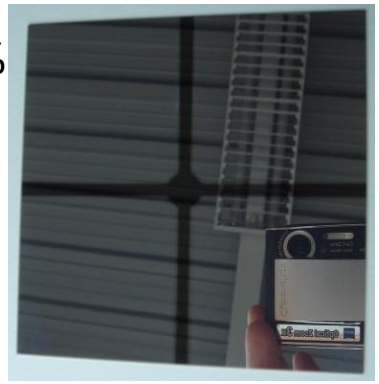



Fully characterized at Lab and test beam with detailed Test Structure studies




Transmittance 20%



Implemented:

- ∅~10 mm window where Al back-metalization has been removed

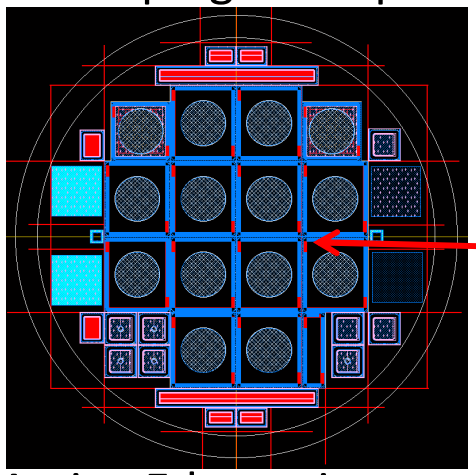
Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)

# Si sensors: how to reach 2012 baseline

***R&D based on developed Lab test infrastructure, expert Labs, Industry, transfer to Industry***

1) Next step on standard strips with HPK: 200 m thick and 8'' *(feasible)*
2) Developing more performing A.F. strips: R&D IMB-CNM and IFCA-CSIC

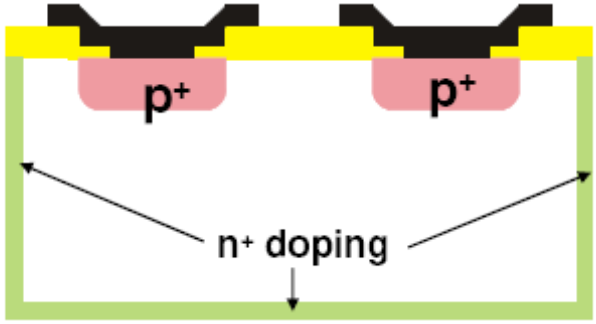


Very detailed simulation studies
Design and production of baby-sensor prototypes with optimised transmittance: 70%
First batch produced by CNM, under test by IFCA:
Promising first results
Once technology is fully proven, transfer to Industry

***Looks in good shape and feasible by 2012***

3) Active Edge strip sensors: two research lines under investigation

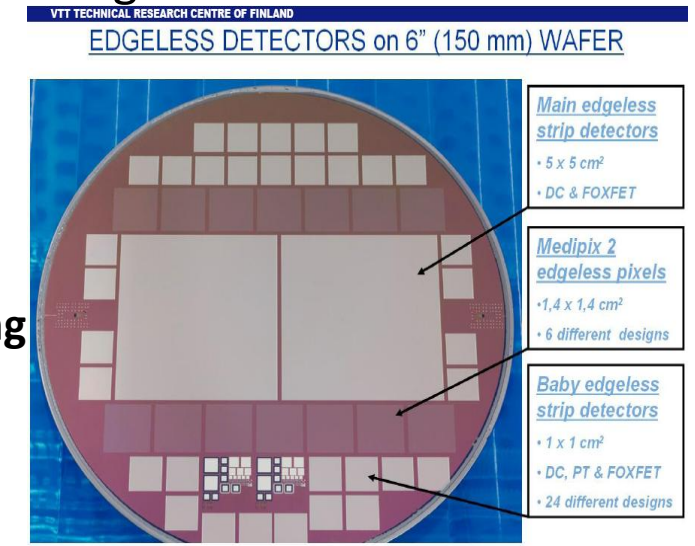
*i) Edgeless Planar strips (IRST)*




2.5x5 cm2 proto sensors by end 2009

*ii) Edgeless SOI strips (VTT)*

Full electrical tests
5x5cm$^2$ sensors
**Look very promising**



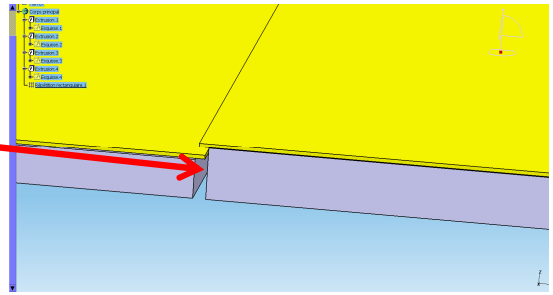

*Once R&D is achieved and techno proven: transfer to Industry*

# Edgeless strips sensors: Why?

Edgeless sensors decrease the non active edge regions of sensors (usually of a few hundreds of microns) down to about 10 to 20 µm.

Our interest in edgeless or active edge sensors is motivated by:

- ✓ allow building large area Silicon trackers seamlessly tiled detector matrices,
- ✓ thus no need for sensor overlap
- ✓ easier to build
- ✓ decrease of the material budget
- ✓ improvement of the tracking performances both in momentum and spatial resolution.



*Two solutions based on the edgeless strip based on Edgeless planar and Edgeless SOI technologies are pursued.*

# FE & R.O Electronics

- **Baseline**: *mix-mode analogue & digital SiTR design, in 90 nm DSM technology, blocks of 256 channels, direct connection with strip sensors, connection to DAQ (cabling, signal transmission)*

- **Current status:** in preparation, SiTR_128, 130nm UMC, to equip a large number of test beam prototypes.
  - Preliminary versions with various levels of design integration produced and tested:
  - SiTR_180 (VFE), SiTR_130-4 (all analogue+A/D), SiTR_130-88 (full mix-mode design)
  - SiTR_130-128: *produced by early 2010, available end 2010 for equipping Si tracker prototypes for test beams.*

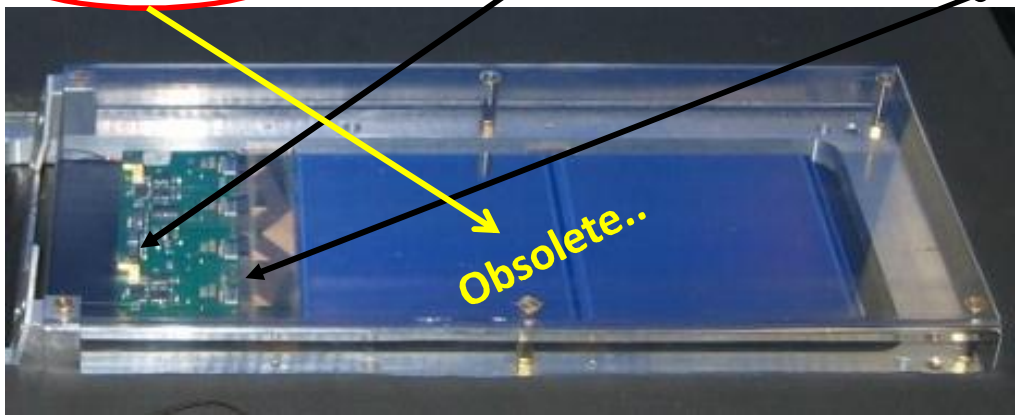
# FE/RO Electronics: how to reach 2012 baseline

**ROADMAP ON ELECTRONICS**

- Go to 256 channels, block of 8x256ch in one
- Thinning (50 µm)
- Go to 90nm CMOS techno
- Direct connection of the FE chip on strip sensor (wire bonding -> bump bonding -> 3D interconnect)
- Adapting FE to CLIC cycle (complete revisit of FE)
- Bunch tagging at CLIC
- Develop the TOT (B. Schumm's presentation)
- Develop Data processing and data handling (DAQ)

# Direct connection sensors-FEE

**Major R&D objective: NO MORE Hybrid FEE board +pitch adapter**




**ALL in ONE SOLUTION => direct connection of FE chip onto the sensor**

- material budget,
- simplification of elementary module (tile) and
- of overall detector construction (burden put on sensor and FEE chip),
- improvement in performances
- Use high tech advances (cost?)

SiLC is pursuing with the different steps: wiring onto the sensors: HEPHY + Polish firm (proto at CERN t.b); bump bonding: HPK+LPNHE (proto sensor+FE chip in 2010); going in // to 3D vertical interconnect. (part of the worldwide 3D interconnect effort)

# Mechanics and Detector Integration

**Baseline:** Modules based on planar strip sensors (no ...) and with FEE chip on sensors are the elementary tile of the detector. Light support structures and proper alignment systems and cooling included in the overall Si detector schema.

**Present status**: The work done
- for the construction of the various prototypes (test beams) and
- for the ILD-LOI on the preliminary design of each component (still GEANT 4 based)
- and study of the main integration issues, including also alignment etc..)

# Mechanics & Integration: how to reach the 2012 baseline

**The to-do-list:**

- **Elementary module: depends on work packages 1,2,3**
- **Alignment systems**: laser based (A.F.) with IR strips for each components, alignment systems for components between them and with the other components.
- **Cooling**: to be studied with the impact of the other sub detectors
- **CAD design of each components**, including more and more or the details.
- **Support structure studies**: constraint studies, tests with mechanical prototype
- **Construction lines**: design and development of tools for construction lines appropriate to the detector to be built, even in Labs already equipped for LHC, construction set-up have to be adapted.
- **Integration in the overall ILD detector**
- **Push pull** issues to be studied and solved (tests?) but first better defined!

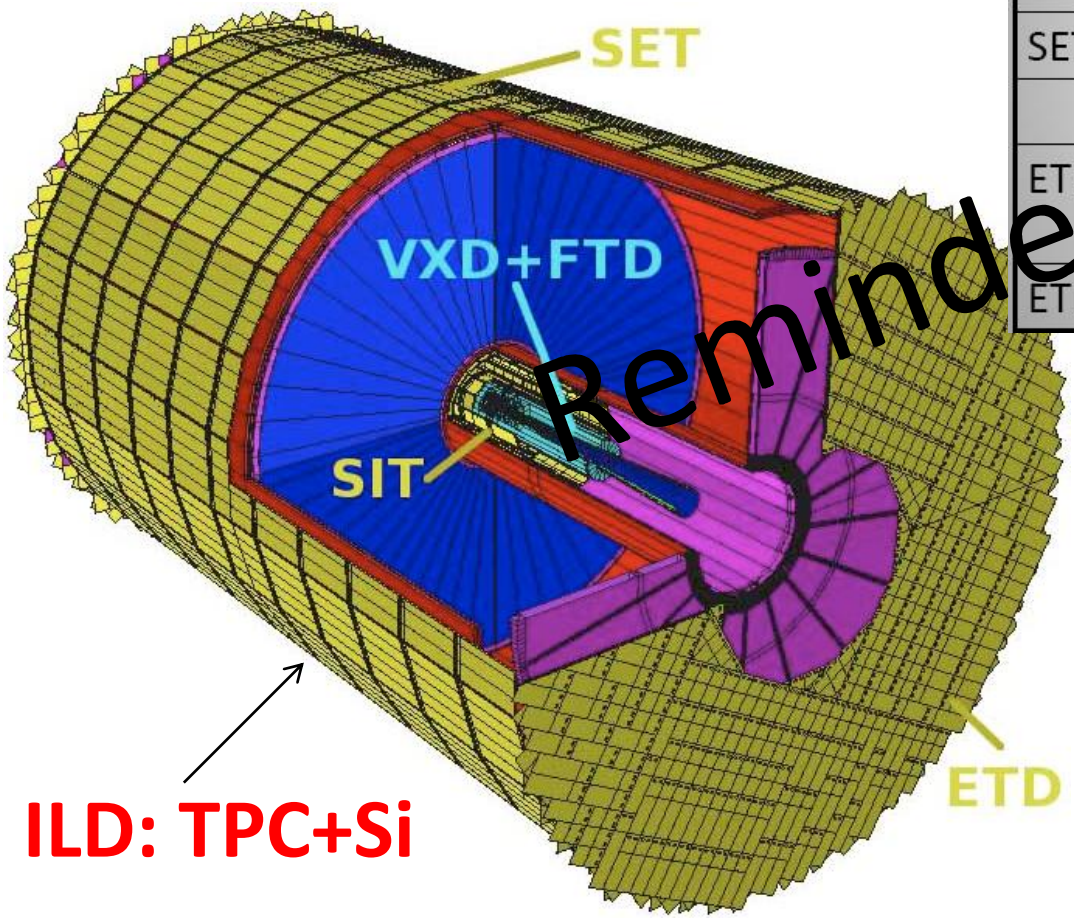
(In red the most critical issues)

*This means CAD studies, detector prototyping for test beams, mechanical prototypes for dedicated studies, definition of the tools and setting up of the construction lines. Completed in parallel with detailed simulation studies and test beams.*

# ILD Hybrid tracking: *The Silicon Envelope*

(in numbers as currently in the ILD LOI)

| Component | Layer # | # modules | # sensors/ module | # channels | Total surface m2 |
|---|---|---|---|---|---|
| SIT1 | 1st layer | 33 | 3 | 66.000 | 0.9 |
| | 2nd layer | 99 | 1 | 198.000 | 0.9 |
| SIT2 | 1st layer | 90 | 3 | 180.000 | 2.7 |
| | 2nd layer | 270 | 1 | 540.000 | 2.7 |
| SET | 1st layer | 1260 | 5 | 2.520.000 | 55.2 |
| | 2nd layer | 1260 | 5 | 2.520.000 | 55.2 |
| ETD_F | X or U or V | 82/quad =328/layer =984/ETD | 2 or 3 or possibly 4 | 2.000.000 | 30 |
| ETD_B | idem | idem | idem | idem | 30 |




**ILD: TPC+Si**

**Total number of channels:**

$10^6$ (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)

= **10 $x10^6$ channels**

**Total area:**

7 (SIT)+110 (SET) +2x30(ETDs) = **180 $m^2$**

**Total number of modules:**

500 (SIT) + 2500 (SET) + 2000 (ETDs)=

**5000 modules with same sensor unit.**

**Unique sensor type (except FTD) but variable length strips wrt module location**

GEANT4 simulation **(here)& mechanical design** (CATIA) in progress

# Plan & timeline (still tentative)

Legend: 90nm*=change in technology; New version**= 90nm+8x256 block+thinning

| Workpackage | item | 2010 | 2011 | 2012 |
|---|---|---|---|---|
| 1) **sensors** | Strips 200µm/8'' | Collab with | Industry Test | 1st series |
| | A.F. strips | R&D → | Full proof Ind | ustry transfer |
| | Active edge strip | R&D | R&D | Industry transfer |
| **2) Direct** | Wire bonding | Prototyping & | R&D with firm | industrialisation |
| **connection** | Bump bonding | Prototyping | & R&D with | Industry (HPK) |
| **Chip-strips** | 3DVert connect | R&D | R&D | R&D |
| | alternative | R&D | R&D | prototyping |
| **3) FEE chip** | 130nm-128ch | Foundry/test/ | New prod for | Test beam protos |
| **R.O.->DAQ** | 90nm*, 256ch | design | Layout test | Equip protos F.P. |
| | New version** | | | New version |
| | Connect/Cabling | R&D | R&D & tests | R&D & tests |
| | Path to DAQ | R&D | R&D & tests | |

# Si tracking-ILD: Plan & timeline (cont'd)

| Workpackage | item | 2010 | 2011 | 2012 |
|---|---|---|---|---|
| **4)Detector** | Elem. Module | → | → | → |
| **Construction** | cooling | → | → | → |
| **&integration** | Alignment syst. | → | → | → |
| | Support struct. | → | → | → |
| | CAD detector studies | → | → | → |
| | Integration study | → | → | → |
| **5) Test beams** | Will accompany | & complete the | R&D studies & | developments |
| **& simulation** | Will accompany | & complete the | R&D studies & | developments |
| **studies** | | | | |
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