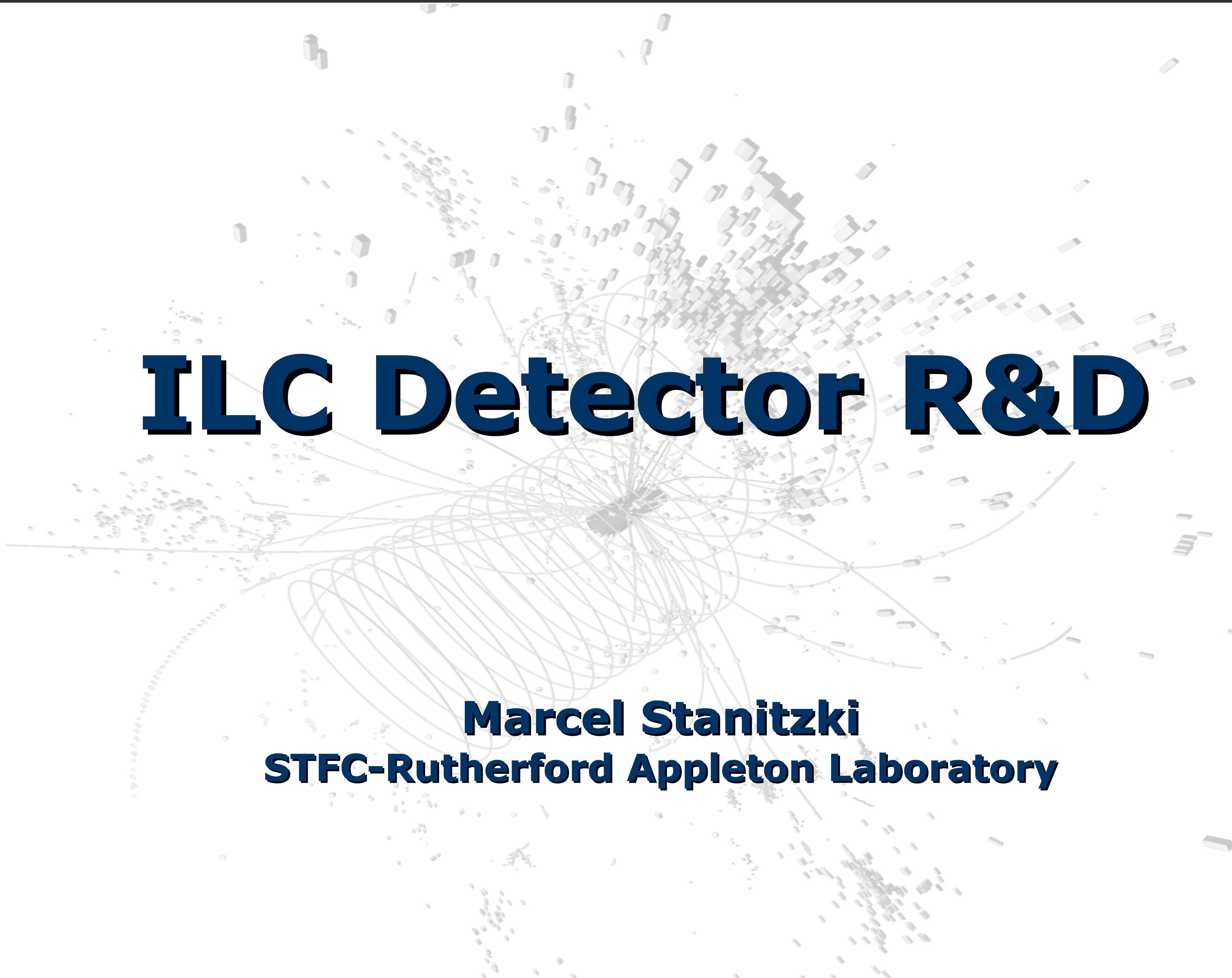
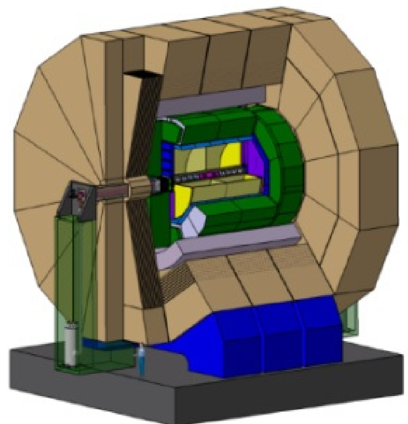


ILC Detector R&D

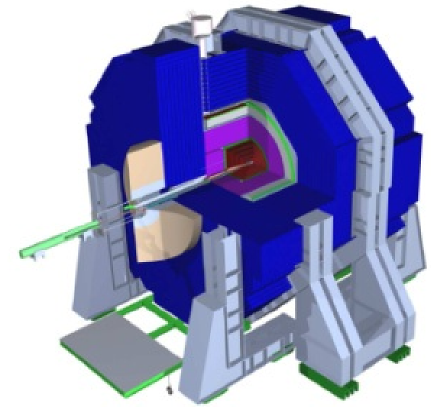
Marcel Stanitzki
STFC-Rutherford Appleton Laboratory

Entering the Post-LoI phase

- IDAG has validated two concepts:



ILD



SiD

- Both were invited to prepare a detailed baseline design for 2012
- ILD & SiD build on
  - particle flow paradigm
  - push-pull-able
- ILD & SiD have complementary approaches

Complementary approaches

- Tracking approach
  - ILD: TPC full track following due to large number of hits
  - SiD: Silicon provides robustness due to short time sensitivity and bunch time-stamping
- Radius and Field
  - ILD: Large radius optimizes PFA performance
  - SiD: Large field, small radius optimizes vertex detector performance

Detector Requirements

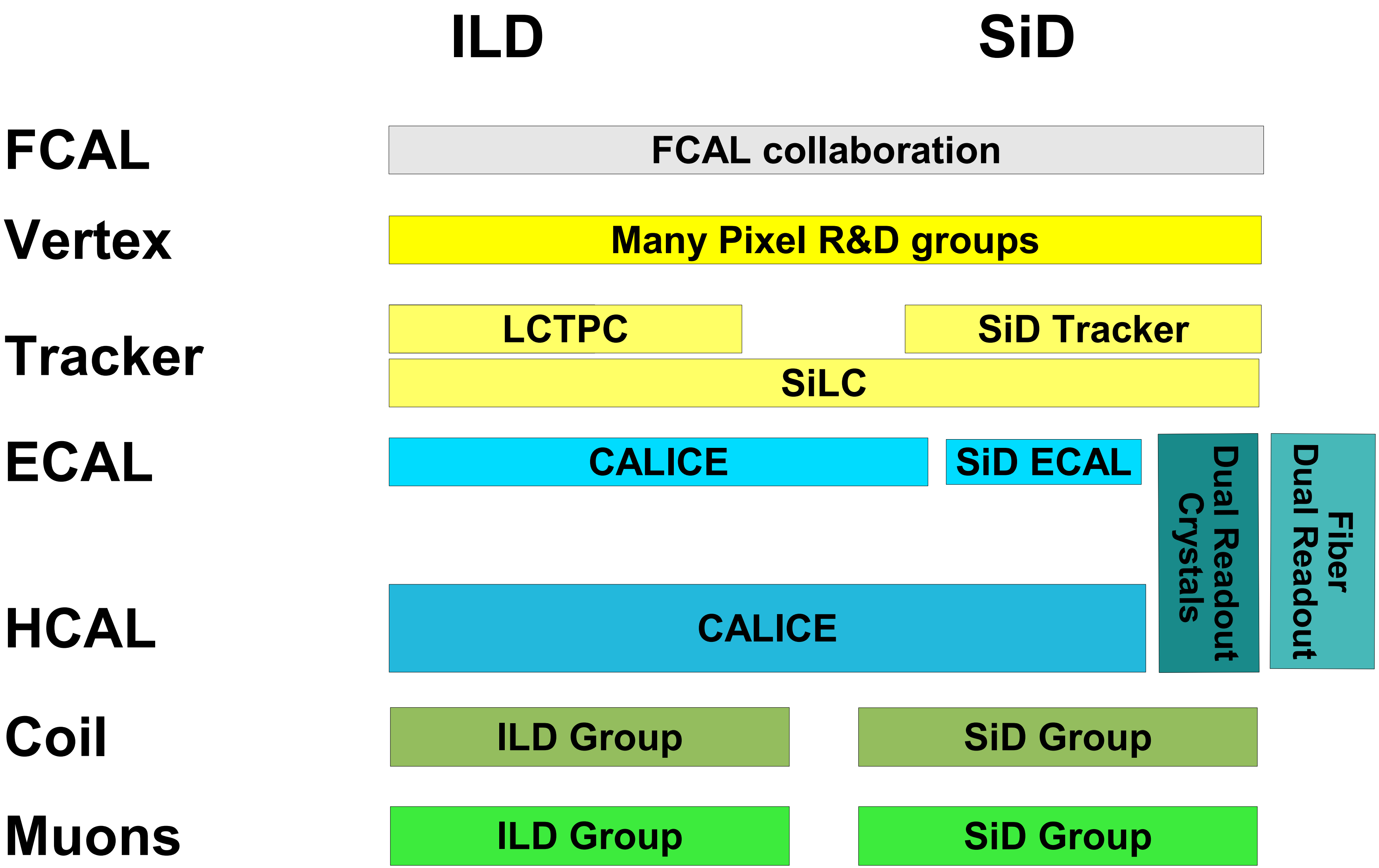
- Have remained unchanged ...
- Exceptional precision and time stamping
  - Bunch train is ~3000 bunches over 1 ms (ILC)
- Vertex detector
  - < 4 μm precision w/ ~20 μm pixels
- Tracker
  - $\sigma(1/p) \sim$ few $\times\ 10^{-5}$
- Calorimeter
  - $$\frac{\sigma_{E_{Jet}}}{E_{Jet}} = 3-4\%,\ E_{Jet} > 100\ \ GeV$$

The validated detectors

Detector	ILD	SiD
Design Paradigm	PFA +TPC	PFA + Si-Tracker
FCAL	SiW	SiW
Vertex	5/6-layer silicon pixel	5-layer silicon pixel
Tracking	MPGD-TPC + Silicon strips	Silicon strips
ECAL	SiW	SiW
HCAL	Analog Fe+Scint	Digital Fe+RPC
Solenoid	3.5 T	5 T

These are the baseline choices as defined in the LoIs

R&D groups



ILD
SiD
FCAL
Vertex
Tracker
ECAL
HCAL
Coil
Muons
FCAL collaboration
Many Pixel R&D groups
LCTPC
SiD Tracker
SiLC
CALICE
SiD ECAL
Dual Readout Crystals
Fiber Dual Readout
CALICE
ILD Group
SiD Group
ILD Group
SiD Group

Critical Areas of R&D defined

Area	ILD	SiD
Vertex Pixel R&D	x	x
Silicon Strips	x	x
TPC	x	
ECAL	x	x
HCAL	x	x
Dual Readout Crystals		x
Muon	x	x
FCAL	x	x

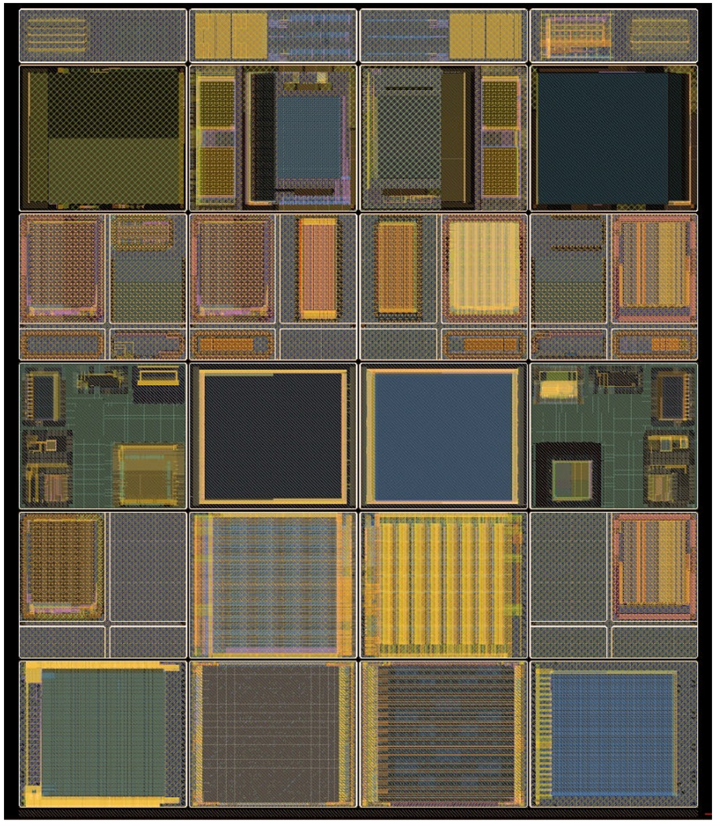
A lot of common interest !

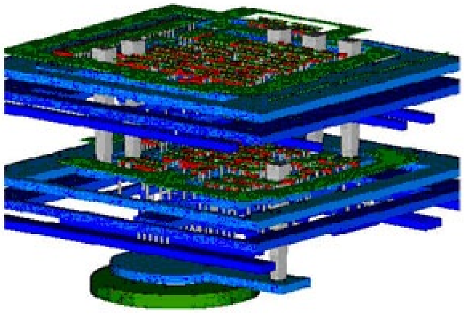
Pixel R&D

- Continues to be very active
- Work on existing concepts
  - MAPS, CCD, ISIS, DEPFET, SoI …
- Some new ideas
  - 4T-MAPS, 3D Integration
- Can only cover a few items ...

3D Silicon Pixel HEP run

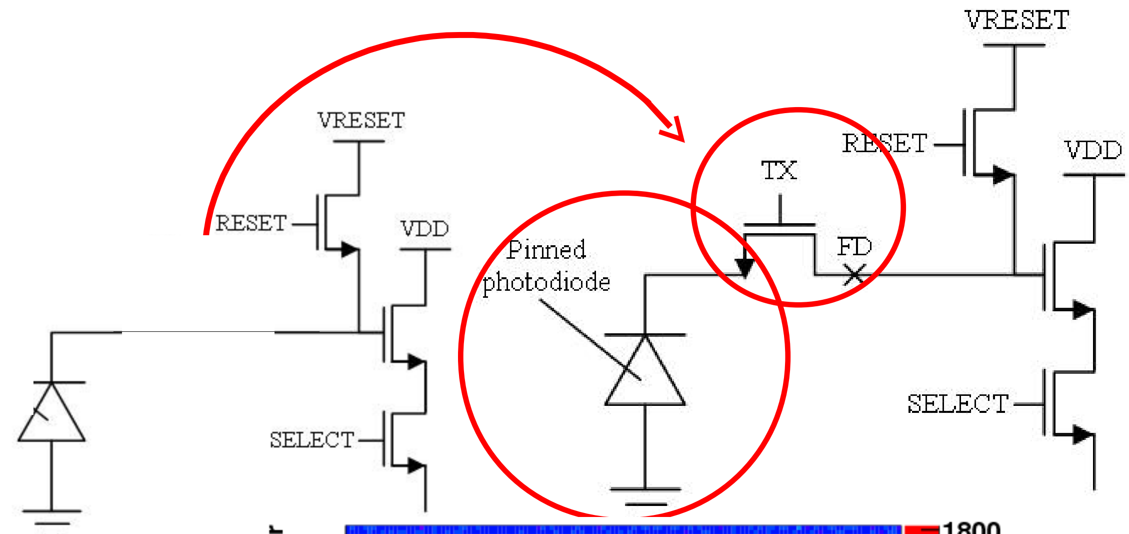
- 130 nm process
  - Chartered Semiconductor
- 3D processing by Tezzaron
  - wafer processing & interconnects
- MPW organized by Fermilab
- 3D Consortium
  - 15 institutes
  - 5 countries
- Silicon Pixels for ILC, SLHC, B factories and more

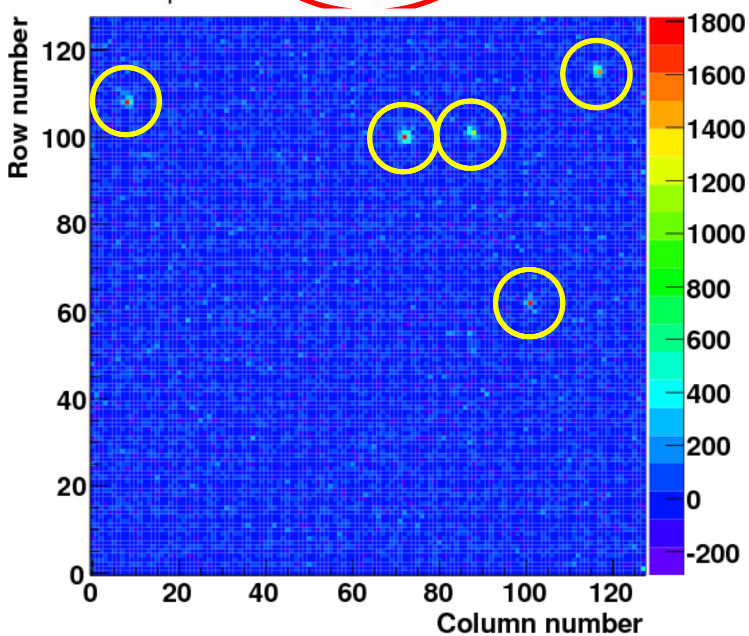




4T Pixels

- **3T MAPS**
  - Simple architecture
  - Readout and charge collection area are the same
- **4T MAPS**
  - Three additional elements
  - Readout and charge collection area are at different points
  - First Chip tested in beam (13 different pixels with 15-45 μm)

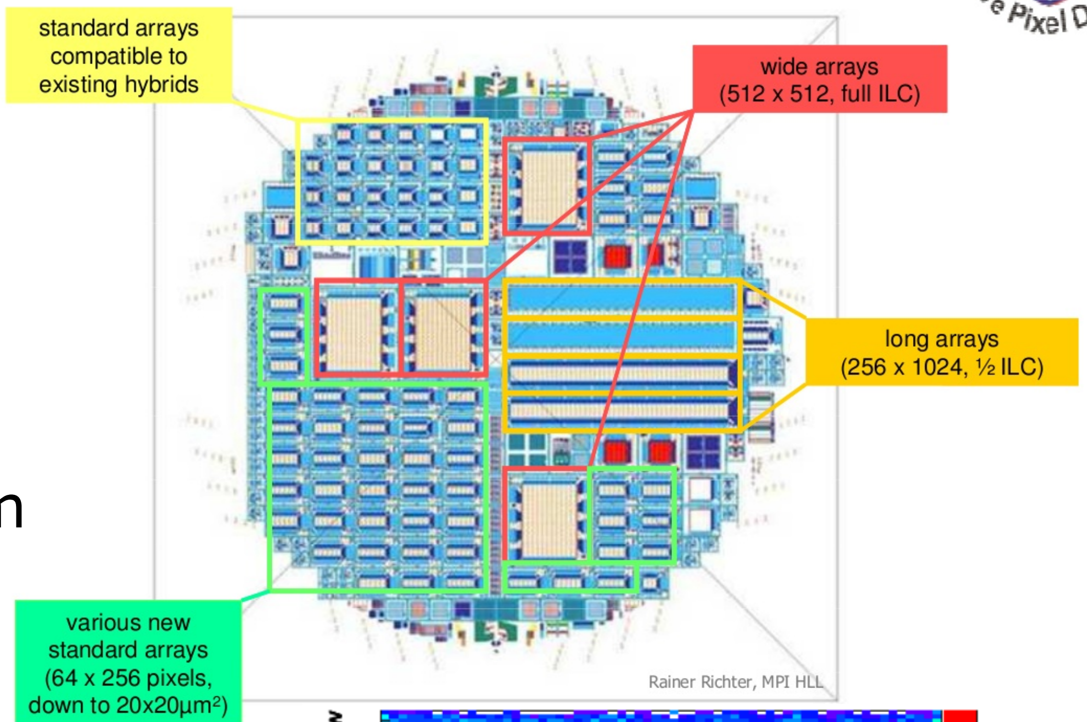


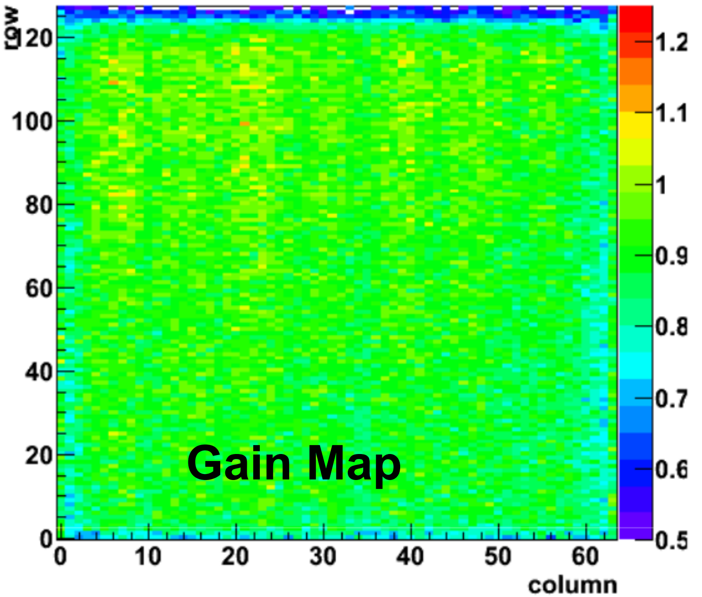


CERN Testbeam August/September 2009

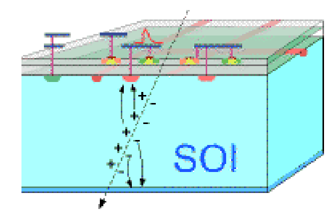
DEPFET

- New generation PXD5
- Longer pixel arrays
  - 256x64 pixels
- New DEPFET variants:
  - Very small pixels (20μm x 20μm)
  - Capacitively Coupled Clear Gate (C3G) → New step forward in gain
  - Shorter Gate lengths → Increased internal amplification → Factor 2 better expected)

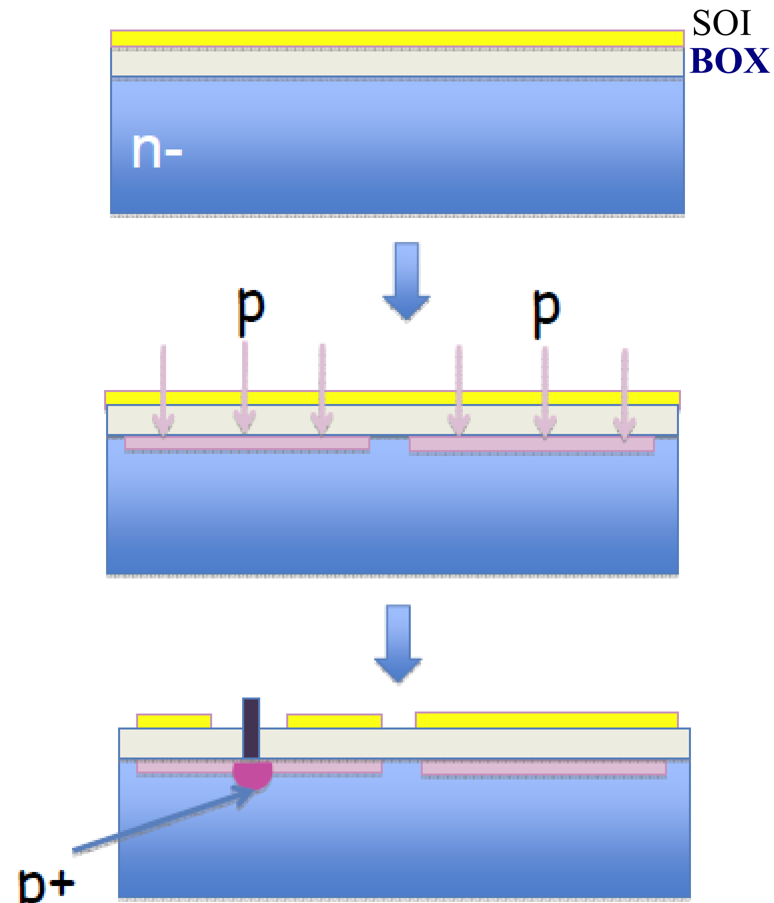




SoI Pixel R&D



- SoI Pixel R&D
  - 200 nm process by OKI
  - KEK sponsored MPW
- Main problem
  - Back-gate effect
- Solution
  - Buried p-Well implant
- Add. Benefits
  - Reduce electric field around p+ sensor
  - improve radiation hardness
- Major step for SoI technology

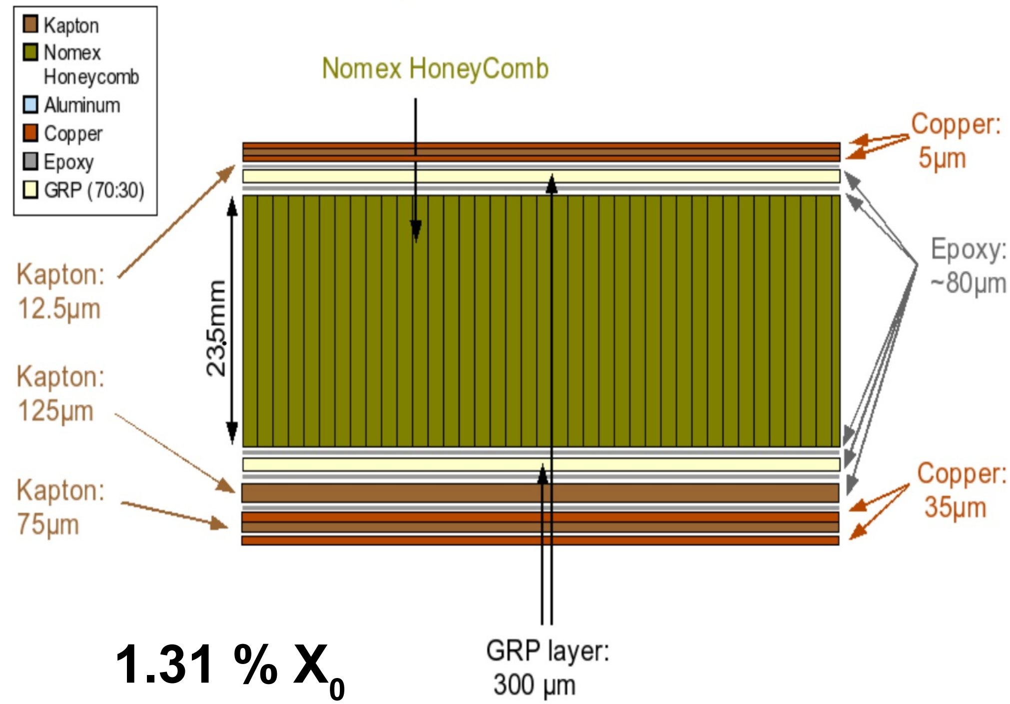


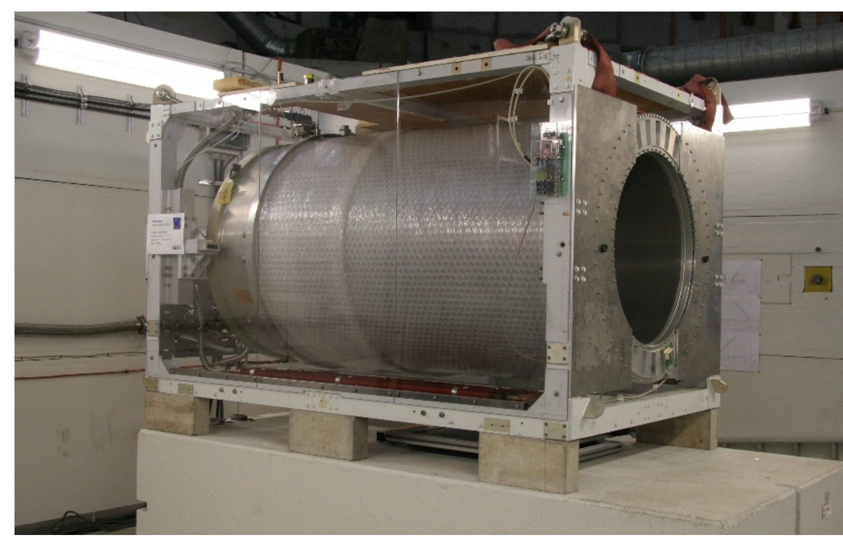
Successfully tested up to 100V bias voltage

For more Details see
http://rd.kek.jp/project/soi/

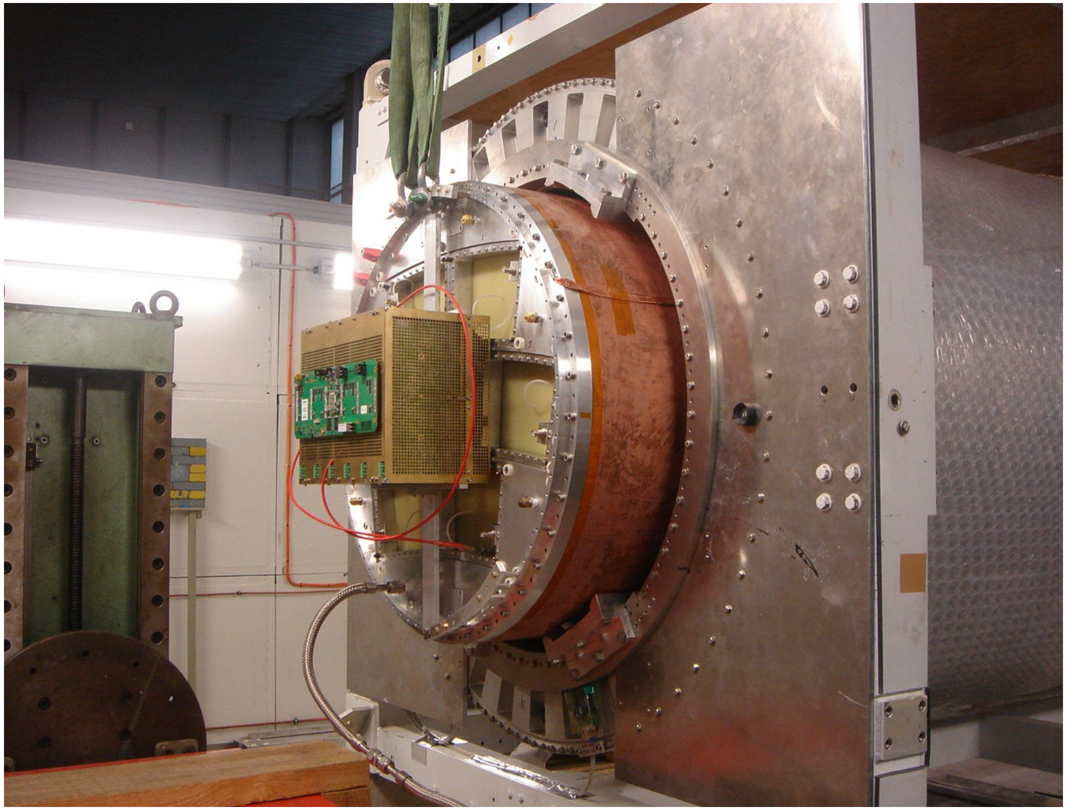
LCTPC

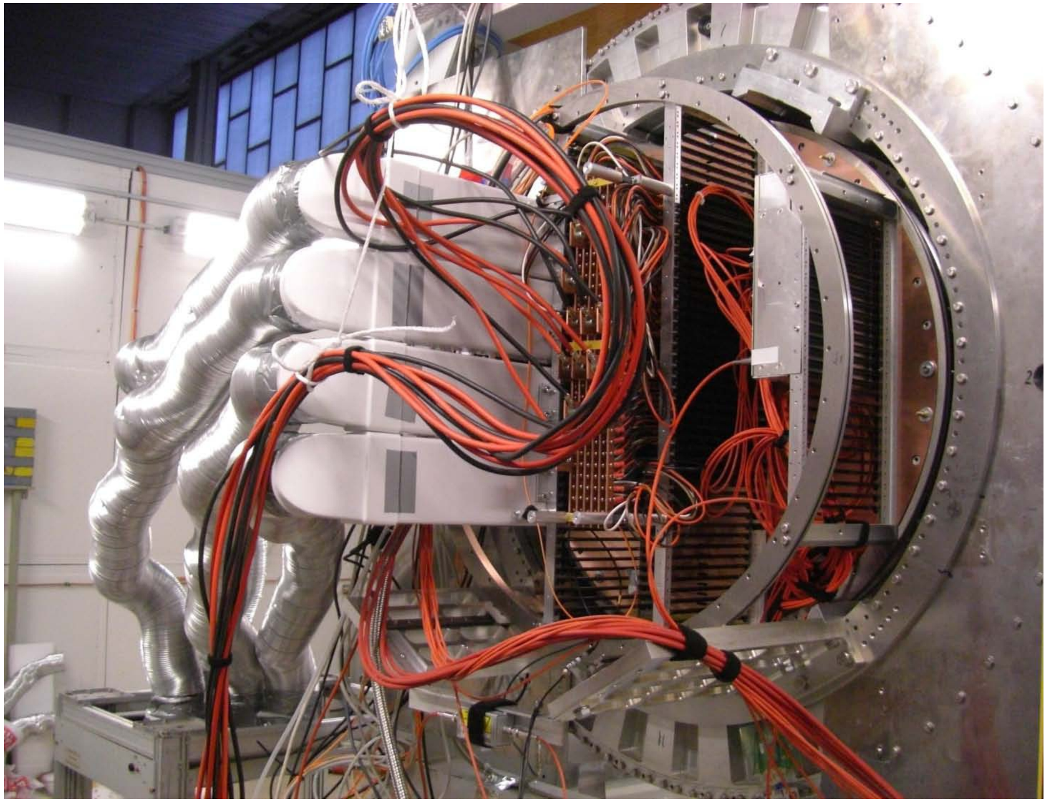
- Large Prototype
- Field Cage
  - Diameter: Inner 720 mm,
  - Outer 770 mm
  - Wall thickness 25 mm
  - Length 610 mm
  - HV up to 20 kV
- Testbeam at DESY
  - Electrons 1-6 GeV
  - using PCMAG (1 T magnet)





LCTPC at DESY

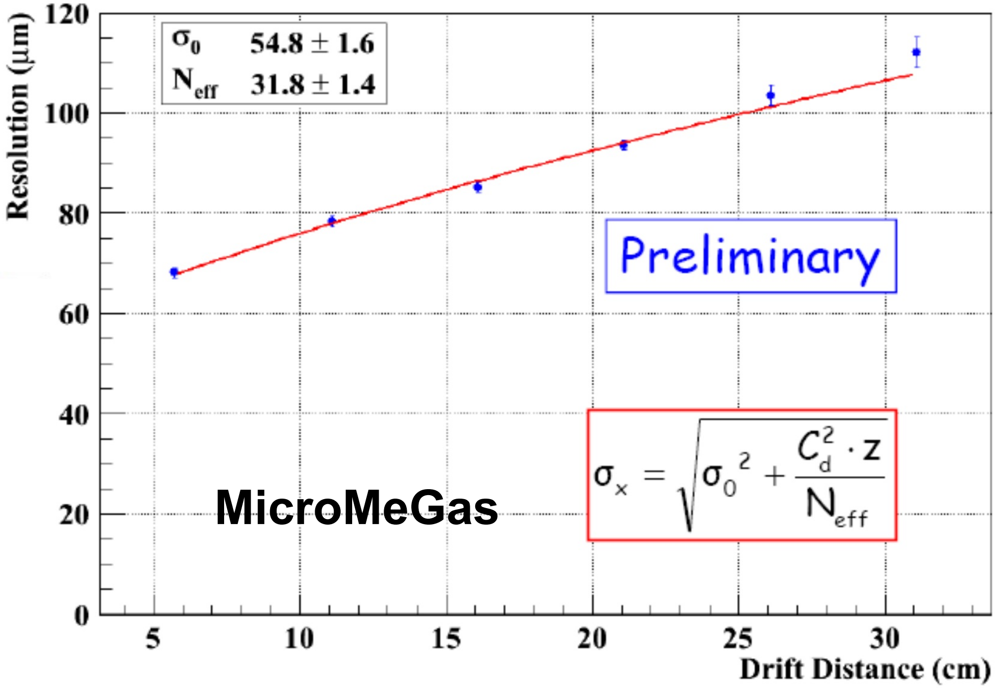


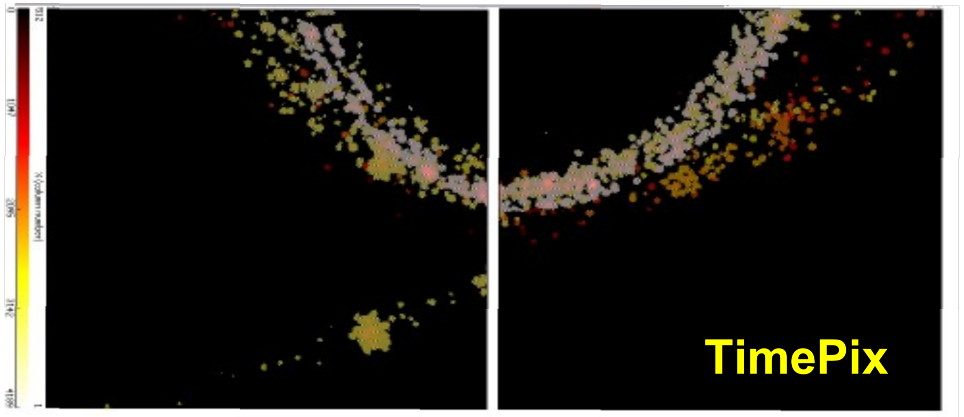


LCTPC inside the PCMAG at DESY

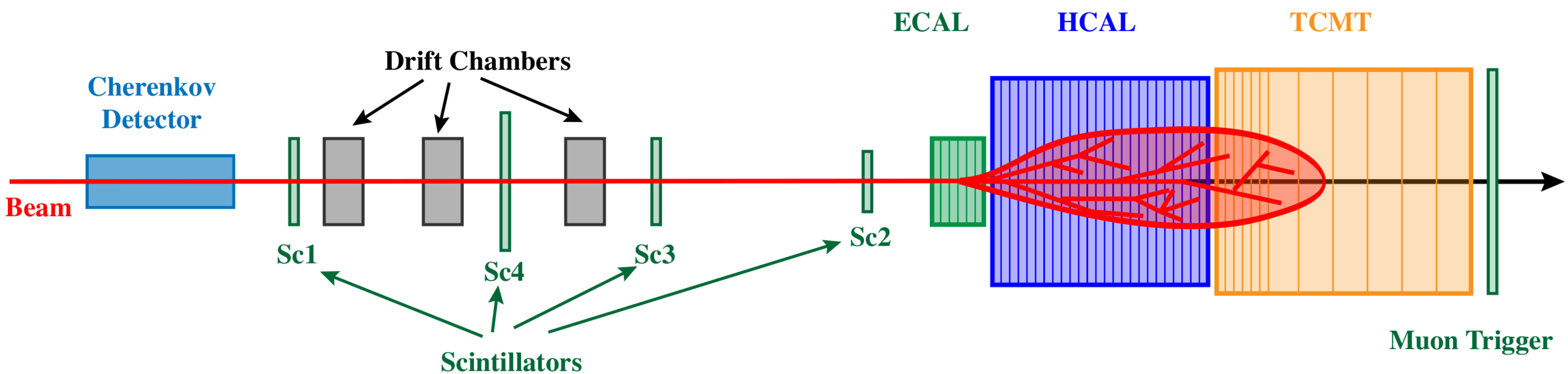
LCTPC readout

- Testing several technologies
- MicroMegas
- Double and Triple GEMS
  - pad readout with ~3000 channels
  - Testing Silicon Pixel readout (TimePix)
- Future Plans
  - Move to a high energy beam in 2011
  - Start designing a TPC for the ILC

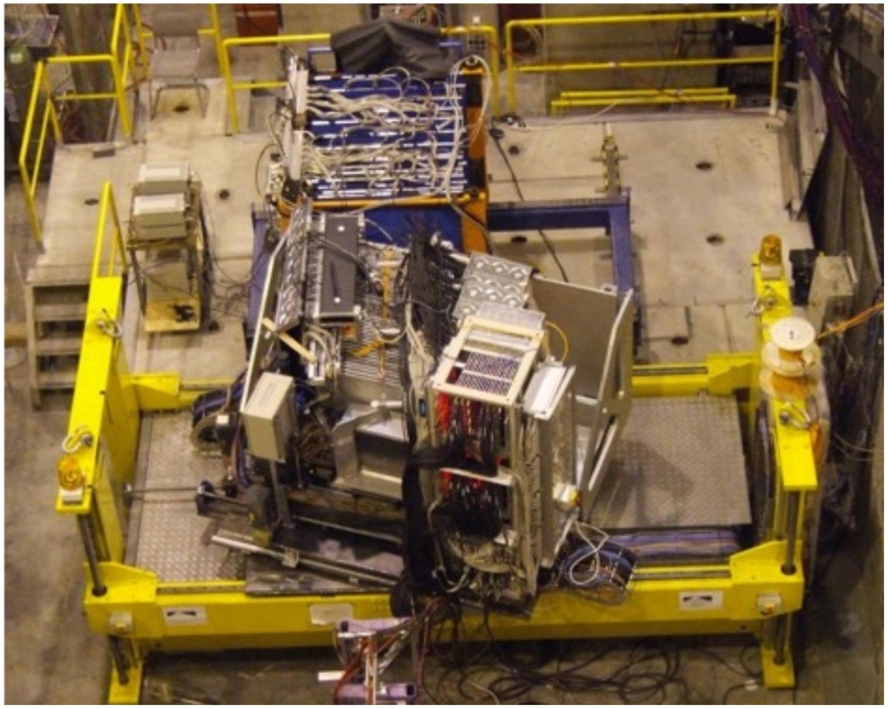




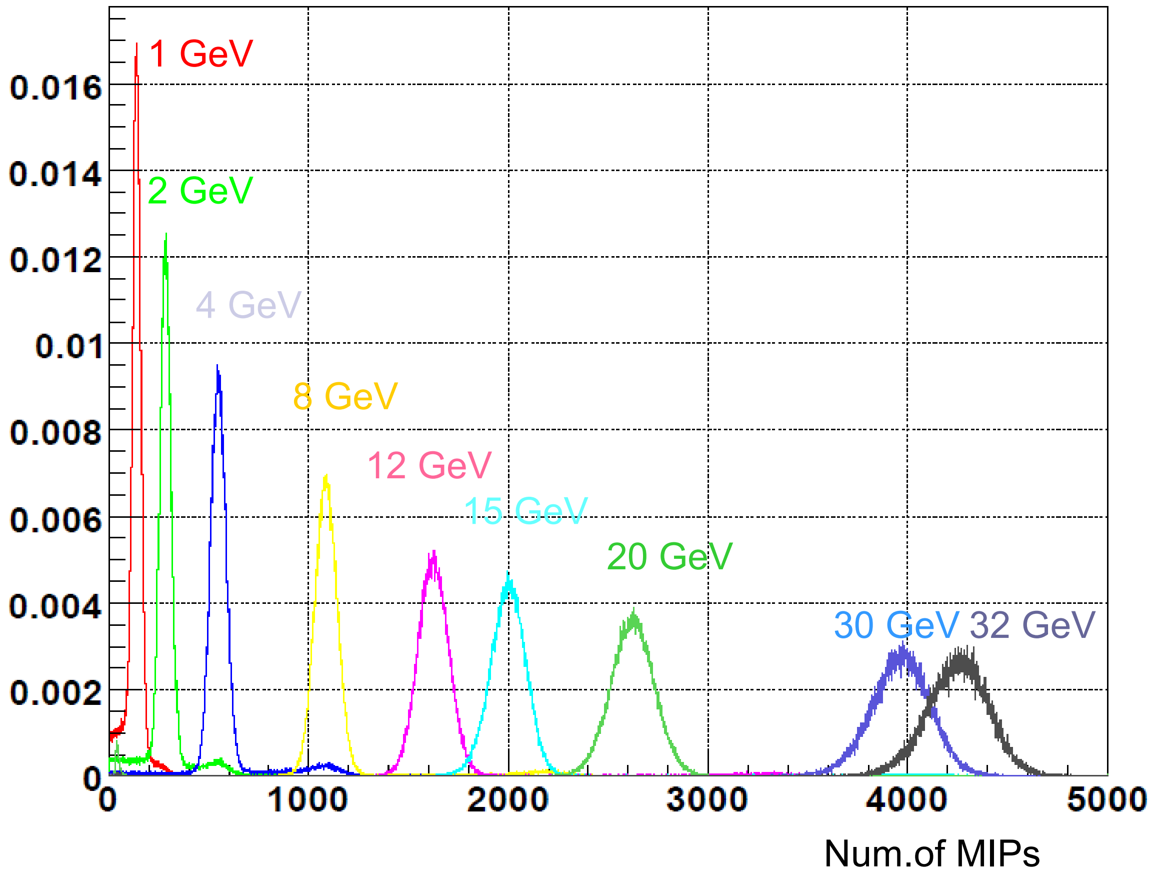
CALICE Beam Test Setup

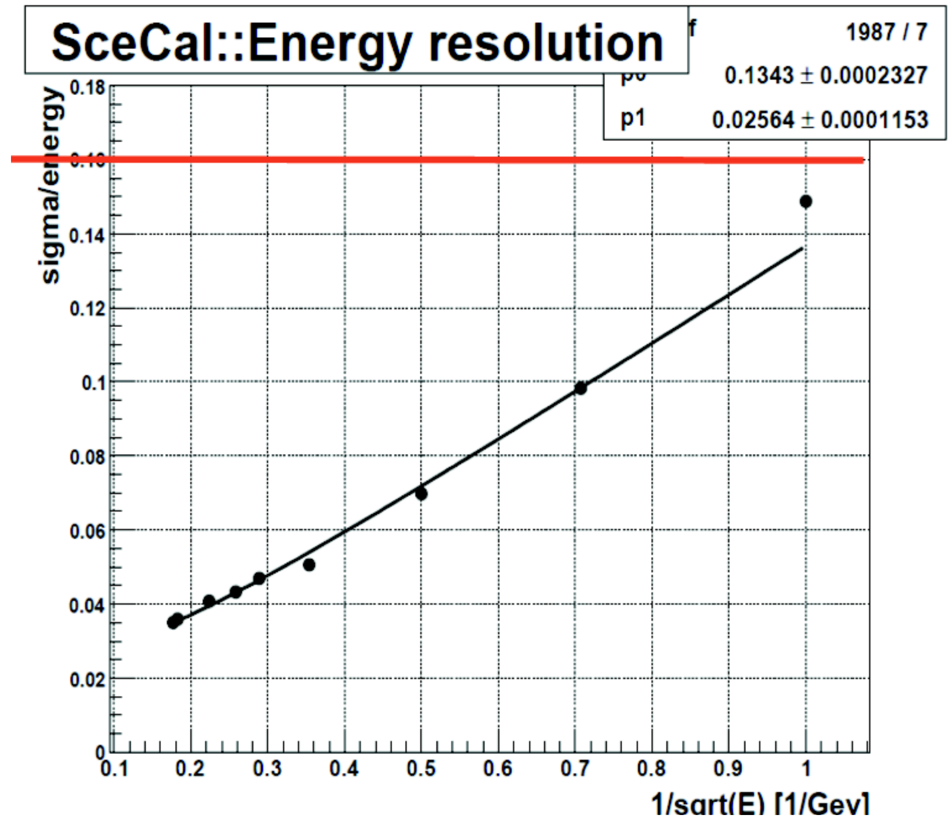


- Extensive test beam campaign
  - DESY: 2006
  - CERN: 2006, 2007
  - FNAL: 2008, ...
- Various beams and energies
  - 2 GeV to 80 GeV
  - μ, $e^{\pm}$, $\pi^{\pm}$, hadrons



CALICE Scint-ECAL

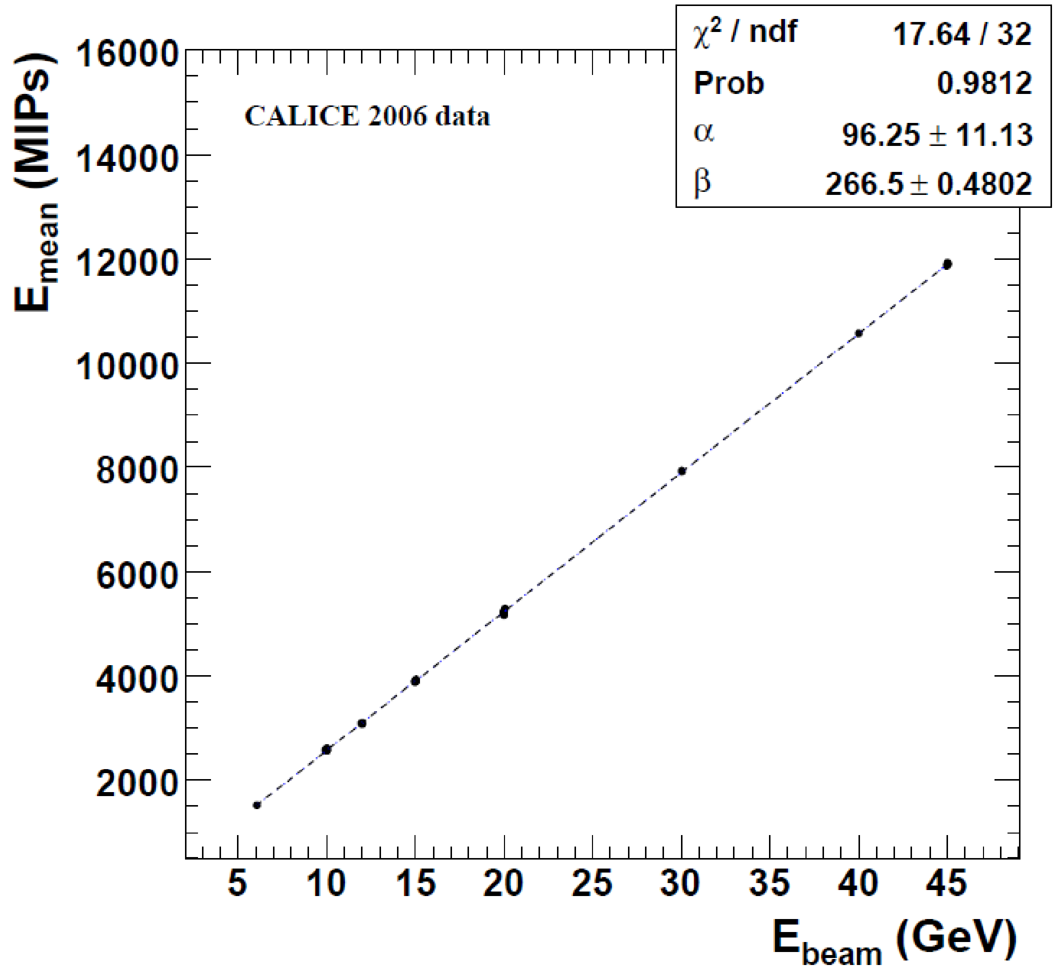


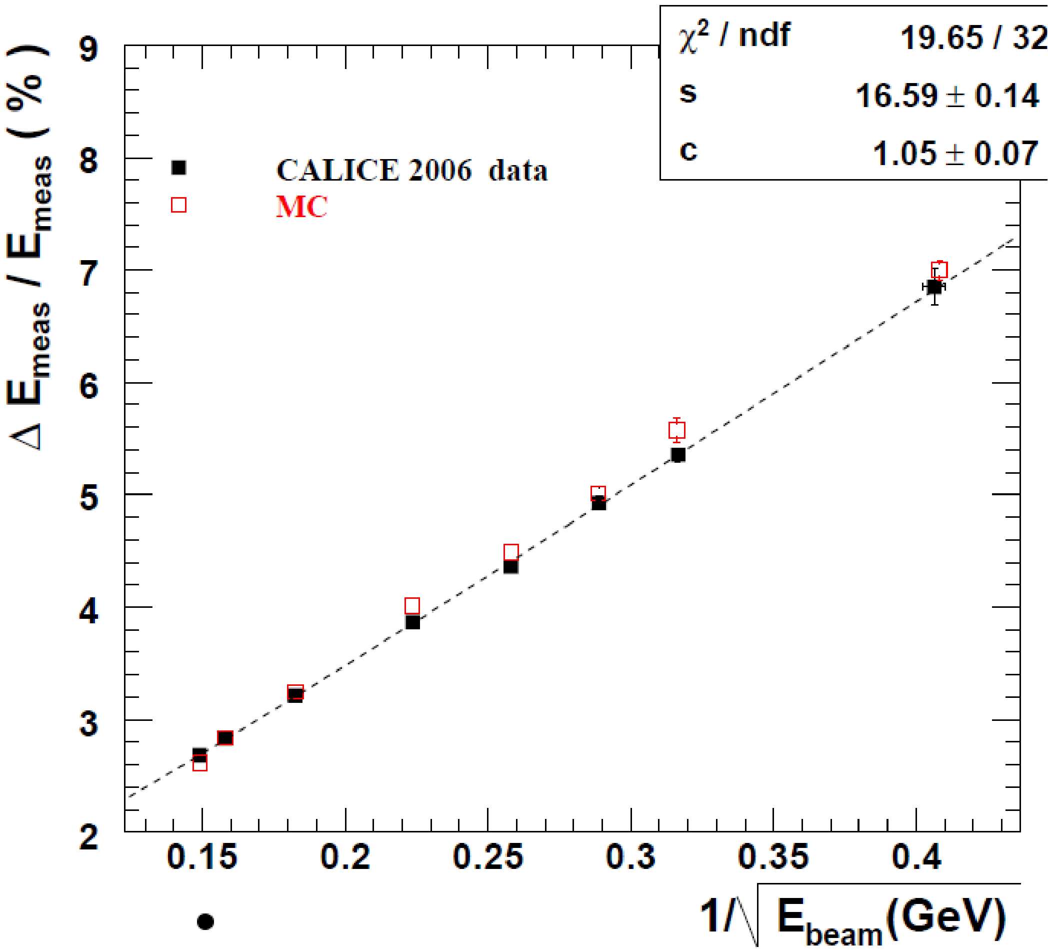


Beam test with W+Scintillator ECAL at Fermilab

$$\frac{\sigma_E}{E} = \frac{13.56\%}{\sqrt{(E)}} \oplus 2.56\%$$

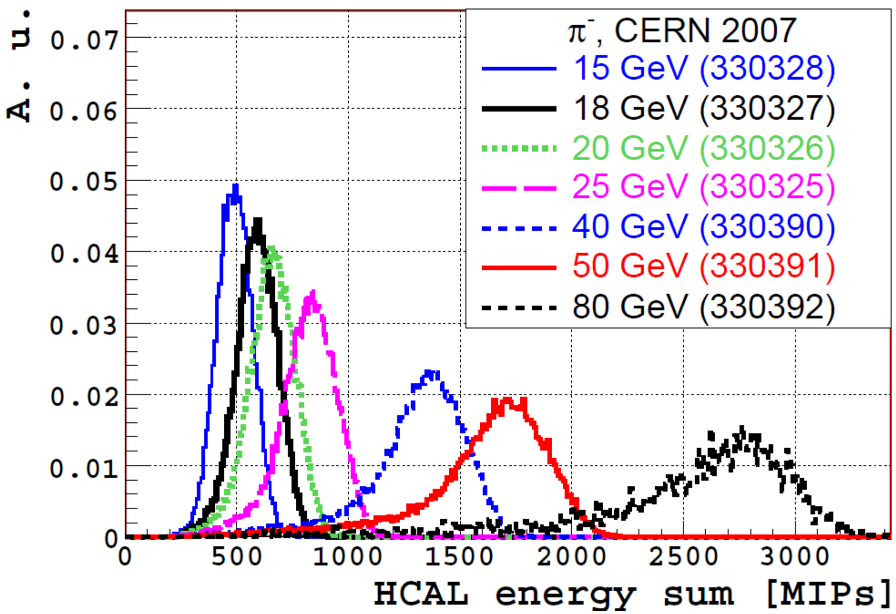
ECAL SiW Results 2006

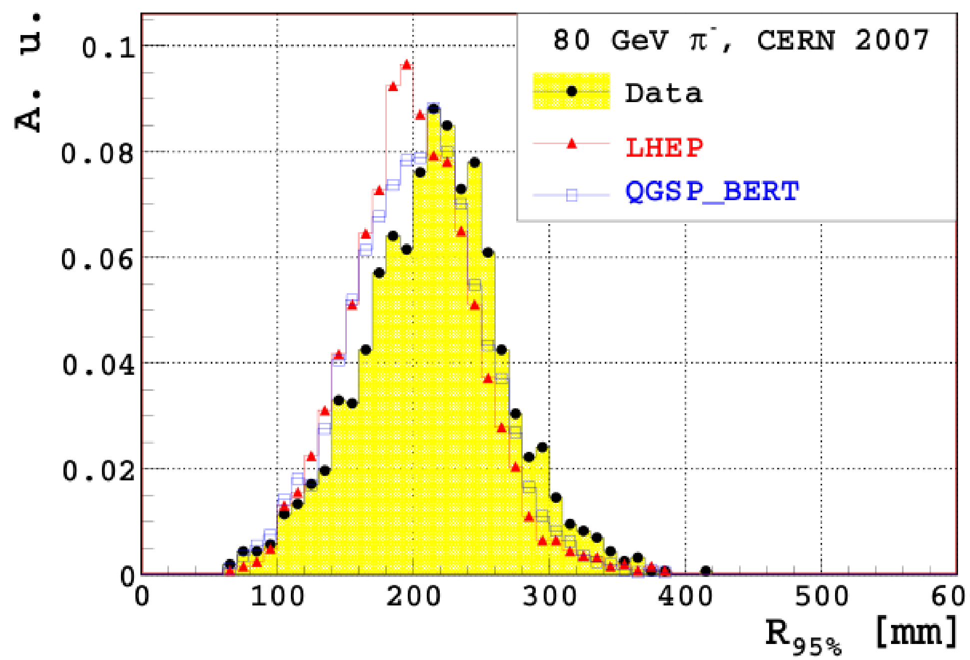




$$\frac{\Delta E_{\mathrm{meas}}}{E_{\mathrm{meas}}} = \left(\frac{16.6 \pm 0.1}{\sqrt{E(\mathrm{GeV})}} \oplus (1.1 \pm 0.1) \right) \%$$

CALICE AHCAL



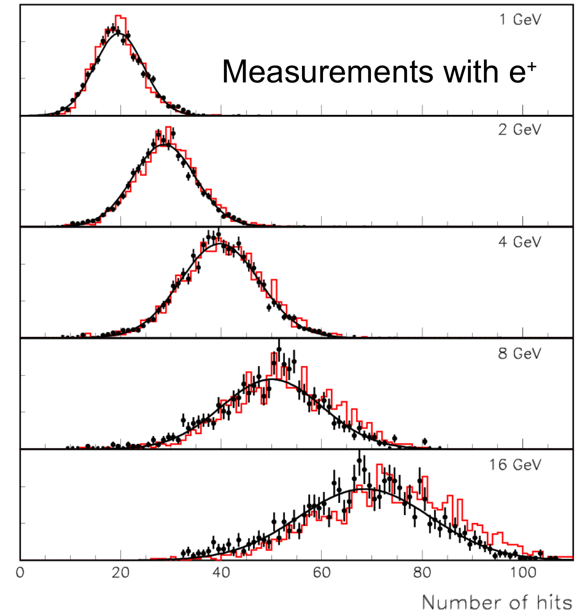


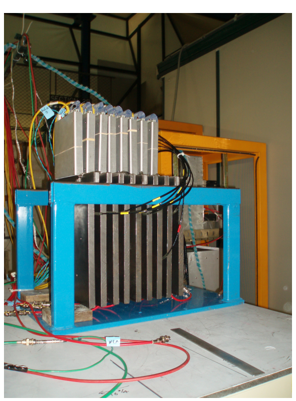
$R_{95\%}$ - shower radius, at which approx. 95% of the total AHCAL energy is transversally deposited

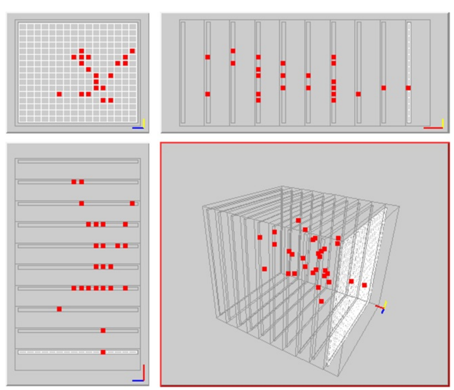
- Data Analysis of 2007 makes good progress
- Tests of hadronic shower models
  - Now have the sensitivity to do this

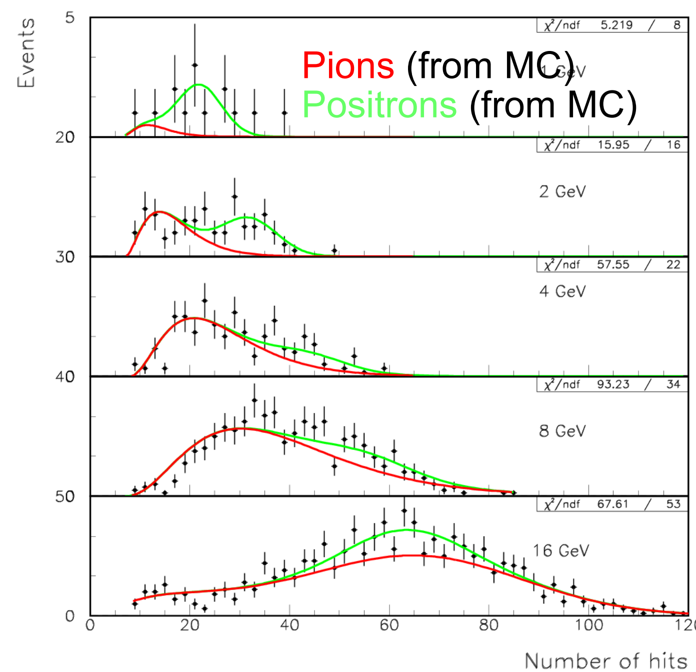
CALICE DHCAL

- Preliminary investigations completed
- Development and study of thin (glass) RPCs
- Development of a digital (1-bit) readout system for large number of channels
- Tests of a small prototype with cosmic rays and in the FNAL testbeam
- Reasonable agreement between measurements and Monte Carlo simulations of the set-up



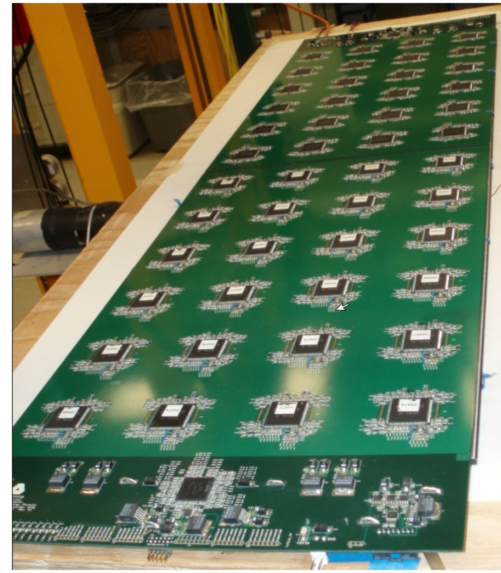


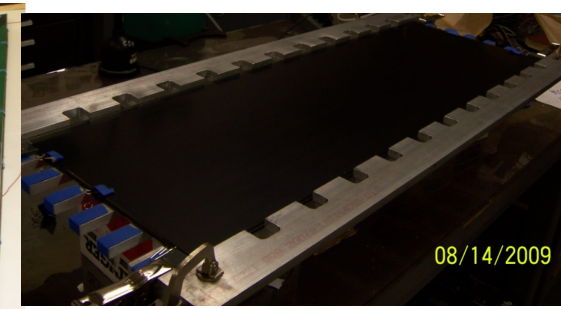


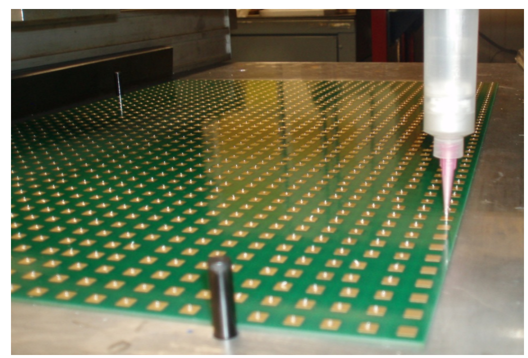


DHCAL 1 m^3 Stack

- 7/114 chambers (32 x 96 cm2) assembled and tested
- Front-end chip (DCAL III) produced (~ 10,600) and fully tested → no design flaws detected
- Readout boards prototyped and tested with cosmic rays
- Almost all fixtures for mass production in hand
- Construction to be completed by **April 2010**
- Tests in FNAL test beam in 2010/2011



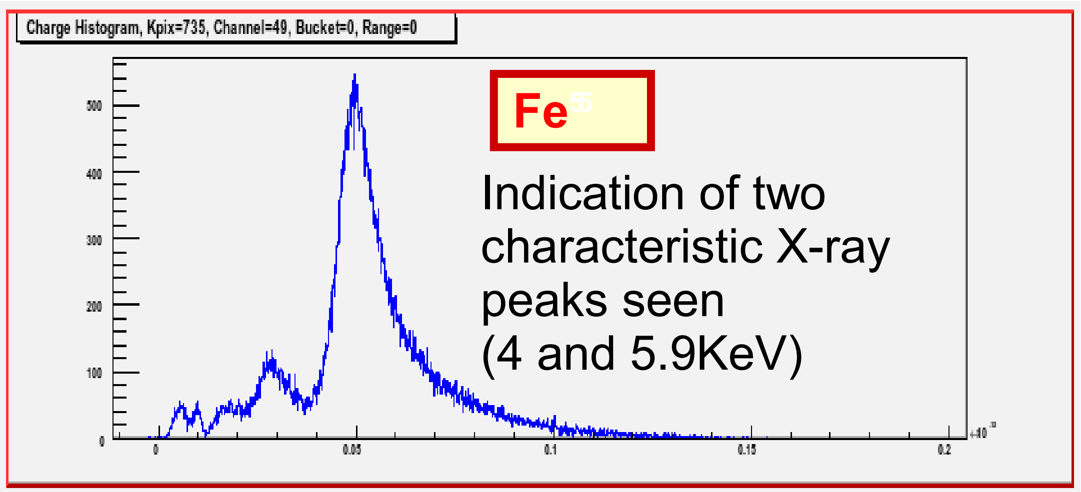


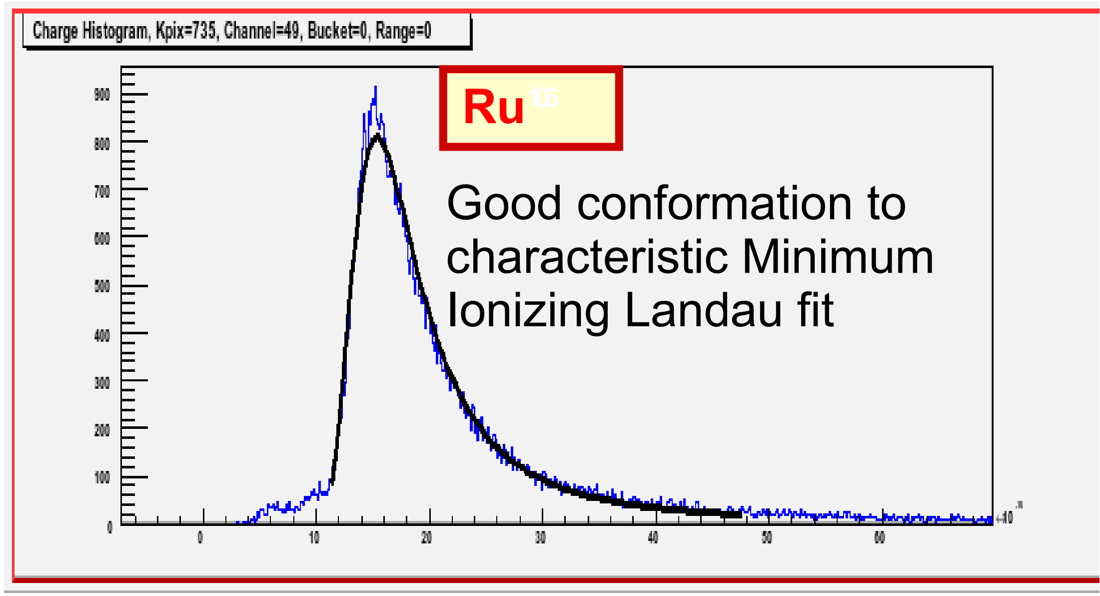


Collaborative effort of
Argonne, Boston, FNAL, Iowa and UTA

DHCAL GEM

- Double-layer GEM
  - Readout using KPiX
- Development of GEM foils
  - Collaboration with CERN
- Plans for Beam test
  - 30x30 cm array (2010)
  - 30 x100 cm array (late 2010)
  - 100x100 cm planes to use in CALICE HCAL (2011)

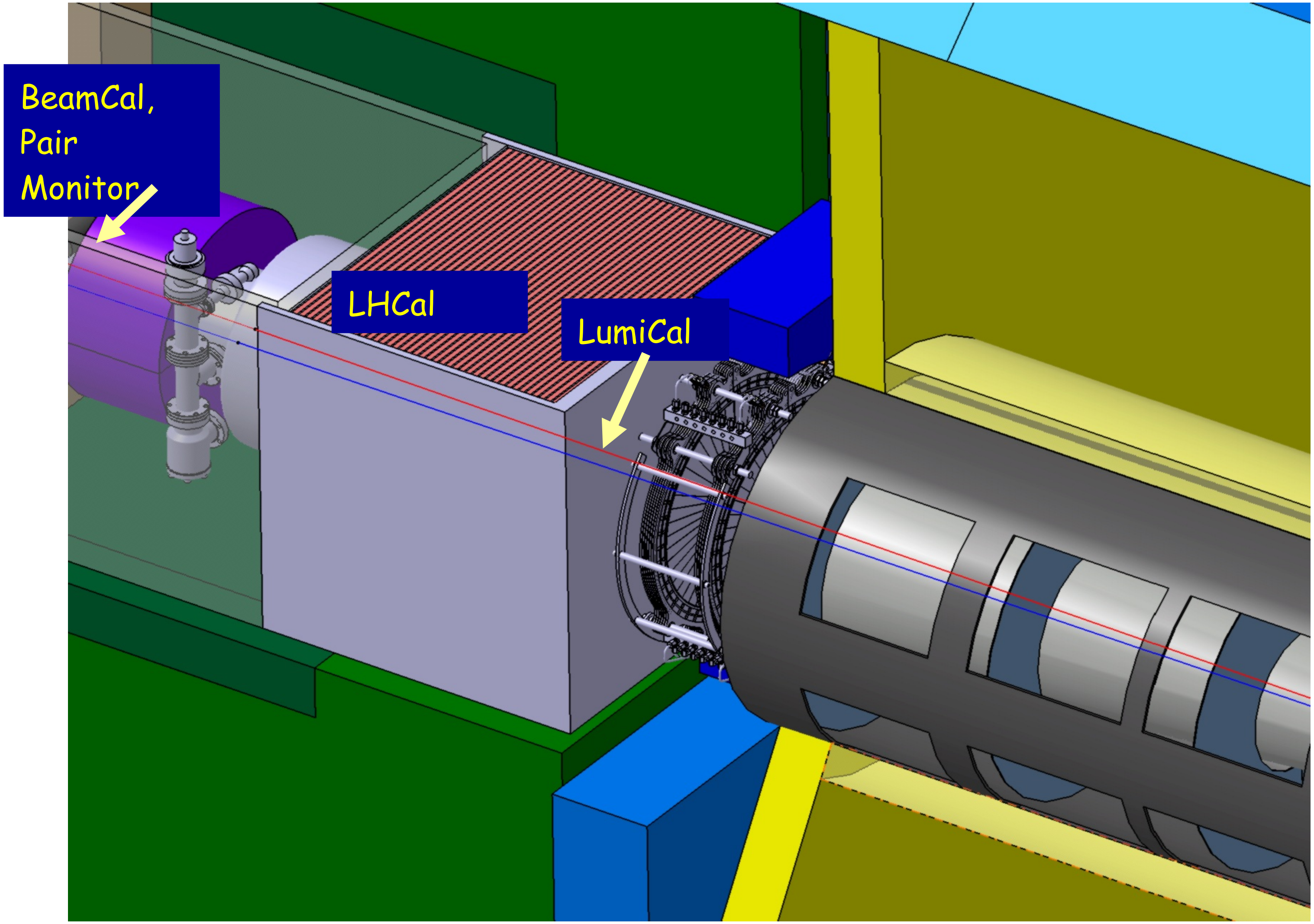




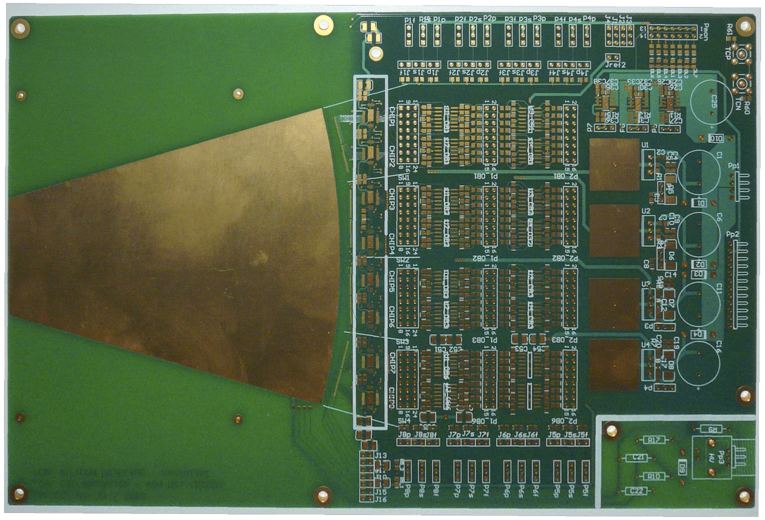
CALICE

- Future Plans focused around technical prototypes
  - Minimize dead areas
  - System integration
  - Power pulsing
- Will help for realistic designs for the TDR

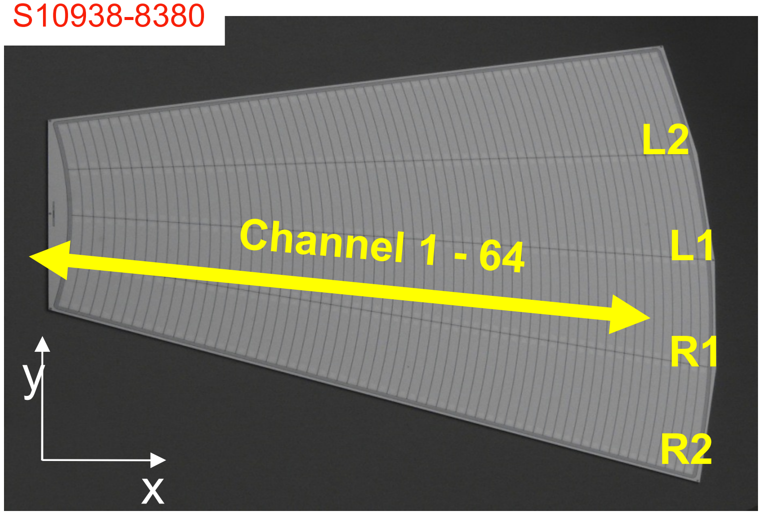
FCAL

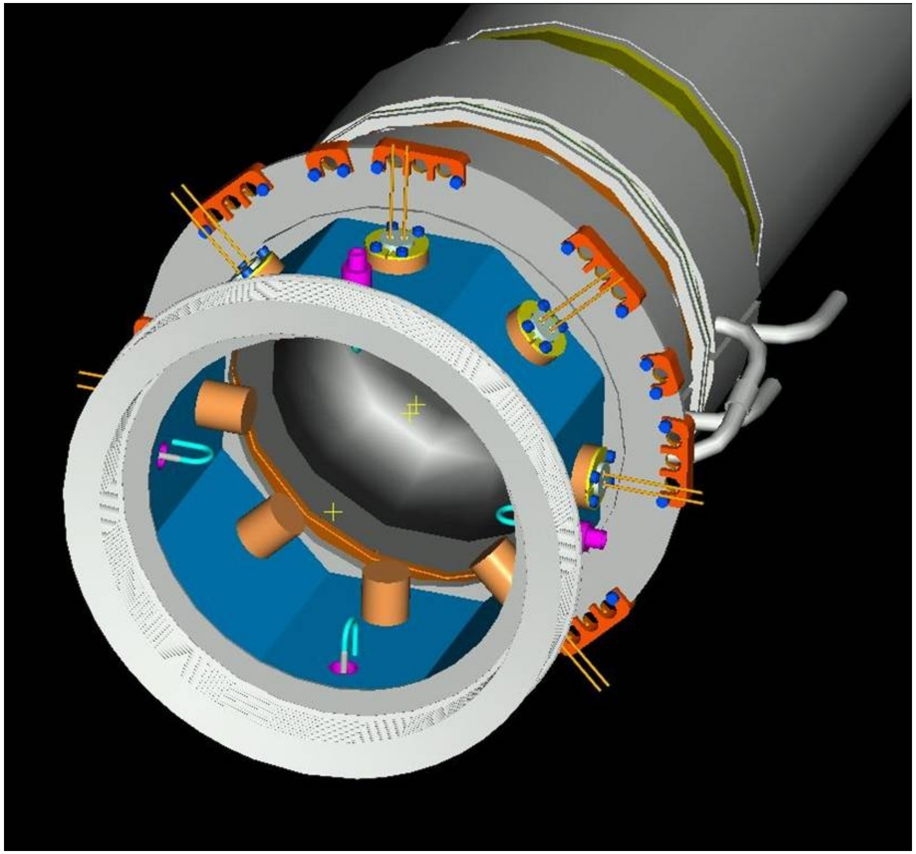


FCAL



Hamamatsu
S10938-8380



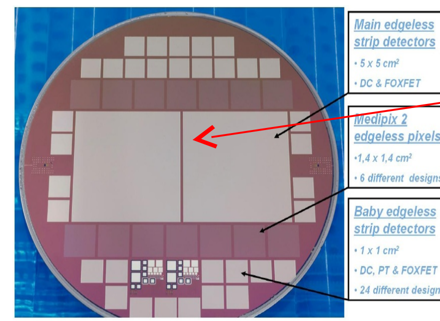


FCAL designed, constructed and installed a Beam-Condition Monitor at FLASH
(4 diamond and 4 sapphire sensors)

SiLC

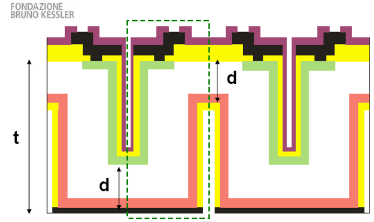
- Baseline
  - 6″ microstrip silicon strips
- Recent developments
  - Active edge SOI strips
  - strips, 8″, 200 µm thick, 50 µm RO pitch, active edge
  - 3D Short strips & pixels
- Readout ASIC work
  - Explore 90nm
  - Direct connection
  - Time over Threshold

Active edge SOI strips



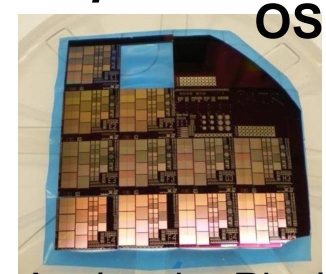
6'' wafer, 5x5cm^2 Electrically characterized. Soon in test.

3D Short strips & pixels



3D short strips proto *produced by IRST, test LPNHE (2010)*

OSU

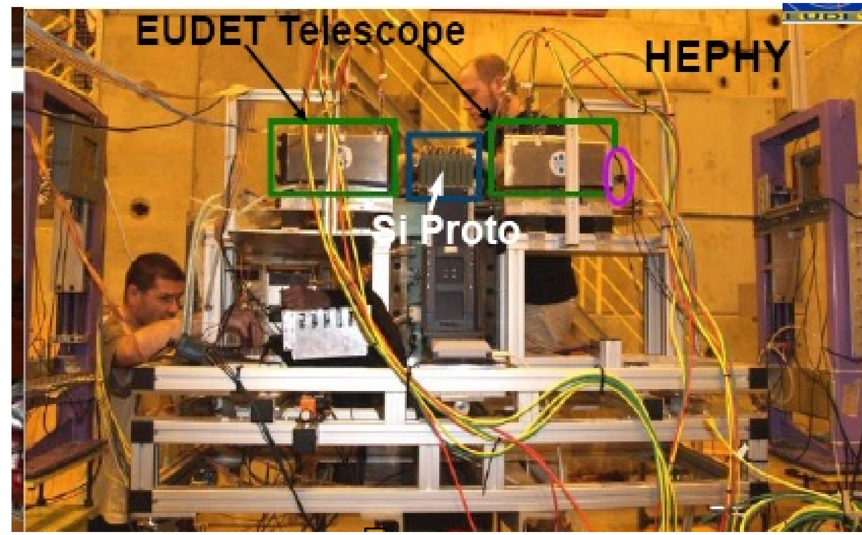


Avalanche Pixel Sensor: high Gain, low % X0

SILC Testbeams

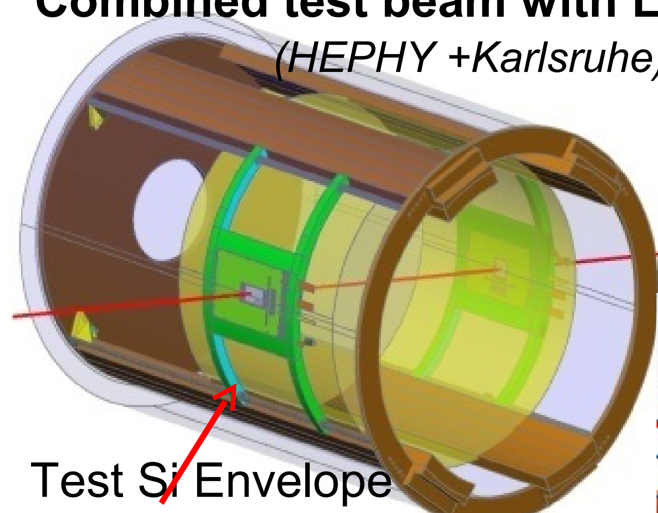
- Beamtest at CERN
  - SPS & PS
- Whole Test beam chain in place
  - DAQ, Mechanics, Software
- Plans
  - In preparation 2010-12: combined test beams with calorimeters
  - Tests on new FEE, new sensors;
  - Larger size prototypes

Combined test with EUDET MAPS telescope (SPS)



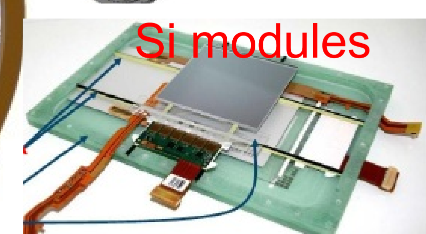
Combined test beam with LCTPC (DESY)

Combined test beam with LCTPC (DESY)



Mechanical support

Si modules



The other side

- ILD & SiD have also identified these areas as critical:
  - Alignment
  - Advanced Powering Schemes (DC-DC, Serial powering)
  - Power pulsing
  - Mechanical structures
  - Superconductors

From Marcel Demarteau @TILC09:
Many detectors, and a large part of the physics program, depends on novel powering schemes such as power pulsing, serial powering or DC-DC conversion
Yet there is very little R&D ongoing in the community addressing these issues

IDAG also picked up on this

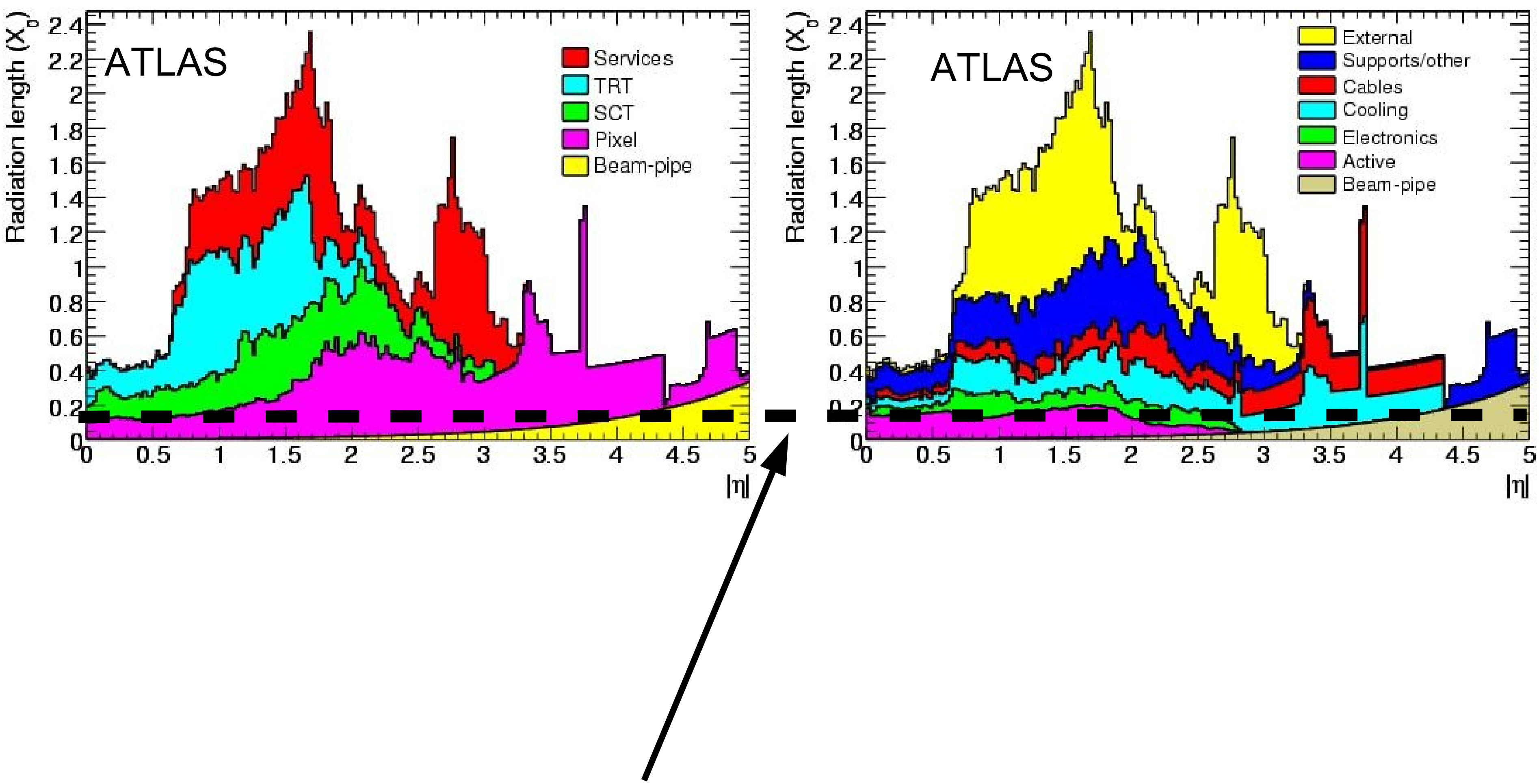
SiD and ILD plan to employ pulsed powering for the silicon detectors. This scheme and the mechanical stability of the detector still need to be demonstrated.

Power-pulsing of detectors in intense magnetic field should also be the subject of a dedicated R&D program.

It should be noted that pulsed power operation remains a potential, and as yet untested, issue for ILD and, indeed, for all the ILC concepts.

Taken from *IDAG Report on the Validation of Letters of Intent for ILC detectors*

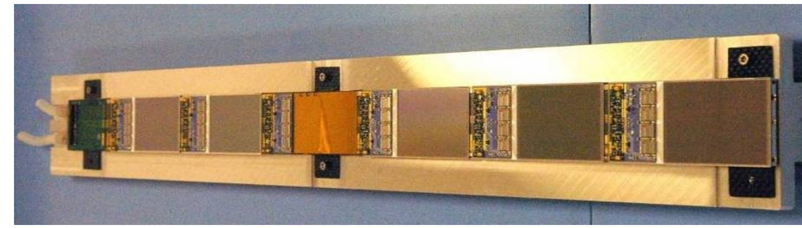
Remember the LHC !

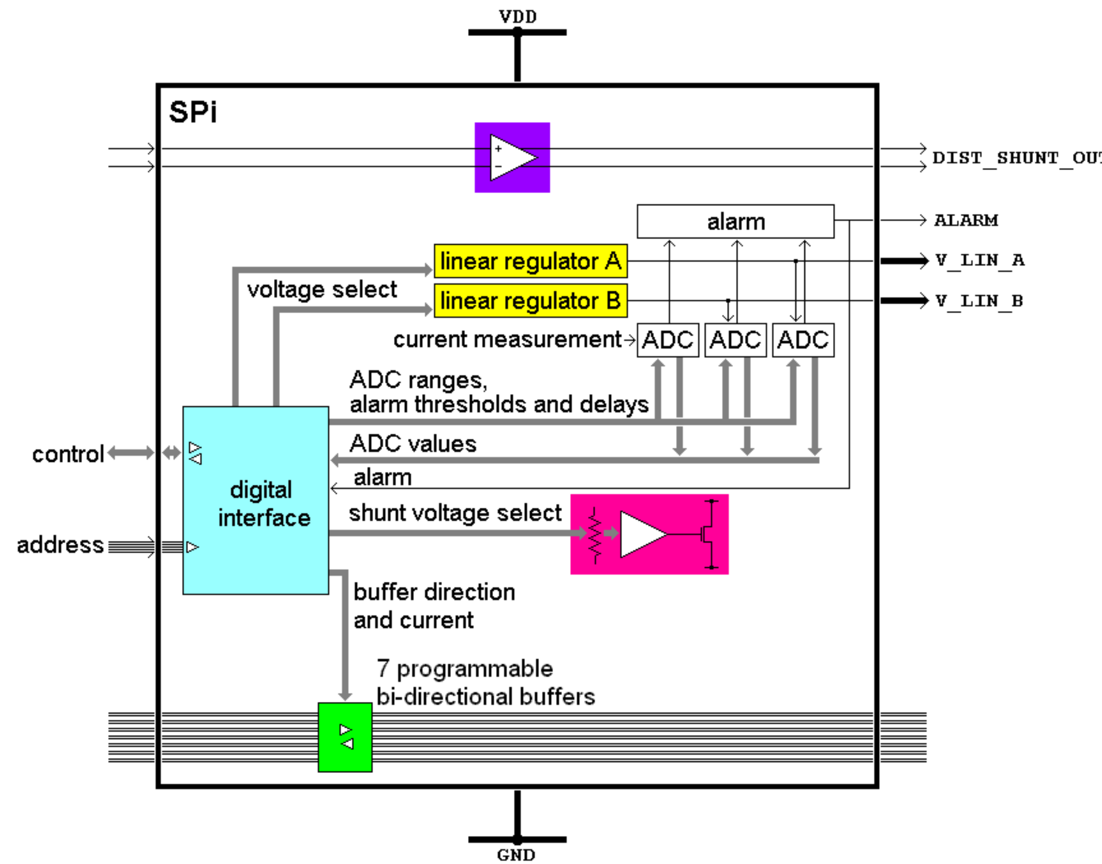


ILC Goal for the entire Tracking System

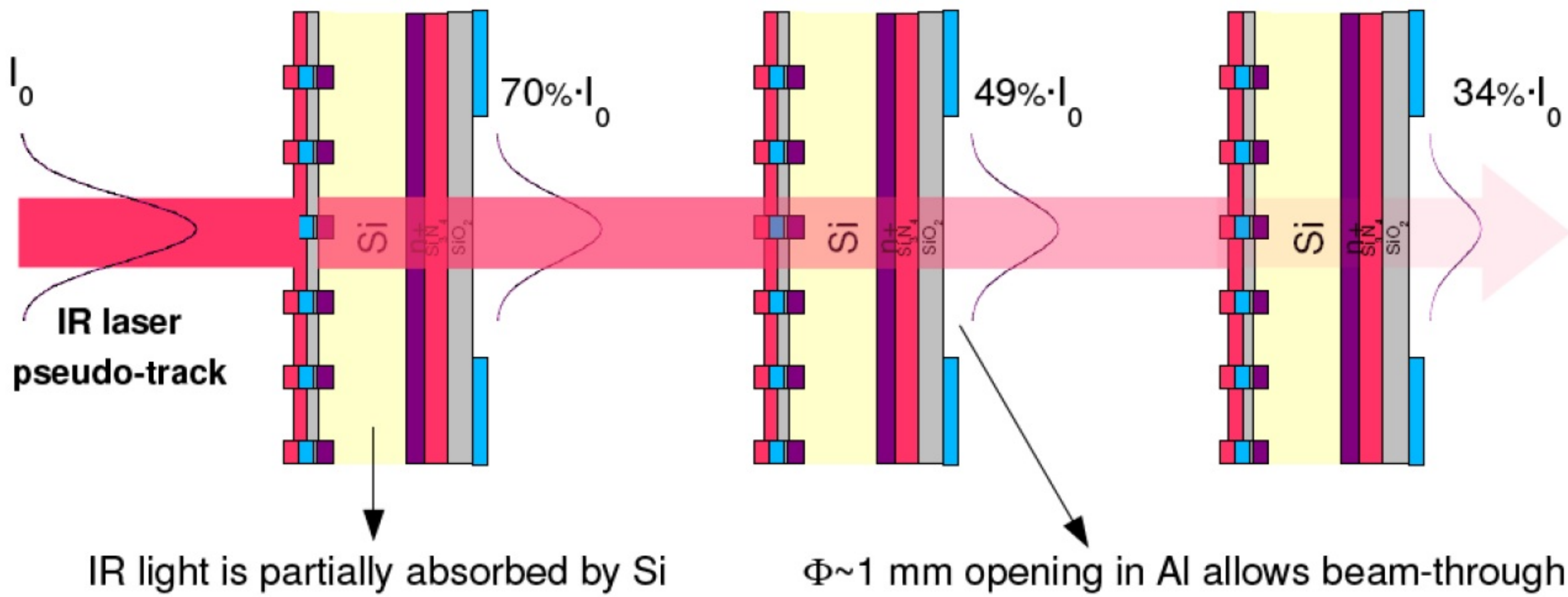
Serial Powering & SPi

- Driven by ATLAS upgrade
  - Serial Powered Staves
- SPi Chip
  - Generic Serial Powering ASIC
  - 0.25 µm CMOS
  - Made by Fermilab, RAL, UPenn
- Open question
  - How well does this work with pulsed power ?
- DC-DC also very active field





IR Silicon Alignment

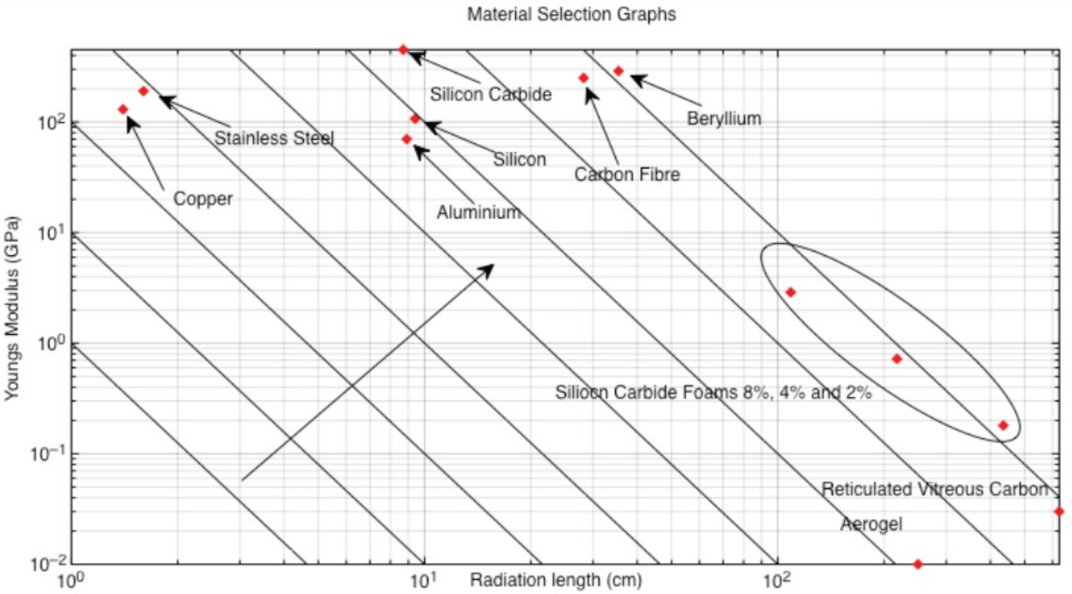


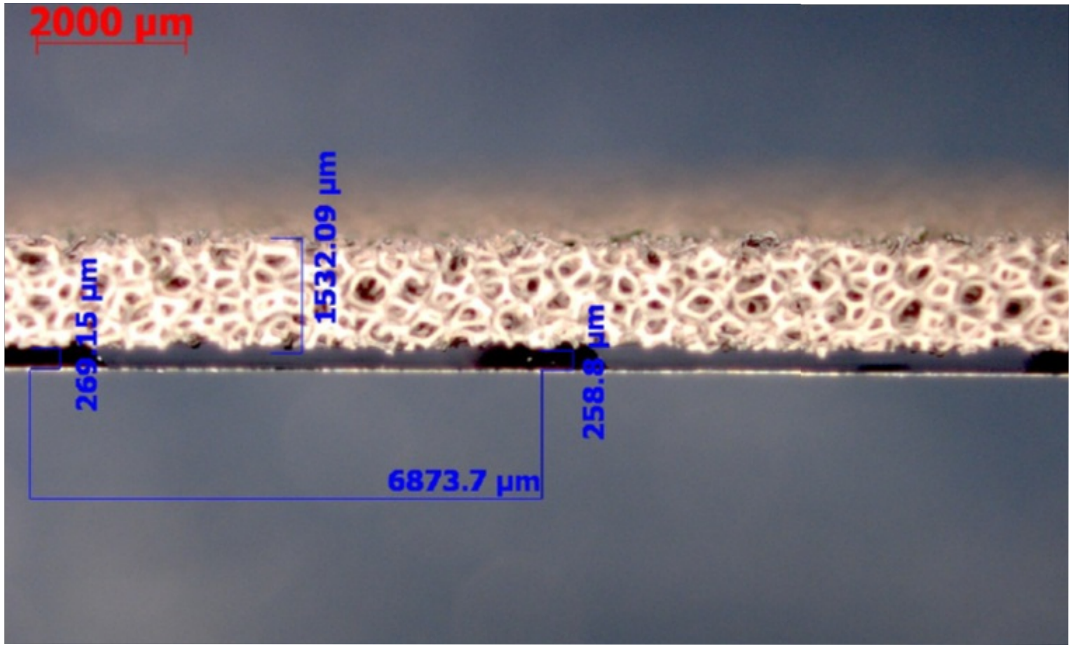
- Si is almost transparent to IR light.
- IR beam plays role of straight tracks
- Measure position across several sensors
- Minimum impact on system integration & material budget
- Straightforward DAQ integration

See Talk by Daniela Bassignana

Low Mass Structures

- Low Mass Collaboration
  - *Investigate use of low mass support structures for detectors using silicon sensors.*
- Focus on SiC foams
  - Construct ladders
  - Integrate cooling
  - Mechanical properties
  - Machining



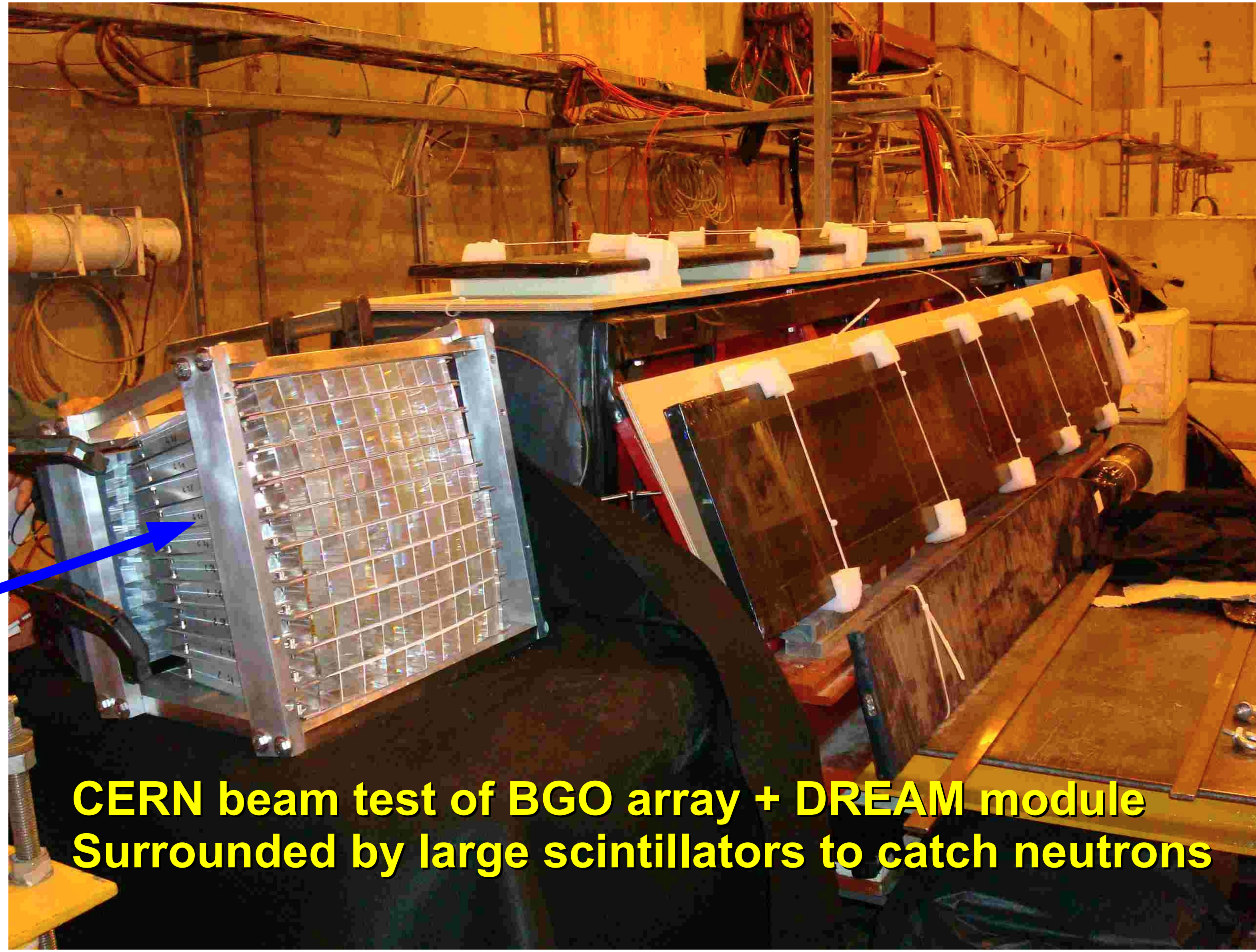


What about higher energies

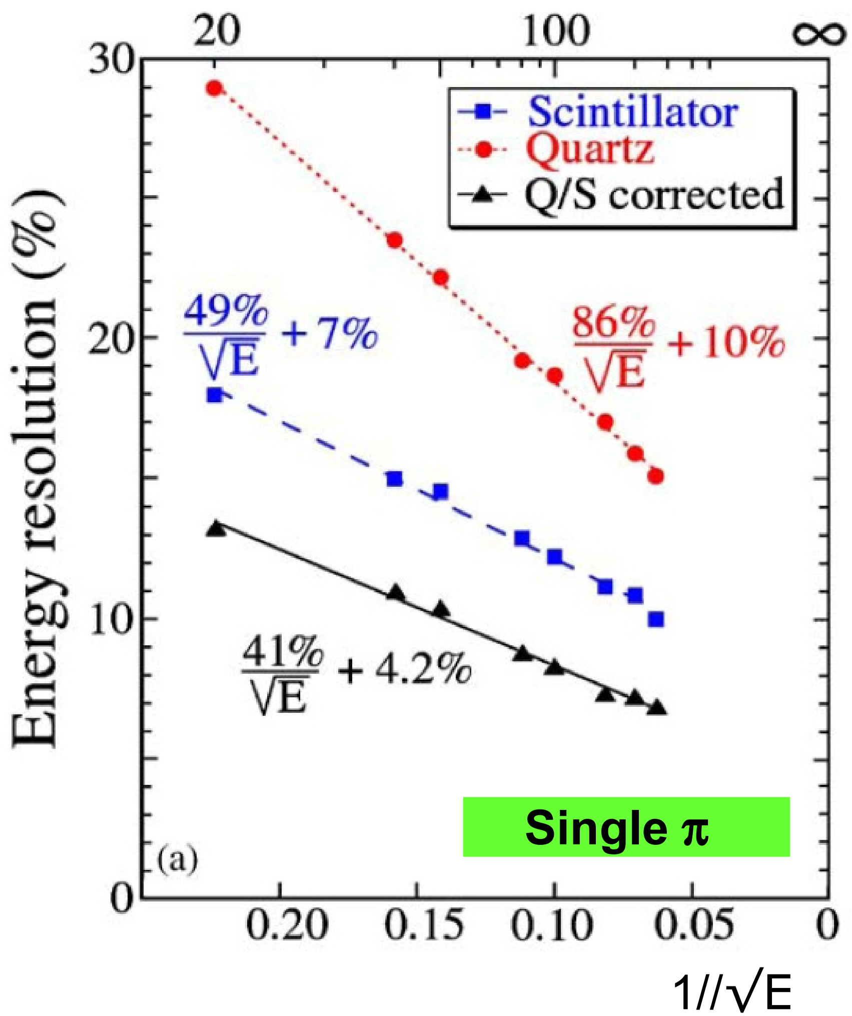
- LHC may tell us
  - Need to run at 1 TeV or beyond
- ILC detectors not optimized for >1 TeV running
  - PFA at higher energies (See Mark's talk)
  - Or go for dual-readout ?
- If CLIC-type machine
  - Very different beam structure
  - Specific R&D needed

Dual Readout Progress

SPS Beam

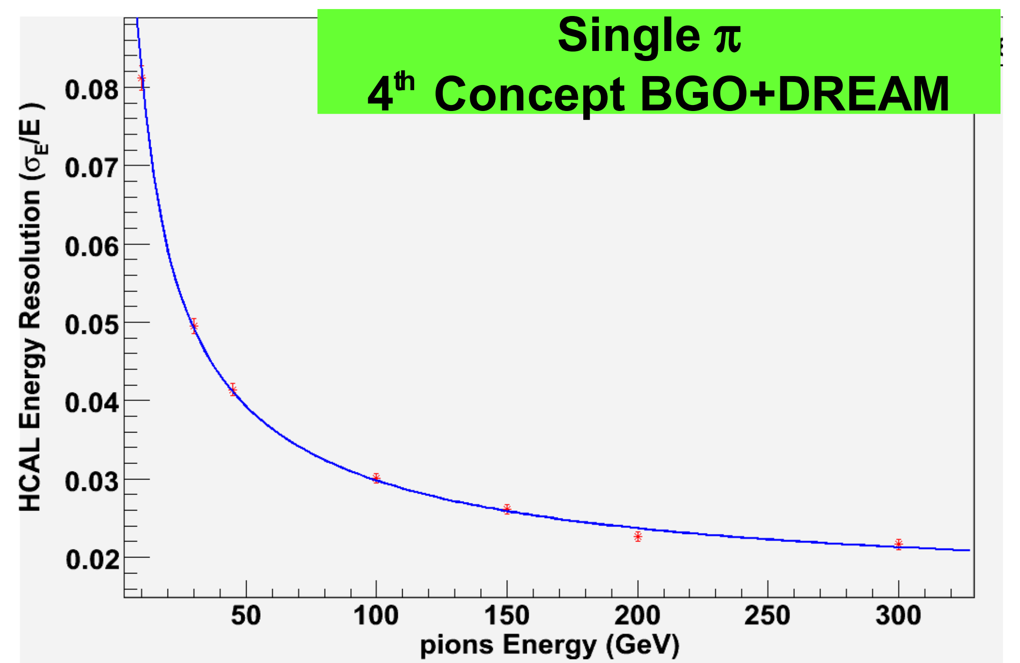


Energy Resolutions



DREAM module results

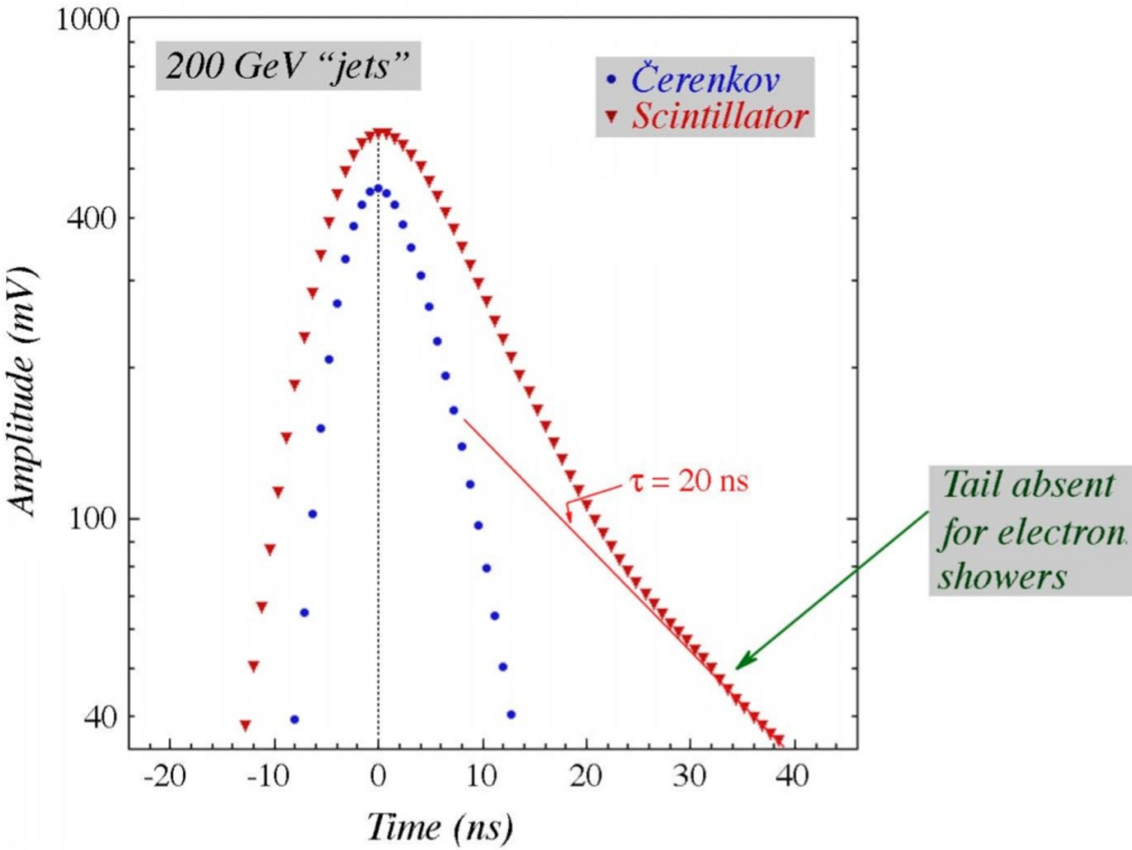
- Not using particle energy
- see NIM A 537 (2005) 537–561

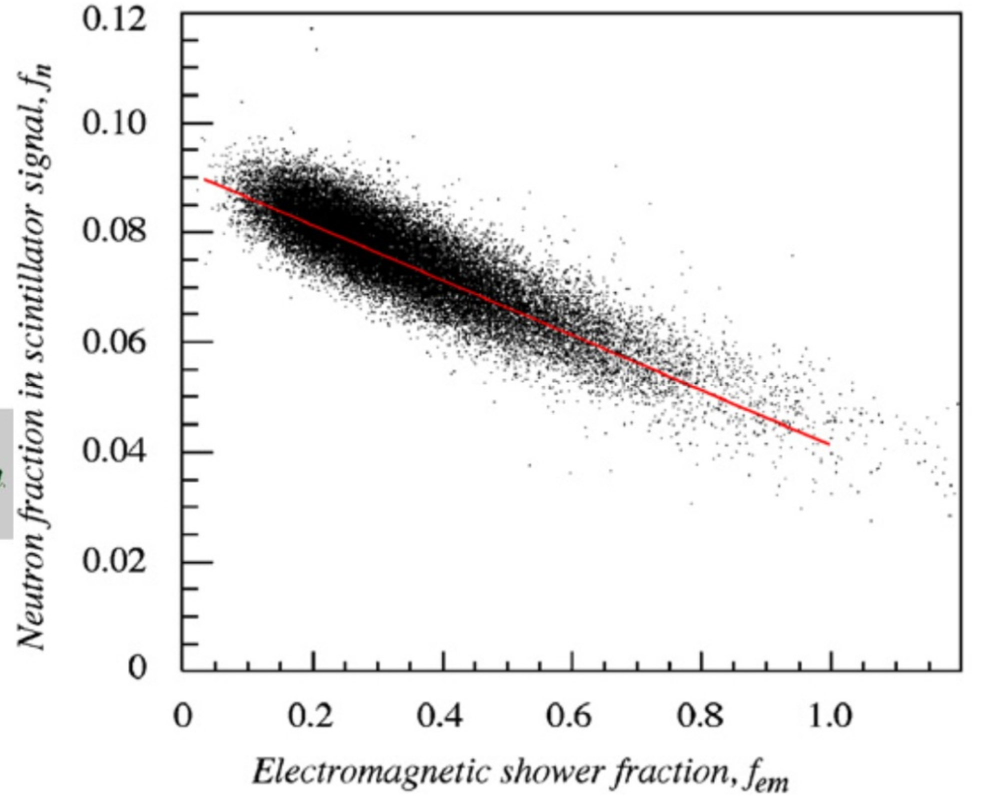


$$\frac{\sigma_E}{E} = \frac{29\%}{\sqrt{(E)}} \oplus 1.2\%$$

From Simulation

MeV Neutron Particle ID





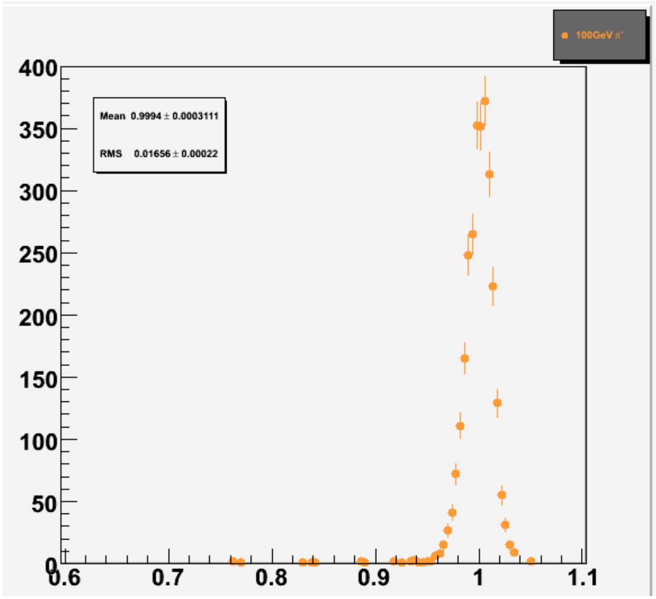
Neutron fraction, f_n

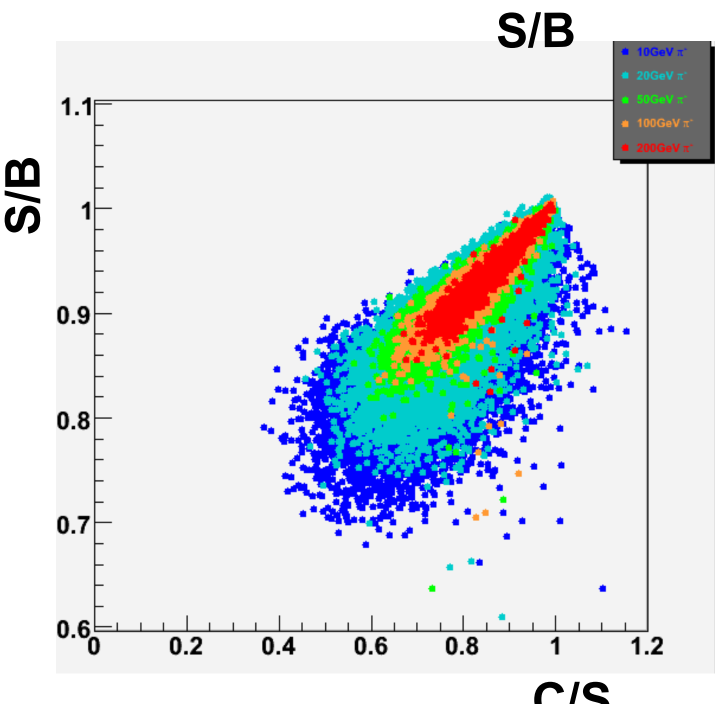
- improve energy resolution
- form "hadronic" ID

"Neutron signals for dual-readout calorimetry," NIM A598 (2009) 422.

DualReadout using Crystals

- Alternative approach
  - Total Absorption HCAL
- Readout
  - Čerenkov +Scintillation
- Extensive GEANT4 studies
  - 15 %/√E achieved
- Investigating suitable crystals
- Come up with a system design
  - Can it be build ?



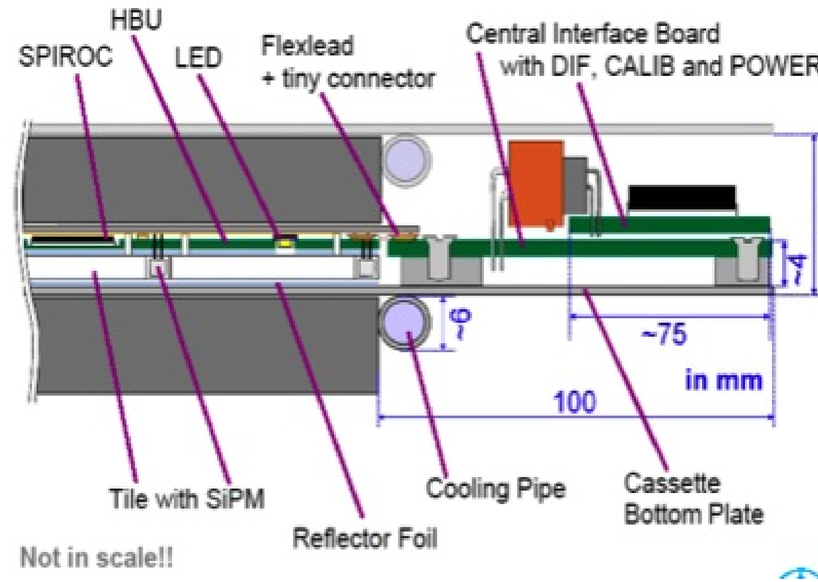


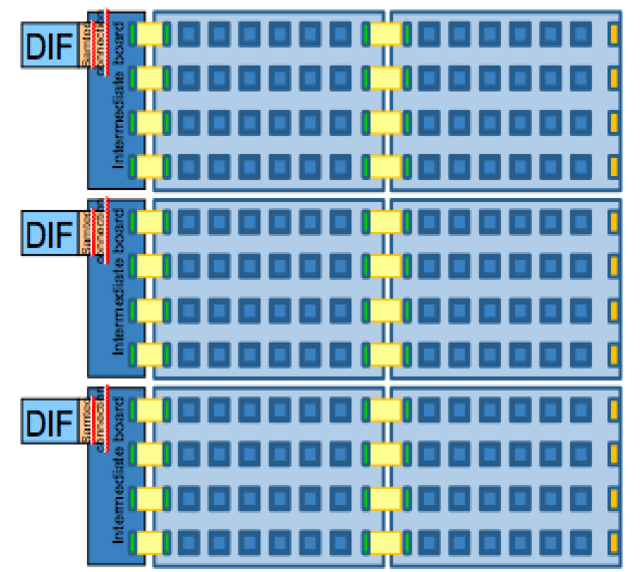
CLIC R&D

- R&D needed beyond present ILC developments:
- Time stamping
  - Most challenging in inner tracker/vertex region; trade-off between pixel size, amount of material and timing resolution (~10ns)
  - Needed for most other sub-detectors (e.g. calo at ~20 ns level)
- Power pulsing and DAQ developments (Timing)
- Hadron calorimetry
  - Dense HCAL absorbers to limit radial size (PFA calo based on tungsten)
- Solenoid coil
  - Reinforced conductor (building on CMS/ATLAS experience)
  - Large high-field solenoid concept
- Overall engineering design and integration studies
  - For heavier calorimeter, larger overall CLIC detector size etc.
  - In view of sub-nm precision required for FF quads

W-HCAL R&D

- Motivation:
  - To limit longitudinal leakage CLIC HCAL needs ~7λ_i
  - A deeper HCAL pushes the coil/yoke to larger radius (significant cost and risk increase
  - A tungsten HCAL is more compact than Fe-based HCAL, while resolutions are similar (increased cost of tungsten barrel HCAL compensates gain in coil cost)
- Plans
  - Use CALICE HCAL mechanics
  - Replace Fe with T
  - Scintillator planes & MicroMegas
  - Beam test in 2011





Coil R&D

- CLIC/ILC put high demands on solenoid (beyond CMS experience)
- Possible R&D subjects
  - Reinforced conductor (new Al alloys, nano-structured aluminium, cable-in-conduit)
  - Overall solenoid design and ways to reduce yoke mass
  - Optical-fiber based temperature/strain measurements in winding pack
- Several institutes have show interest (CEA-Saclay, CERN, Genova-INFN, FNAL, KEK, Protvino, SLAC)
- Two upcoming meetings are foreseen:
  - At CERN on October 15th (in the margin of CLIC'09)
  - Hefei China, in the margin of MT21 (October 18-23)

Summary

- ILC Detector R&D continues to be an exciting field
  - Impossible to do justice in 30 minutes
- R&D results need to make choices for the TDR's
  - These results will require additional funding
- Cost of Detectors components is becoming a concern
  - **Especially for Silicon**
- S(LHC) and ILC share common problems
  - Common R&D tasks ?
- Acknowledgments
  - J. Brau, M. Breidenbach, M. Demarteau, J. Goldstein, J. Hauptman, R. Ichimiya, R. Lipton, L. Linssen, W. Lohmann, A. Para, R. Poeschl, J. Repond, A. Ruiz, A. Savoy-Navarro, F.Sefkow, R.Settles, J. Timmermans, M. Trimpl, M. Vos, D. Ward, M. Weber, A.White, J. Yu