Status of the ATF Damping Ring BPM Upgrade

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Fermilab

Agenda

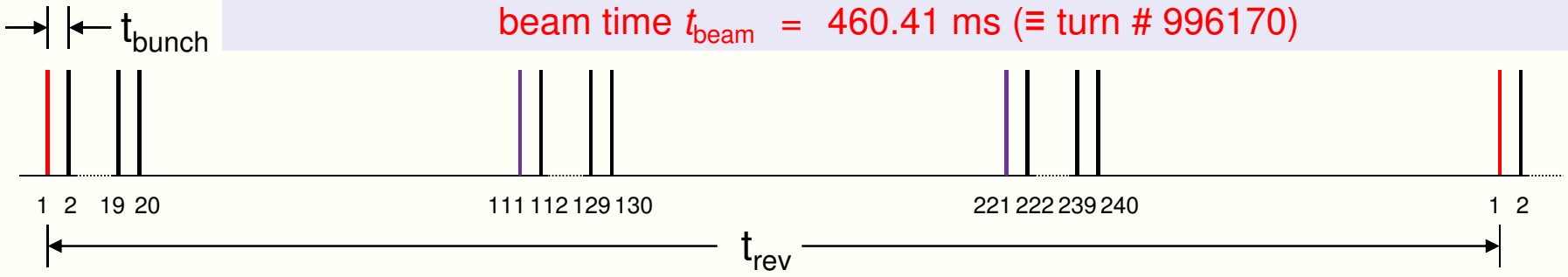
- Motivation
- The ATF Damping Ring
- BPM Upgrade overview
- Details on the downconverter and digitizer
- Status and next steps…

Motivation

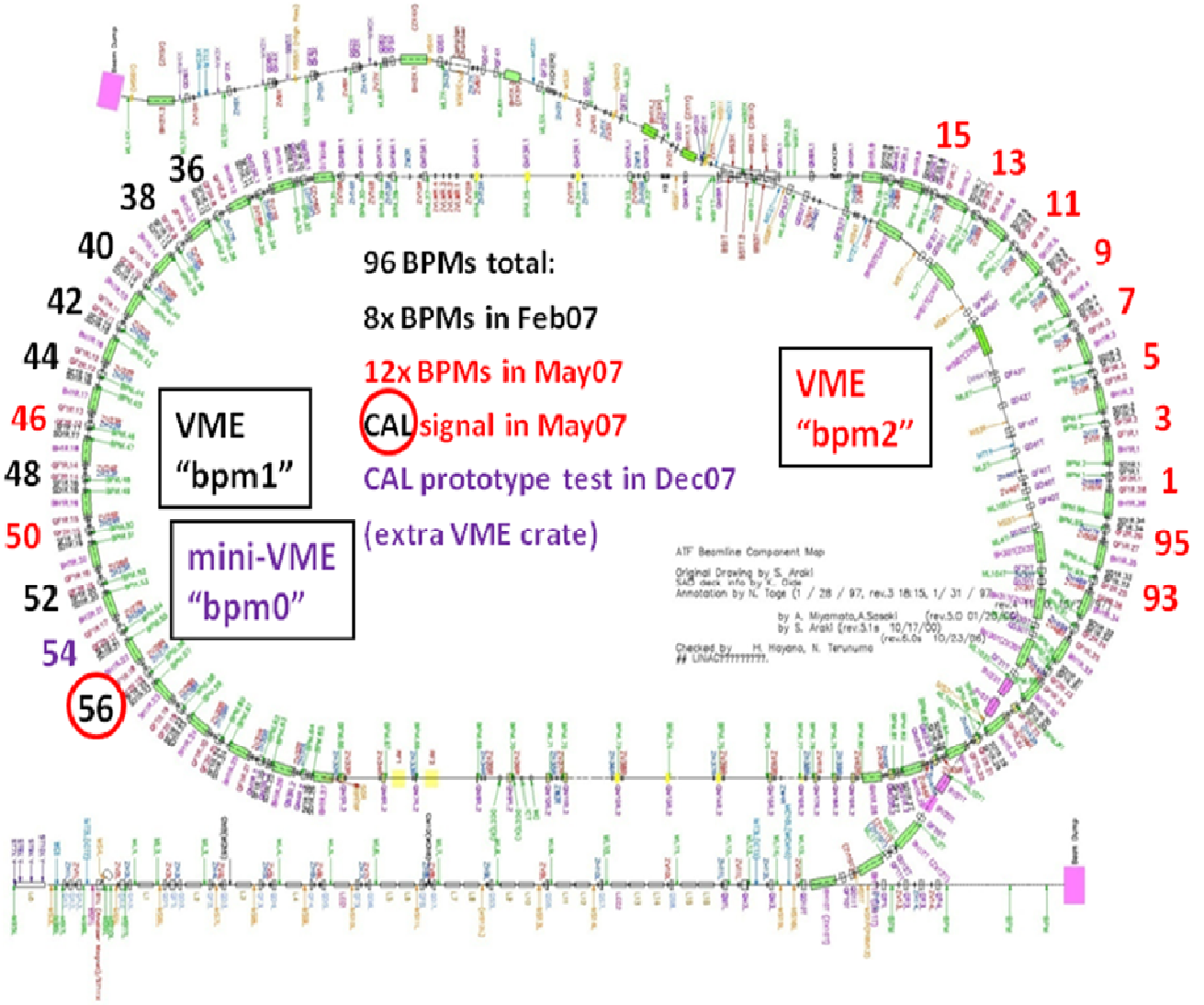
- **ILC damping ring R&D at KEK's Accelerator Test Facility (ATF):**
  - **Investigation of the beam damping process (damping wiggler, minimization of the damping time, etc.)**
  - **Goal: generation and extraction of a low emittance beam (ε_{vert} < 2 pm) at the nominal ILC bunch charge**
- **A major tool for low emittance corrections: a high resolution BPM system**
  - **Optimization of the closed-orbit, beam-based alignment (BBA) studies to investigate BPM offsets and calibration.**
  - **Correction of non-linear field effects, i.e. coupling, chromaticity,…**
  - **Fast global orbit feedback(?)**
  - **Necessary: a state-or-the-art BPM system, utilizing**
    - **a broadband turn-by-turn mode (< 10 μm resolution)**
    - **a narrowband mode with high resolution (~ 100 nm range)**

The ATF Damping Ring

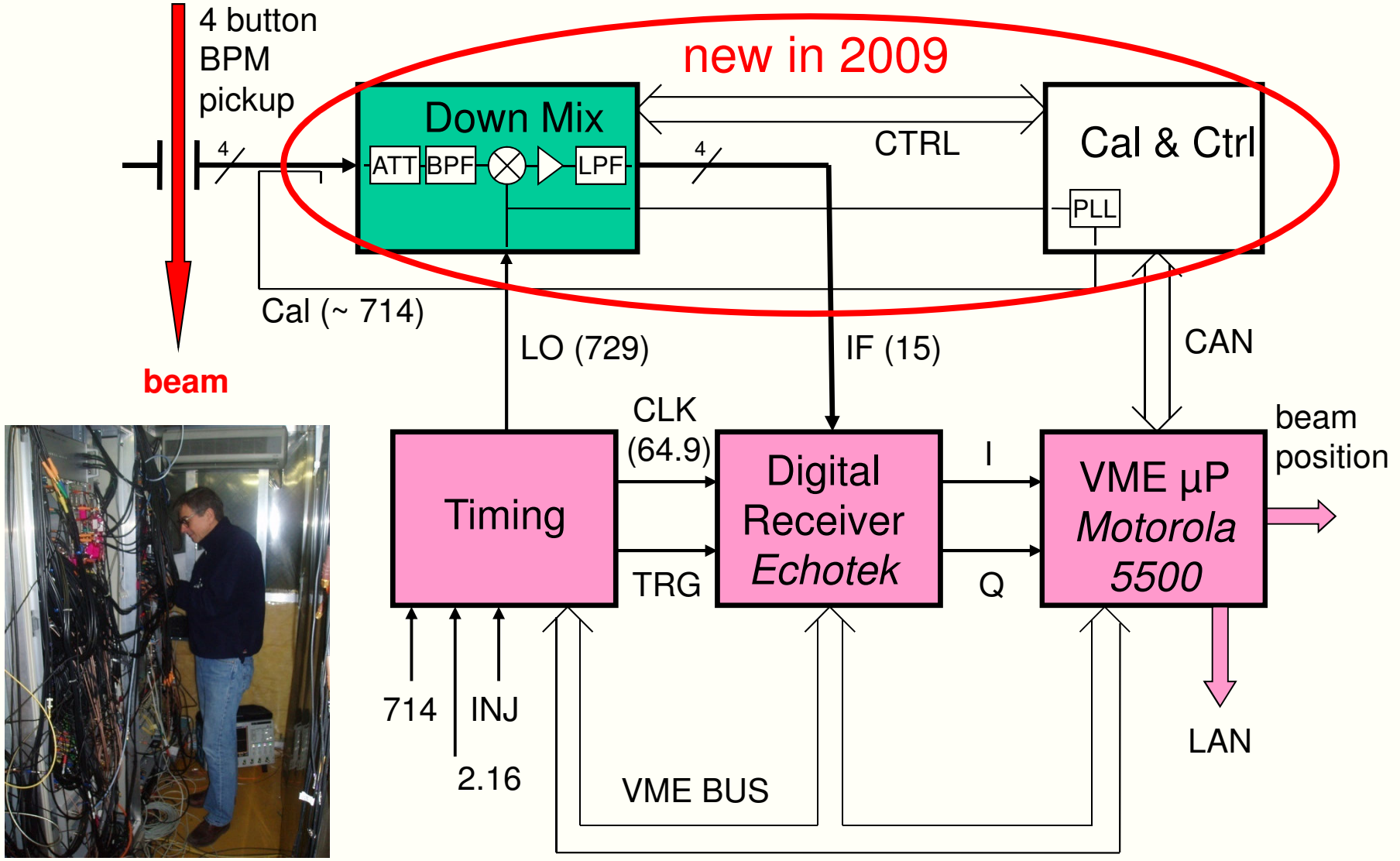
Machine and Beam Parameters		
beam energy E	=	1.28 GeV
beam intensity, single bunch	≈	~1.6 nC ≡ 10^{10} e^- (≡ I_{bunch} ≈ 3.46 mA)
beam intensity, multibunch (20)	≈	~22.4 nC ≡ 20 x0.7 10^{10} e^- (≡ I_{beam} ≈ 48.5 mA)
accelerating frequency f_{RF}	=	714 MHz
revolution frequency f_{rev}	=	f_{RF} / 330 = 2.1636 MHz (≡ t_{rev} = 462.18 ns)
bunch spacing t_{bunch}	=	t_{RF} / 2 = 2.8011 ns
batch spacing t_{batch}	=	t_{rev} / 3 = 154.06 ns
horizontal betatron tune	≈	15.204 (≡ f_h ≈ 441 kHz)
vertical betatron tune	≈	8.462 (≡ f_v ≈ 1000 kHz)
synchrotron tune	≈	0.0045 (≡ f_s ≈ 9.7 kHz)
repetition frequency f_{rep}	=	1.56 Hz (≡ t_{rep} = 640 ms)
beam time t_{beam}	=	460.41 ms (≡ turn # 996170)



The ATF Damping Ring



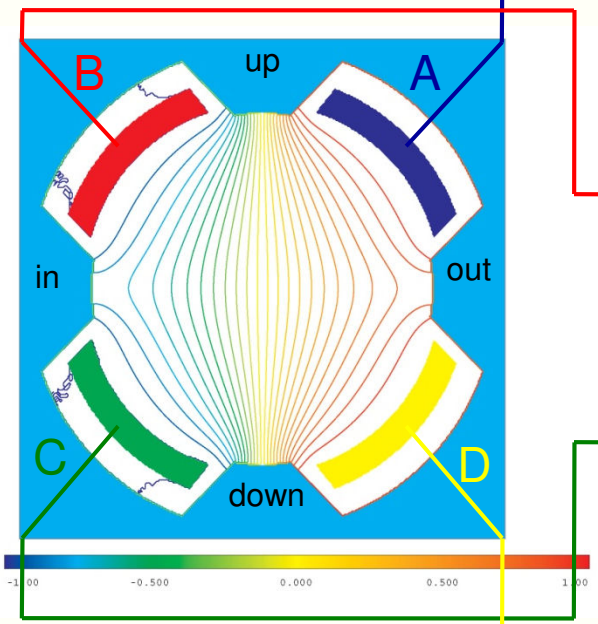
BPM Hardware Overview

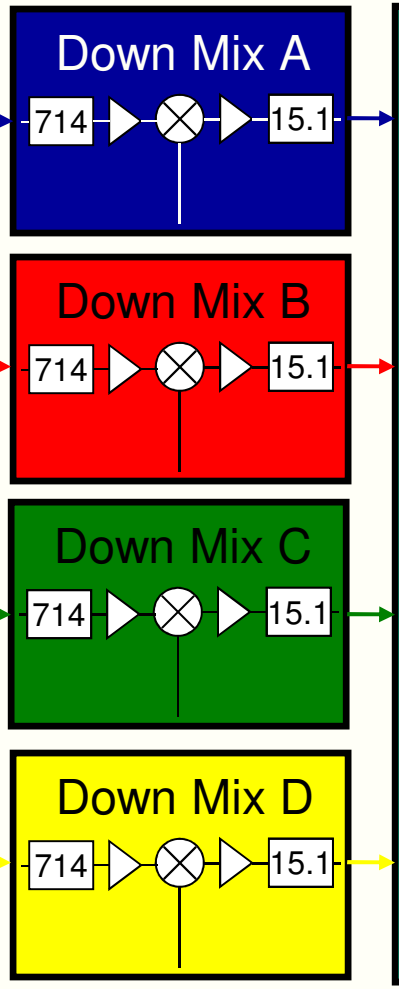


Overview of the BPM Upgrade

- New read-out hard-, firm- and software, BPM pickups (button-style) stay unchanged.
- R&D activities over the last couple of years on 20 BPMs in the arcs, utilizing mixed analog/digital signal processing
  - Test of different analog downconverters (w/o CAL)
  - Digital signal processing based on spare *Echotek* digital receivers.
- Final upgrade scenario (96 BPMs, plus spares)
  - 714-to-15.1 MHz analog downconverter with CAN-bus controlled calibration tone, located in the tunnel.
  - VME hard- & software, in 4 rack locations
    - 8-ch. 125 MSPS digitizer with an *Altera* Cyclone III FPGA
    - 12 ch. VME timing generator (Fermilab).
    - *Motorola* 5500 VME controller, with CAN-bus interface, running VxWorks & EPICS software
  - Auxiliary hardware, e.g. power supplies and distribution, LO-signal distribution, CAN-bus distribution, etc.

Beam Position Signal Processing





"Echotek" digital signal processing:

$$\phi_H = \frac{(A+D)-(B+C)}{A+B+C+D}$$

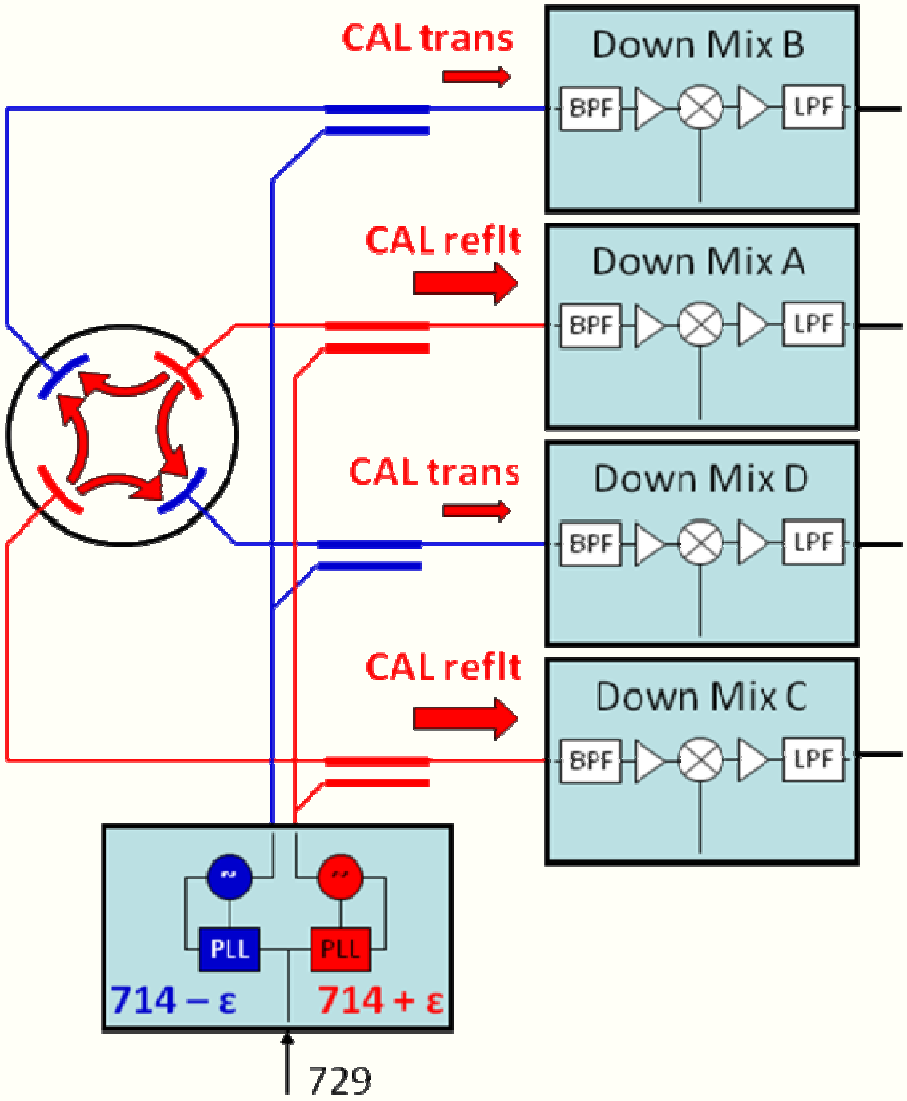
$$\phi_V = \frac{(A+B)-(C+D)}{A+B+C+D}$$

1D polynomial fit:

$$Pos\,[mm] = 9.35\phi + 1.00\phi^3 + 7.79\phi^5$$

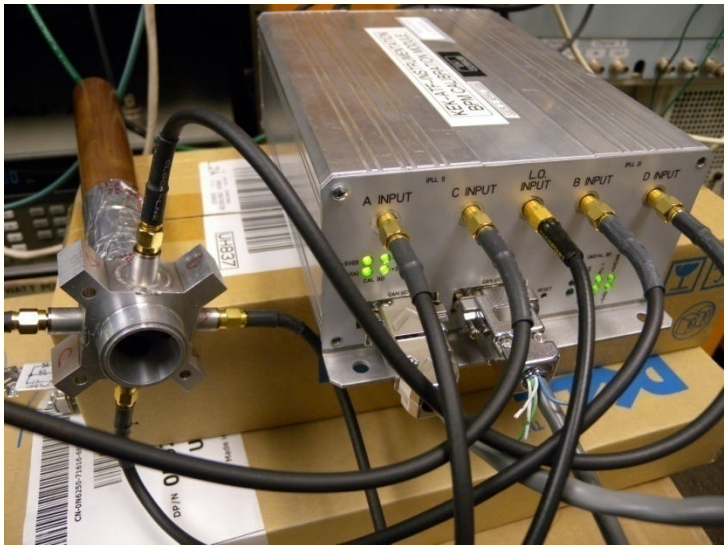
0.1 dB gain error ≡
27 µm offset error !

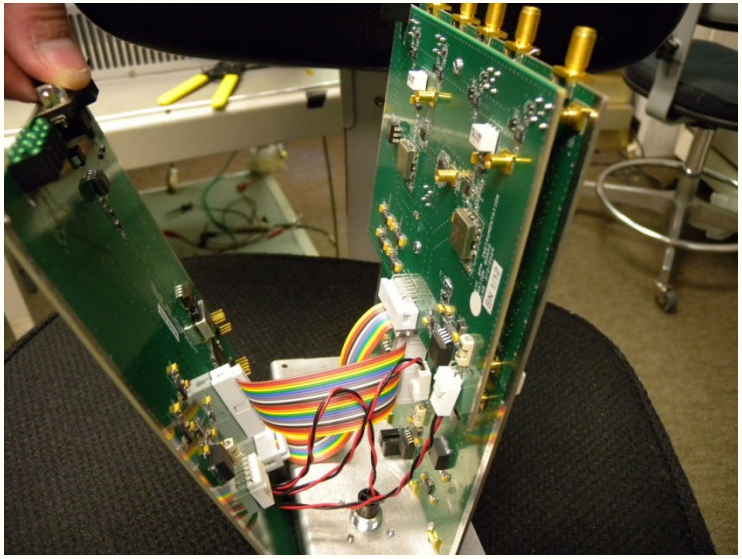
Calibration Schema

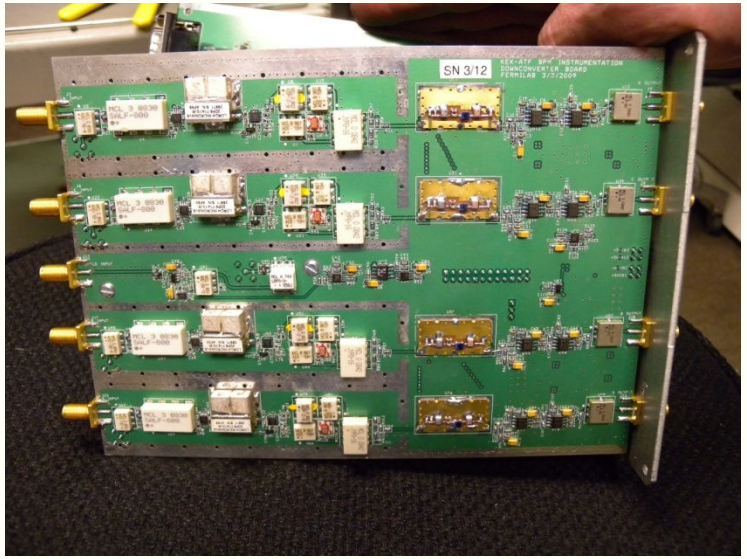


- 2 calibration tones:
  - 714 + ε MHz
  - 714 – ε MHz
  - In passband of the downconverter
  - Coupled through the button BPM
  - Alternative: Reflected CAL signal
- On-line calibration
  - In presents of beam signals
  - Available only in narrowband mode
  - Need separate downconverter channels

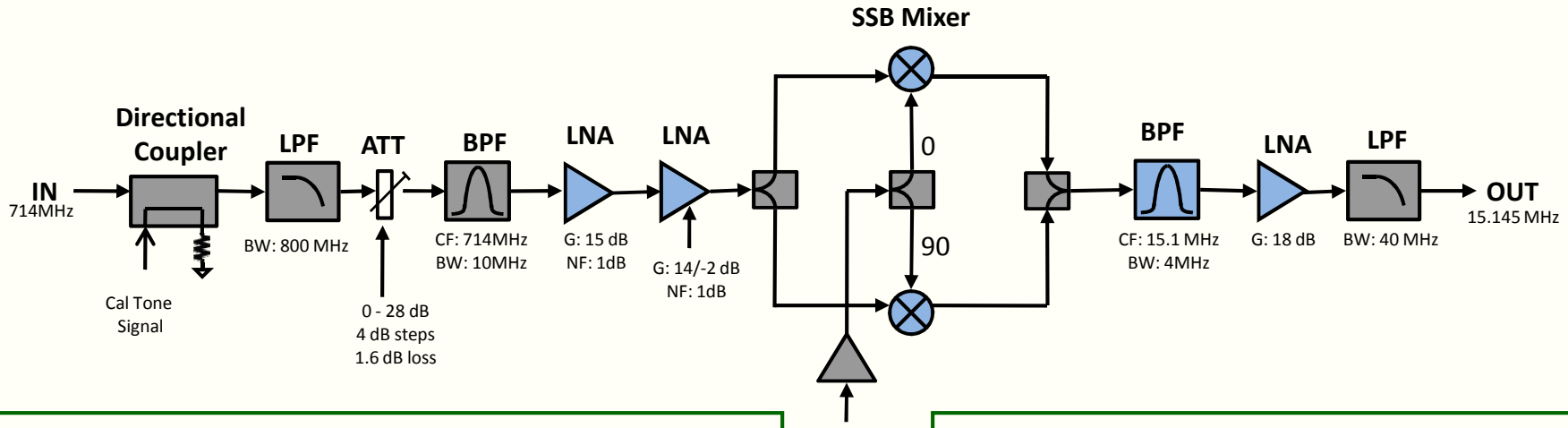
Analog Downmixer (prototype)







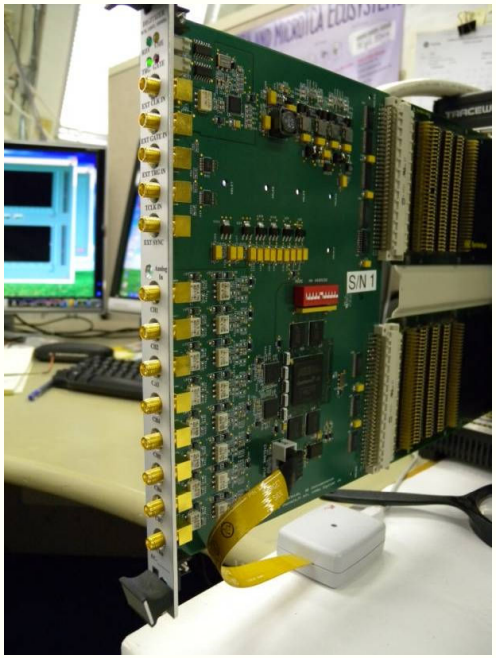
Analog Signal Processing



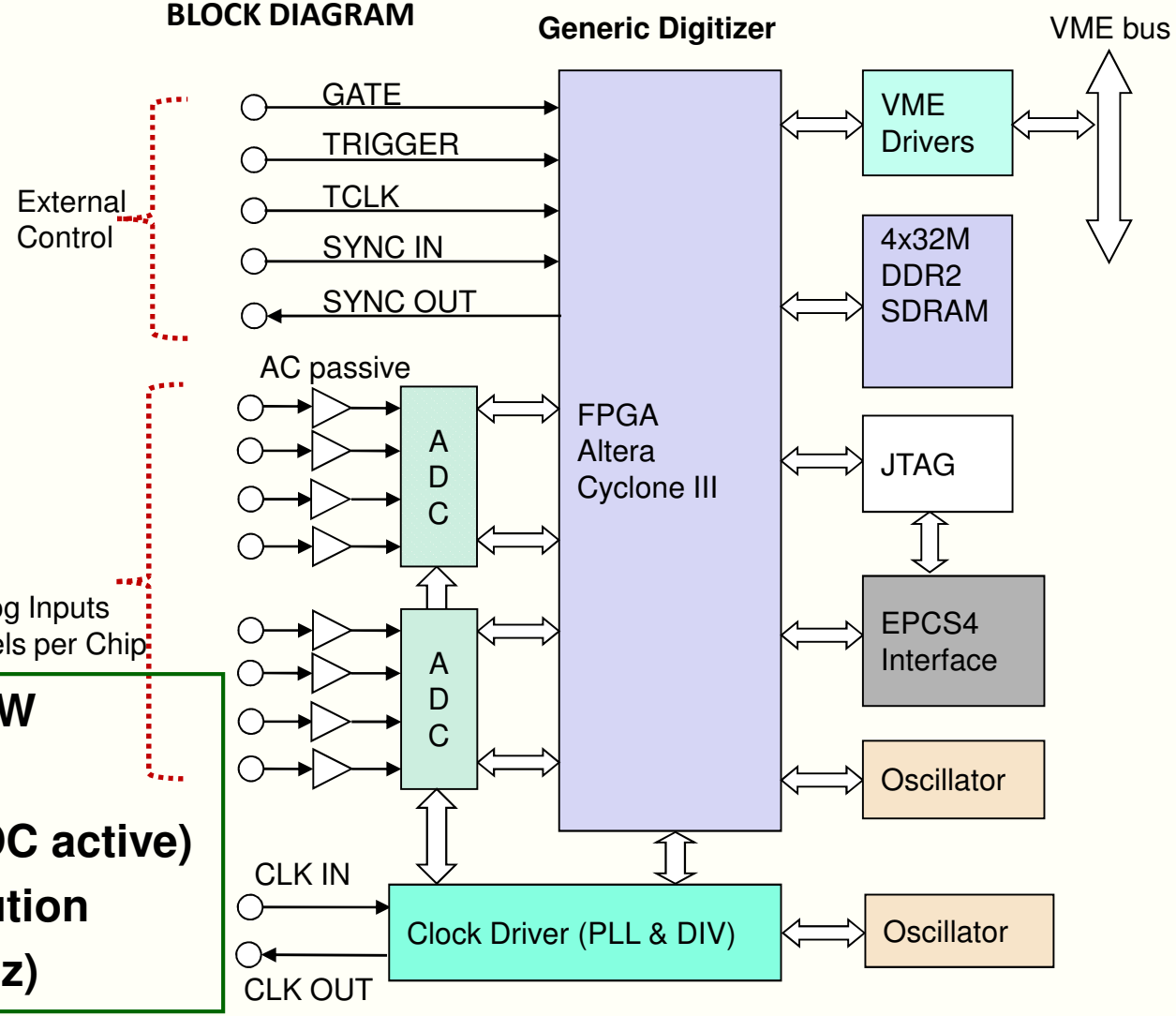
- 4-ch. Analog downmixer
  - IN: 714, LO: 729.1, IF: 15.1 MHz
  - CAN-bus controlled gain, attenuator & cal system
  - Gain switchable, low-noise, high IP3 input gain stage
  - Image rejection (SSB) mixer
  - ~30 dB gain, ultralinear IF stage

- Downconverter changes
  - Change the gain distribution (RF+, IF-)
  - Change mixers (+17 dBm -> +13 dBm)
  - Change response of the IF section BPF

8-Ch,14-bit, 125 MS/s VME Digitizer



BLOCK DIAGRAM

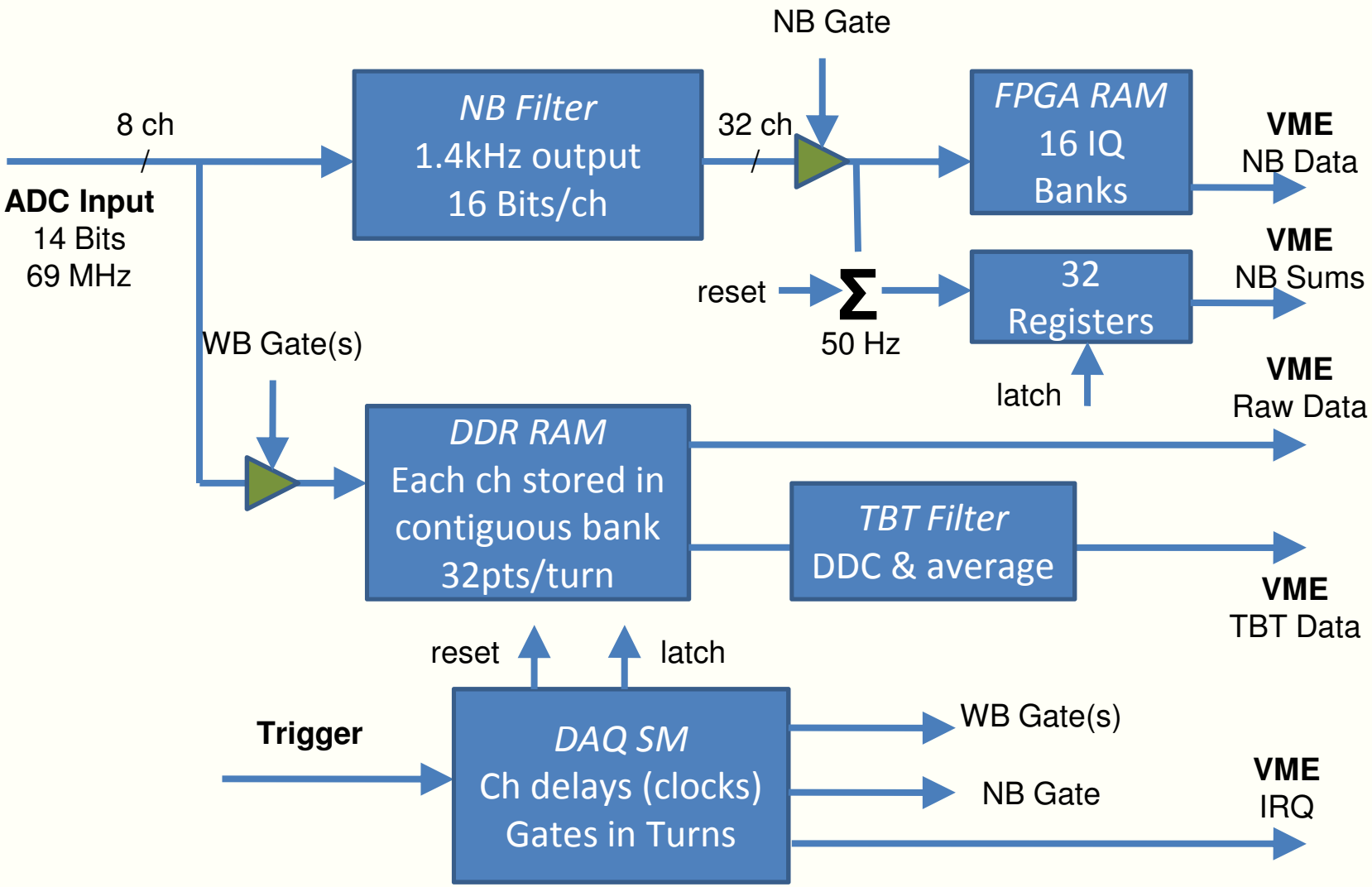


- 125 MSPS, 500 MHz BW
- 4-ch serial ADC chips
- 8-ch, AC passive (or DC active)
- PLL/VCO CLK distribution
- SNR > 72 dB (@50 MHz)

Digital Signal Processing

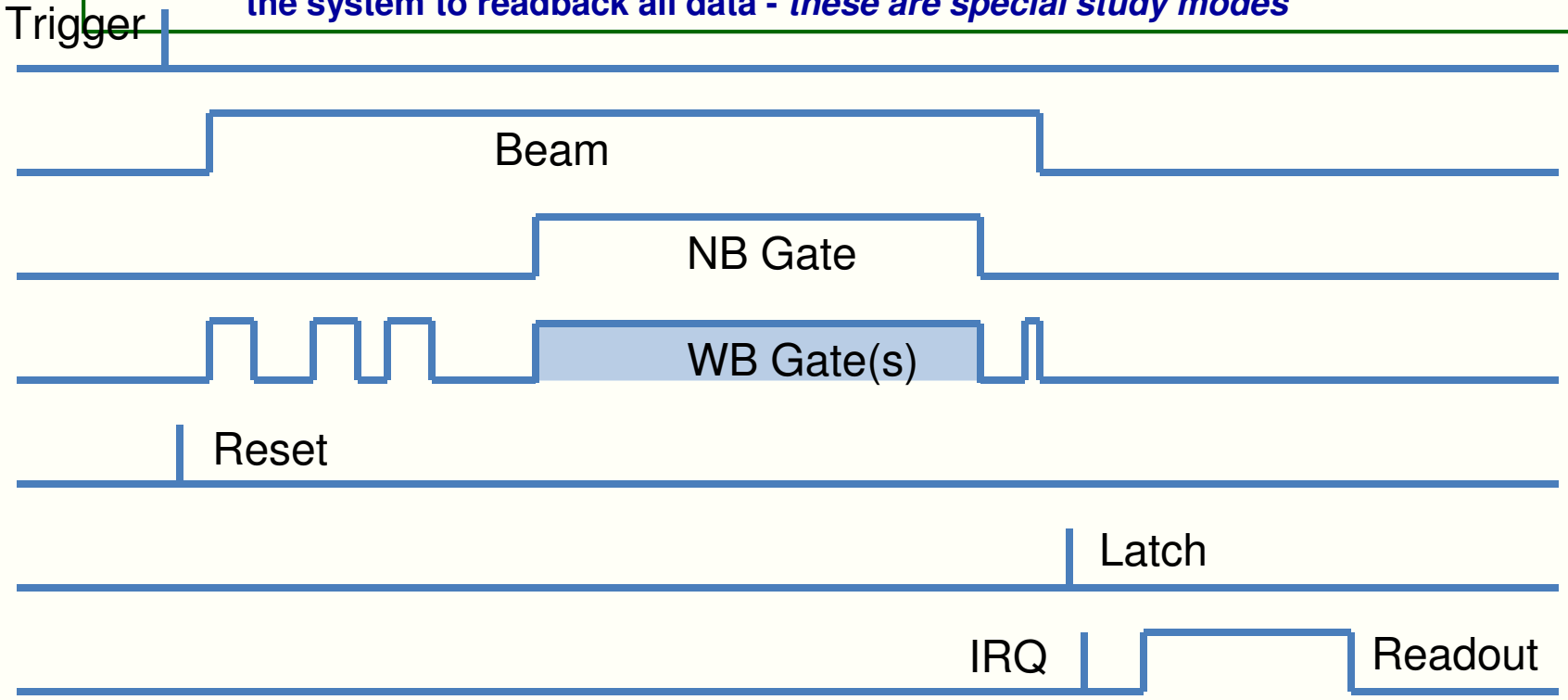
- **No Modes** - on external trigger processes data
  - Raw data to ram
    - TBT readback & process (ddc & average) -> I,Q per turn
    - diagnostic readback
  - Narrowband processing (Filter & Decimate)
    - Store array of I,Q per channel for readback
    - Provide single sum I,Q per channel over n*50 Hz
  - Programmable trigger delay per channel (adc samples)
- Any data type (NB, TBT, Raw) can be readback after each trigger
  - All data will be read out as I,Q pairs
  - Caveat: The CAL tone has to be disabled for TBT data
  - Each board will pull IRQ when data is ready

FPGA Block Diagram



System Timing Cartoon

- **Trigger before beam injection (injection rep rate is ~1.5 Hz)**
  - **Beam in machine for ~1e6 turns (~450 msec)**
  - **Each machine turn is 462.18 nsec -> 32 ADC clocks**
  - **Gates specified in turns (need to account for filter delay/decimation for NB**
  - **Data in boards is overwritten on each trigger**
  - **Note for WB readback (diagnostic and some TBT data) it will be necessary to halt the system to readback all data - *these are special study modes***



Memory Map

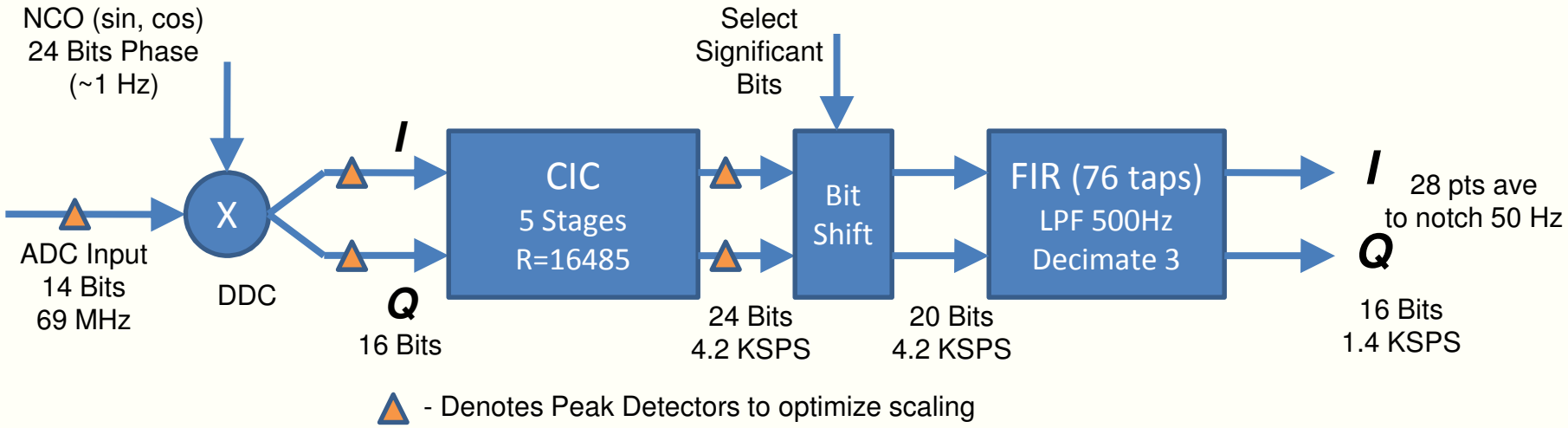
- Control Space
  - Channel delays (8)
    0 to 31 samples
  - Gate parameters (18)
    1 to ~1e6 turns
    - NB specified by start and stop turn
    - WB (8 gates) specified by start and stop turn
  - NCO frequencies (2), CIC shift (1)
    - Possibly FIR coefficients for NB or CIC decimation?
  - Specify TBT box filter –
    1st sample, number to average (2)
  - IRQ Level (1)
  - Diagnostic Peak Detectors (to monitor saturation) each 32 bit register
    - Peak Detectors record max value at each stage for last injection (Reset & Latch from DAQ SM)
    - ADC Inputs (8), IQ stage (32), CIC stage (32)

- Internal RAM (16) 32bits by up to 1024 samples (512kbits)
  - Store I,Q for each channel 31:16 Q, 15:0 I
  - Map each RAM directly to VME
- Store SumI, SumQ for each I,Q channel in 32 contiguous registers
  - Sum will be a multiple of 50 Hz (28 pts out of NB)
- DDR RAM (8 pages)
  - Raw ADC data for each channel stored in contiguous pages
  - To save VME addresses, just map single page to VME (size?)
    - One bank for raw data -> RAM mapped to VME
    - Treat ADC data as 16 bits -> (31:16 sample2 15:0 sample 1)
  - TBT data will have separate address space from raw – up to 4096 turns
    - Read 32 samples/turn from RAM and process (DDC and average)
    - Provide 16 bit result for I,Q (31:16 Q, 15:0 I) per turn

Narrowband Signal Processing

- **Design footprint for 8 ADC channels**
  - 2 NCOs for beam and cal frequencies -> 16 DDCs
  - 32 CIC Filters operating at 6 9 MHz
    - 5 stage CIC uses 13 k LEs and <1% of RAM
  - 1 Serial FIR Filter will process all 32 CIC Filter outputs
    - 76 tap FIR (400 Hz BW, 500 Hz Stop, -120 db stopband)
    - Decimate by 3 to 1.4 KSPS output

- **General Design Considerations**
  - For 256 pts get 183 msec data points
    - *I,Q* will be read out and magnitude/position calculations done in the VME CPU
    - 32 *I,Q* pairs x 16 bits x 256 pts = 128 kbits of memory
    - with Cyclone III (3 Mbits memory), 1024 pts should be ok => full cycle!
  - Provide average in realtime for single *I,Q* readback
    - Average a multiple of 28 to remove 50Hz

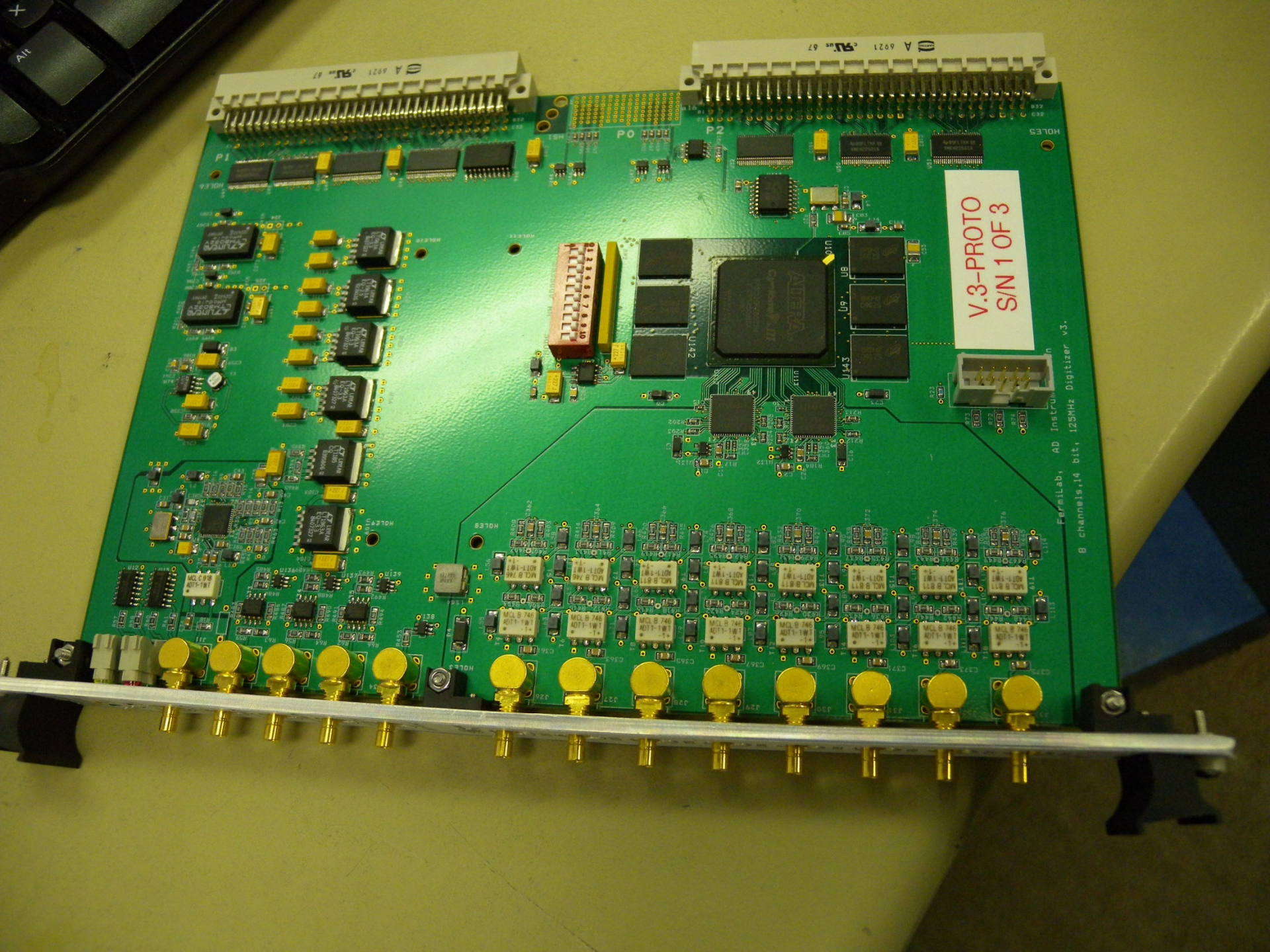


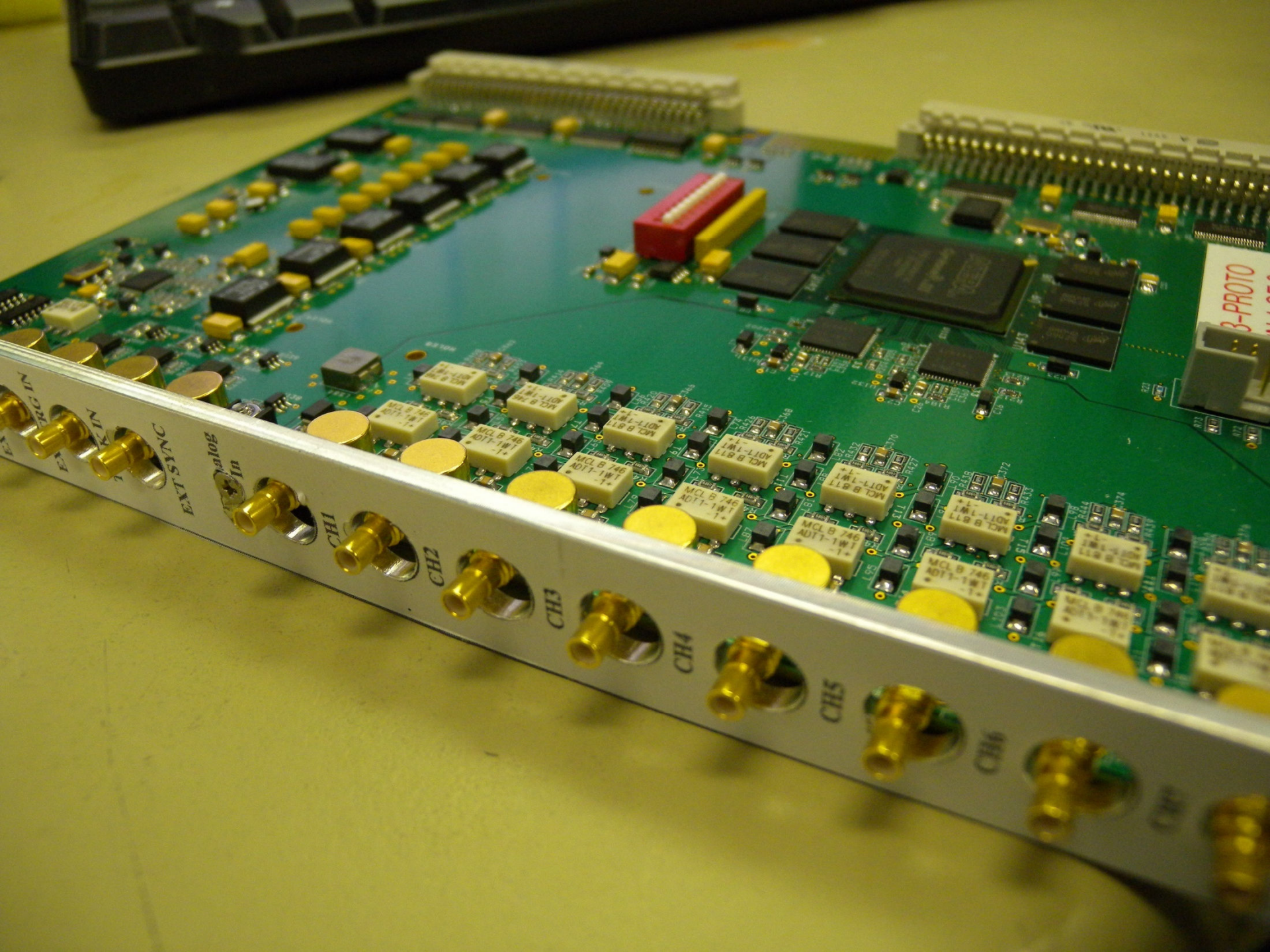
Memory Usage

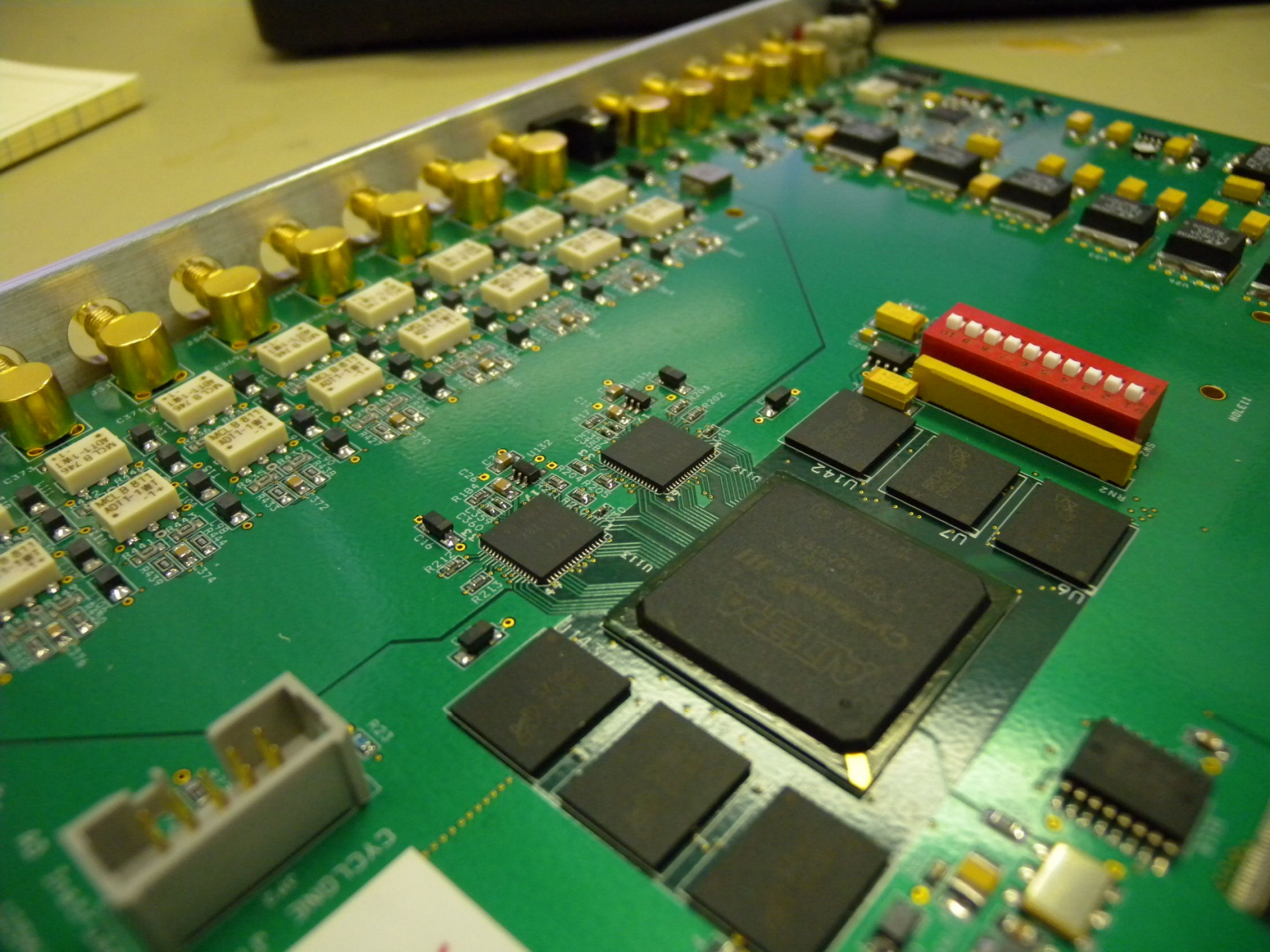
- Would like to write raw ADC data to memory on every trigger
  - Require (14bits)x(8ch) @ 70 MSPS
  - 16K turns results in 1MByte/channel
  - 16MByte/channel available -> 260K turns (~120ms)
  - Can be segmented to record different portions of cycle
- For TBT, will use simple average of N samples per turn
- On TBT data request, raw data will be read from the memory and processed
  - Simplifies writing into memory and reduces rate requirement
  - TBT readback will be limited by network so additional readout time in the front-end will be negligible
- Would also like to write narrowband data to memory on every trigger
  - Require (16bits)x(8ch)x(4) @ ~ few kHz
  - Simple solution is to store this data in FPGA if resources permit
  - 512kbits allows storing NB for entire cycle!

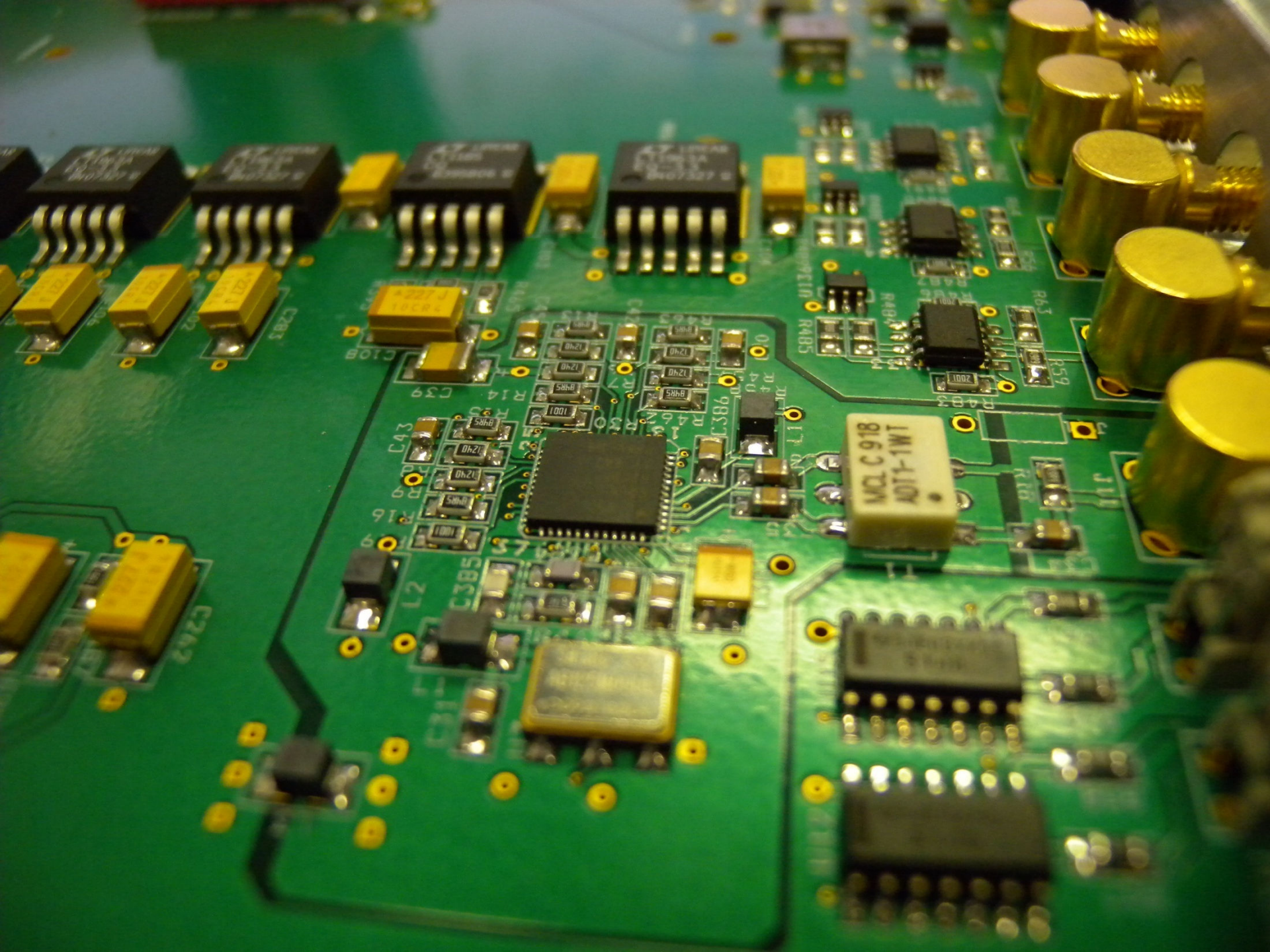
FPGA Design Implementation

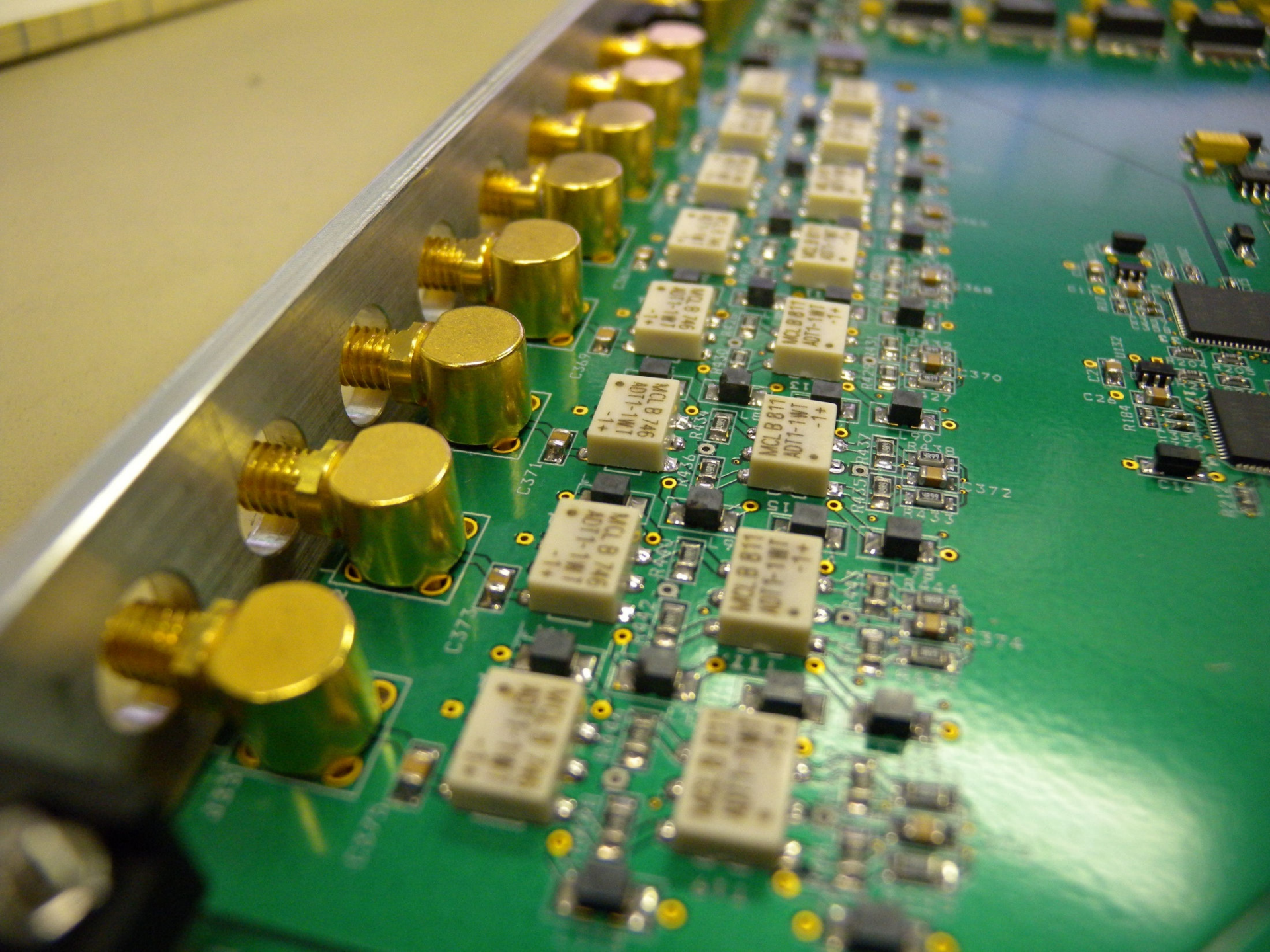
- Initial FPGA draft design
  - FPGA allows modifications & changes simply by change of firmware
- Need to discuss exact specification, to further adapt the final FPGA design implementation
- Your feedback is needed to flesh out the specifications!

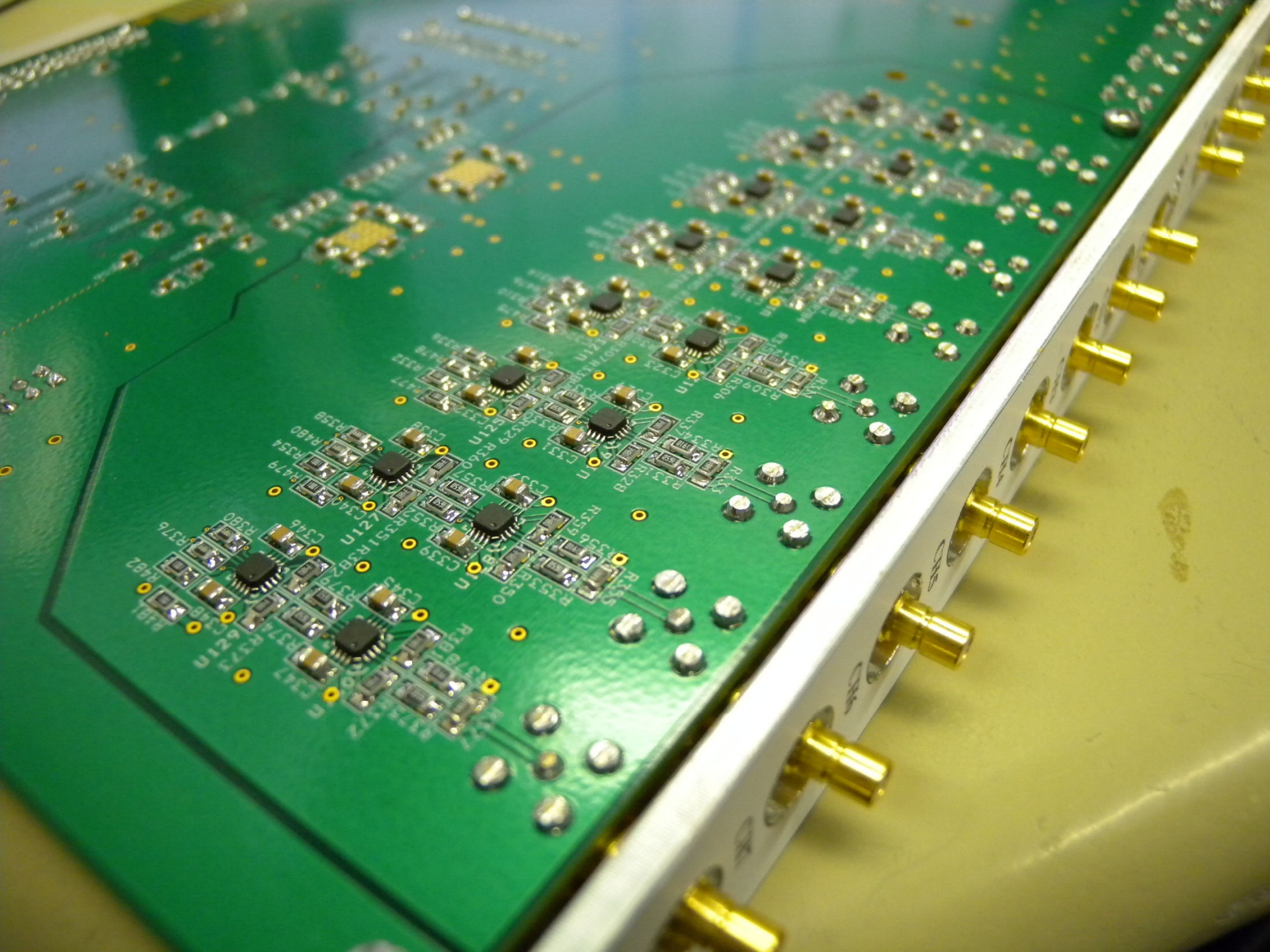

V.3-PROTO
S/N 1 OF 3
P0
P1
P2
FermiLab, AD Instrum
8 channels,14 bit, 125MHz Digitizer v3.


EXT SYNC
Analog In
CH1
CH2
CH3
CH4
CH5
CH6


U142
U7
U6
CYCLONE


MQLC918
ADT1-1WT

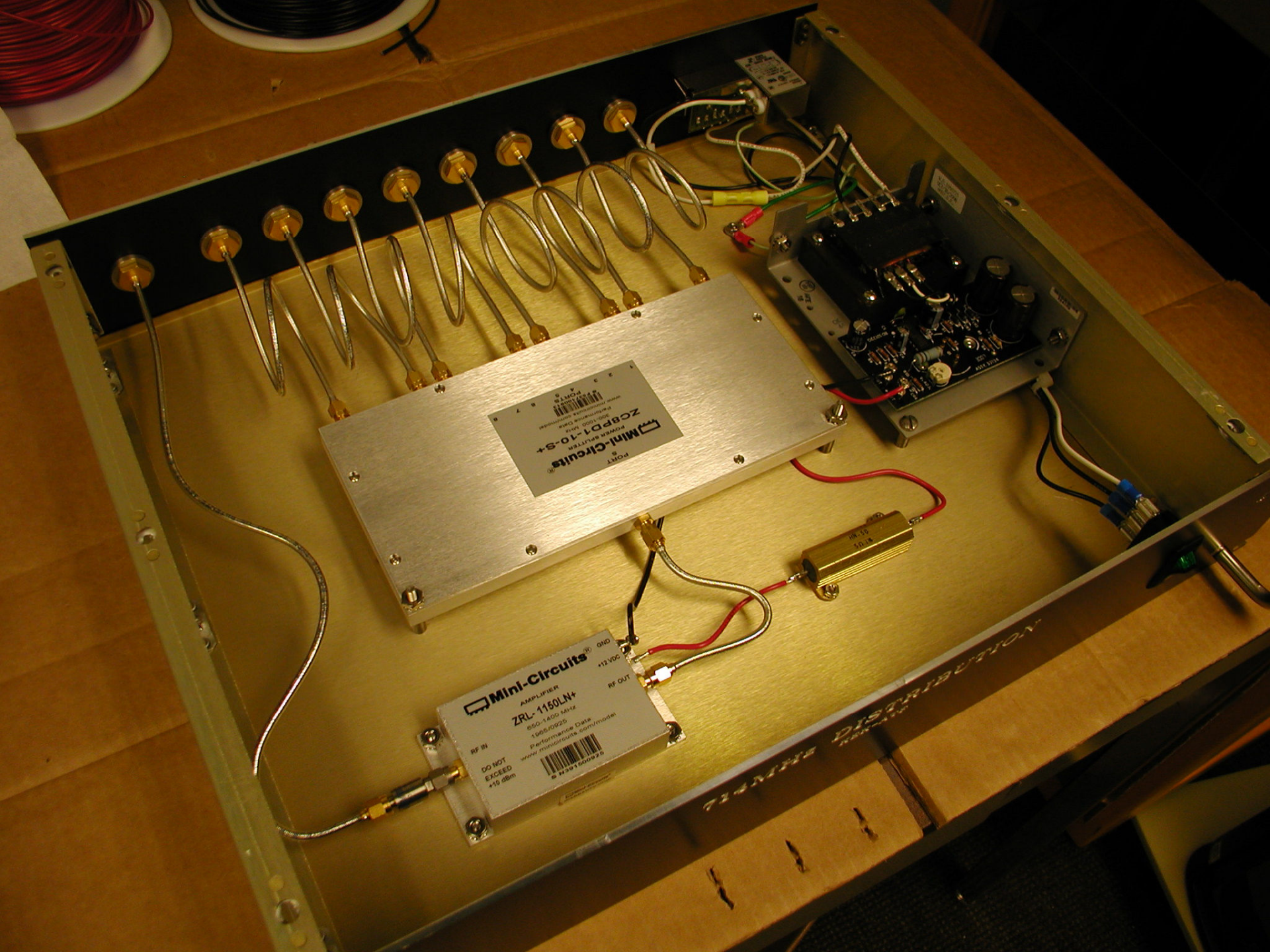

MCL B 746
ADT1-1WT
MCL B 811
ADT1-1WT



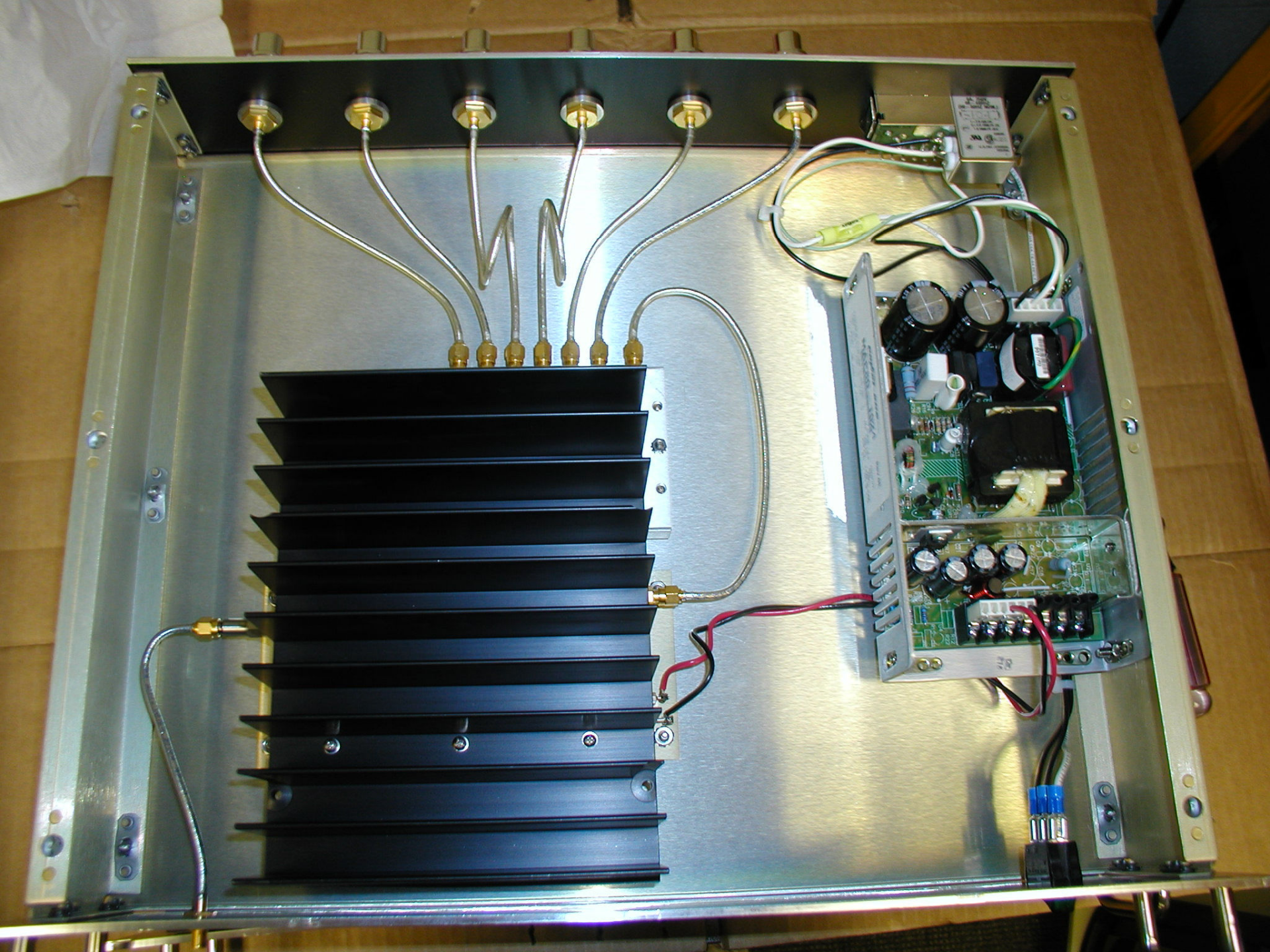
Next Steps…

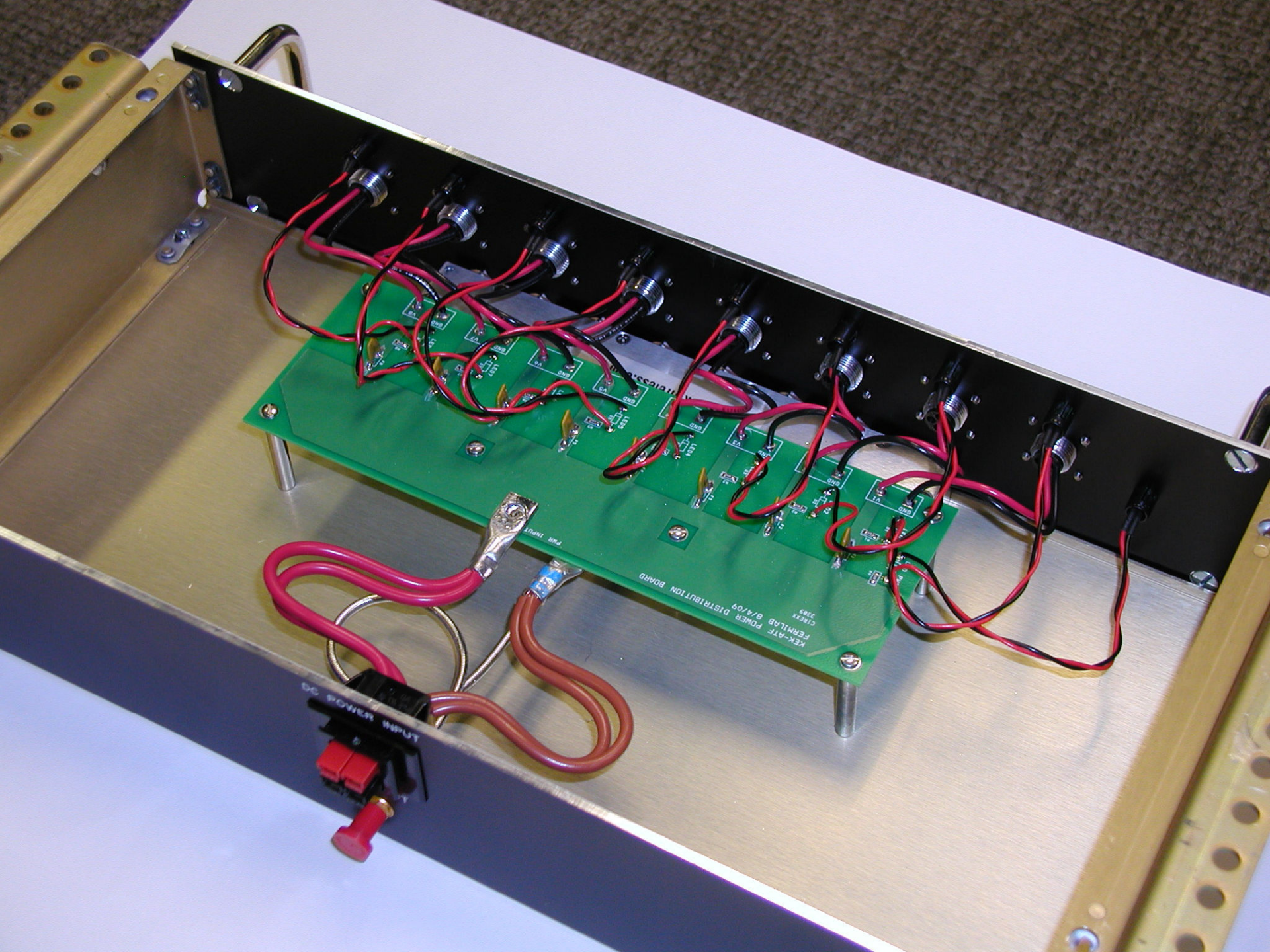
- Installation of infrastructure hardware in the ATF tunnel
  - October 2009: DC and LO distribution boxes, DC-, LO-, and CAN-bus cabling, prepare BPM electronics racks
- Electronics series production & testing
  - October 2009: finalize downconverter and digitizer PCB layouts, order missing parts for series production, finalize prototype testing
  - Fall 2009: Series production of downconverters & digitizer, re-production of 6 timing modules
  - Winter 2009: testing of all electronics modules, integrated system test
- Software / firmware
  - Development of the FPGA digitizer firmware
  - Integration of the digitizer into VxWorks (driver, EPICS interface)
- System installation
  - Spring 2010: Installation and commissioning of the complete BPM read-out system
  - Beam studies and test on the upgraded ATF DR BPMs


714MHz DISTRIBUTION
OUTPUTS
1
2
3
4
5
6
7
8
INPUT
S/N 2


Mini-Circuits
AMPLIFIER
ZRL-1150LN+
650-1400 MHz
Performance Data
www.minicircuits.com/model
RF IN
DO NOT
EXCEED
+15 dBm
GND
+12VDC
RF OUT
Mini-Circuits
POWER SPLITTER
ZC8PD1-10-S+
Performance Data
POWER


729MHz L.O. DISTRIBUTION
KEK-ATF
INPUT
GAIN: 15 dB
729MHz L.O. DISTRIBUTION
KEK-ATF
INPUT
GAIN: 15 dB
729MHz L.O. DISTRIBUTION
KEK-ATF
INPUT
GAIN: 15 dB
729MHz L.O. DISTRIBUTION
INPUT

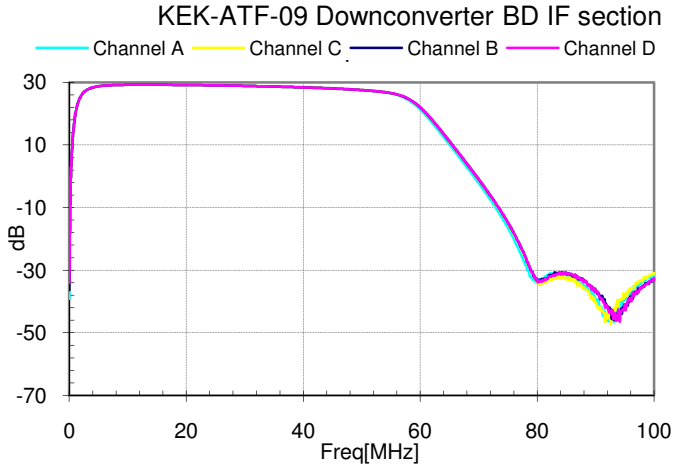


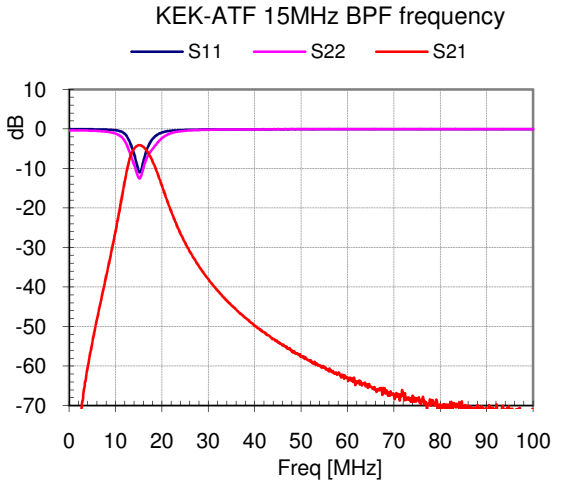

DC POWER INPUT
KEK-ATF POWER DISTRIBUTION BOARD
FERMILAB 8/4/09

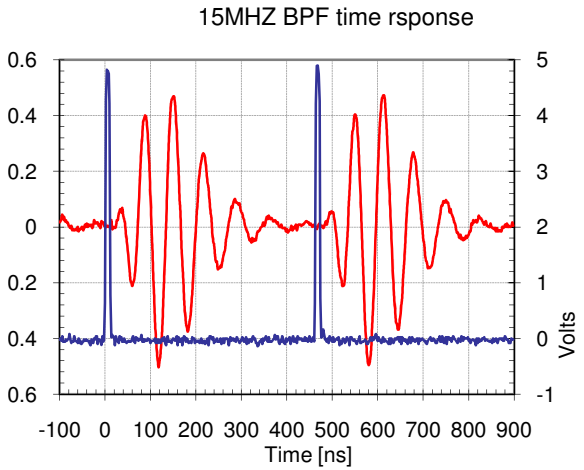

SAFETY WIRES
LAMBDA

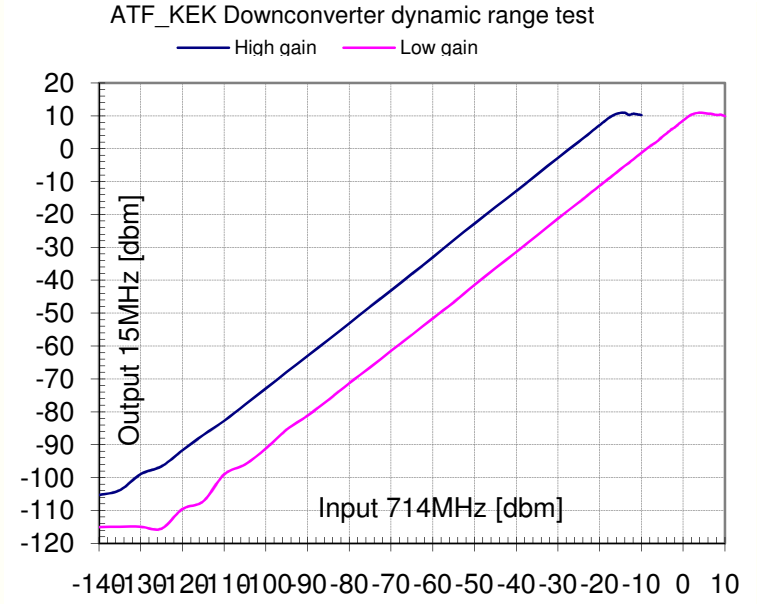
Backup

Analog Downmixer



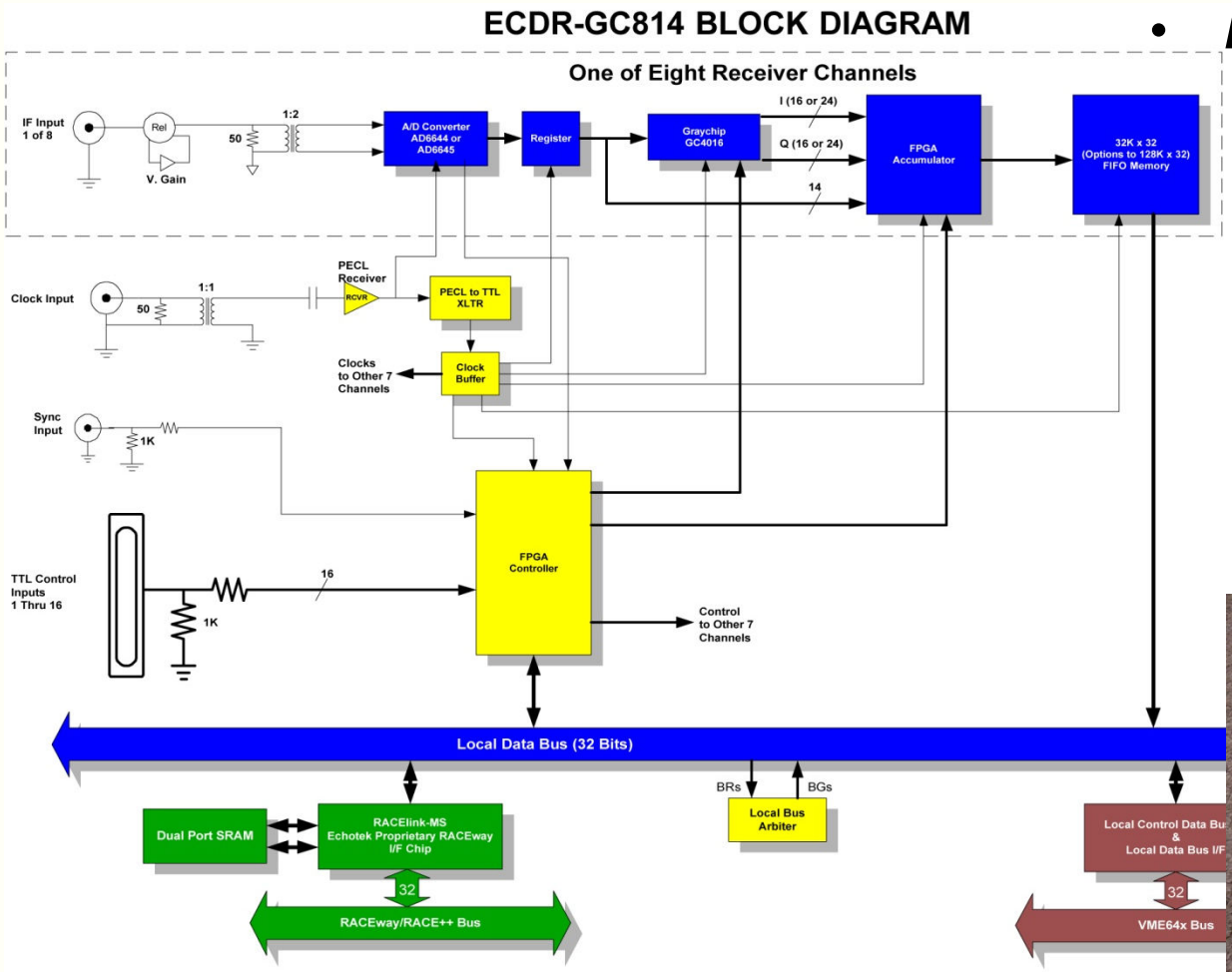




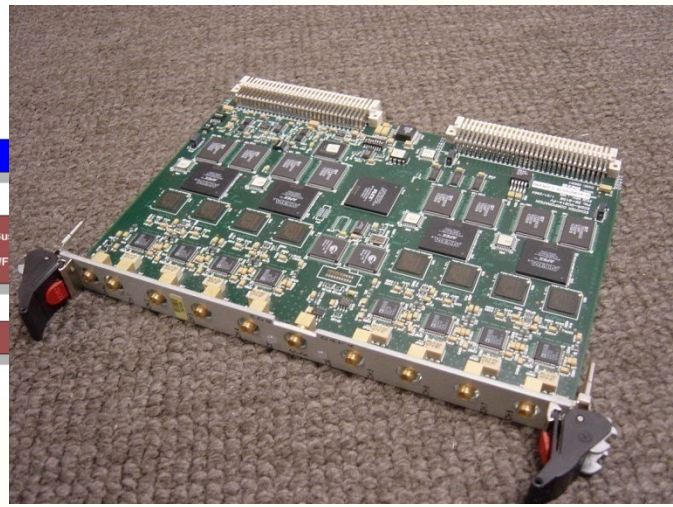


- **Modified IF section**
  - **Low-noise gain stage**
  - **15.1±1.5 MHz BPF, ~400 ns ring-time**
- **Improved NF & dynamic range**
  - **NF = 17 dB (?)**
  - **>90 dB dynamic range**

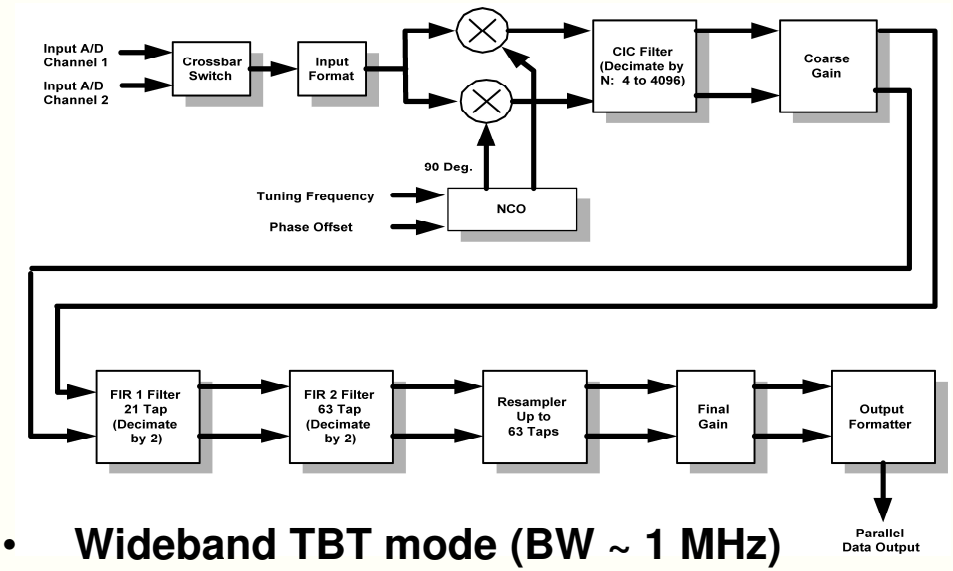
Digital Signal Processing



- ***Echotek*** **digital receiver**
  - **8-ch VME64x module**
  - ***Analog Devices*** **14-bit 105 MS/s AD6645**
  - **Each ADC channel: *Texas Instruments* 4-ch GC4016 "*Graychip*" digital downconverter**
  - **128 kWord FIFO**

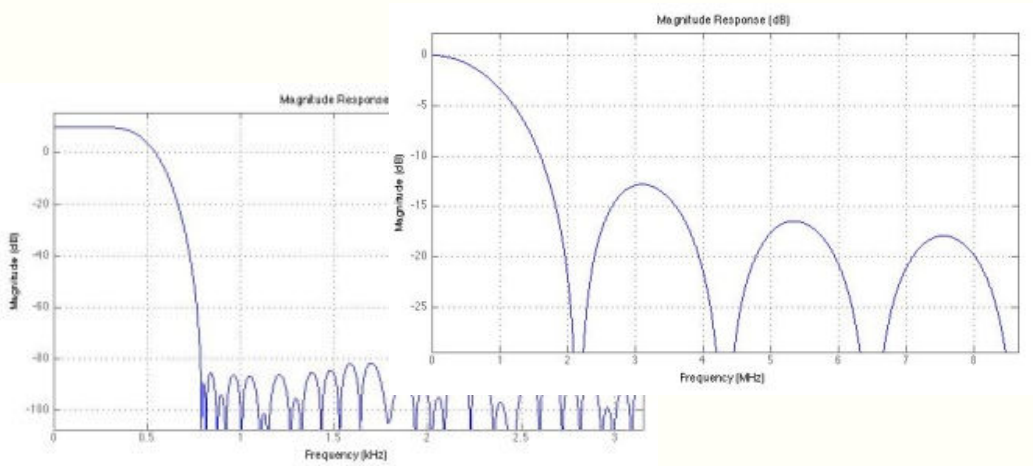


Digital Signal Processing (cont.)



- *Graychip* digital downconverter
  - 4 independent channels per ADC
  - NCO set to f_{IF} = 15.145 MHz (downconvert to DC baseband)
  - ADC clock set to 32 samples per revoltion: f_{CLK} = 32 x f_{rev} = 69.2 MHz
  - Decimation and filtering for wide- and narrowband mode using CIC and FIR digital filters
  - Simultaneous DDC operation of beam and calibration signals!

- Wideband TBT mode (BW ~ 1 MHz)
  - 5 stage CIC: decimate by 4
  - CFIR: 7-tap boxcar, decimate by 2
  - PFIR 1-tap, no decimation
- Narrowband mode (BW ~ 500 Hz), t_{dec} = 158.7 μs, 1280 pt (~200 ms)
  - 5 stage CIC: decimate by 2746
  - CFIR: 21-tap RRC, decimate by 2
  - PFIR: 63-tap RRC, decimate by 2

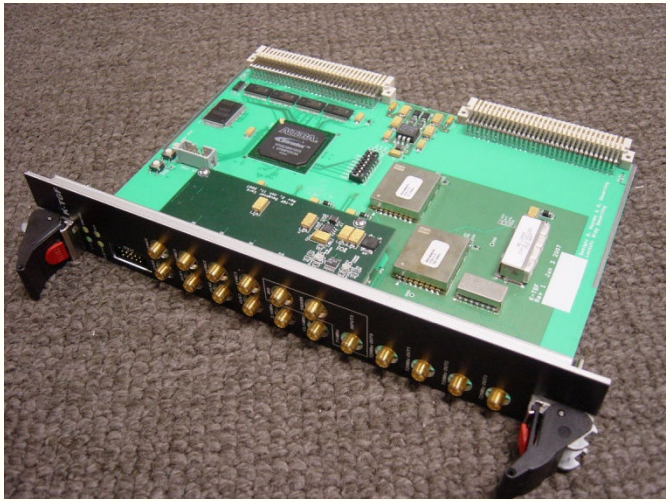


NB mode PFIR response

WB CFIR response

Other Hardware

- **VME Timing module:**
  - $f_{CLK} = f_{RF}*32/330 = 69.236$ MHz clock signals (4x)
  - $t_{rev} = 462.2$ ns turn marker signals (4x), 0…115 double-buckets (2.8 ns) delayable
  - To f_{RF} phase-locked $f_{LO} = 729.145$ MHz
  - Auxiliary f_{rev} and f_{IF} signals
- ***Motorola* 5500 VME CPU:**
  - Data collection and normalization
  - Box-car post-processing filter (20 ms)
  - Local diagnostic and control software
  - EPICS control interface



- **Calibration & remote control unit (prototype):**
  - To f_{RF} phase-locked $f_{CAL} \approx 714$ MHz (*Analog Devices* ADF4153)
  - In-passband, through button-BPM, or reflected signal calibration
  - 2nd and 3rd *Graychip* channels for CAL signal downconversion
  - CAN-bus remote control functions (attenuation, gain, PLL freq., etc.)

Calibration Details

- **Calibration tone frequencies:**
  - f_{CALx} = 713.6 MHz
  - f_{CALy} = 714.4 MHz
- **Calibration procedure:**
  - **Correction values:**

$$A_{Corr} = \frac{A_{CAL} + B_{CAL} + C_{CAL} + D_{CAL}}{4A_{CAL}} \qquad B_{Corr} = \frac{A_{CAL} + B_{CAL} + C_{CAL} + D_{CAL}}{4B_{CAL}}$$

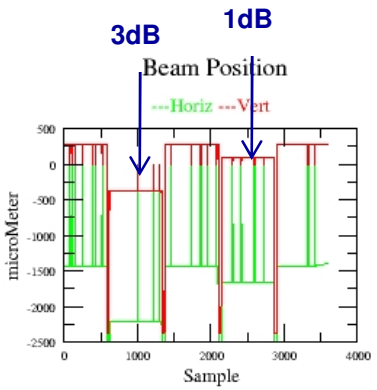
$$C_{Corr} = \frac{A_{CAL} + B_{CAL} + C_{CAL} + D_{CAL}}{4C_{CAL}} \qquad D_{Corr} = \frac{A_{CAL} + B_{CAL} + C_{CAL} + D_{CAL}}{4D_{CAL}}$$

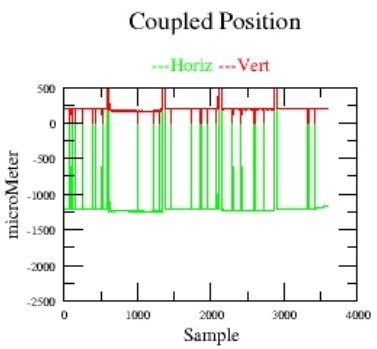
  - **Corrected beam positions:**

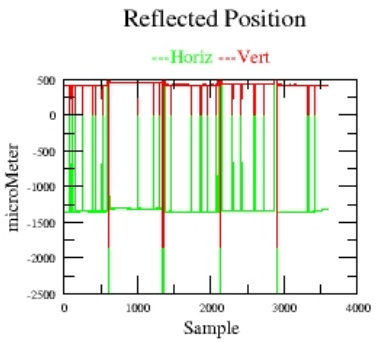
$$\phi_{Hcorr} = \frac{(A\,A_{Corr} + D\,D_{Corr}) - (B\,B_{Corr} + C\,C_{Corr})}{A\,A_{Corr} + B\,B_{Corr} + C\,C_{Corr} + D\,D_{Corr}}$$

$$\phi_{Vcorr} = \frac{(A\,A_{Corr} + B\,B_{Corr}) - (C\,C_{Corr} + C\,C_{Corr})}{A\,A_{Corr} + B\,B_{Corr} + C\,C_{Corr} + D\,D_{Corr}}$$

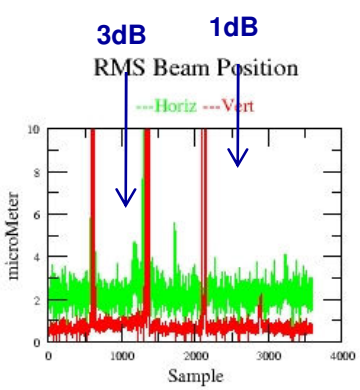
CAL System Test

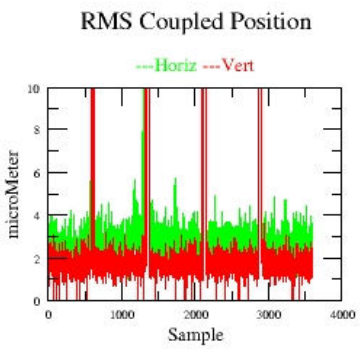


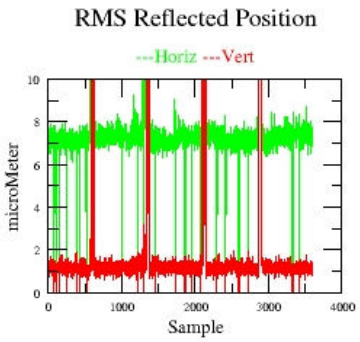




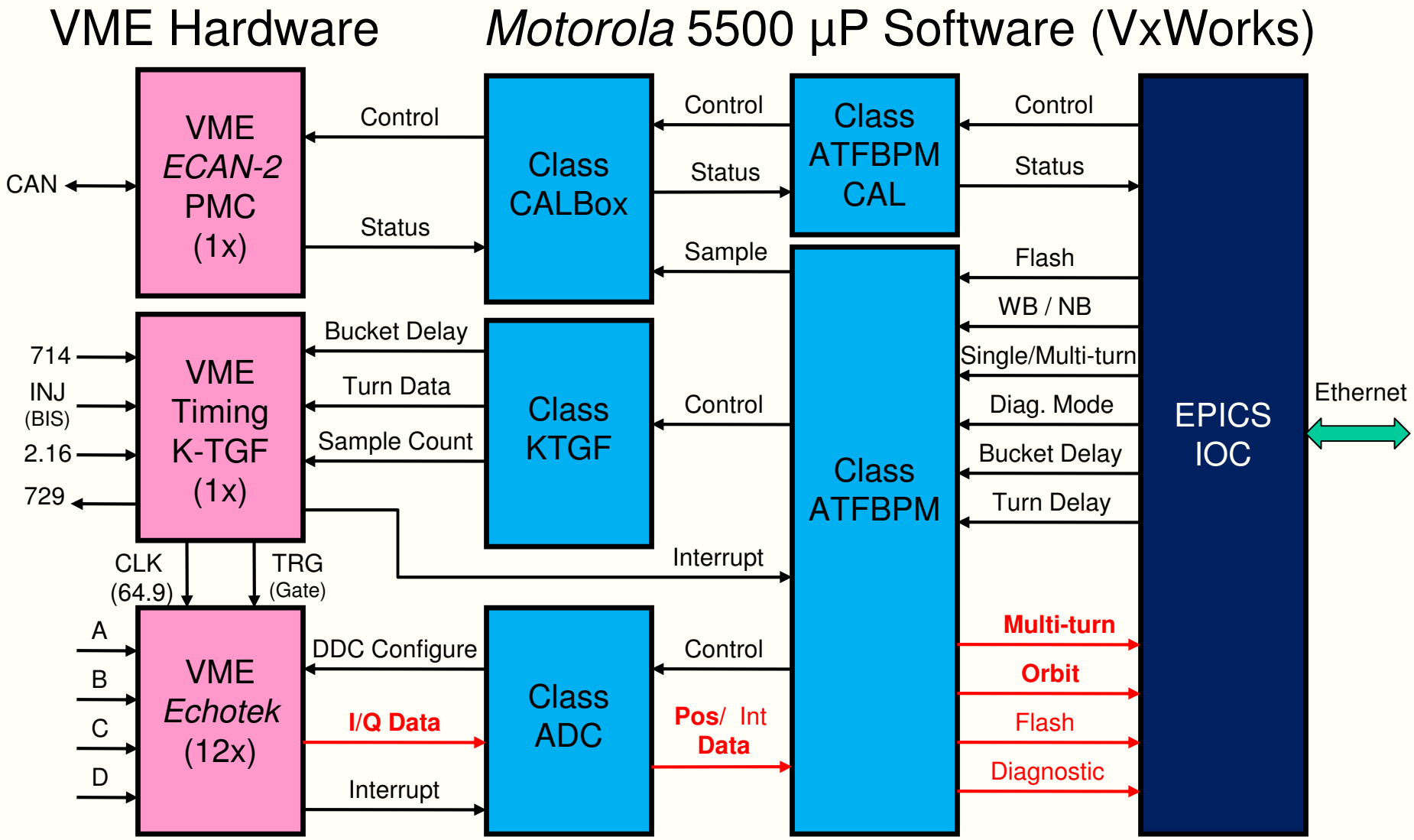
- Calibration on, datalogger on
- Comparing uncorrected, corrected (coupled-through), and corrected (reflected)
- Introduce large 3 & 1 dB gain errors.
- Automatic correction compensates the gain error almost completely!!
- Corrected beam position shows a slight increase of the RMS error (to be further studies!).







Software Components

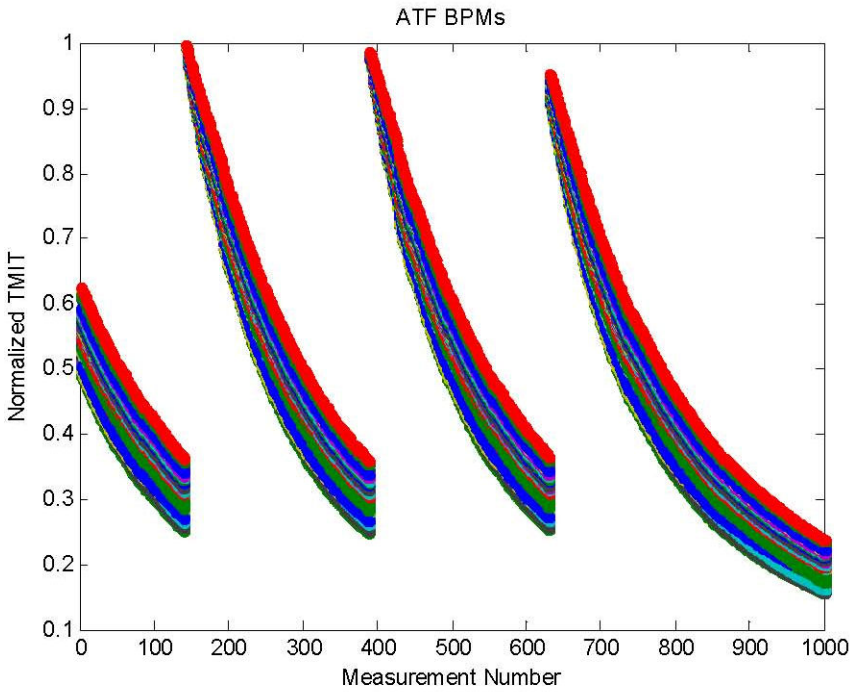


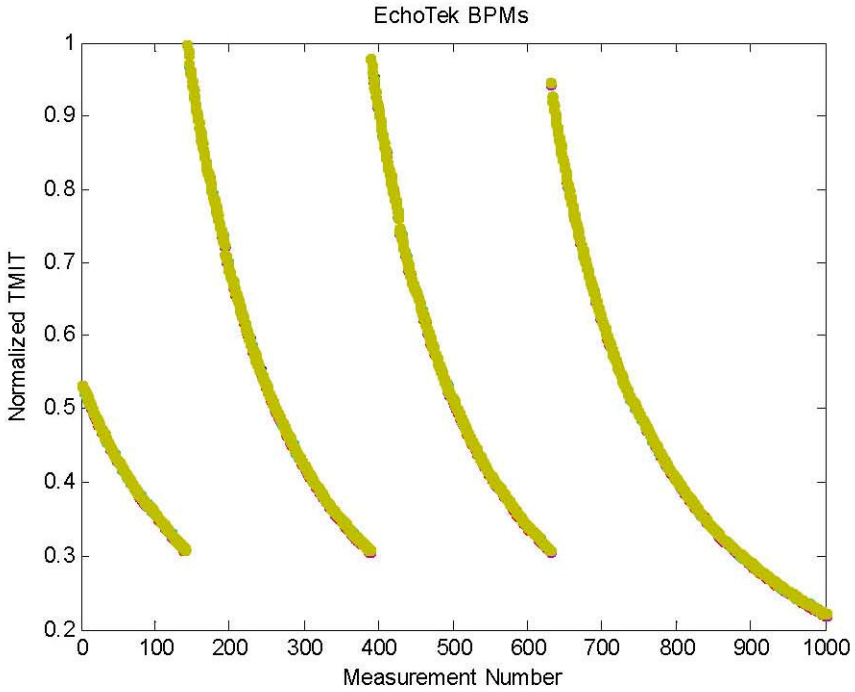
Scrubbing Mode, Intensities

070518

Fermilab

Normalized Intensities





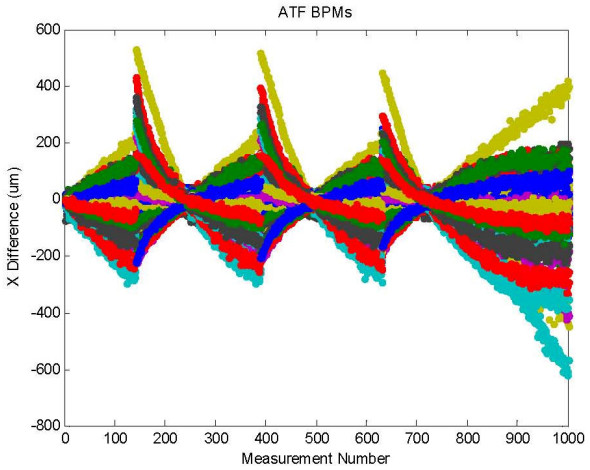
Scrubbing Mode, Positions

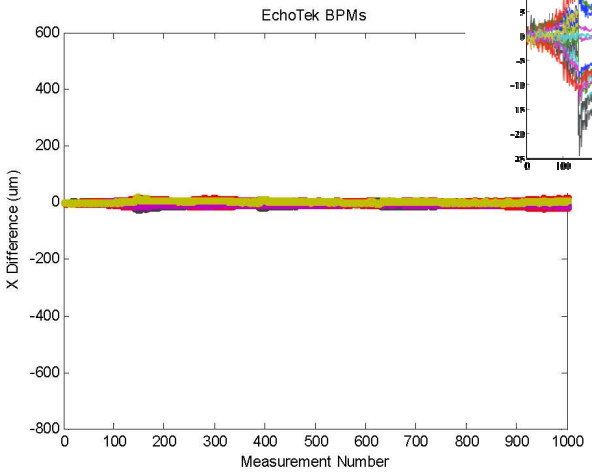
070518

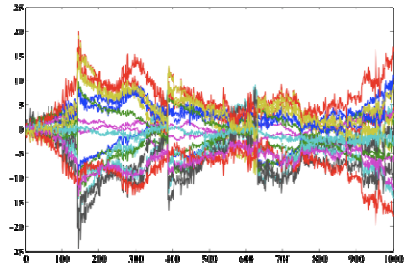
Fermilab

Horizontal Position

± 700 um



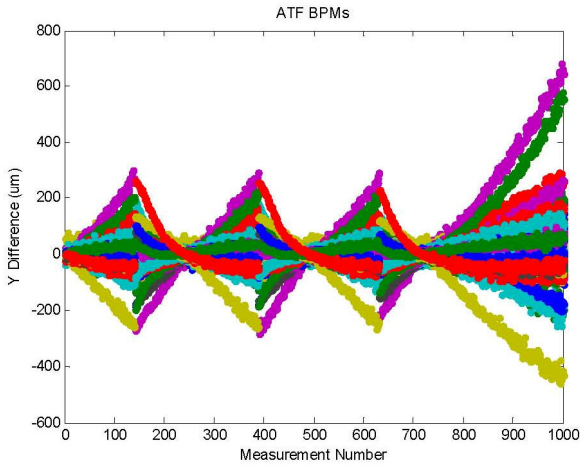


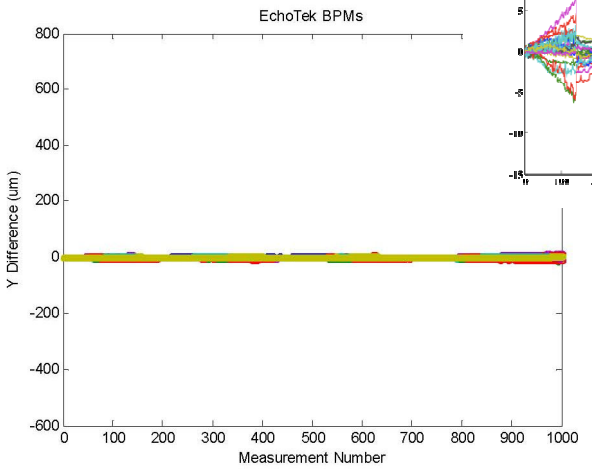


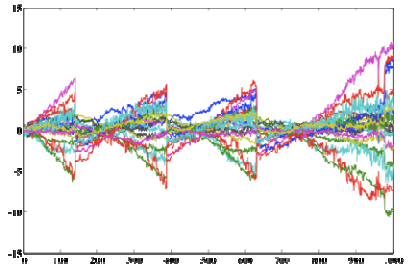
± 25 um

Vertical Position

± 700 um



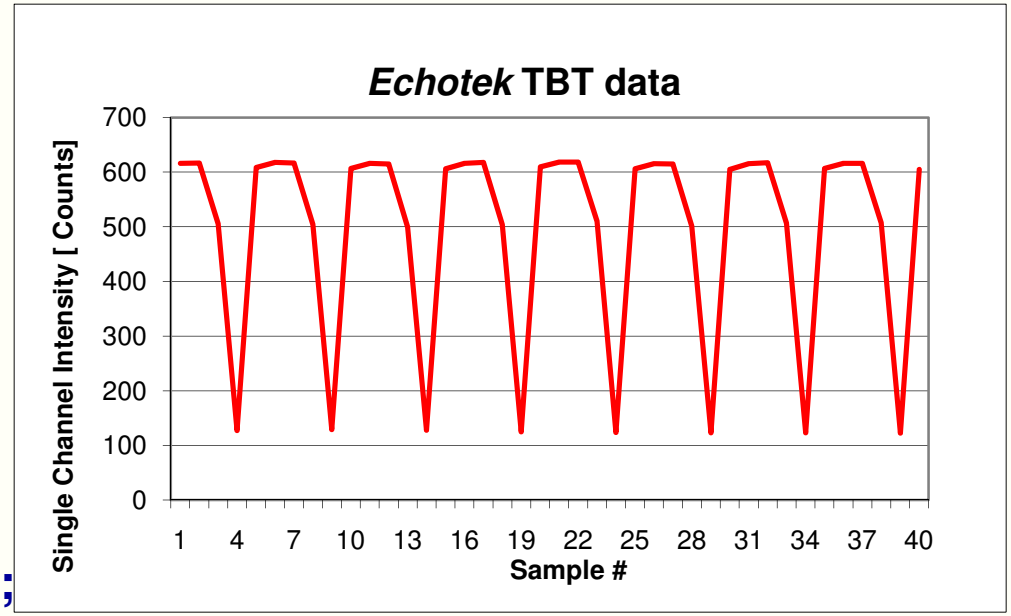




± 15 um

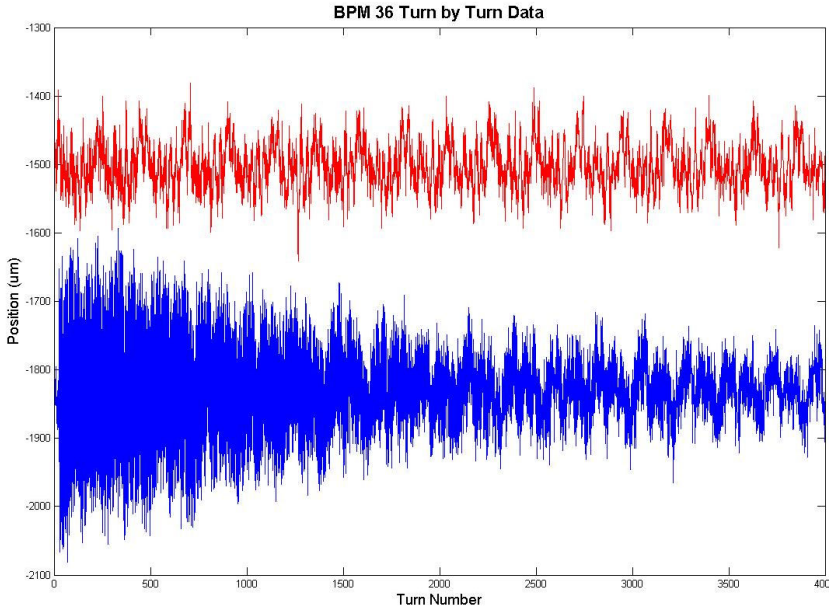
Wideband, TBT Mode Beam Tests

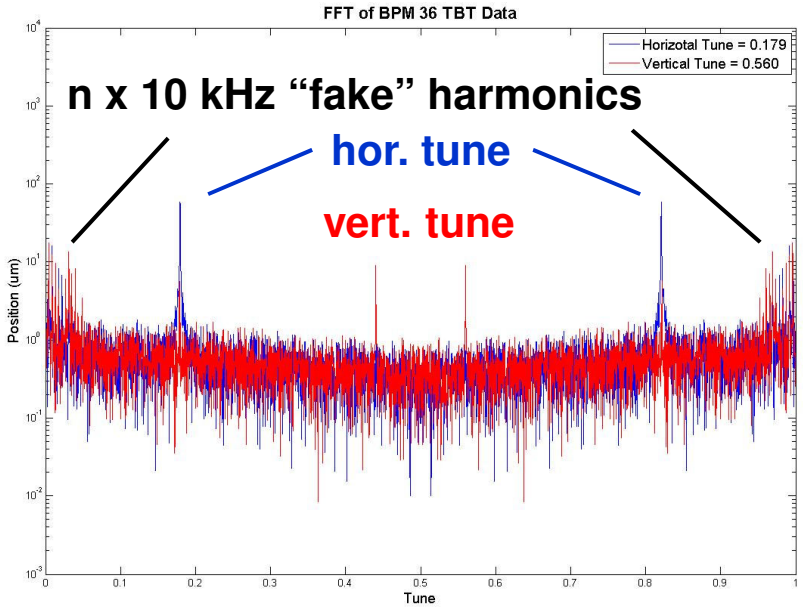
- **Several "issues" had to be resolved:**
  - **CIC & FIR digital filter impulse responses to resolve true turn-by-turn data (no "smearing")**
  - **Timing issues, e.g. channel-to-channel, as well as between BPMs and "houses" (VME crates); and of course the usual "seam" problem.**



- **In particular for the kicked beam TBT response tests:**
  - **Vertical beta at pinger is 0.5 m (12 times smaller than the horizontal one): we had to resort to injection oscillations -> lower resolution.**

Kicked Beam Tests (May 2007)





- Turn-by-Turn data BPM #36 (pinger: On)
- Identifying hor. and vert. tune lines (387 kHz, 1.212 MHz).
- Observed short time, broadband TBT resolution: few µm!
- Observation of "fake" harmonics at n x 10 kHz (not f_s), due to power supply EMI in the analog downconverter unit!

TBT Fourier Analysis

- **TBT data at the *j*th BPM following a single kick in the *z*-plane (*z* ≡ *x*, *y*):**

$$z_n^j = \frac{1}{2}\sqrt{\beta_z^j}\, e^{i\Phi_z^j}\, A_z\, e^{iQ_z(\theta_j + 2\pi n)} + c.c.$$

  - **with**

$n \equiv$ turn number , $\quad A_z = |A_z| e^{i\delta_z} \equiv$ constant of motion

$$\Phi_z \equiv \mu_z - Q_z\theta \quad \text{(periodic phase function)}$$

- **Twiss functions:**

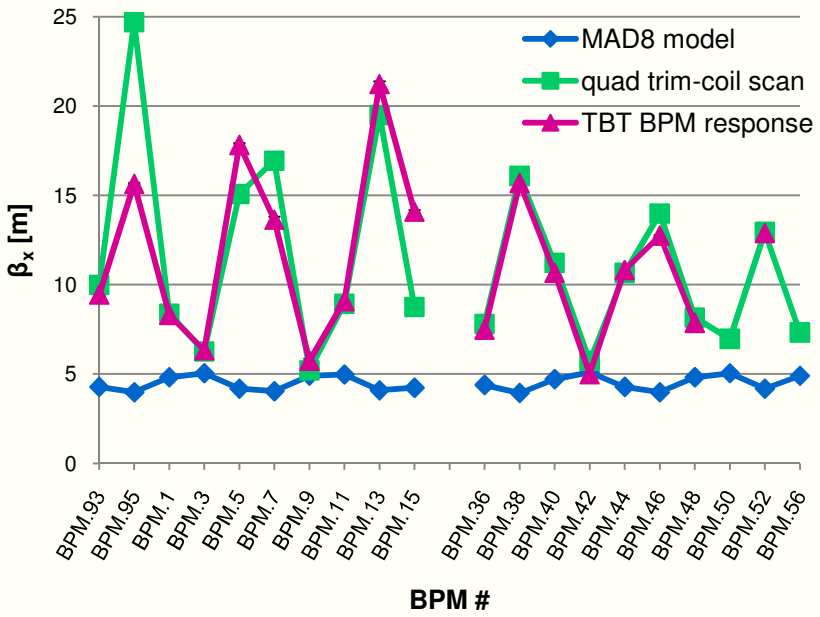
$$\beta_z^j = |Z_j(Q_z)|^2 / |A_z|^2 \qquad \mu_z^j = \arg(Z_j) - \delta_z$$

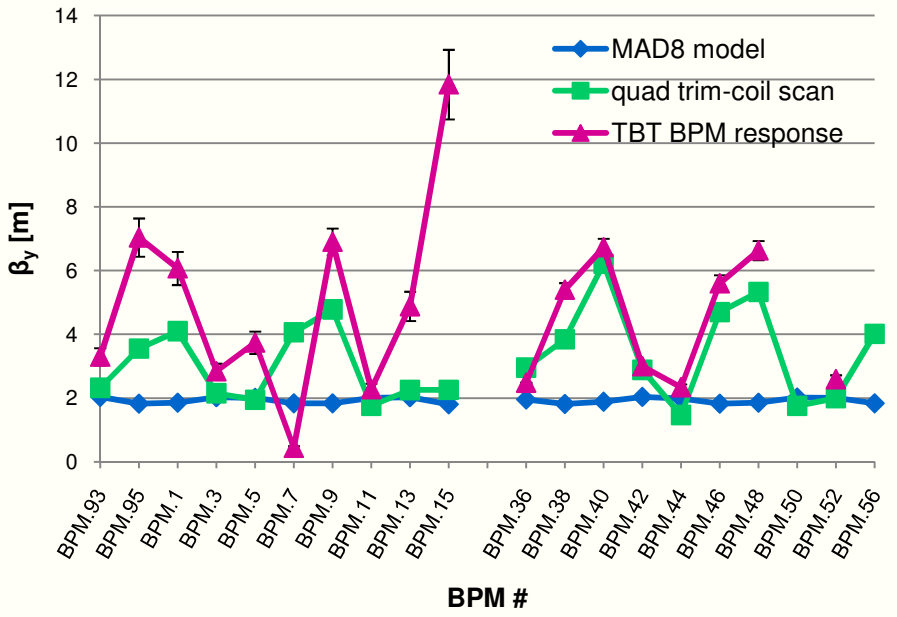
$Z_j(Q_z) \equiv$ *Fourier* component of z_j

- **Amplitude fit:**

$$|A_z|^2 = \frac{\sum_j 1/\beta_z^{0\,j}}{\sum_j 1/|Z_j(Q_z)|^2}$$

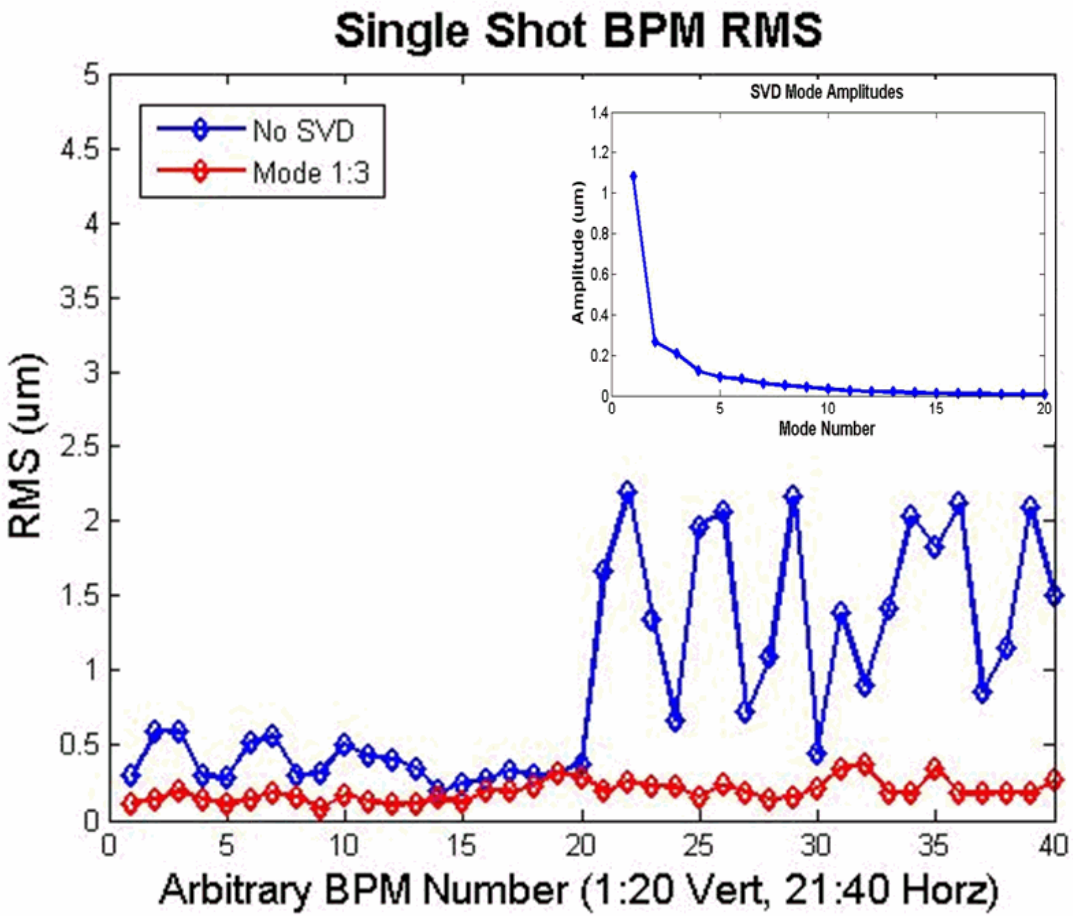
Comp.: Measurements vs. Model





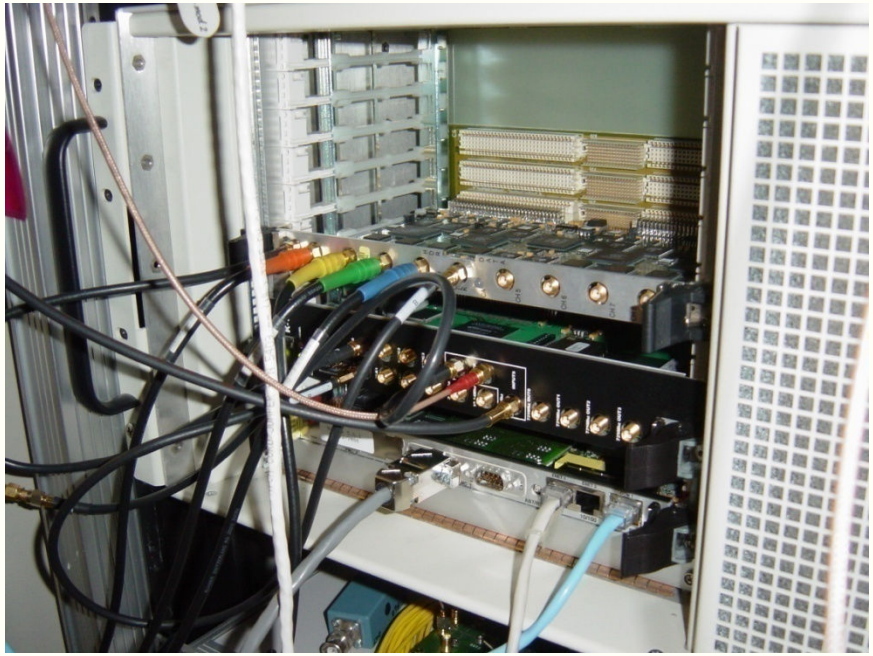
- MAD8 model (M. Woodley, marginal differences wrt. Kuroda SAD model).
- Nearby quadrupole trim coil scan (May 2008).
- TBT Fourier analysis, amplitude by fit to beta measured through trim coil scan (April 2008).

Narrowband Mode Resolution

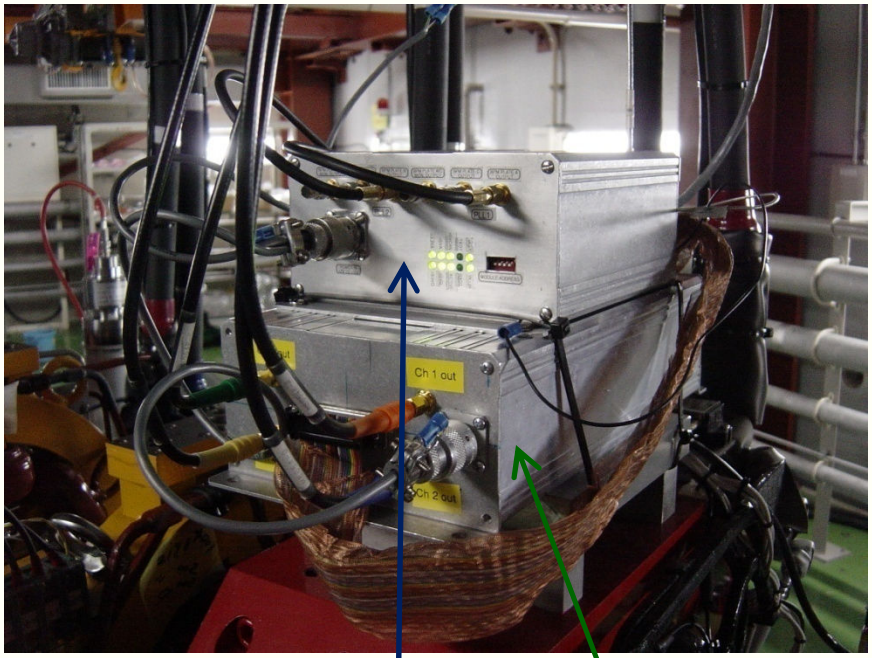


- Triggered at turn #500,000
- ~200 ms position data per shot (1280 narrowband mode BPM measurements).
- 126 tap box car filter to reject 50 Hz:
  - ~ 800 nm resolution
- SVD analysis, removing modes with hor./ vert. correlation:
  - ~200 nm resolution

Downconverter & CAL Proto



- Mini VME crate accommodating:
  - ***Motorola*** **5500 CPU**
  - **PMC CAN bus interface *ECAN-2***
  - **Timing module TGF**
  - ***Echotek*** **digital receiver module**

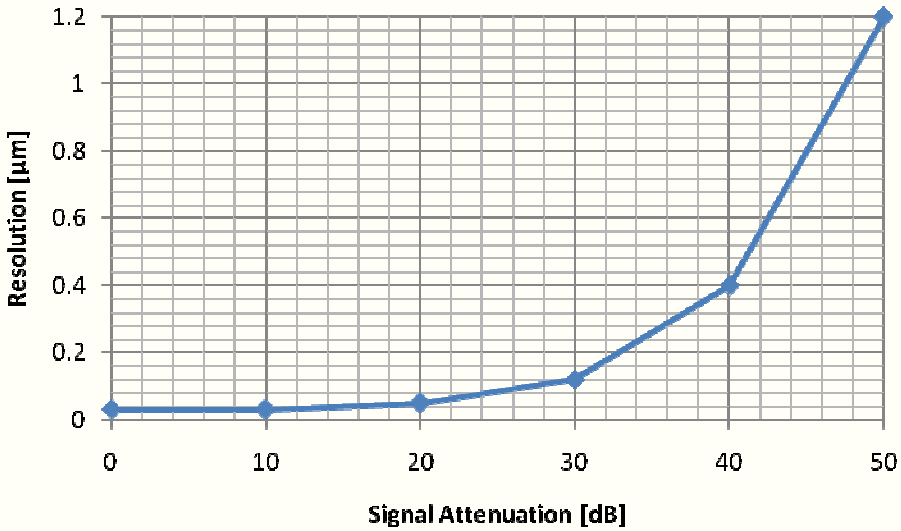


- BPM #54 prototype installation (temporary):
  - **CAN bus remote control & CAL signal PLL unit (Fermilab)**
  - **4 ch. Downconverter unit (SLAC)**

EPICS Data Acquisition

	Multi-turn	Orbit	Flash
Wide-Band	Samples: 4096 Samples/turn: 4 Turns: 1024 POSITION Intensity	Average Samples: 4096 Turns: 1024 POSITION (RMS & StdDev) Intensity (RMS & StdDev)	N^{th} Sample (1) POSITION Intensity
Narrow-Band	Samples: 1280 µsec/Sample: 158.73 Turns: 439600 POSITION Intensity	Average Samples: 126 (50 Hz Boxcar) Turns: 43273 POSITION (RMS & StdDev) Intensity (RMS & StdDev)	N^{th} Sample (1) POSITION Intensity

NB Mode Resolution Limit



Theoretical:

- ADC SNR: 75 dB
- Process gain: 40.4 dB
- NF 1st gain stage: ~ 1 dB
- CAL tone level: -10 dBm
- Splitter attenuation: 6 dB
- Effective gain: ~ 100 dB
- BPM sensitivity: 240 µm/dB
- Calculated equivalent resolution: ~ 20 nm

CAL tone resolution measurement on BPM #56: ~30 nm(!) equiv. resolution (no beam operation at ATF!, magnets off)