ILC Instrumentation R&D at SCIPP

ALCPG '09
University of New Mexico
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Bruce Schumm
Santa Cruz Institute for Particle Physics

The SCIPP/UCSC SiLC/SiD GROUP (Harwdare R&D Participants)

Faculty/Senior	Collaborator	Undergrads
Vitaliy Fadeyev	Rich Partridge	Jerome Carman
Alex Grillo		Kelsey Collier
Bruce Schumm		Jared Newmiller
		Dale Owens
		Sheena Schier
		Amy Simonis

Lead Engineer: Ned Spencer

Technical Staff: Max Wilder, Forest Martinez-McKinney

All participants are mostly working on other things (BaBar, ATLAS, biophysics…)

Students: undergrad physics and/or engineering majors at UCSC

Recent Areas of Inquiry

ILC-Specific

- SiD sensor testing
- Performance of KPIX as a tracking chip
- LSTFE front-end chip development

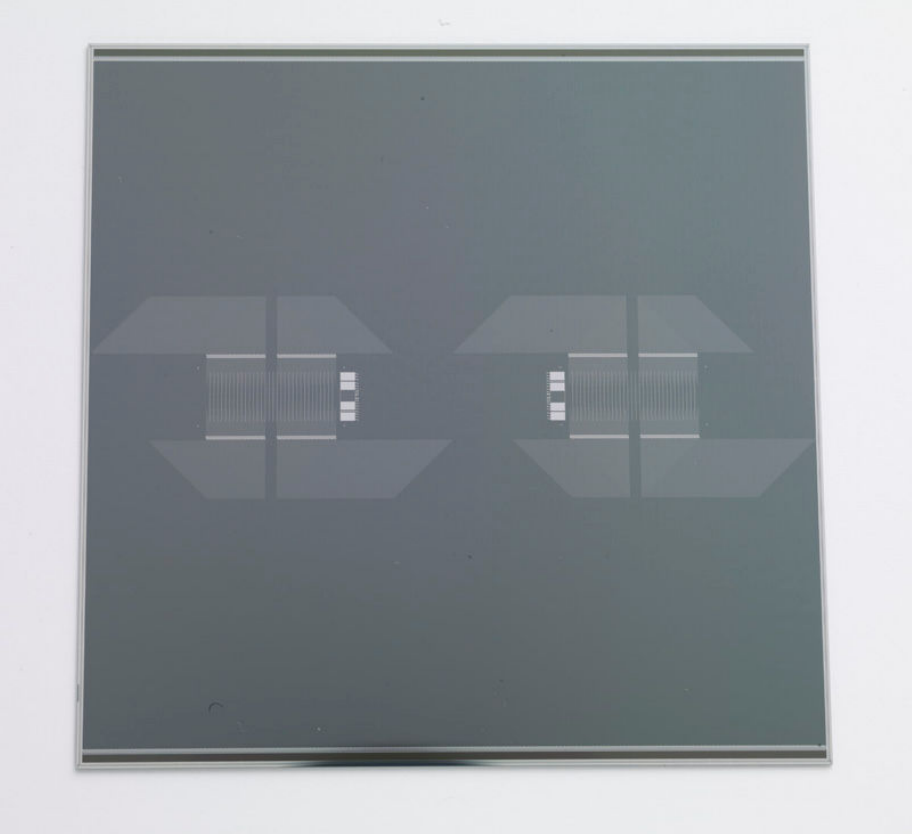
Generic

- Charge division and longitudinal resolution (see Jerome Carman talk)
- Noise sources in high-resolution limit

KPIX/DOUBLE METAL

TESTING

SiD Sensor Testing



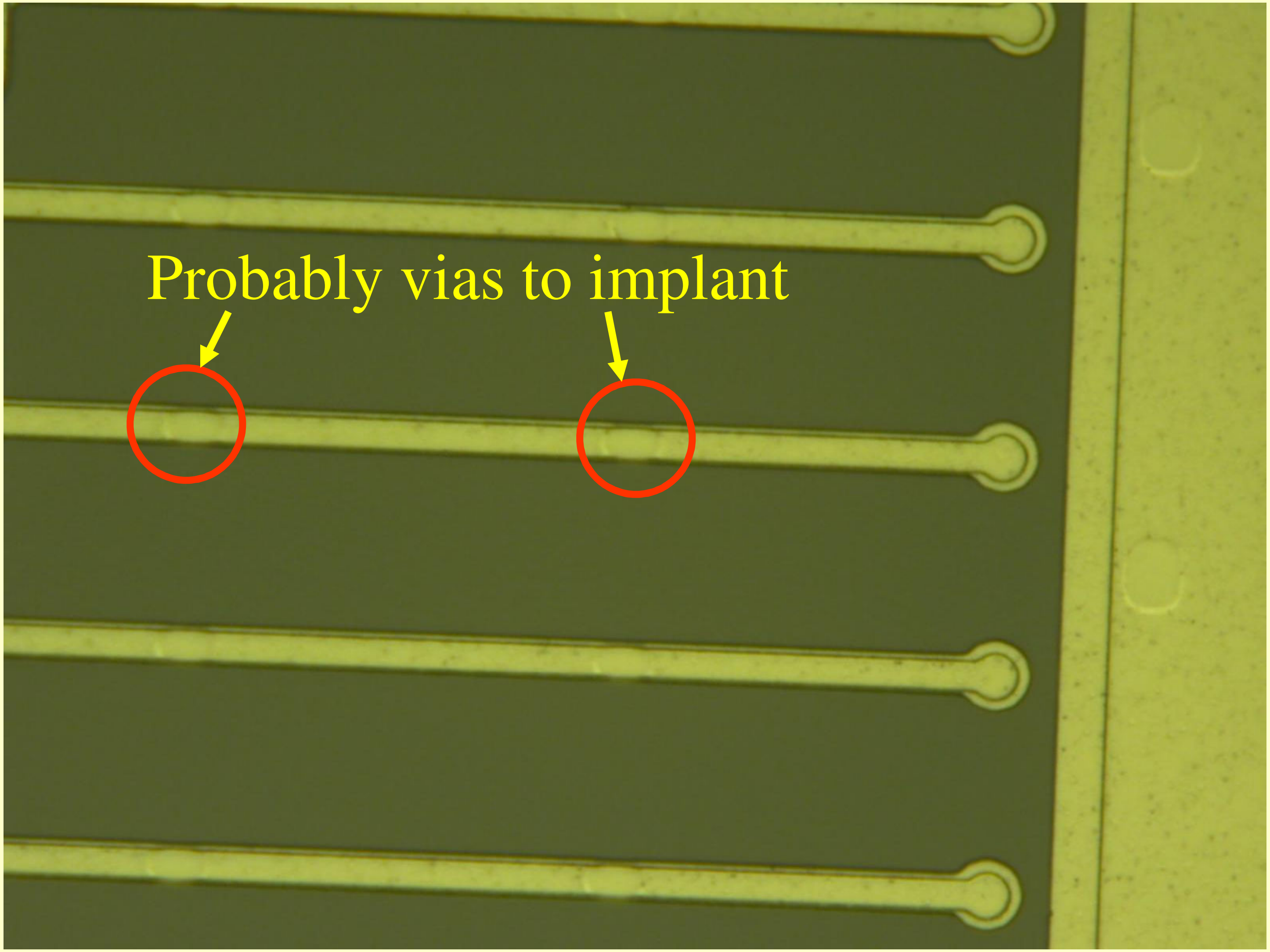
SiD 10cm x 10cm "tile" intended for "KPIX" kilo-channel bump-bond ASIC.

Resistance from strips as well as traces.

First look by SCIPP (Sean Crosby)

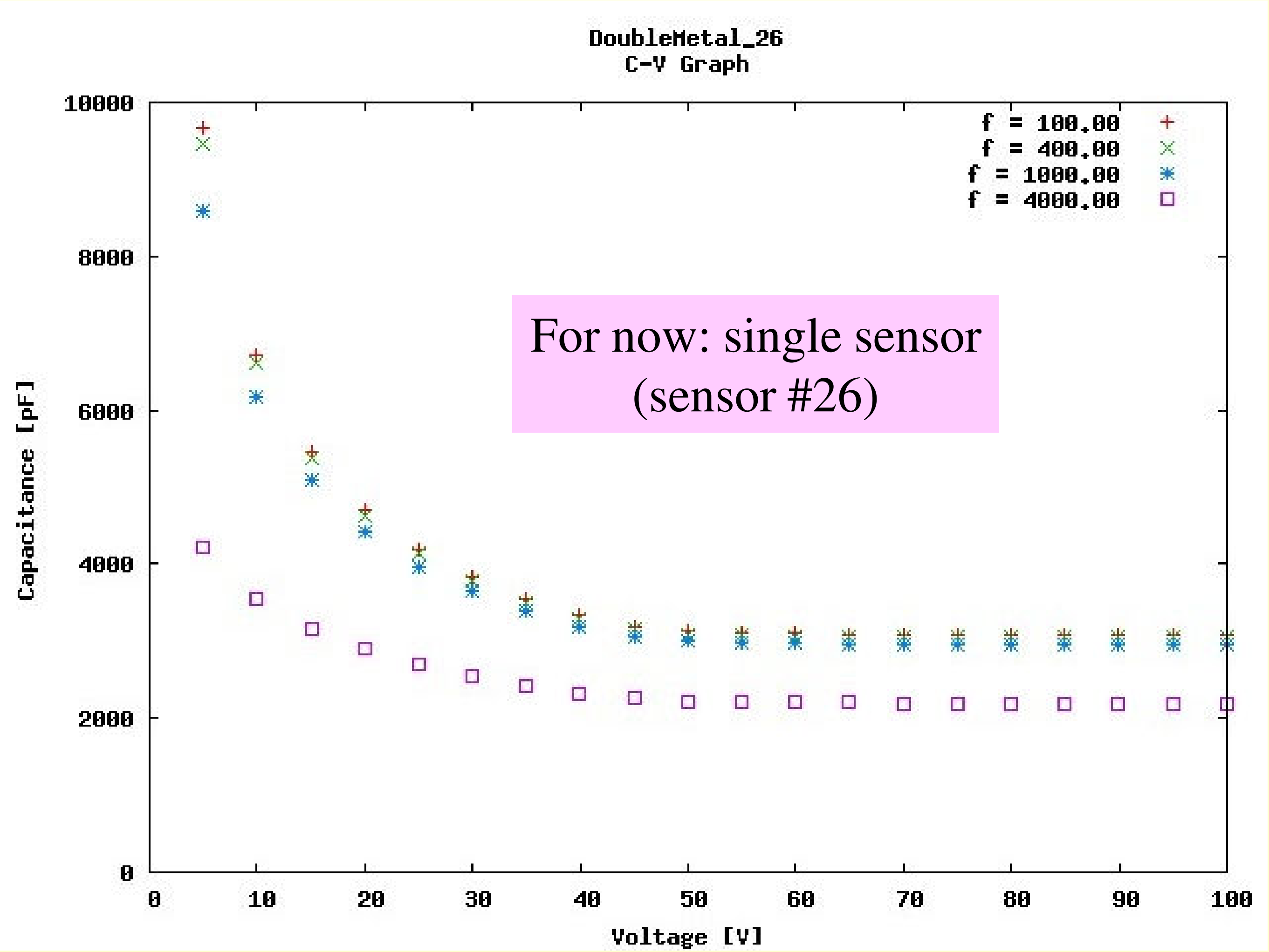
Also looked at "charge division" sensor; want to read out 600 kΩ implant at both ends; confirmed strip that shorts implant (268Ω) mistakenly added by manufacturer.
(Were able to confirm ~500KΩ implant resistance)

Magnification of SiD “Charge Division” Sensor

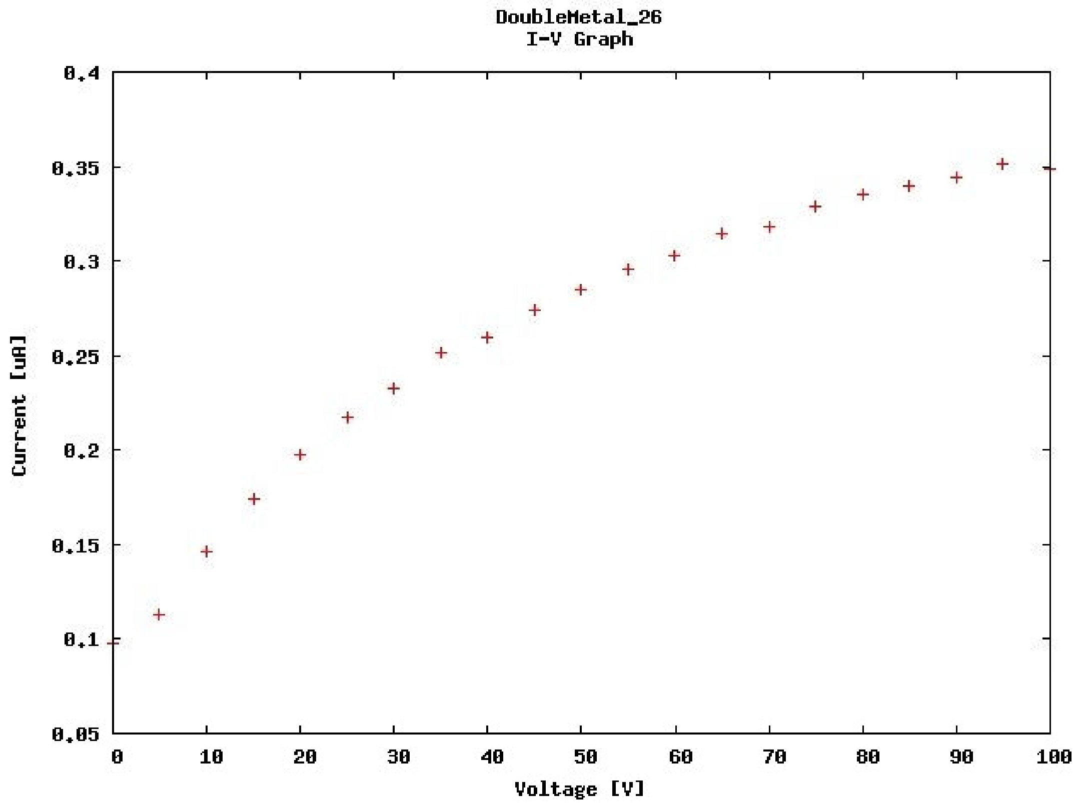


SiD Tiles: Biasing and Plane-to-Plane Capacitance

Sensors bias at ~50 V.
Capacitance shown is for all 1840 strips, but strips to backplane only



For now: single sensor
(sensor #26)



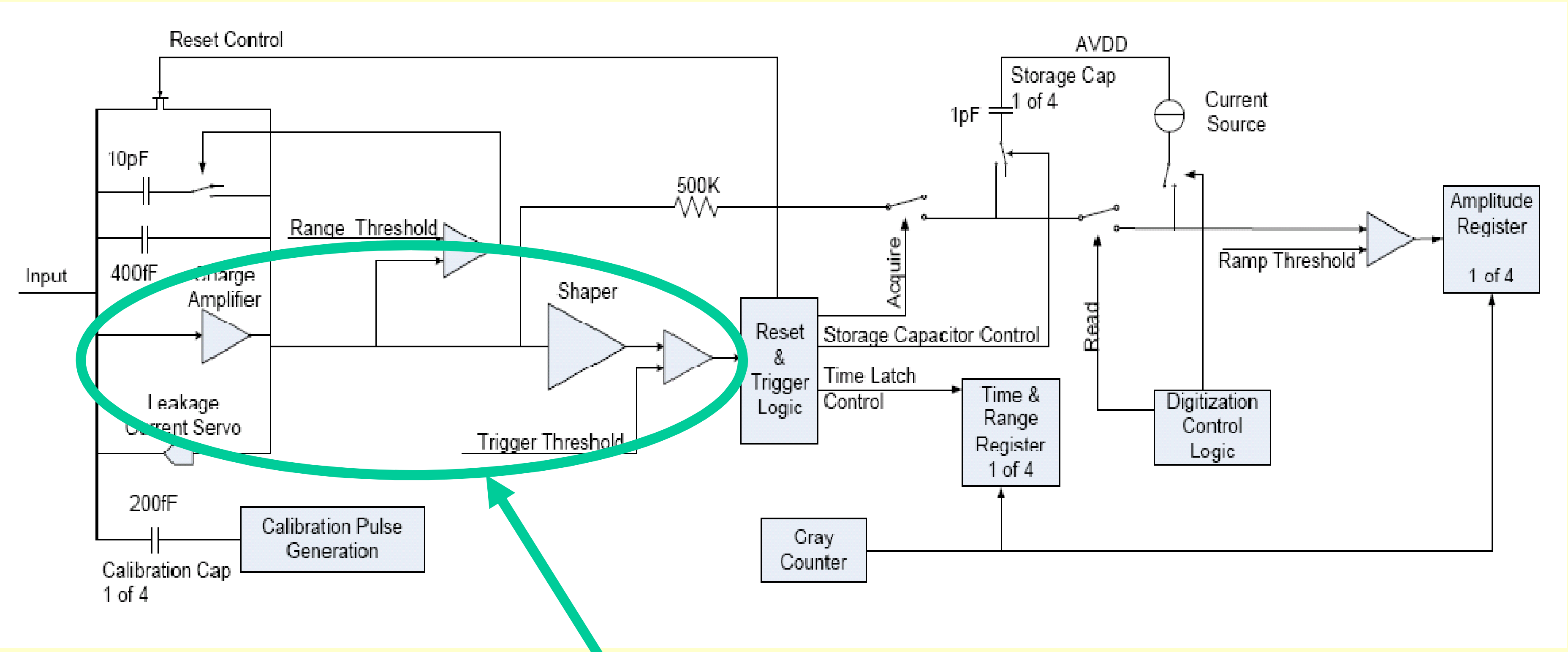
SiD Leakage Current (sensor #26): Average leakage for 1840 channels is about ~160 pA/channel

Measured strip and double-metal trace (routing to bump bond array) resistances for two sensors:

Sensor Number	Strip Res.	Typical Trace Res.
24	578 Ω	225 Ω
26	511 Ω	161 Ω

Studies of KPiX Performance as a Tracking Chip

- Just getting underway at SCIPP; expect to ramp up over the next 12 months.



Start with amplifier/discriminator studies (essential for tracking); use maximum gain setting

Use of KPiX as a Tracking Chip

Studies just getting underway at SCIPP (Sheena Schier, UCSC undergrad)

Use comparator setting to measure amplifier response properties

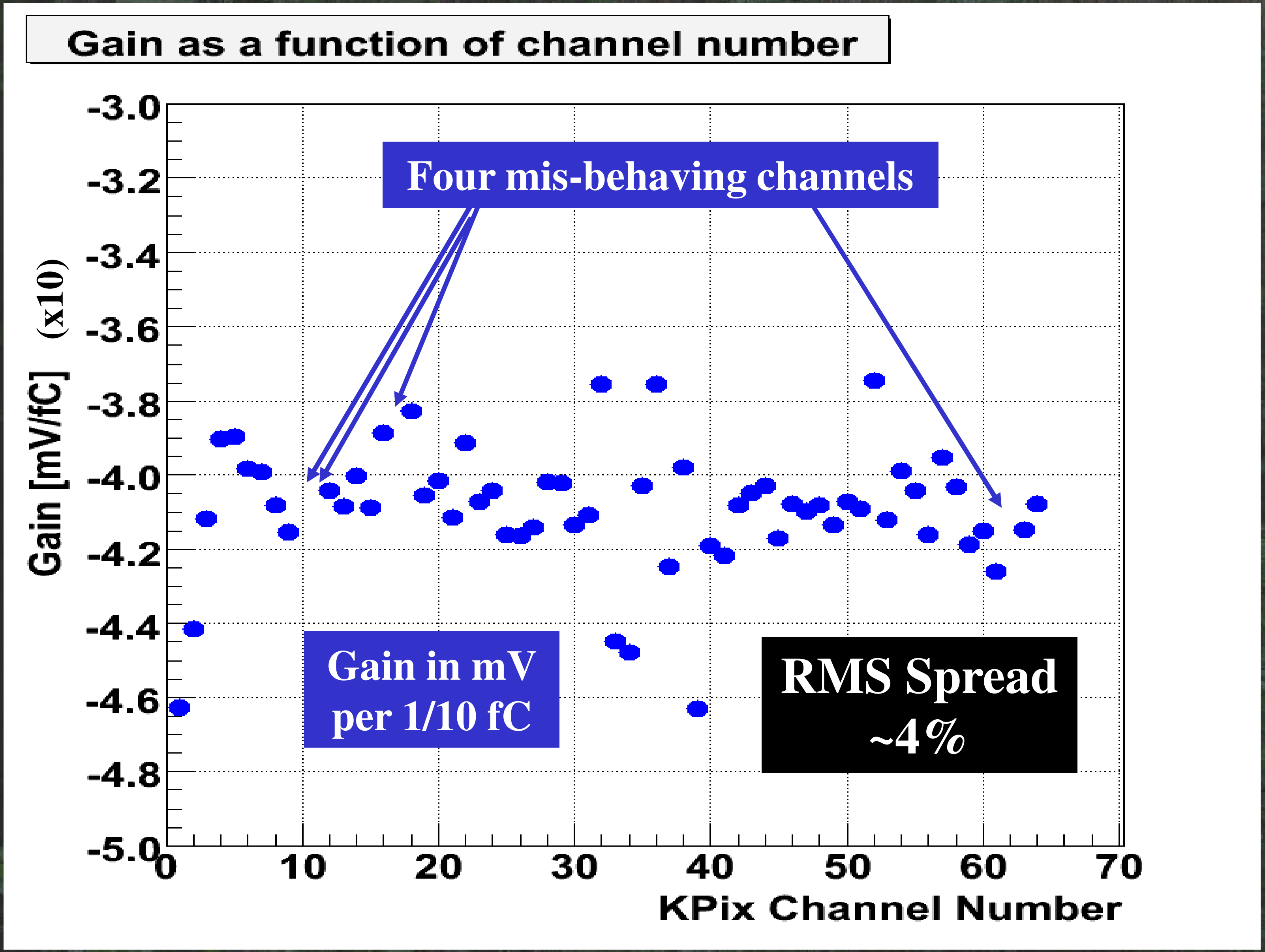
Look at 64-channel KPiX-7

Four channels appear to give uncharacteristic behavior (looking into this)

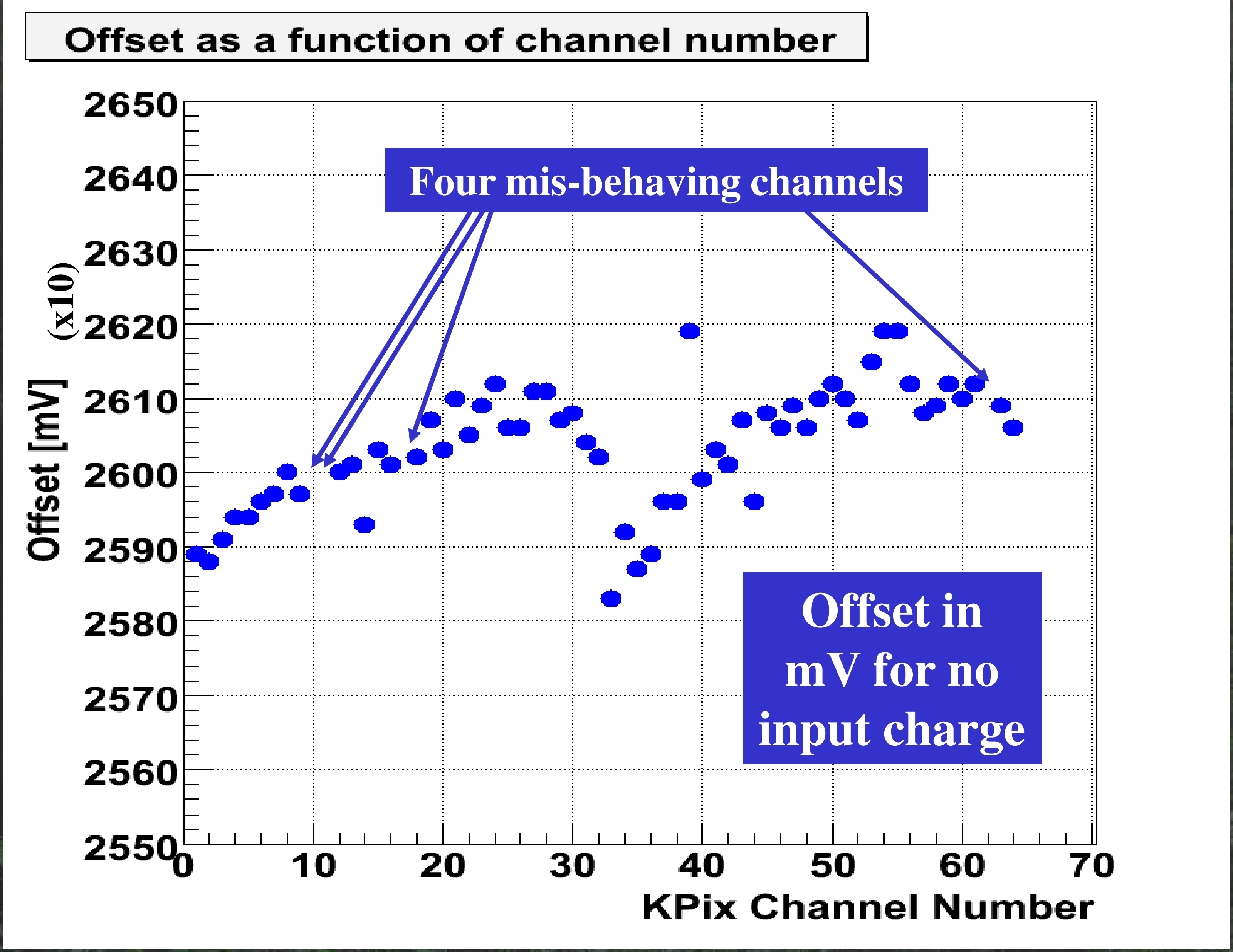
Look at gain, offset, comparator variation for remaining 60 channels

Much thanks to SLAC group (Ryan Herbst)

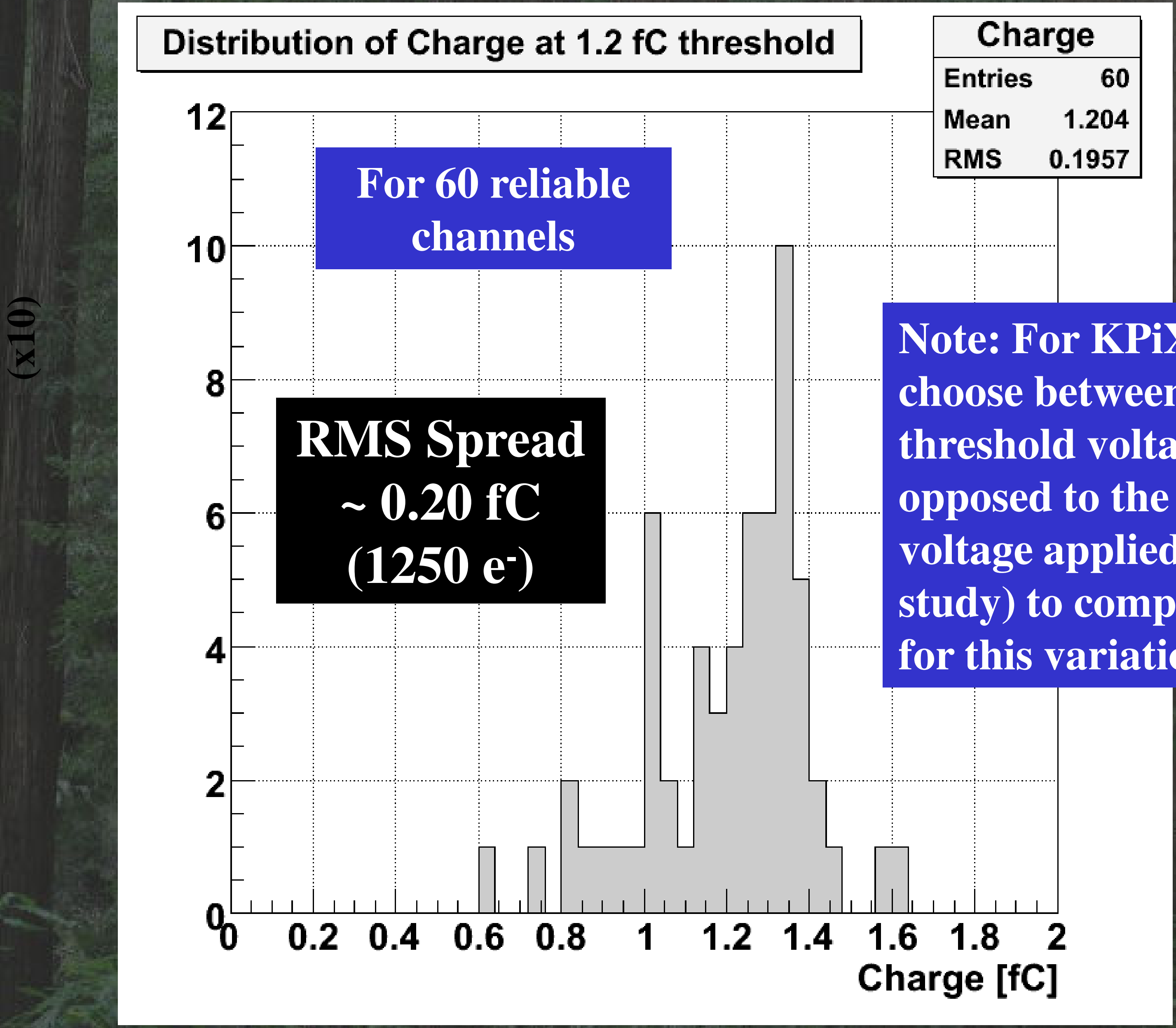
KPiX “Gain” (mV/0.1fC) by Channel



0-Charge Input Offset (mV) by Channel



True Input Charge; Nominal 1.2fC Threshold



For 60 reliable channels

RMS Spread ~ 0.20 fC (1250 e^-)

Note: For KPiX, can choose between four threshold voltages (as opposed to the single voltage applied for this study) to compensate for this variation.

Comments on SCIPP KPiX Studies

Studies very preliminary (first results last week)

Chip unloaded → not quoting noise results yet (working on sensor connections)

• Need to look at four "failing" channels

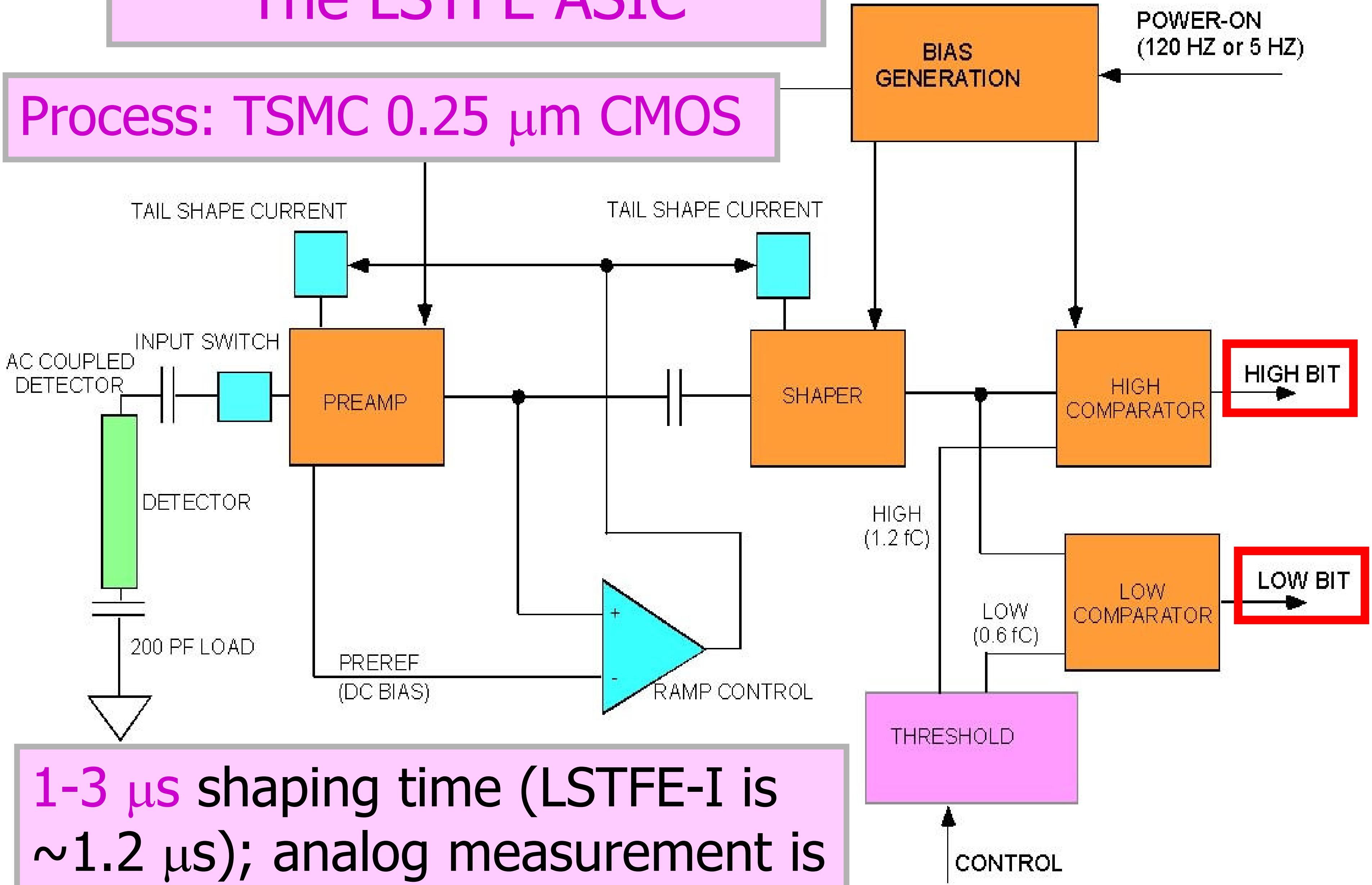
• Need to understand effect of outliers in "true input charge" distribution

→ Channel yield issue?

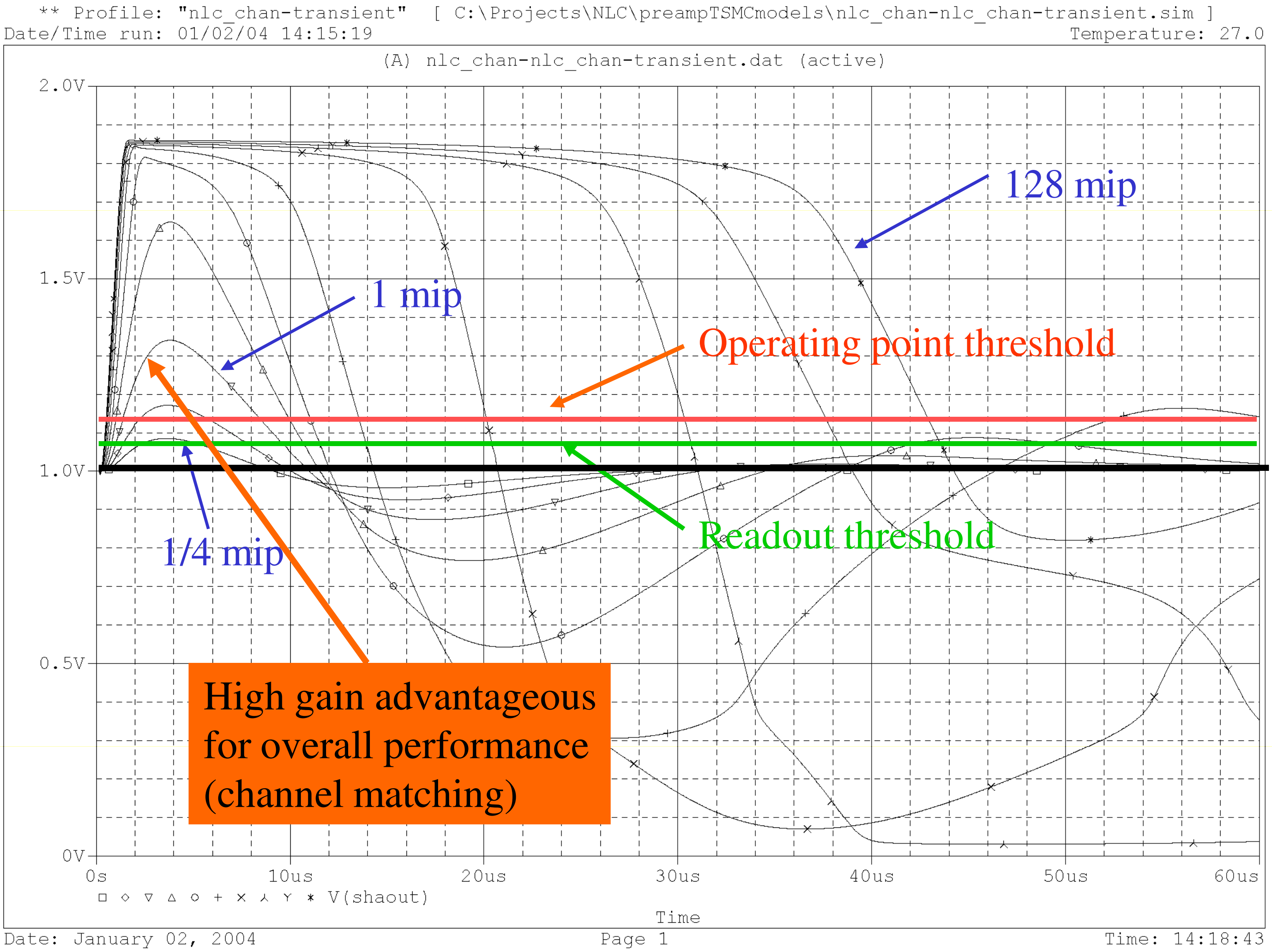
DEVELOPMENT OF THE LSTFE FRONT-END ASIC

The LSTFE ASIC

Process: TSMC 0.25 μm CMOS



1-3 μs shaping time (LSTFE-I is ~1.2 μs); analog measurement is Time-Over-Threshold


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
V(shaout)
Time
128 mip
1 mip
Operating point threshold
Readout threshold
1/4 mip
High gain advantageous
for overall performance
(channel matching)
Date: January 02, 2004
Page 1
Time: 14:18:43

EQUIVALENT CAPACITANCE STUDY

Noise vs. Capacitance (at τ_{shape} = 1.2 μs)

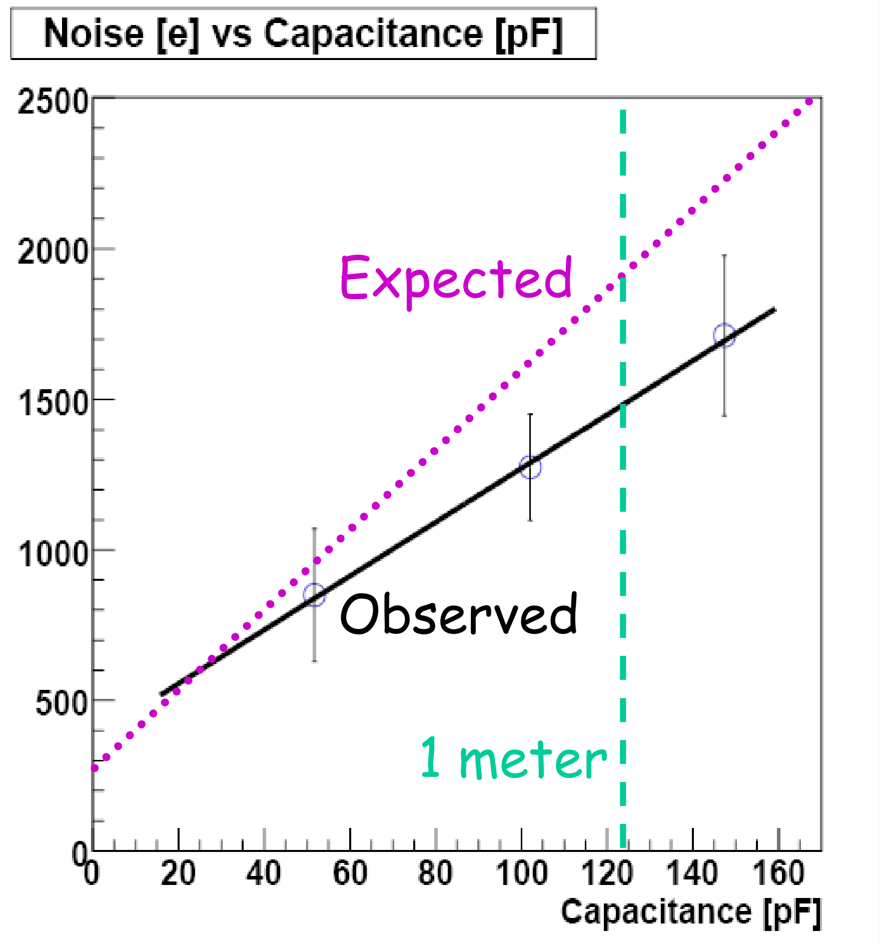
Measured dependence is roughly (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

with *C* in pF.

Experience at 0.5 μm had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 μm model parameters are accurate

➔ Noise performance somewhat better than anticipated.



LSTFE-II Prototype

Additional "quiescent" feedback to improve power-cycling switch-on from 30 msec to 1 msec

Improved environmental isolation

Additional amplification stage to improve S/N, control of shaping time, and channel-to-channel matching

Improved control of return-to-baseline for < 4 mip signals (time-over-threshold resolution)

128 Channels (256 comparators) read out at 3 MHz, multiplexed onto 8 LVDS outputs

Fast power-switching problem; traced to "standard" analog memory cell (probably process leakage).

READOUT NOISE FOR LINEAR COLLIDER APPLICATIONS

Readout Noise for Linear Collider Applications

Use of silicon strip sensors at the ILC tend towards different limits than for hadron collider or astrophysical applications:

- Long shaping time
- Resistive strips (narrow and/or long)

But must also achieve lowest possible noise to meet ILC resolution goals.

- How well do we understand Si strip readout noise, particularly for resistive networks?
- How can we minimize noise for resistive networks?

Standard Form for Readout Noise (Spieler)

Parallel Resistance

Series Resistance

$$Q^2 = F_i \tau \left(2eI_d + \frac{4kT}{R_B} + i_{na}{}^2 \right) + \frac{F_v C^2}{\tau} (4kTR_s + e_{na}{}^2) + 4F_v A_f C^2$$

Amplifier Noise (parallel)

Amplifier Noise (series)

F_i and F_v are signal shape parameters that can be determined from average scope traces.

CDF L00 Sensor "Snake"

CDF L00 strips: 310 Ohms per 7.75cm strip (~3x GLAST)

➔Long-ladder readout noise dominated by series noise (?)

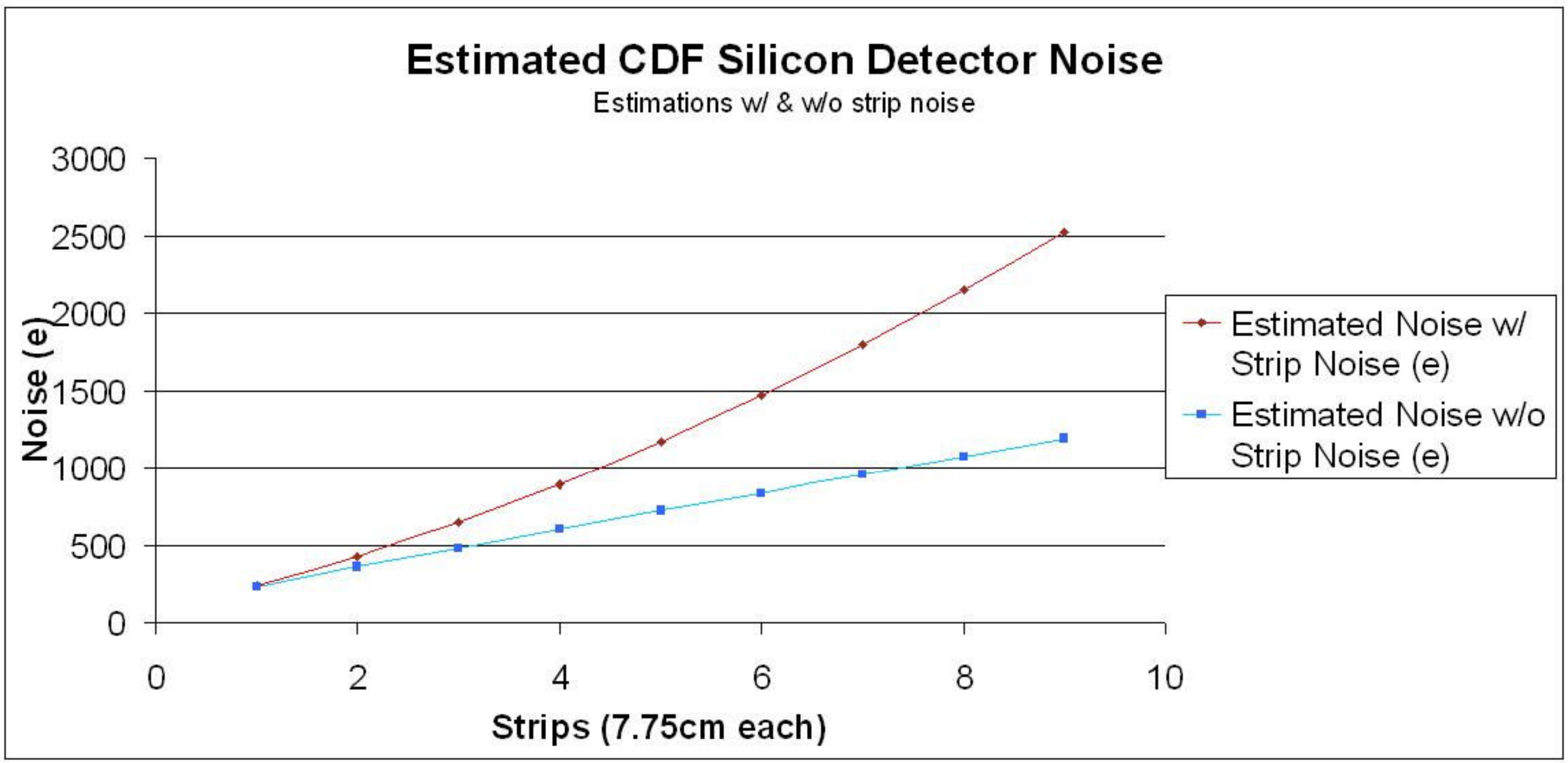
Construct ladder by bonding strips together in "snake" pattern (Sean Crosby)

At long shaping-time, bias resistors introduce dominant parallel noise contribution

➔Sever and replace with custom biasing structure (significant challenge…)

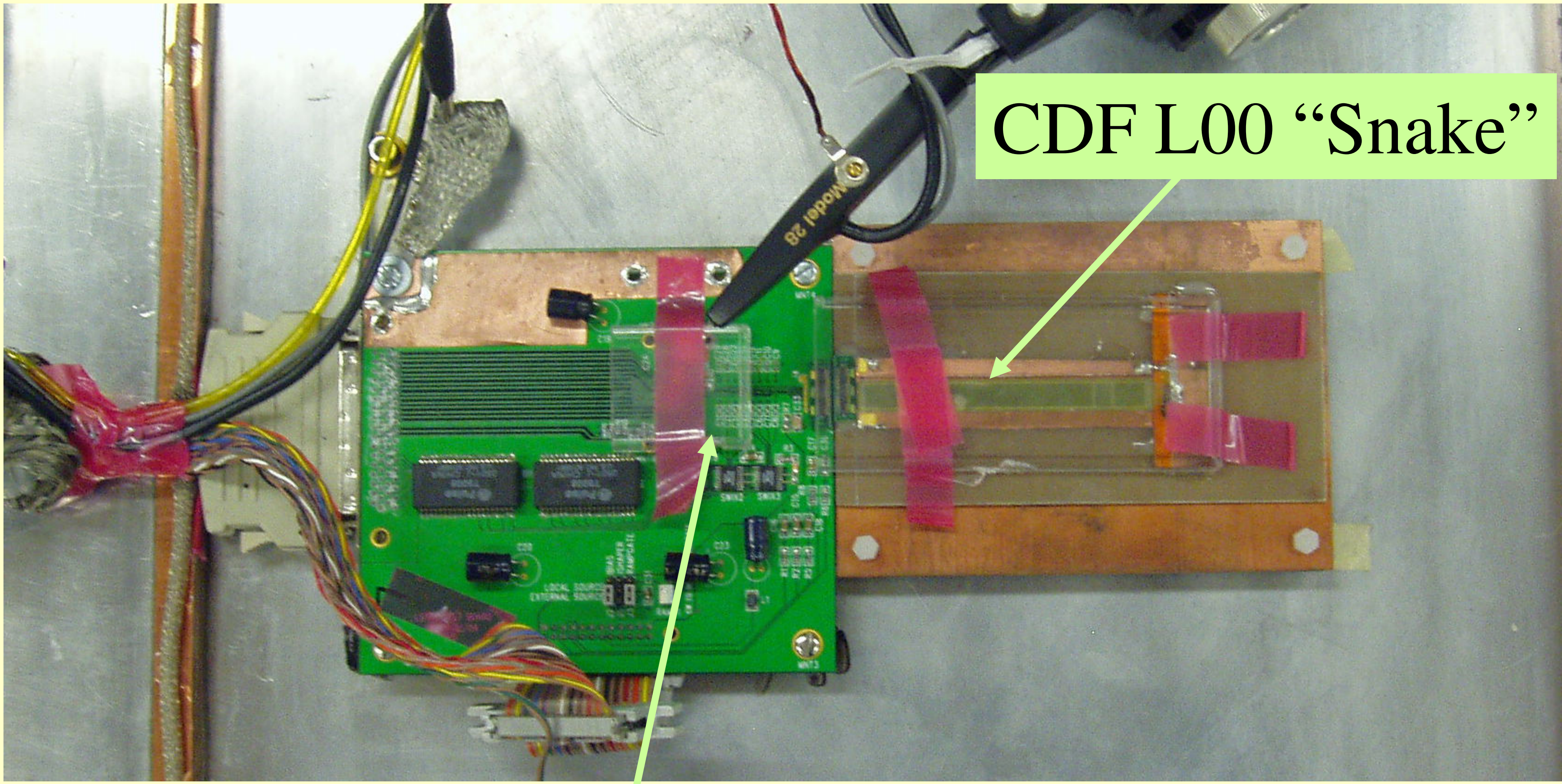
Thanks to Sean Crosby and Kelsey Collier, UCSC undergraduate thesis students

Expected Noise for Custom-Biased L00 Ladder



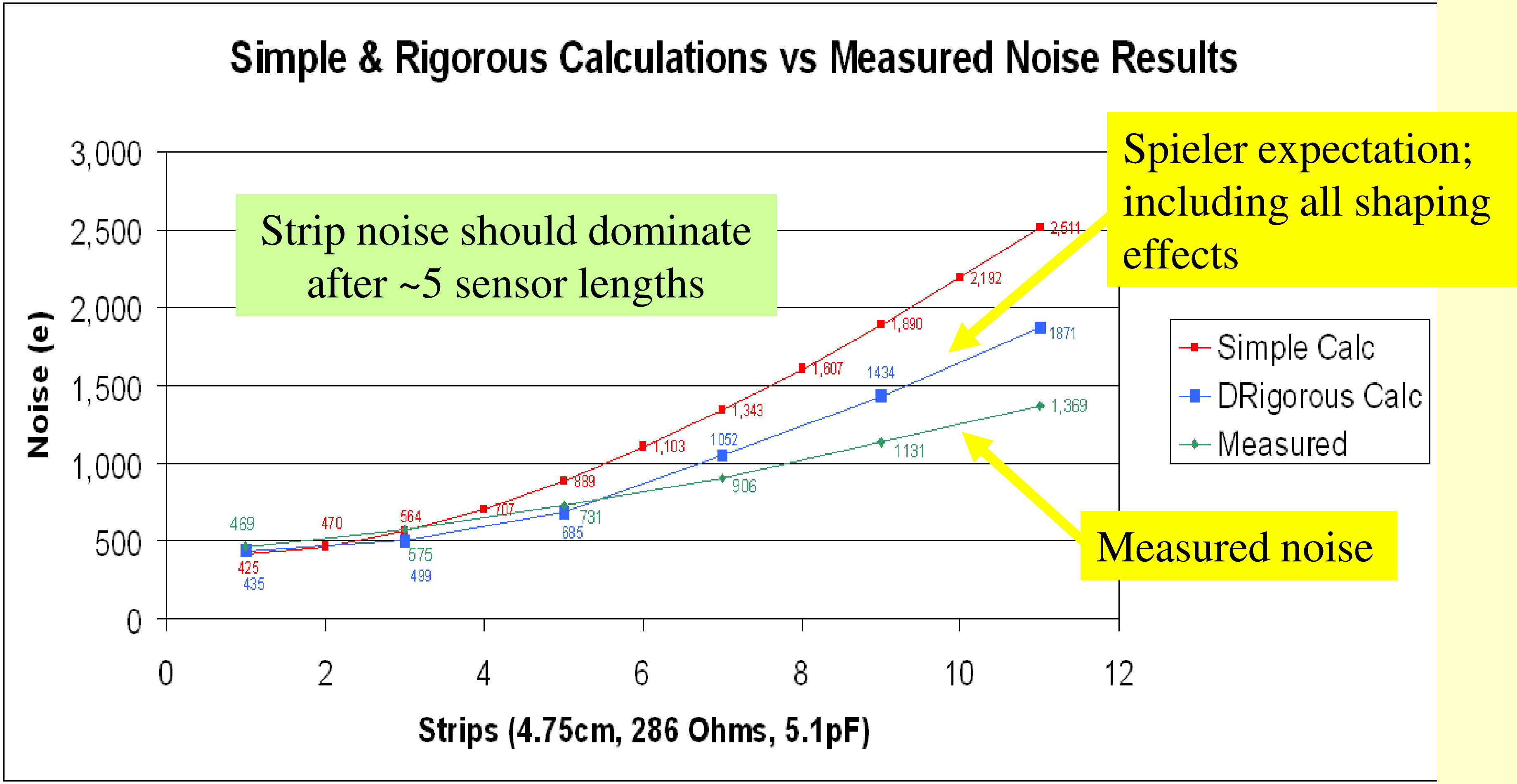
Spieler formula suggests that series noise should dominate for ladders of greater than 5 or so sensors.

CDF L00 Sensor “Snake”



LSTFE1 chip on Readout Board

Preliminary results, after lengthy effort to eliminate non-fundamental noise sources…



Repeating measurement, refining calibration (Kelsey Collier); will also develop PSpice simulation & explore readout from center of "snake" ladder

SCIPP ILC DETECTOR R&D SUMMARY

- Diverse program driven by undergraduate participation
- LSTFE-2 looks promising, except for power-cycling performance, which appears compromised by leakage ➔ studies must continue
- First SCIPP look at KPiX as a tracking chip; looking forward to 256-channel KPiX-8 loaded with double-metal sensor
- Interesting results on charge division (see Jerome Carman talk)
- Nearing results on noise in long-ladder limit; need to match with simulation