Pixel readout for a LC TPC

LCWA 2009 – Detectors Tracking session

30 September 2009

Jan Timmermans

On behalf of the Bonn/CERN/Freiburg/Nikhef/Saclay groups

Full post-processing of a TimePix

· Timepix chip + SiProt + Ingrid:

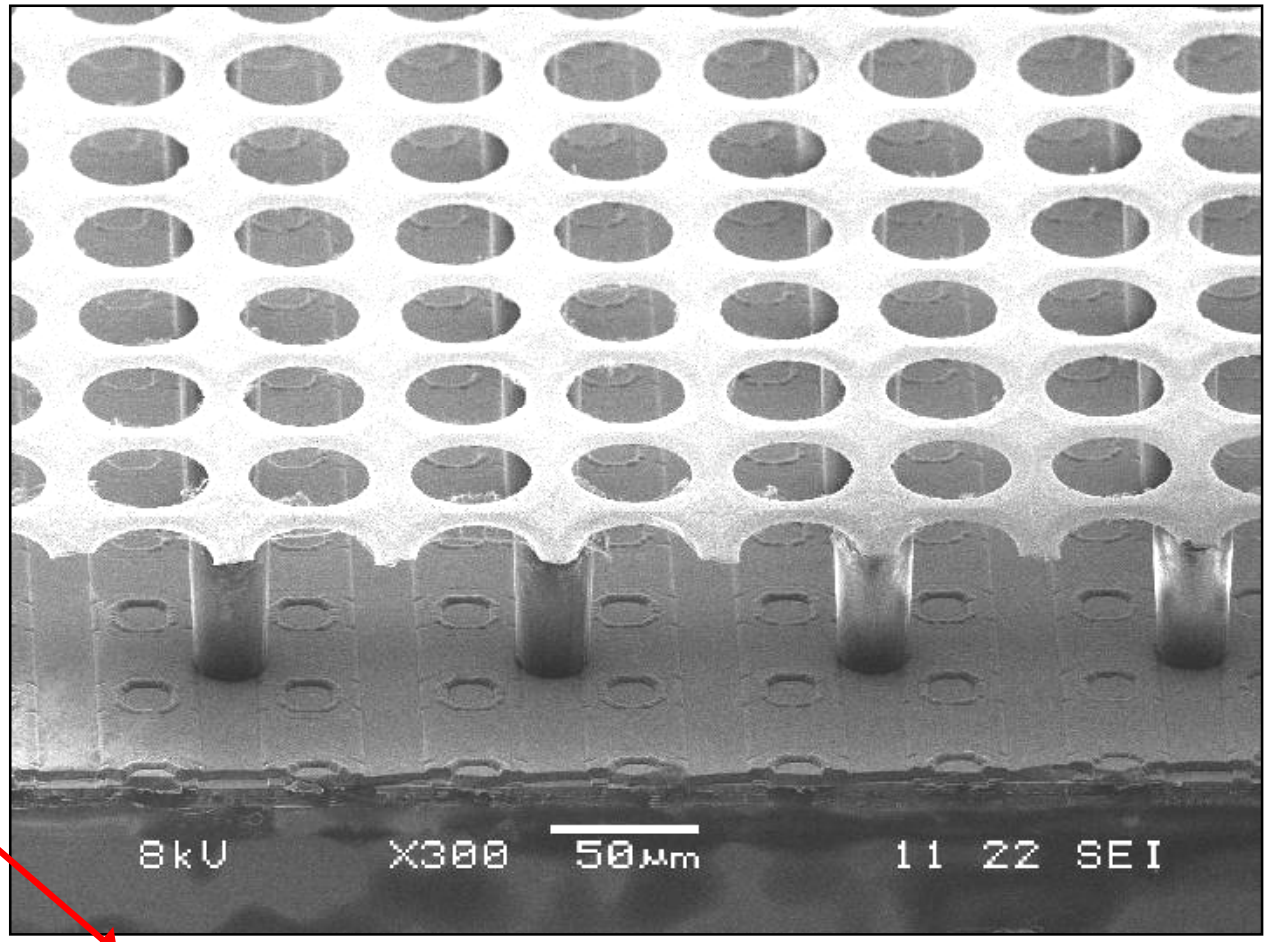
Timepix chip:

- 256x256 pixels
- pixel: 55x55 μm^2
- active surface: 14x14 mm^2

MESA+: Ingrid

IMT Neuchatel:

15 or 20 µm highly resistive aSi:H protection layer



Now also Si_3N_4 protection layers (7 µm)

Reminder of "SITPC" tasks within EUDET:

- ✓ Develop the Timepix chip that allows to measure the 3rd coordinate (drift time)
- ✓ Implementation of Timepix together with GEM and Ingrid into diagnostic endplate system (with GEM working; with Ingrid in progress)
- ✓ Performance measurements in test infrastructure at DESY (analysis GEM+Timepix data in progress)
- ✓ Develop simulation framework (continues)
- ✓ Develop DAQ system and integrate in overall DAQ of EUDET infrastructure (first used in June'09)

“final” SITPC deliverable is endplate infrastructure consisting of (at least) one LP module with Timepix readout

- Original “due” date was Dec. 2008
- Later delayed to (and done in June 2009)

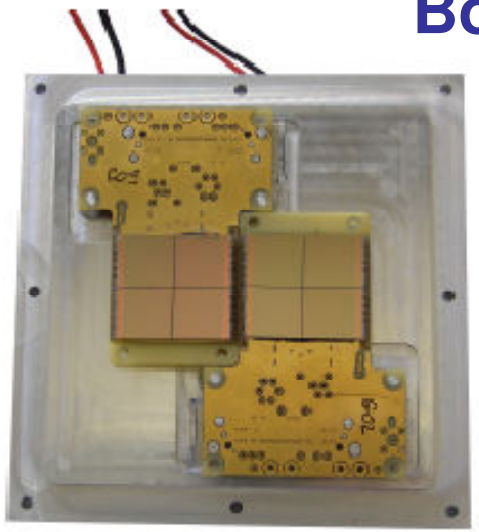
Reasons:

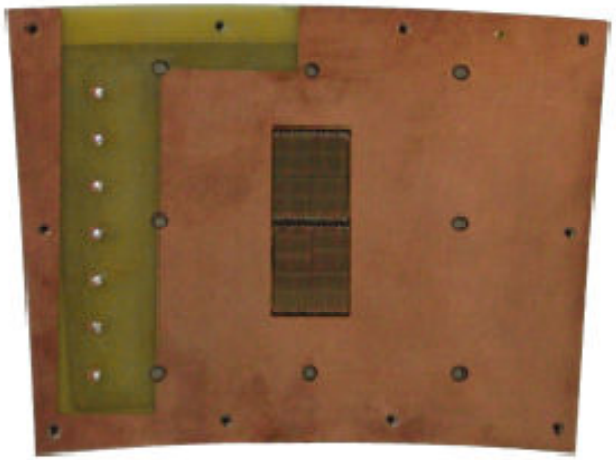
- Difficulties with control and readout of 4 or 8 chips on multichip PCBs
- Difficulties with reliable production of integrated grids (INGRIDs) in ‘wafer’ postprocessing technology

Today: most of the difficulties overcome, although large quantities are still not trivial

Module with GEMs & Timepix

Bonn/Freiburg





anode plane

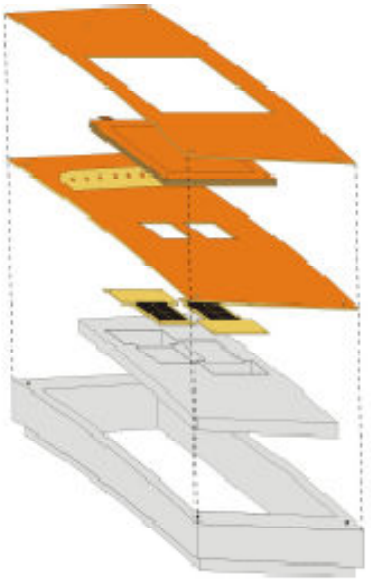
GEMs

readout plane

quad-boards

reinforcement of anode plane

redframe



Gas amplification stage:

3 standard CERN GEMS (60/70/140)

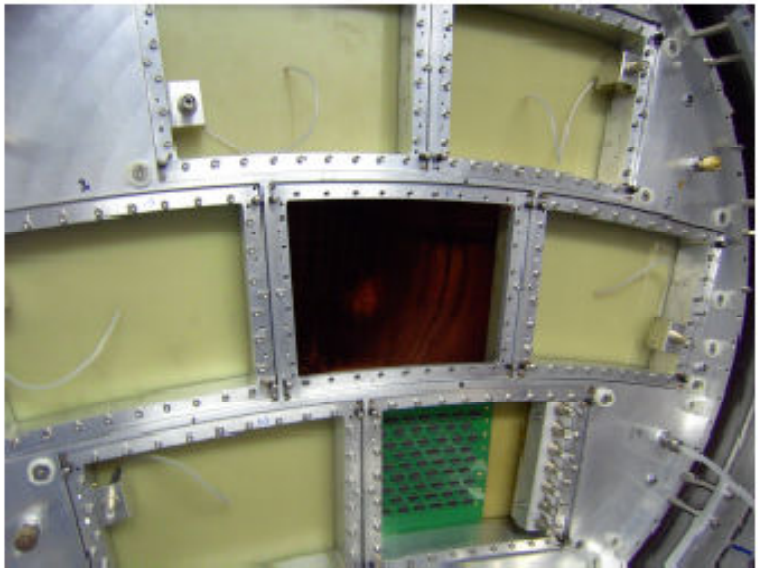
1 mm spacing between GEMs

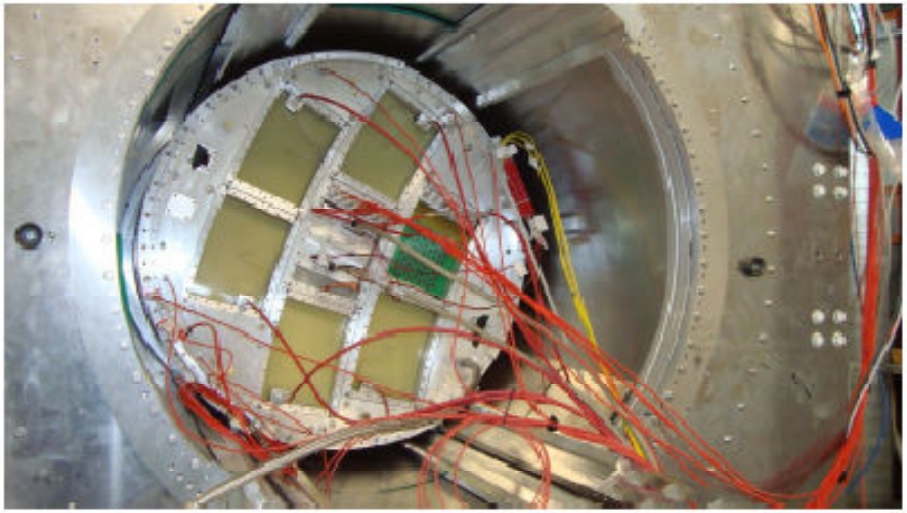
Readout:

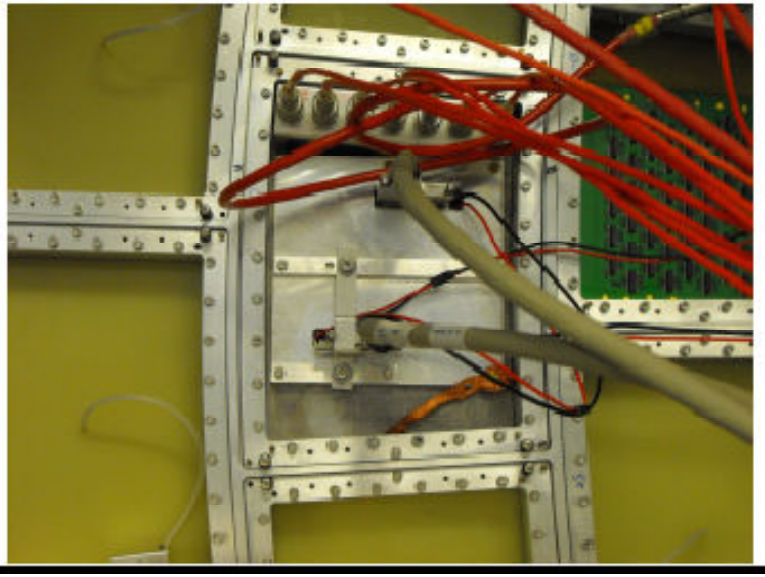
2 quadboards (4 Timepix chips each)

Nikhef

Pictures from Installation

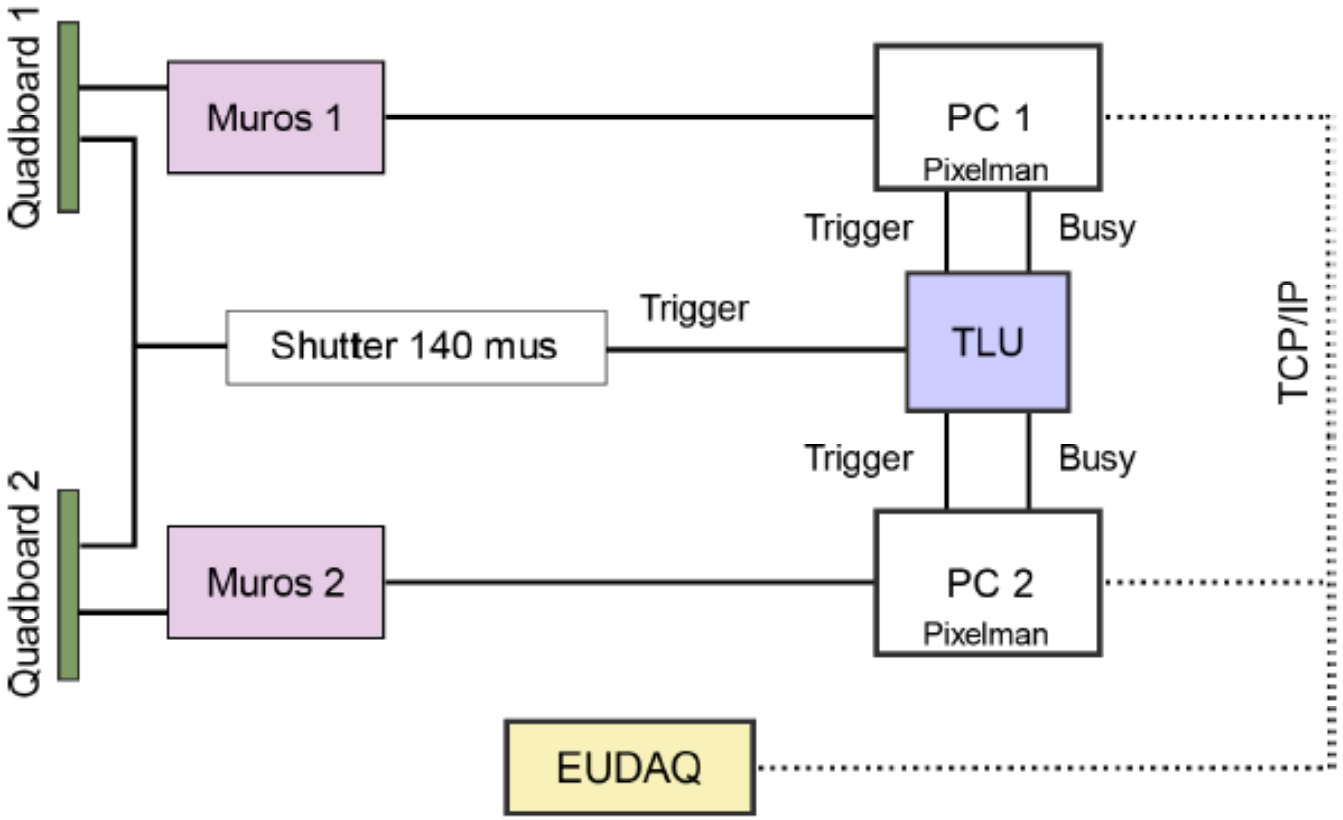






Readout scheme

Using 2 Muros systems synchronized by TLU and EUDaq



Data is written directly in the LCIO format.

universitätbonn

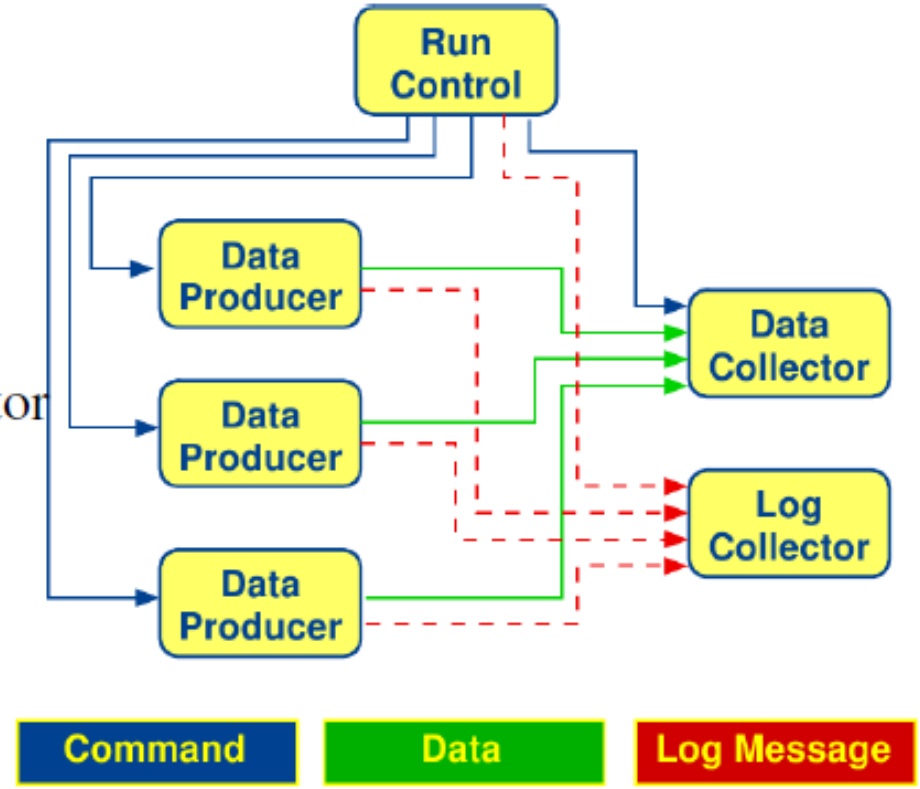
EUDAQ: The Eudet Data Acquisition System

DataProducer: Pixelman plugin communicates with EUDAQ

- Receives commands from Run Control
- Sends data to Data Collector
- Sends messages to Log Collector

DataCollector:

- Receives raw data
- Performs event building
- New: Plugin mechanism
- LCIO converter plugin for every raw data format



universitätbonn

5

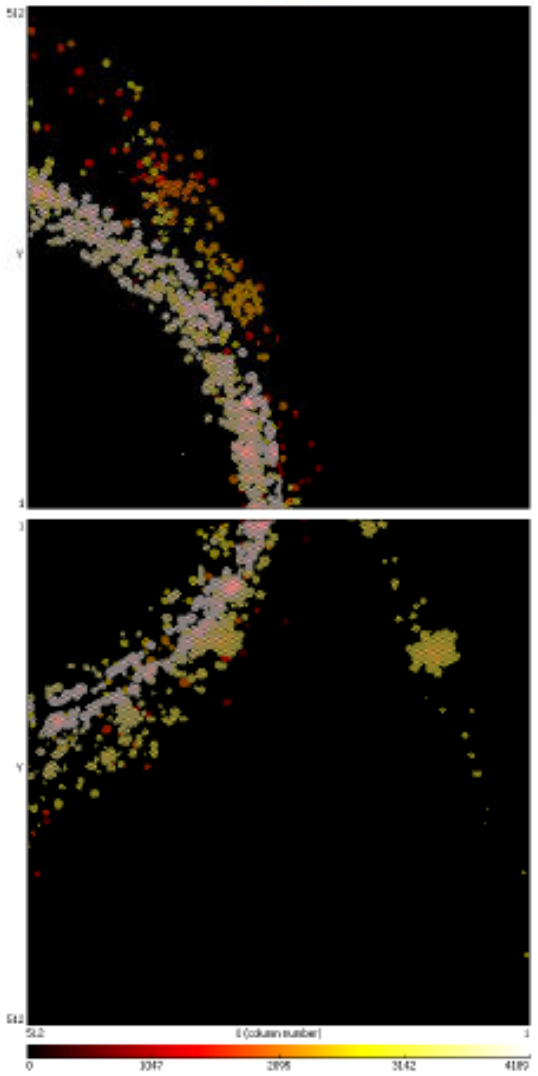
Data Sets

He:CO_2 70:30:

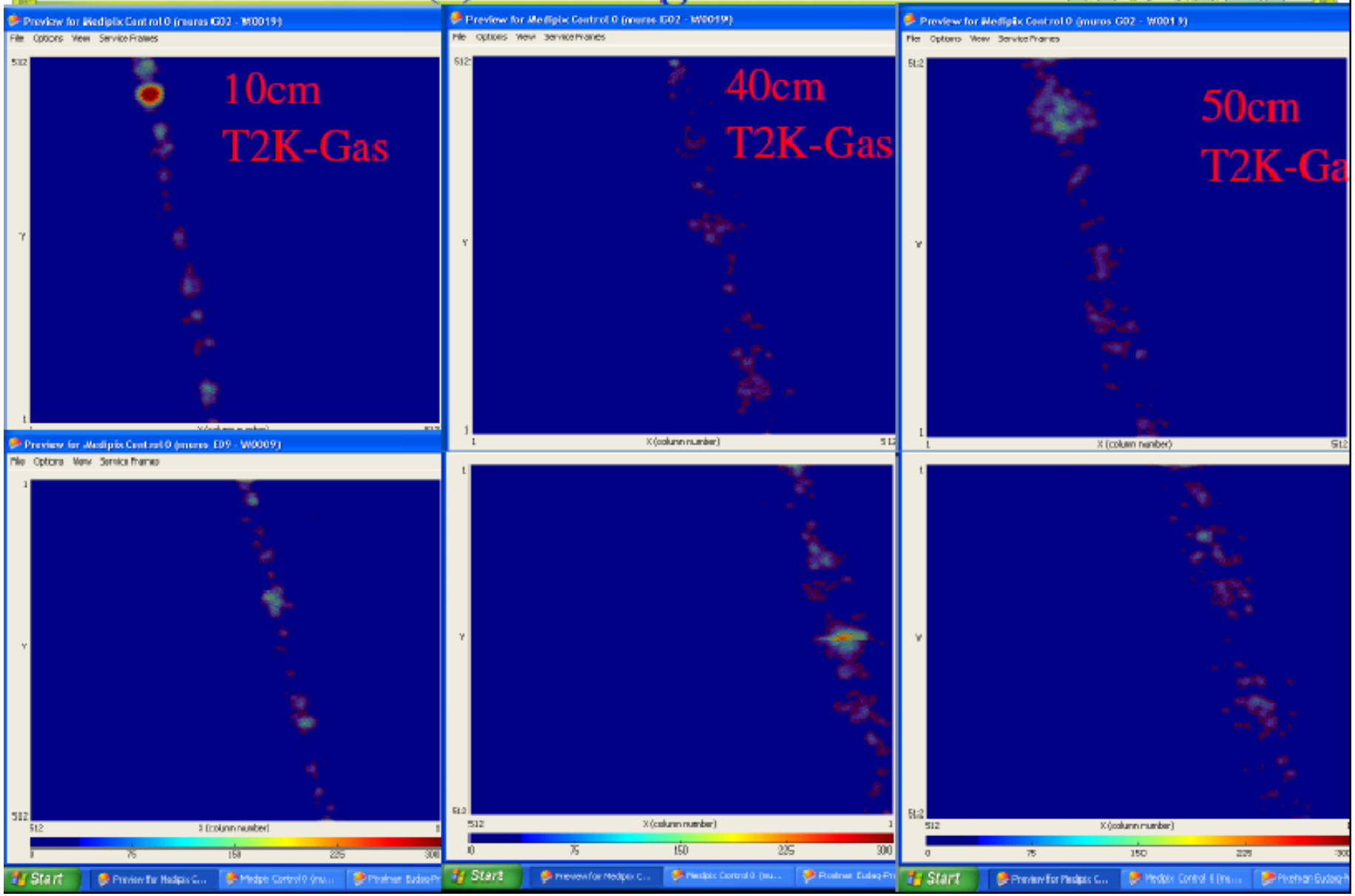
- Different drift distances
- Different angles
- Different particle energies
- Different GEM settings

T2K Gas:

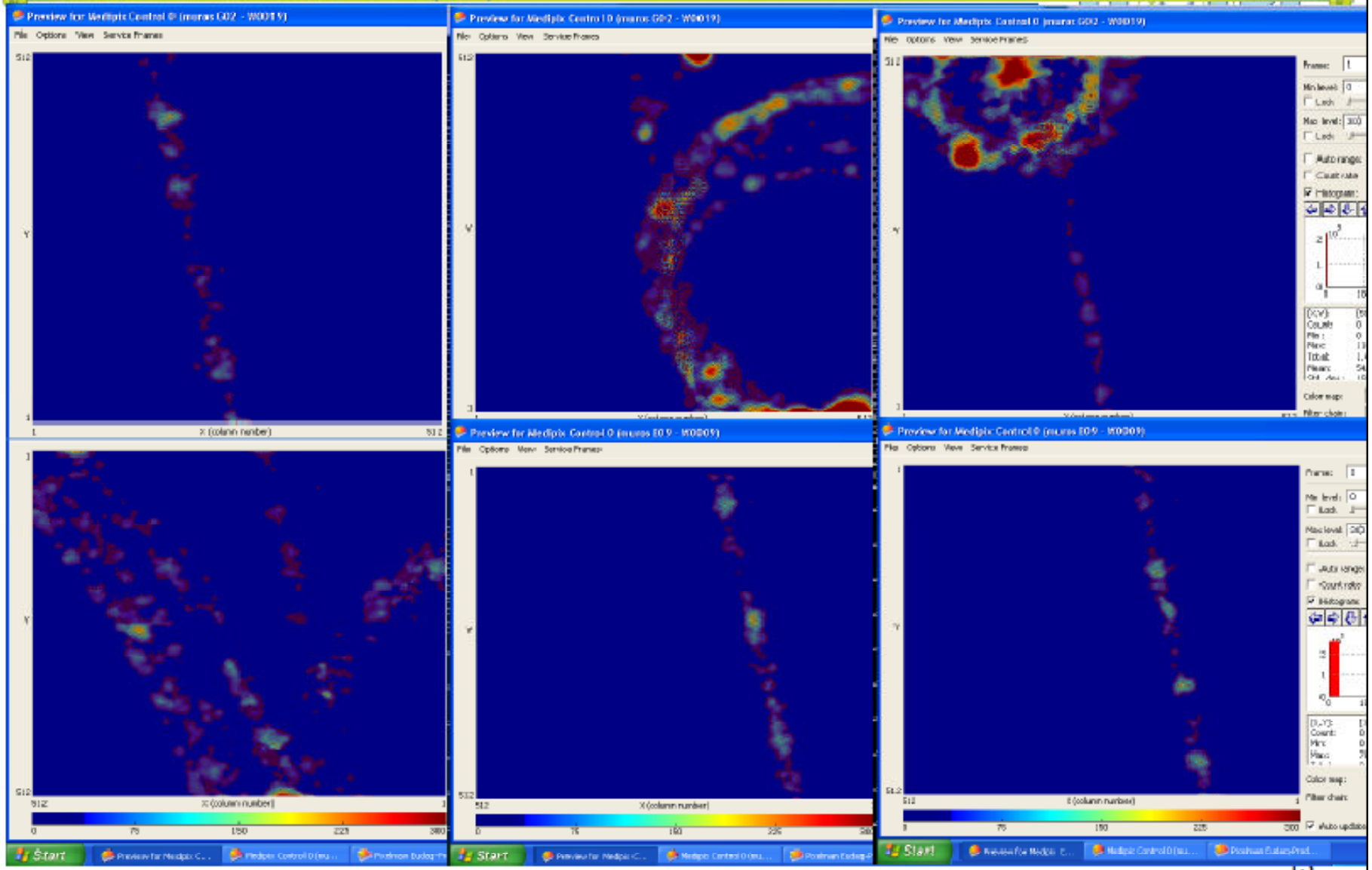
- Different drift distances
- Different angles
- Different particle energies
- Different GEM settings
- Laser dots



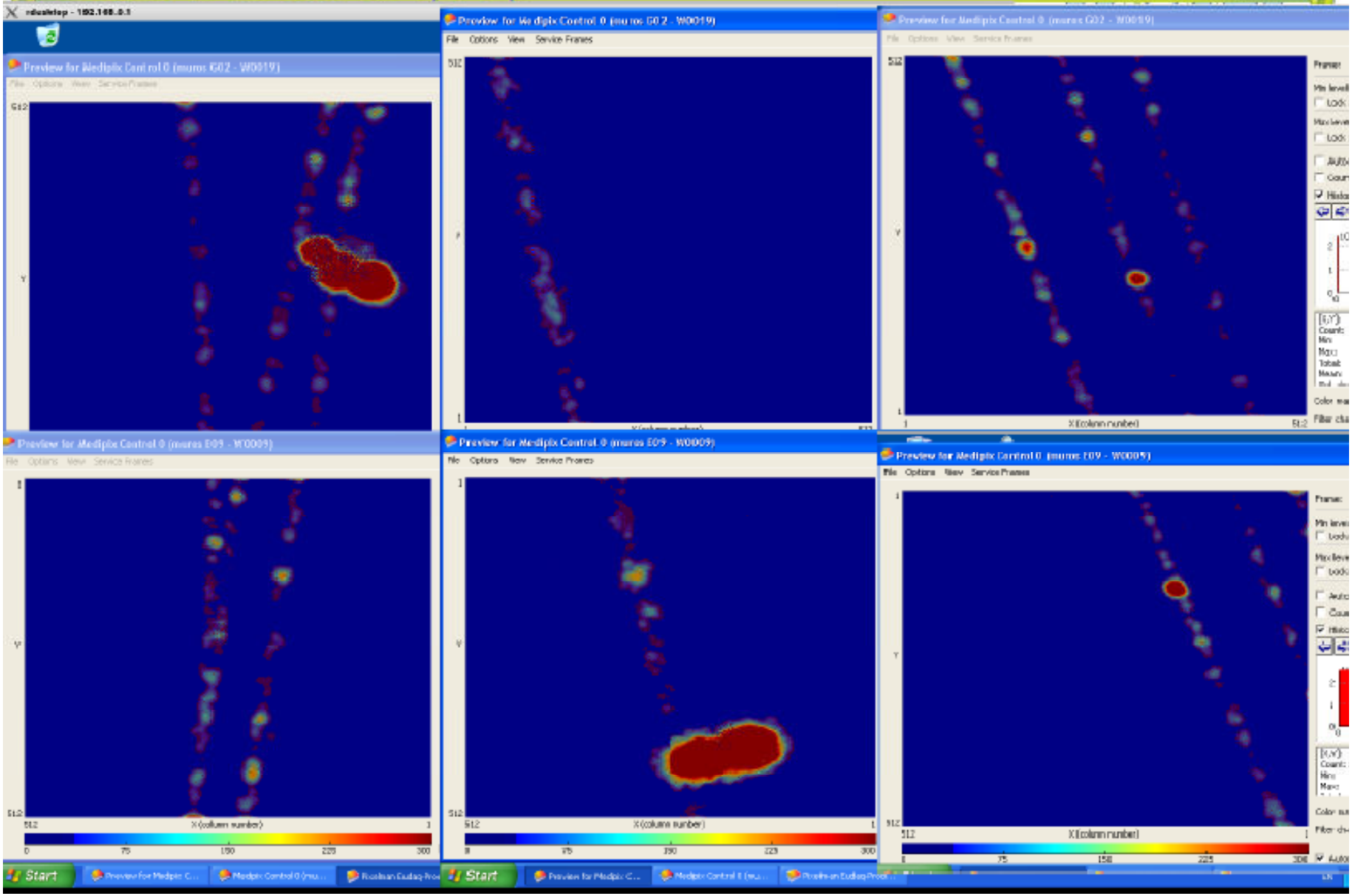
Some Pictures (I) – straight tracks



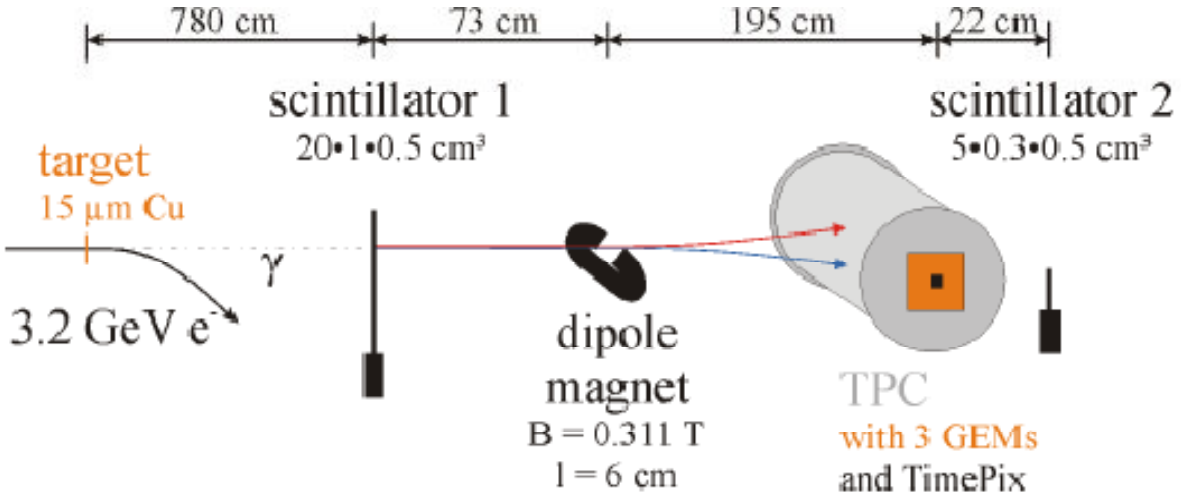
Some Pictures (II)

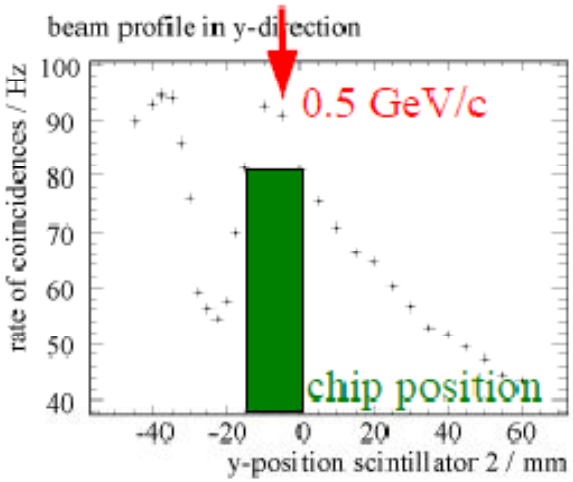


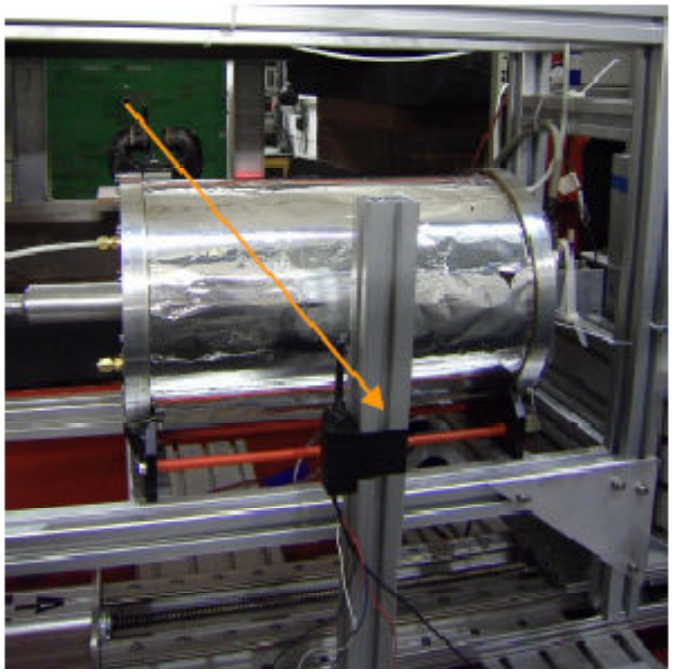
Some Pictures (III)



Test Beam Setup at ELSA, Bonn







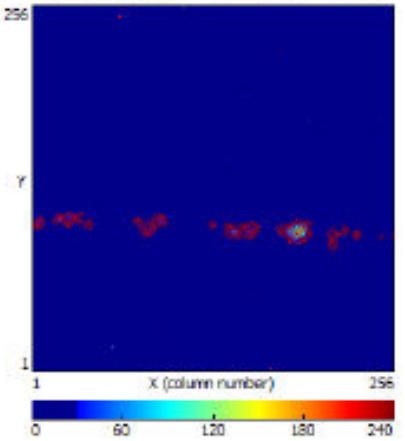
- γ were created at a target
- primary e^--beam was dumped
- photons converted in scintillator 1
- dipole separated e^+e^-
- coincidence of scinti 1 and 2 select single particle events

universitätbonn

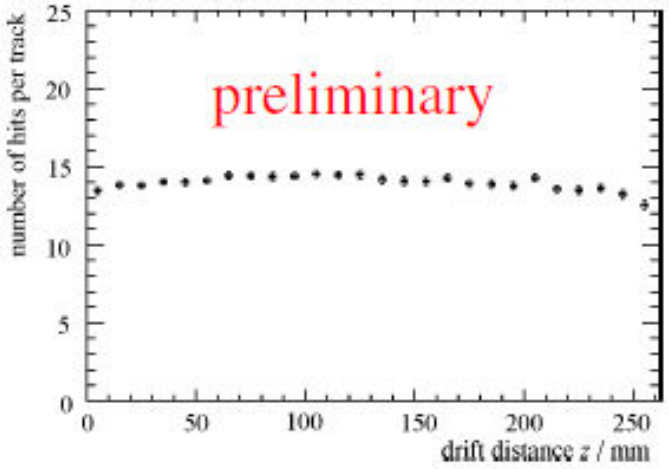
High Magnetic Fields

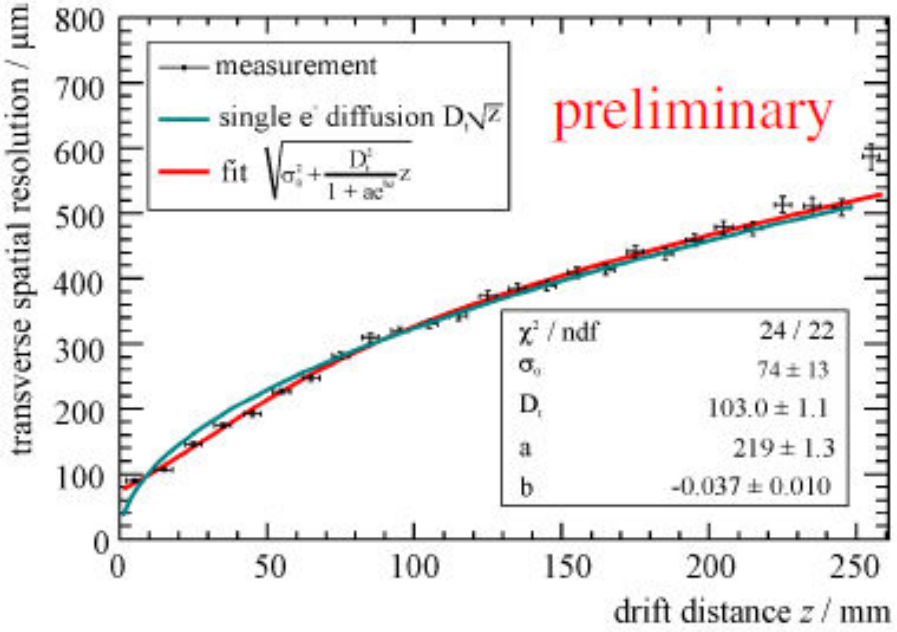
old ZEUS compensation magnet
supraconducting solenoid
reaches up to 5 T

detector is operated in magnet
first results with low statistics



$He:CO_2$ 70:30
at 4T

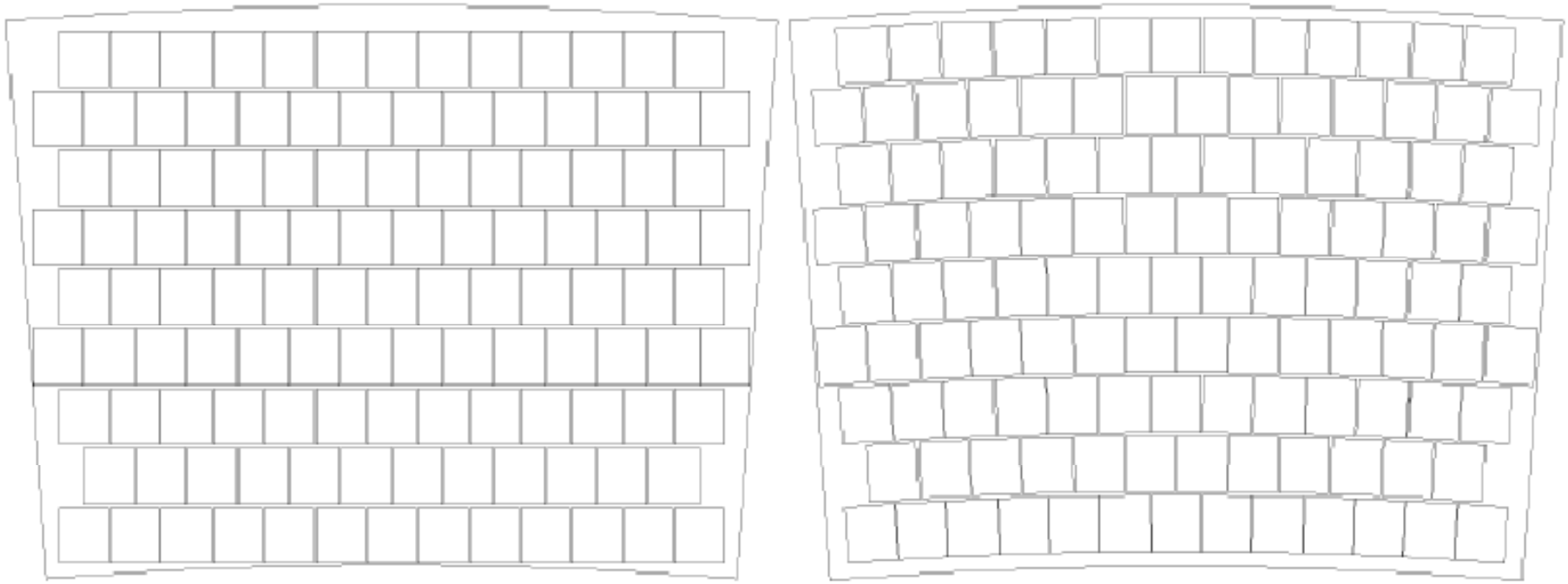




'Long-term' plans (end 2010)

LP1 module covered completely with Timepix modules

First ideas: 119 Timepix chips (more than 1 wafer, $\approx 7.8 \cdot 10^6$ channels)

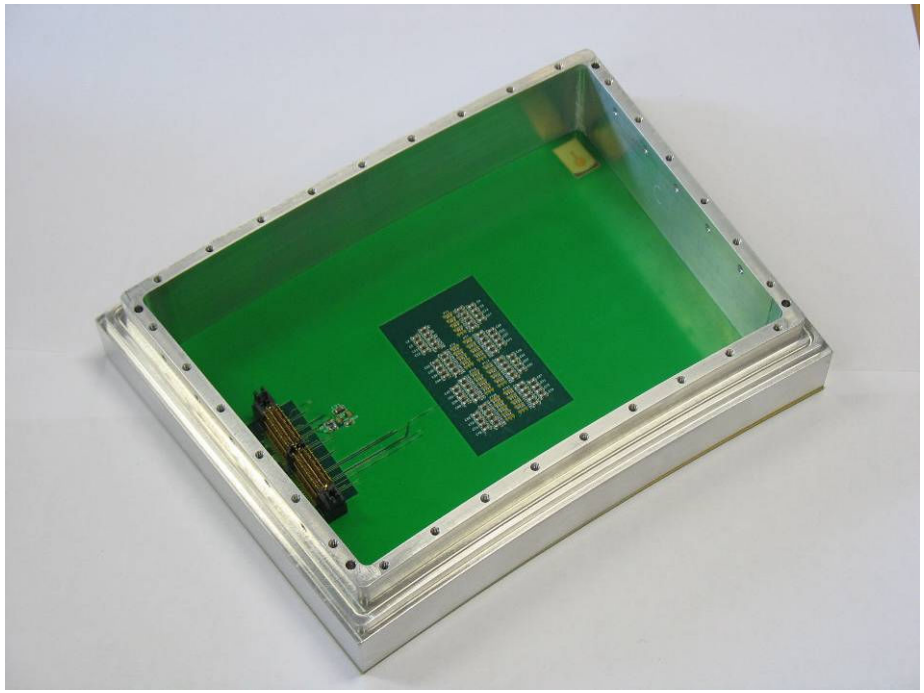


Gas amplification: triple GEM, possibly also InGrids

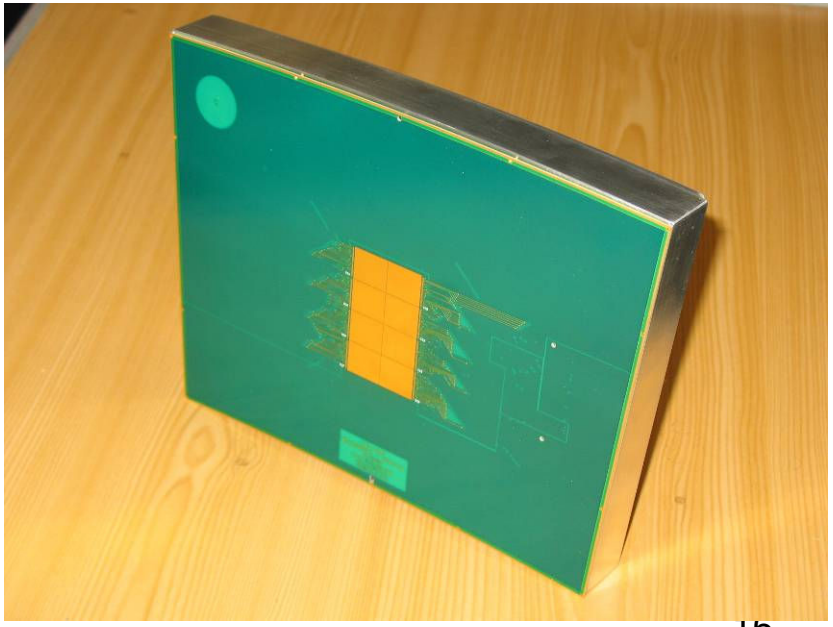
Readout electronics: 'Scalable Readout System' developed at CERN in the framework of RD-51

universitätbonn

Saclay

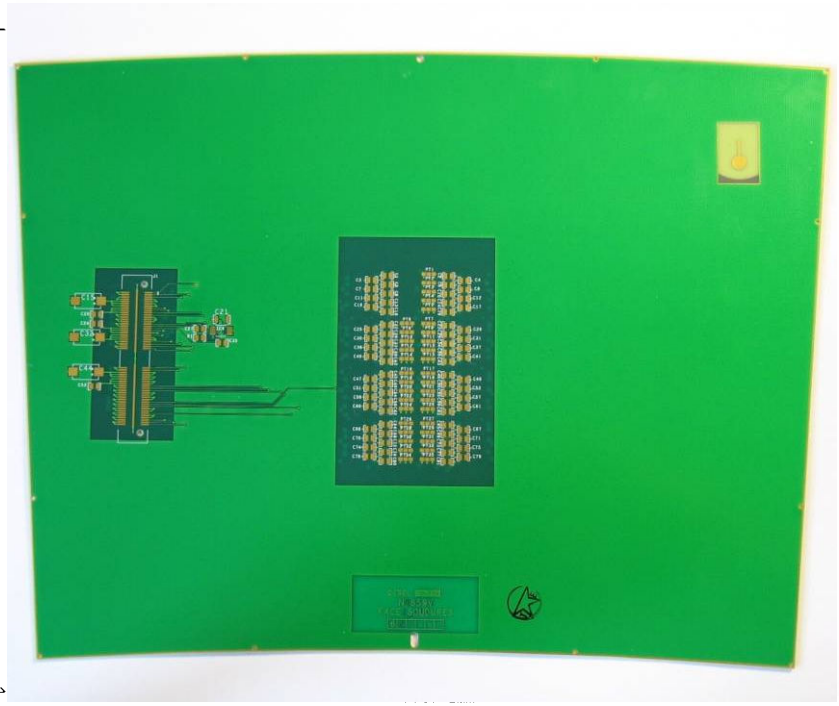


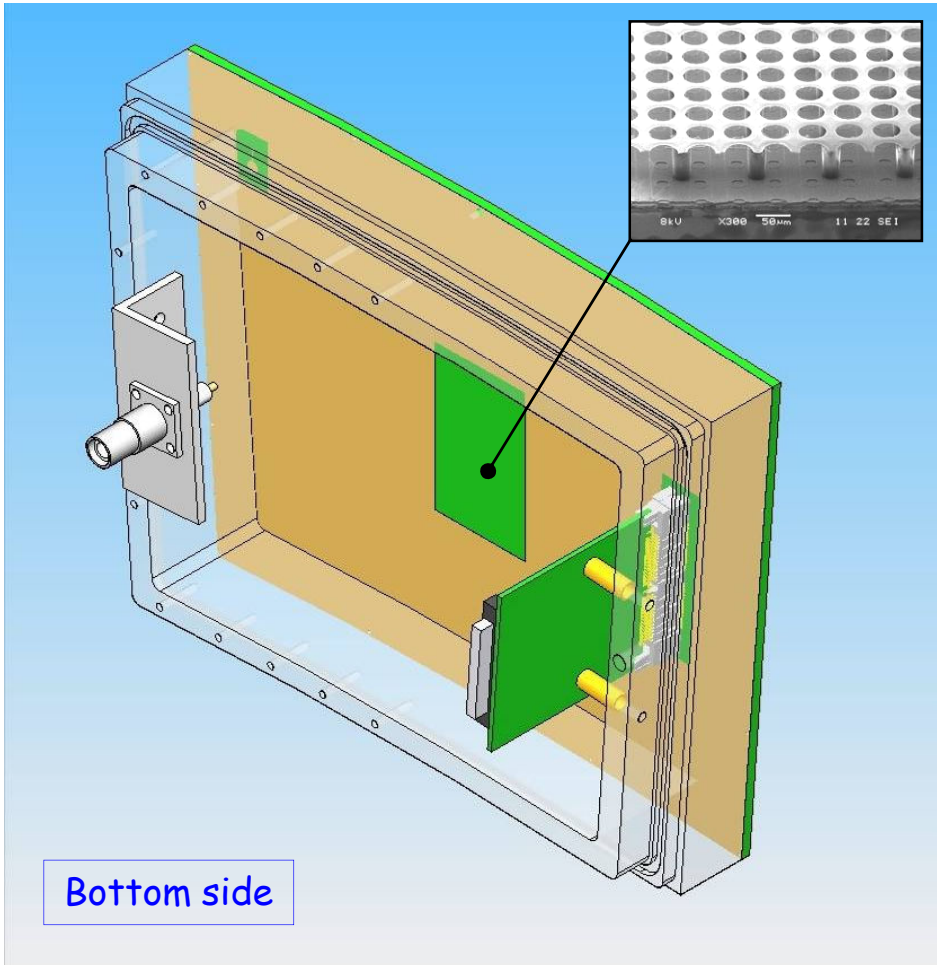
- 8 Timepix chips
- bug in Pixelman software fixed
- Now waiting for Ingrids from Nikhef/Twente
- Expect module for test in fall 2009



TimePix/Ingrid Panel

- TimePix panel with a 2x4 matrix of TimePix chips + InGrids for the TPC Large Prototype
- 6-layers PCB
- Transfert card for VHDCI cable

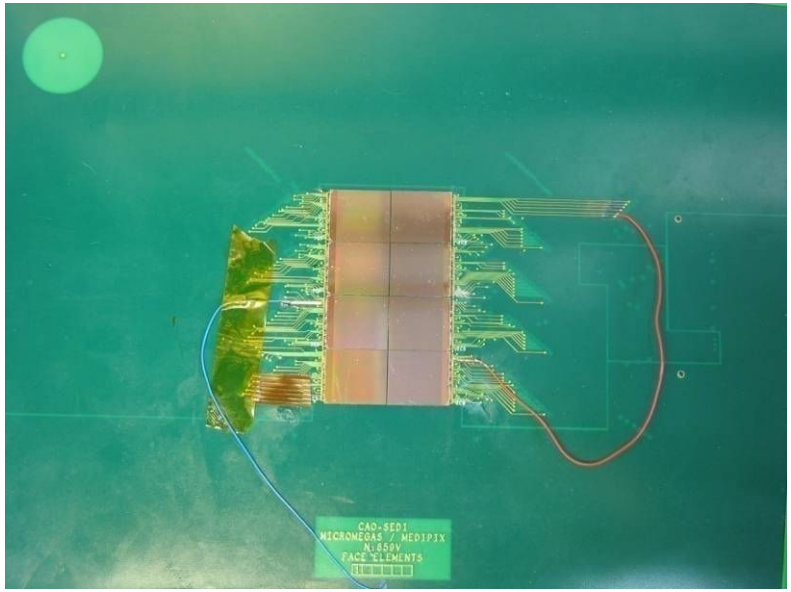


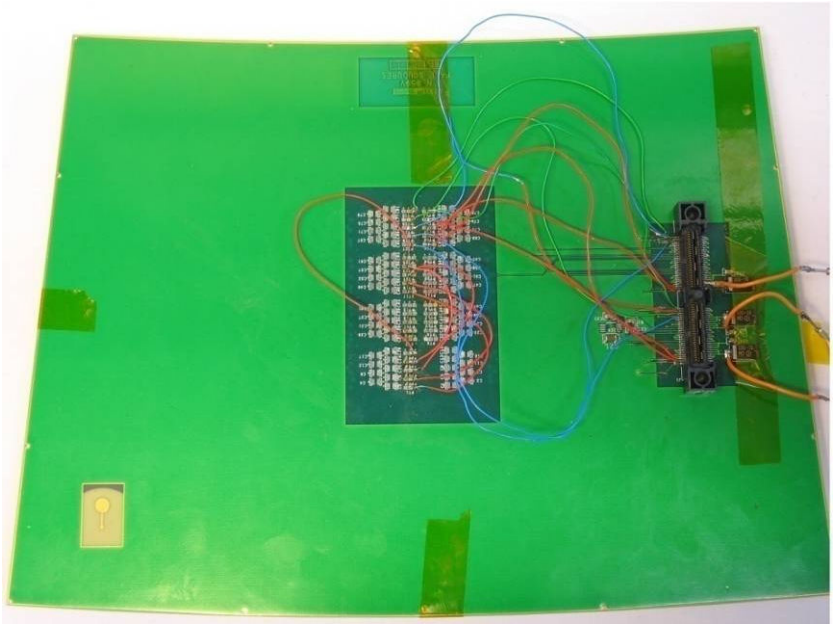


First tests

- 8 TimePix chips have been connected on the PCB
  - issues for the wire bonding
  → two chips were broken by the bonding factory

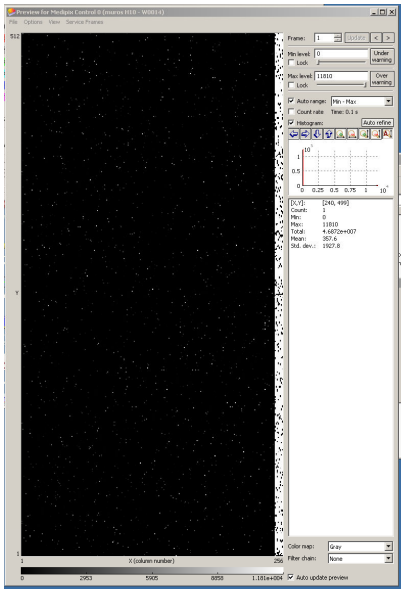
- Electrical test
  - an error of routing was found and corrected using external wires
  - power supply by MUROS only was insufficient (0.2 A per puce)
  → 3 voltage to stabalize (LV) to 2.2V

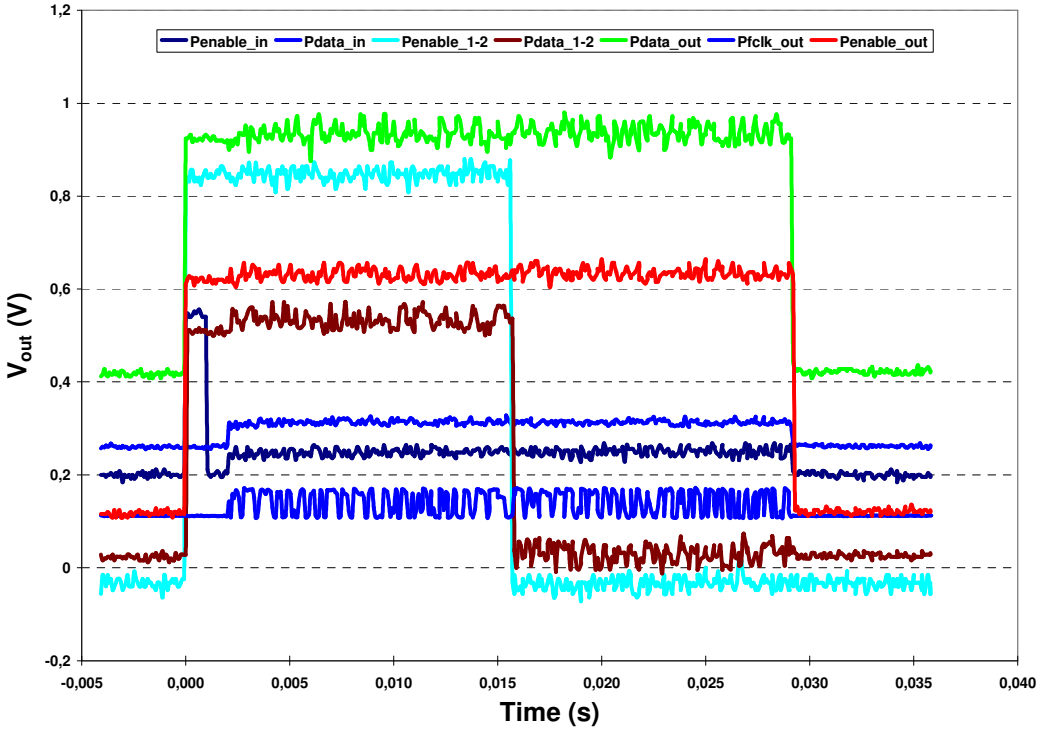


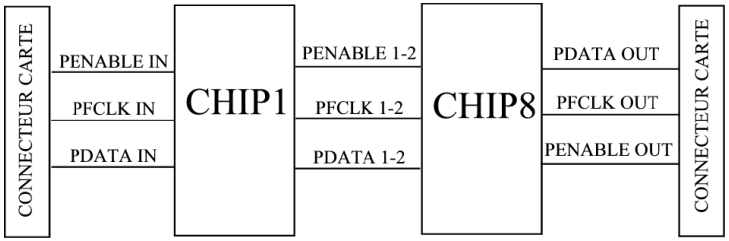


Test with 2 chips

- The 8 chips were removed and replaced by only two
- New test at CERN (January 20th, 2009)
  - the hardware was validated
  - but, correction needed in the official software Pixelman







New card in progress

- A new card was designed taking into account what we learn with the previous

- New design :

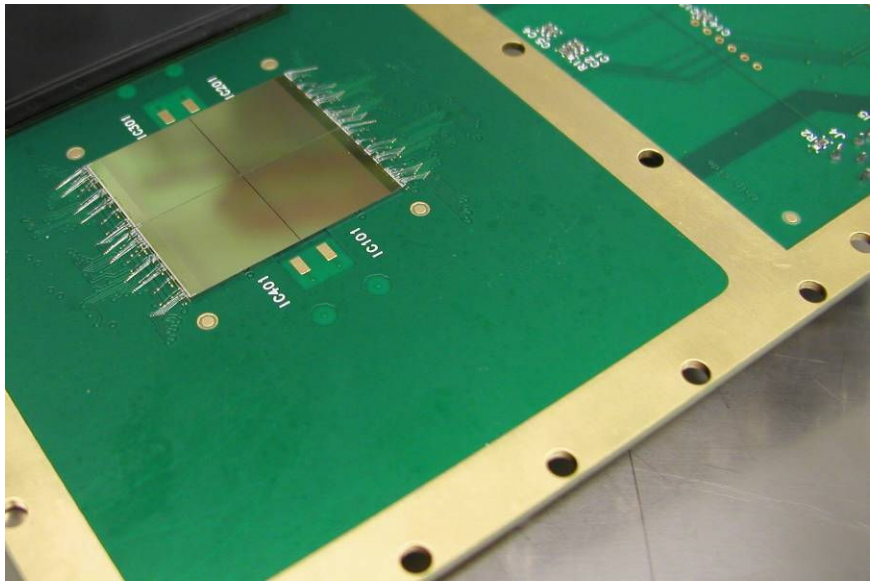
  - the 2x4 matrix is place on top a mezzanine to make easier the wire bonding

  - power regulators was implemented

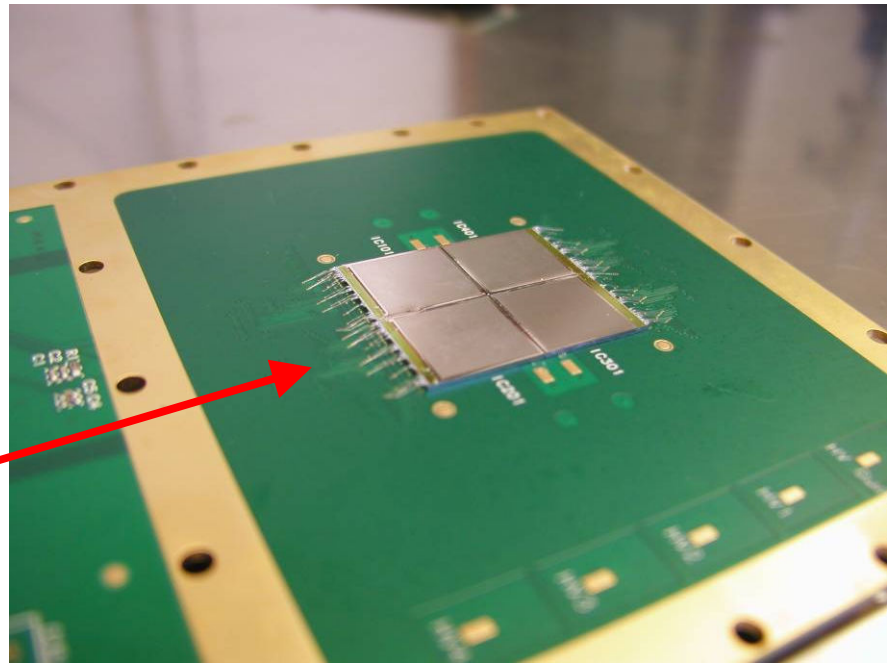
- Waiting for Ingrid → a batch of 8 Ingrids was produced in August'09, but after final probing only 3 were still accessible in readout (under investigation)

- Should be tested on the Large Prototype TPC by the end of this year

NIKHEF: emphasis on Ingrids

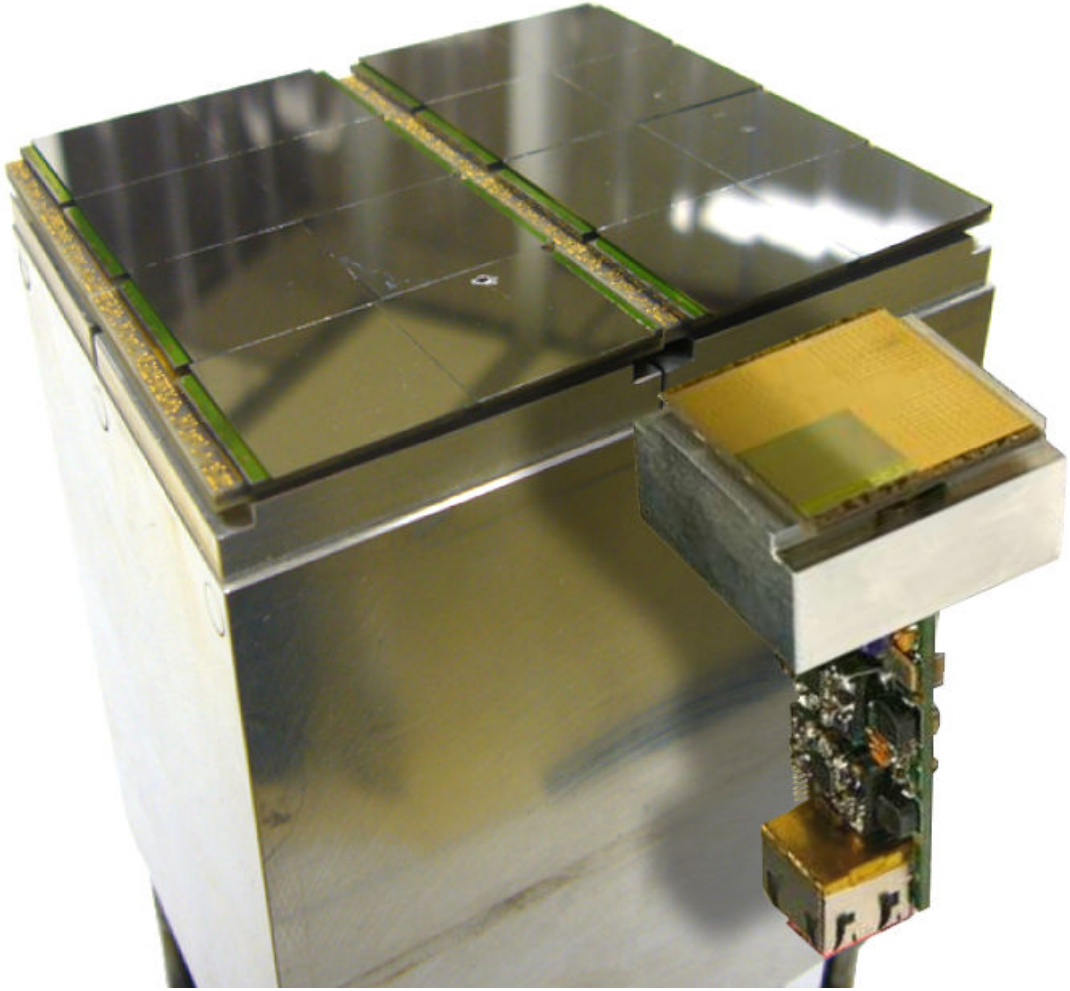


- within Relaxd project: 4x4 Medipix chips in compact mounting
- Will evolve in 8x8 Timepix chips for EUDET



- QUAD chips board tested OK in 2008
- Equiped with Ingrids in June ‘09
- Could become standalone “traveling” TA infrastructure

NIKHEF



- within Relaxd project: 4x4 Medipix chips in compact mounting

- Will evolve in 8x8 Timepix chips for EUDET/LCTPC

Several single chip systems produced for:

- Test detector performance with different thickness of Si_3N_4 protection layers (in DESY T22 beam)

- Test efficiency and resolution in Gossip-like geometry (only 1.5 mm gas layers) in CERN testbeam

- Data analysis in progress
- Sometimes still discharges that kill Timepix chips; some indication it is on the ‘outside’ edges of Ingrid/Timepix

All groups have established contacts with outside institutions for 8” wafer scale post-processing:

- Freiburg Metallforschungszentrum (pixel enlargement)
- IZM Berlin: Ingrid technology
- SMC (Scottish Microelectronics Centre) Edinburgh: Ingrid technology
- LAAS (CNRS) Toulouse (max. 6” wafers)

Conclusions

- SITPC final infrastructure deliverable available (1st "leg") – analysis beam data in progress
- Waiting for sufficient number of Ingrids to equip 2nd "leg"; 8 Ingrids hopefully soon
- Test of 2nd "leg" at LP possibly still before end 2009
- 3rd "leg" with Quad-Ingrid detector(s) ready for tests in coming weeks

- Longer term (end 2010): working on larger systems of 64 and 119 chips