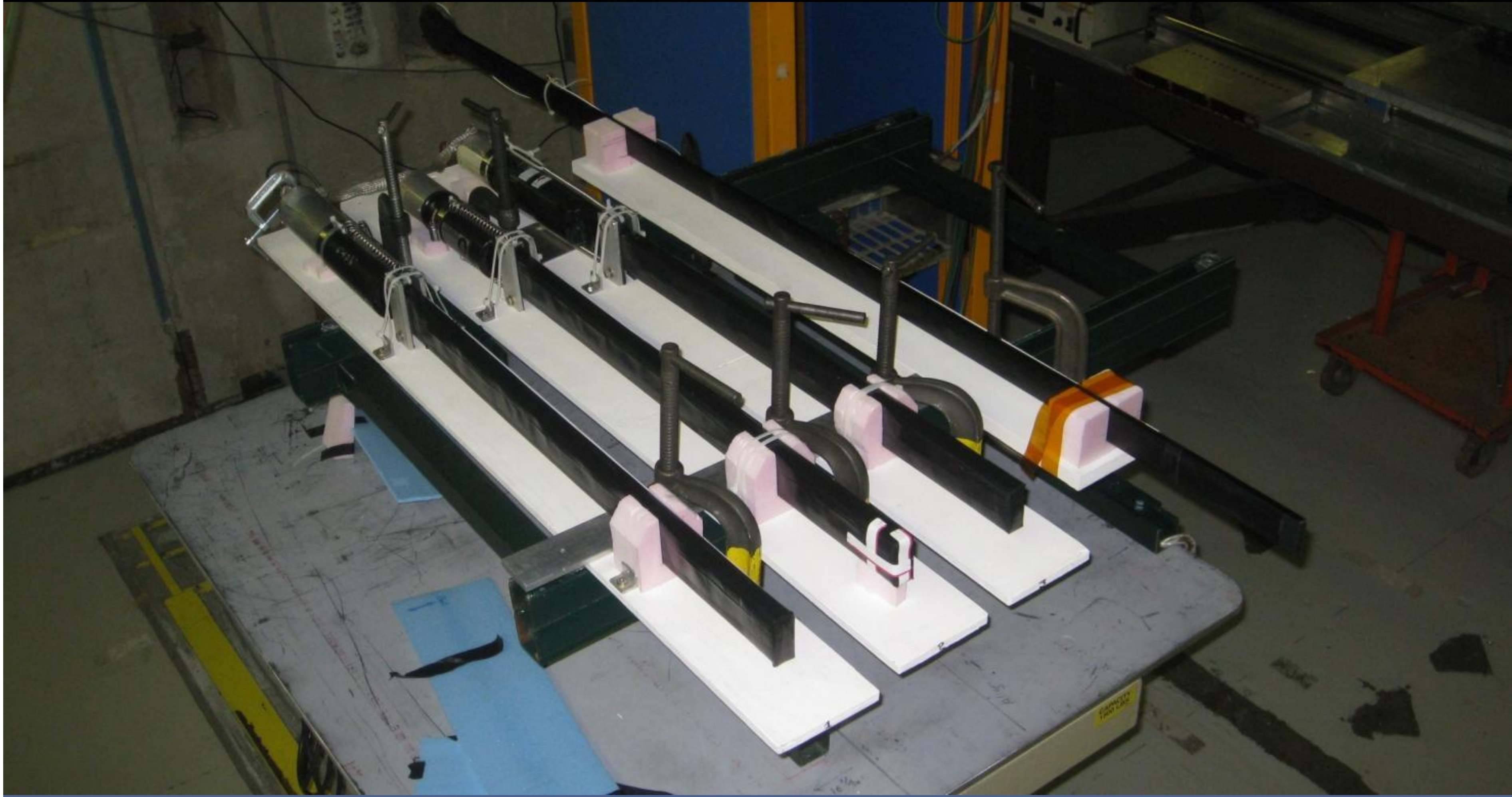
2009 LCW Paul Rubinov Fermilab

PLANS FOR MUON/TAIL CATCHER TEST BEAM AT FERMILAB

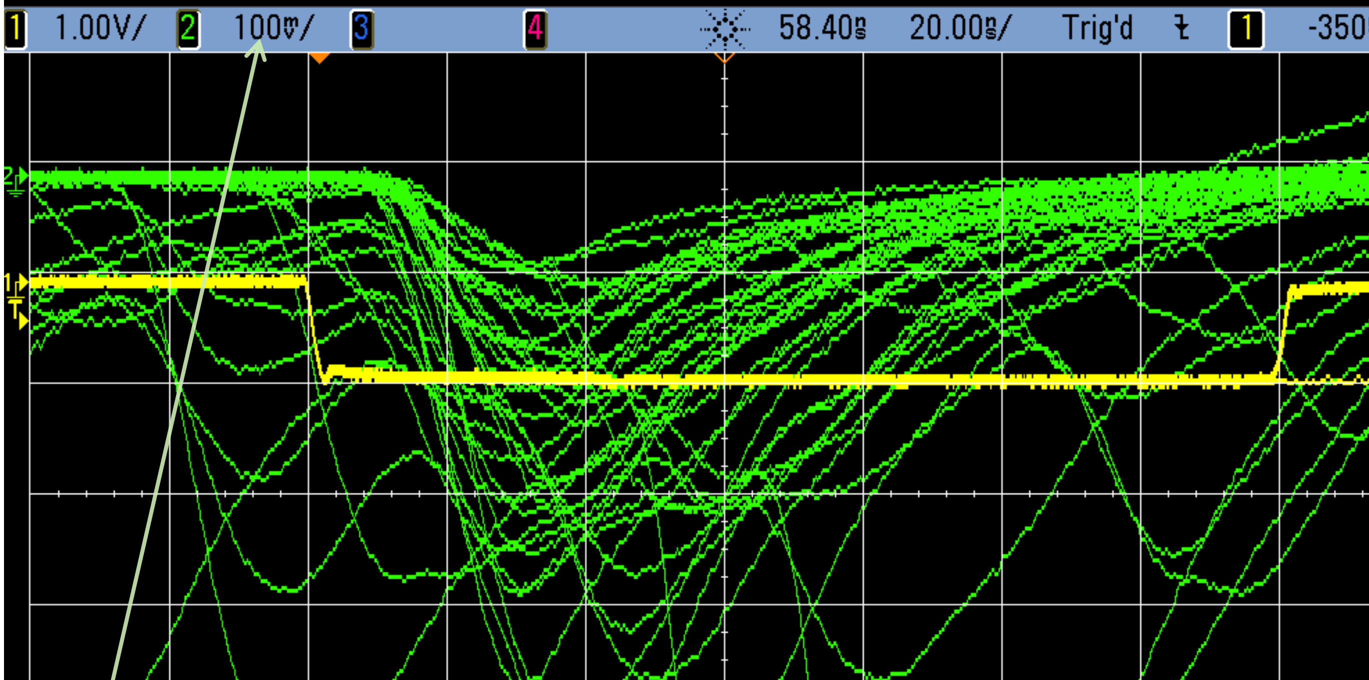
Previously, at MT6

- We did a quick run in 2008 (parasitic with Minerva)

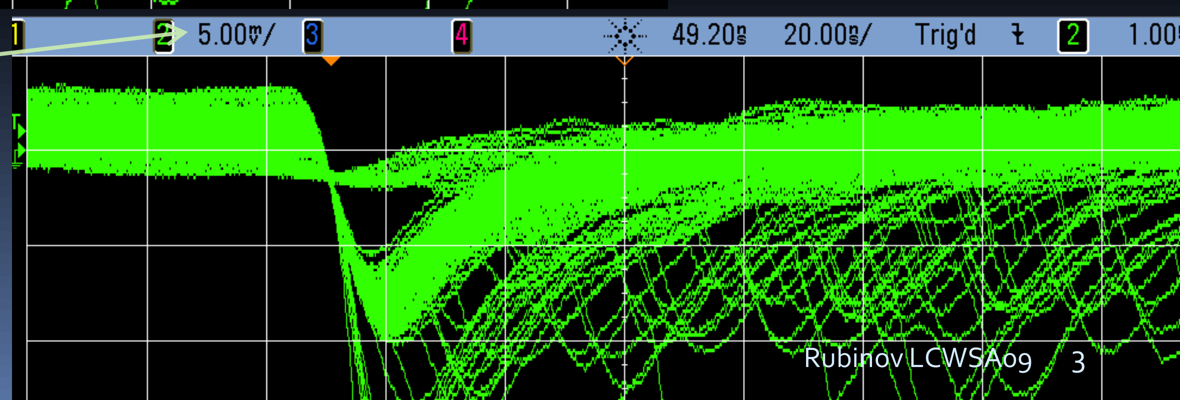


From testbeam

- ~100% Efficient ?! A few hundred traces from 1 spill



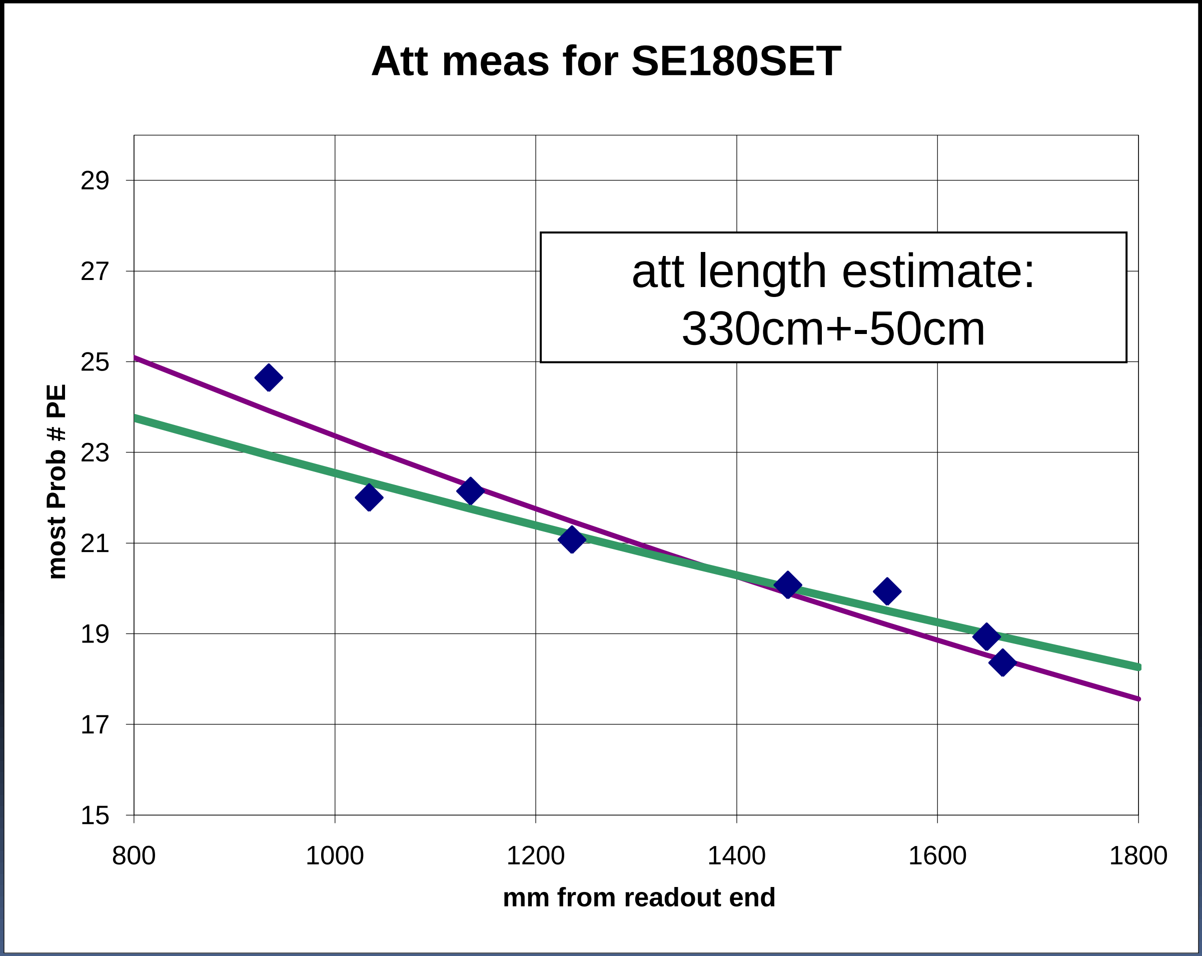
Noise



Don't miss the scale change!

From testbeam

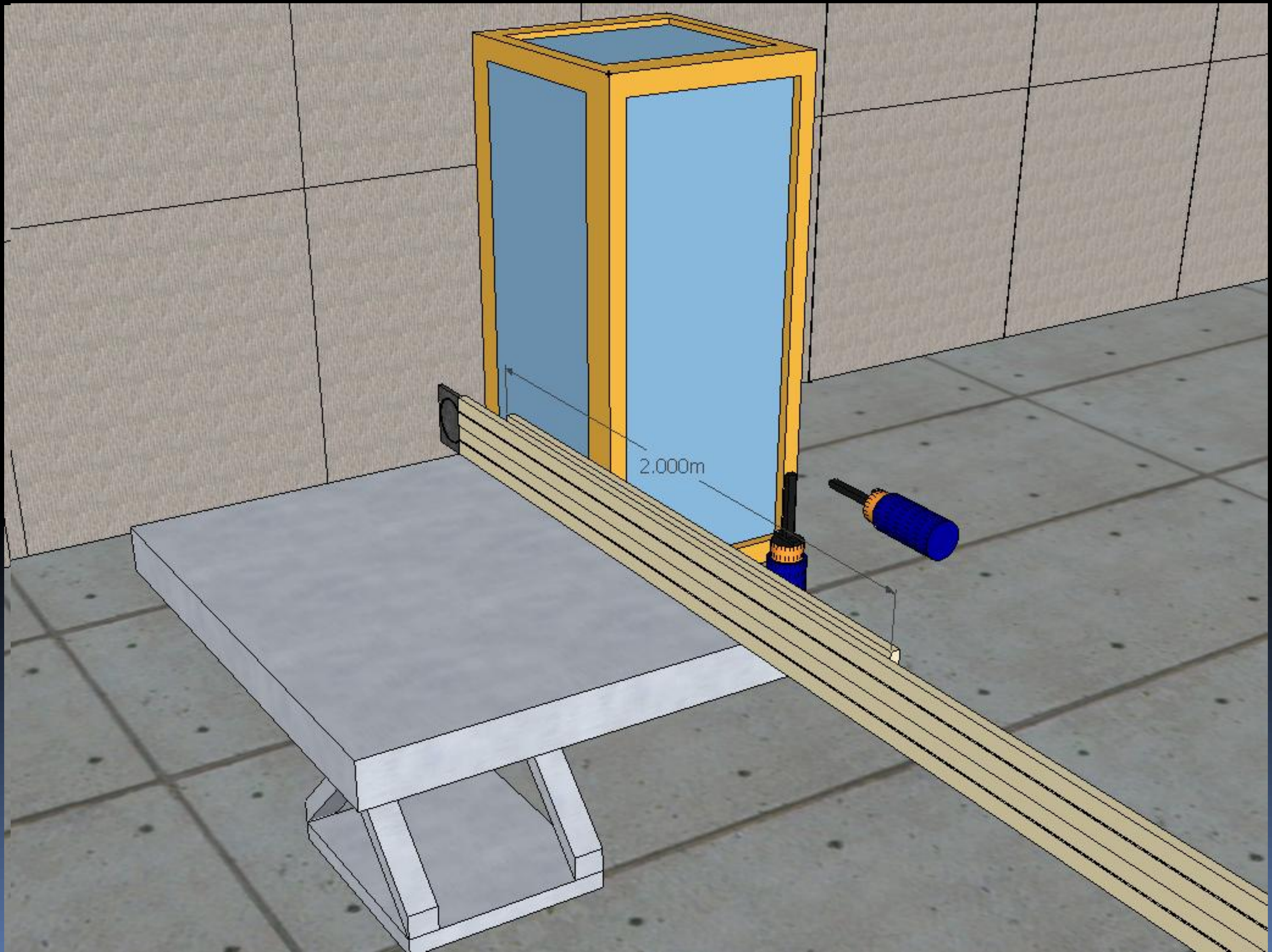
- We even tried to measure attenuation



Need more lever arm!

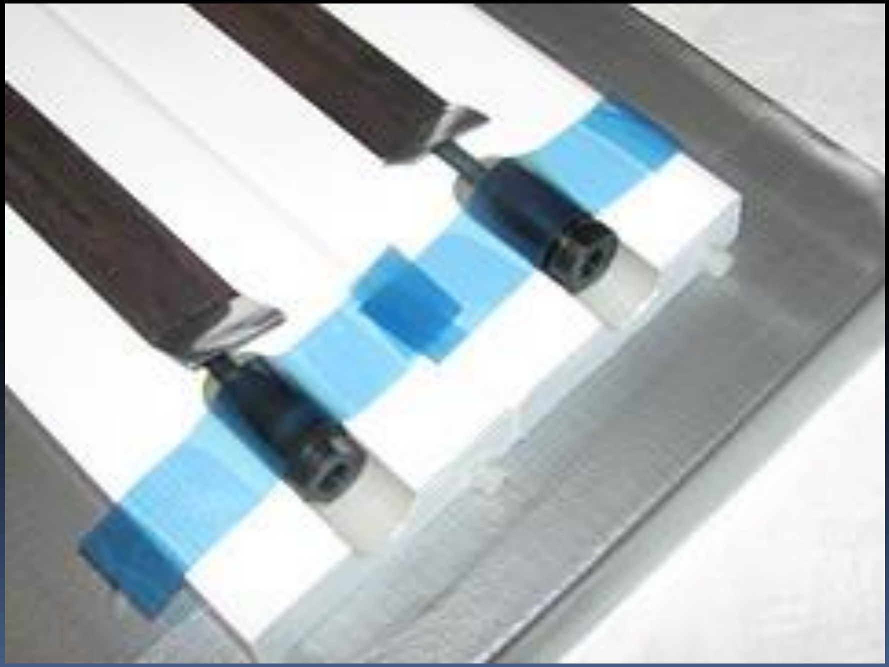
From testbeam

- Sketch of the TB 2008 setup



New tests

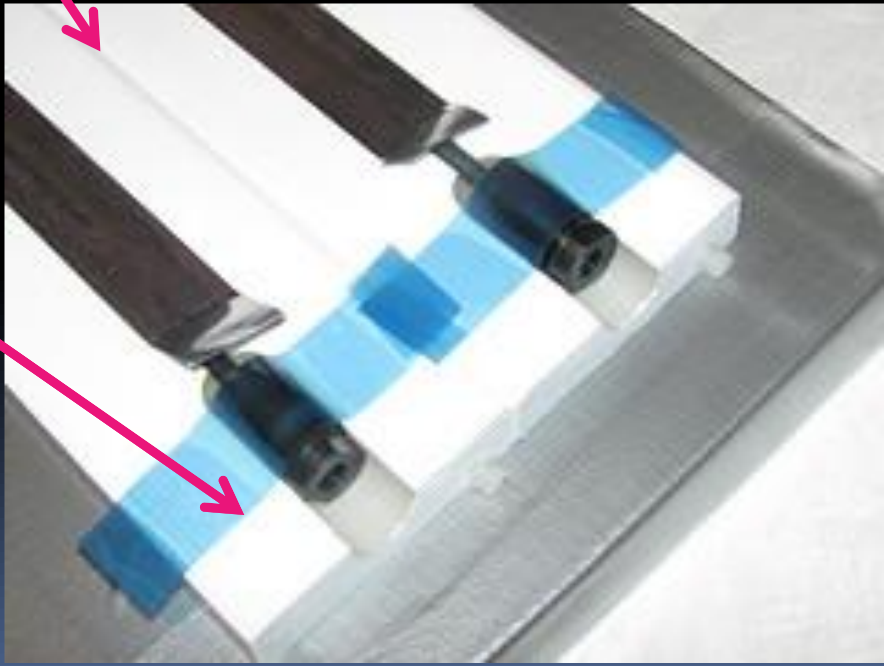
- Want to measure
  - More channels
  - Much longer strips (284 inches)
  - Double ended readout



New tests

- Losses in the crack between adjacent strips
- Losses in scint behind SiPM

MUST KNOW THE POSITION OF PARTICLES PRECISELY



Do we need tracking for Muon TB

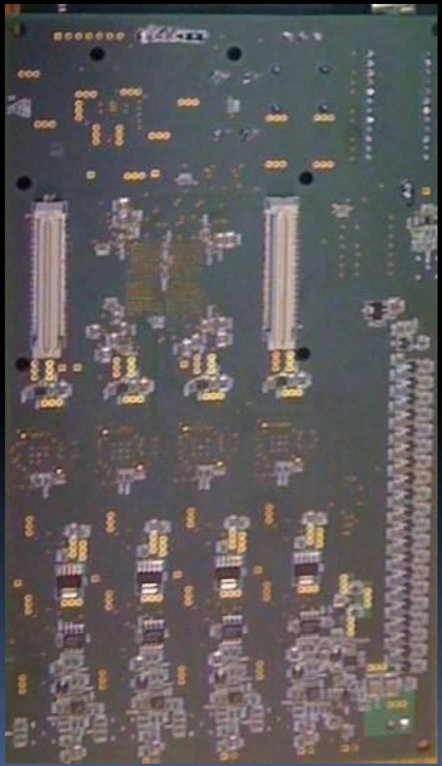
- NO
  - Heterogeneous system – everything different
  - Num of channels goes from 16 or 32 to 1016 or 1032
  - I'm scared of tracking because I'm a wimp
- YES
  - Very good position resolution without hurting rate
  - Very good two track rejection
  - Powerful tool that can be used in future studies
    - E.g. testing of dual readout crystals
  - I'm scared of tracking because I'm a wimp

New tools

- New strips
- New electronics – my main emphasis

New since LCW08

- Our plan for readout was (and is)
  - Fall 08: just an amplifier in a NIM bin using 50ohm cables
  - Spring 09: Integrate amp, ADC, bias on one board
  - Fall 10?: SiPM readout ASIC
- New electronics ready to go for TB
  - A board that strikes a good balance of high performance and reasonable cost to support SiPM studies
  - self sufficient, simple to use and flexible
  - reuse known designs whenever possible.

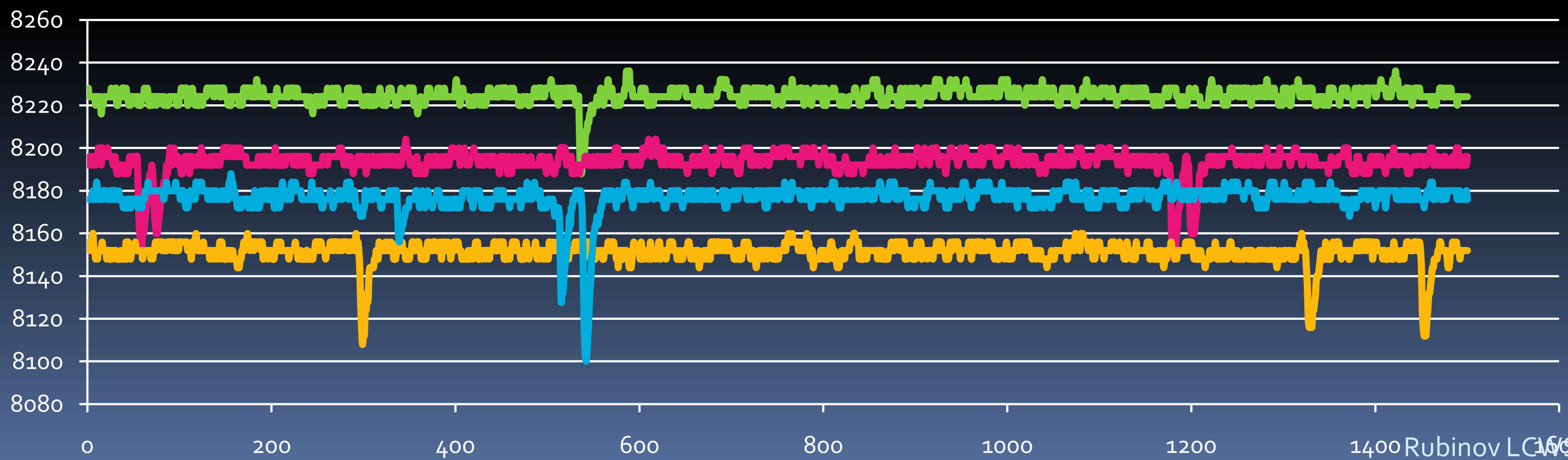


TB4

TB4 key features

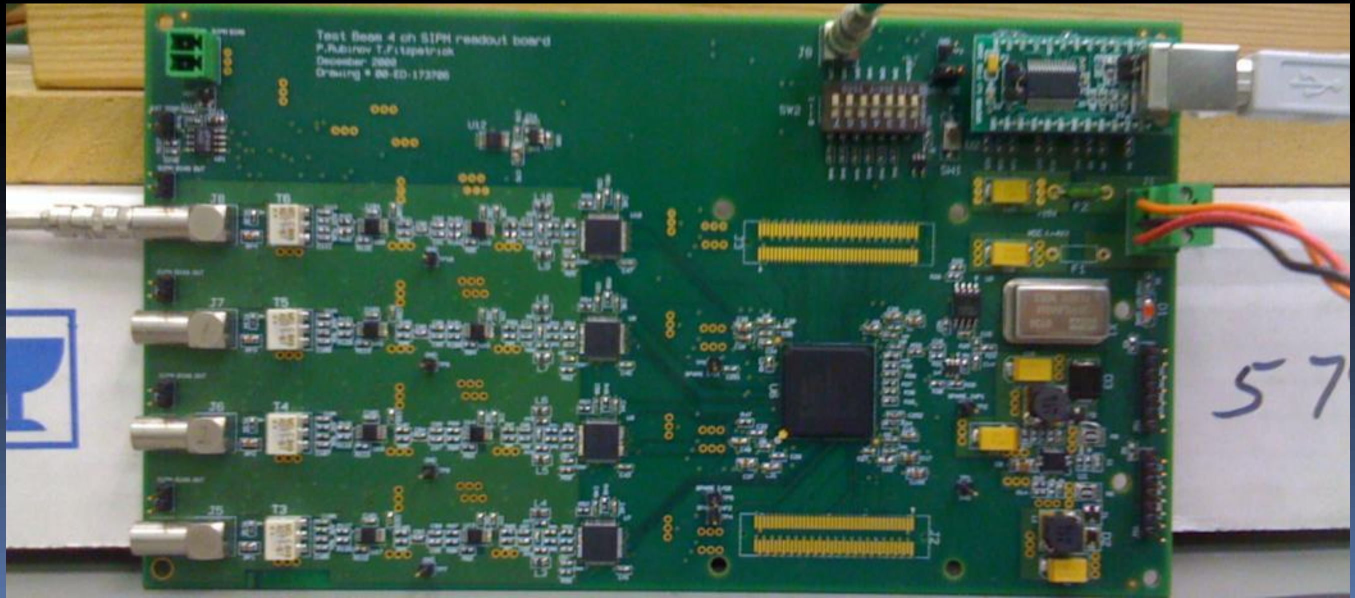
~$1K for 210MSPS 12bit
~$1.2K for 14bit

- Works like a 4ch of digital scope, but one that has a 0.5mV/DIV scale and precision 100V power supply
  - 12 or 14 bit, 210 or 250 MSPS, gain up to ~40db
  - Largish FPGA (with 4kpts memory/ch)
  - USB interface, High Speed i/o
  - On board bias generation for SiPMs (and current meas)



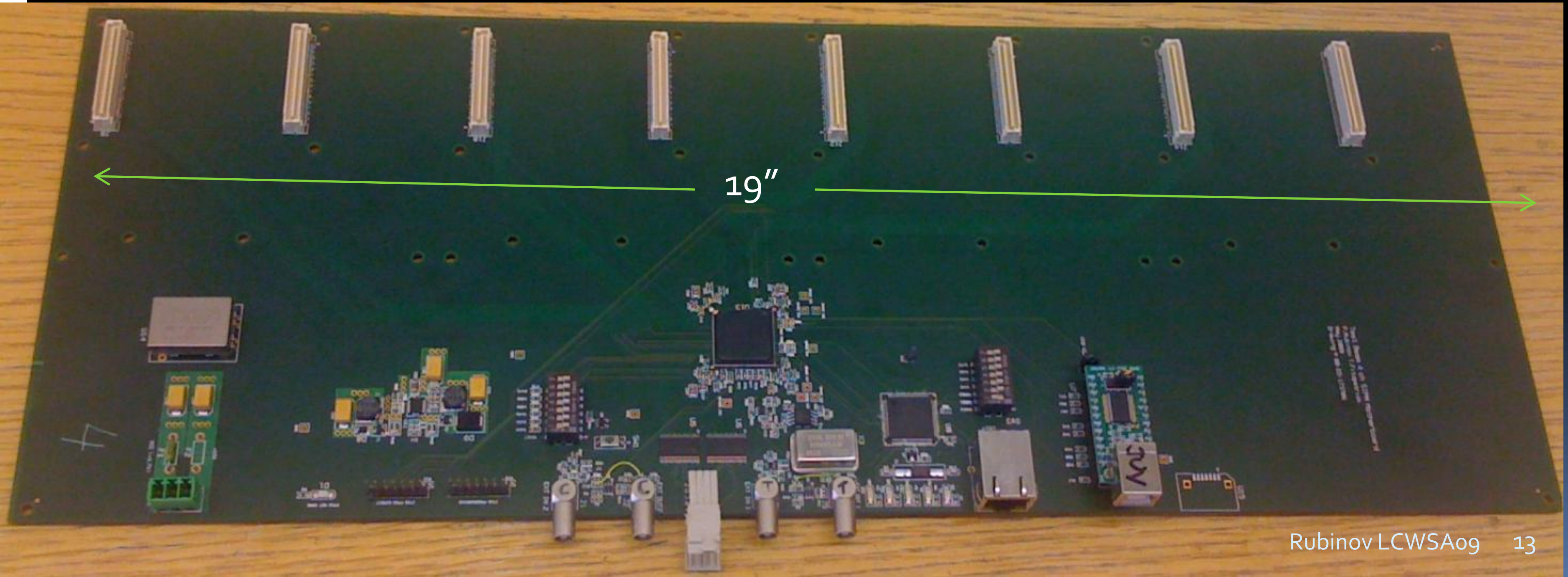
Emphasis on simple

- Plug in 5V/15V power
- Plug in SiPM into an end of a 50 ohm cable
- Plug the other end of the cable into the TB4 board
- Plug in the USB connector into your computer
- Start the software, and press the RUN button



TB4 continued

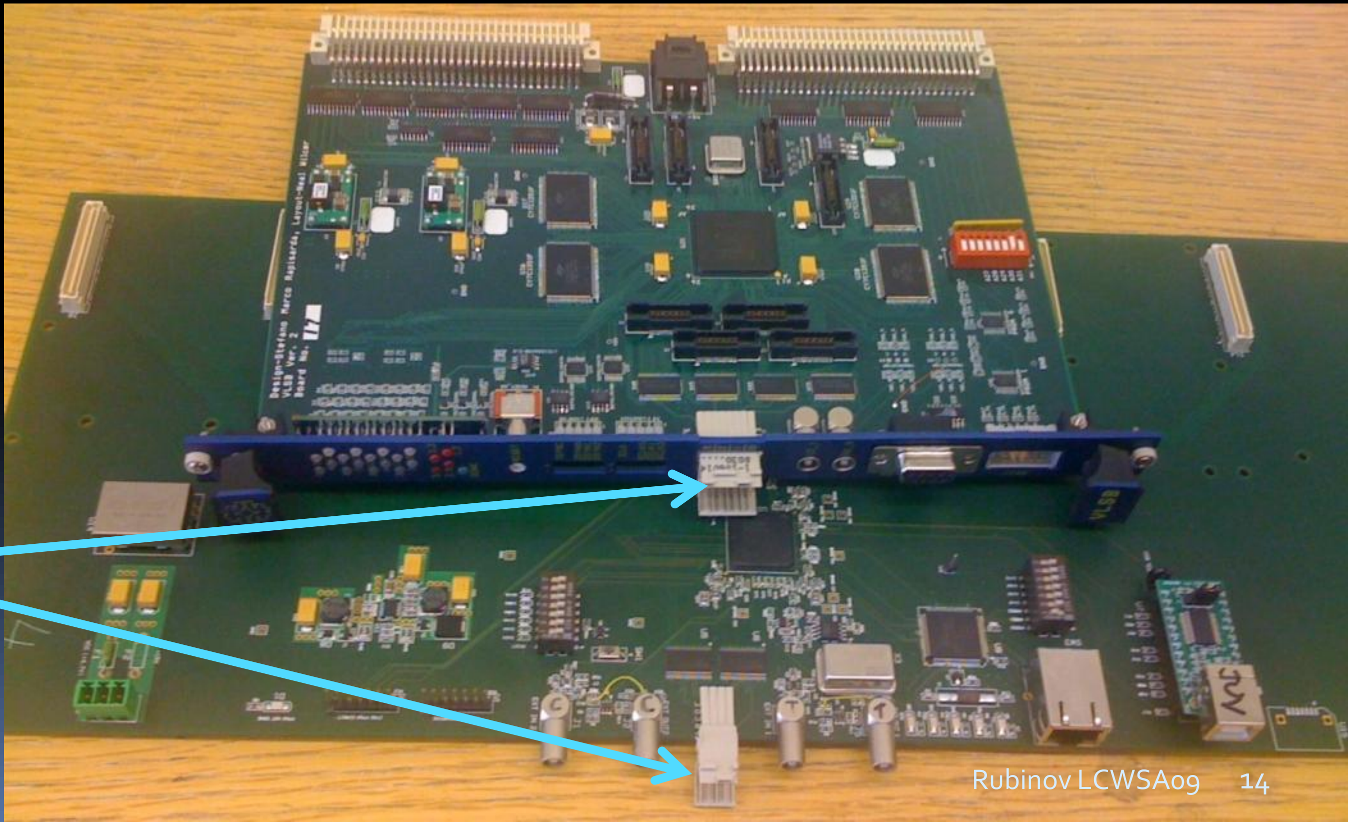
- For slightly larger applications, like test beam
  - 4x TB4 combined on 1 motherboard
  - Mother board provides:
    - Ethernet interface, USB interface, triggering, clocking
    - High speed LVDS (2 x 1 Gbps)

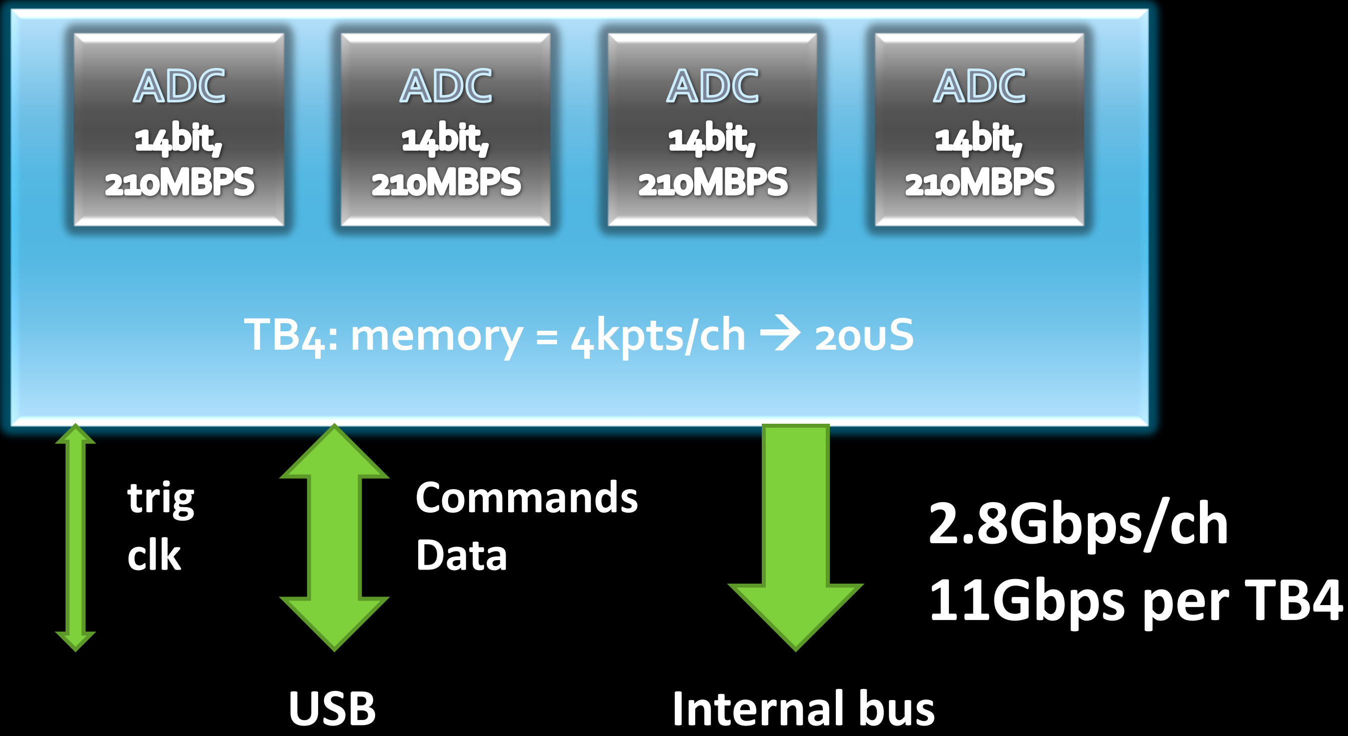


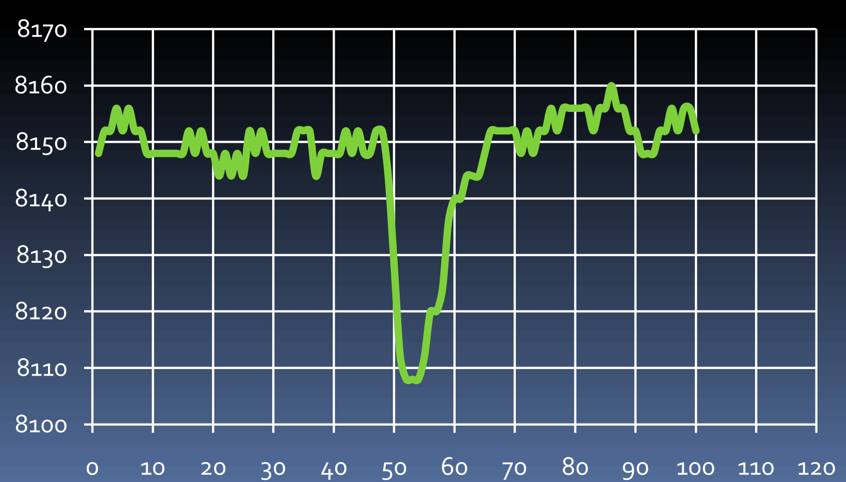
TB4 continued

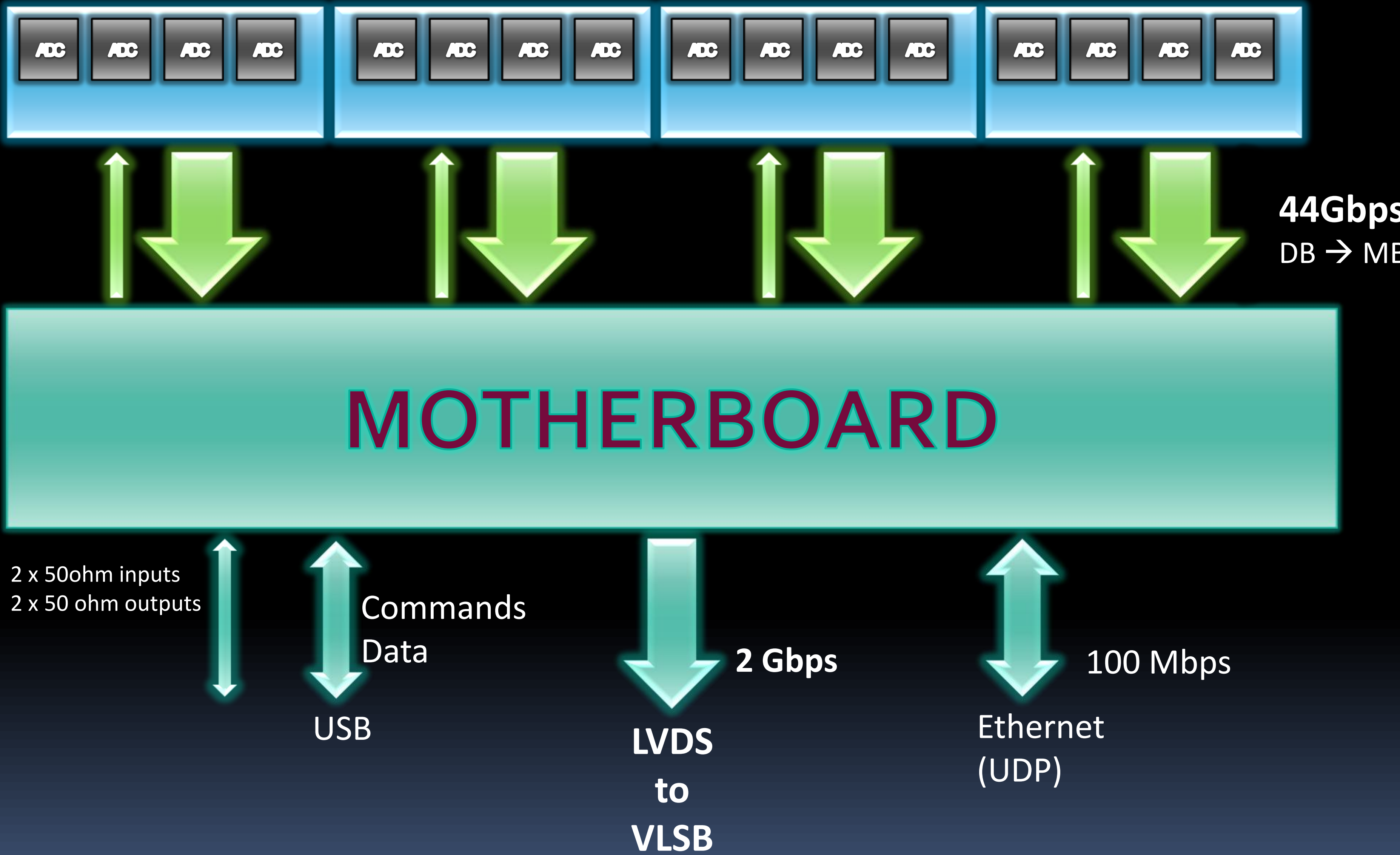
- For fast readout: LVDS links (2 x 1 Gbps) go to a VME module (1 module has 4 links) with sufficient memory (512KB) to act as a buffer for better throughput

LVDS links run from MB to VLSB
(old Dzero module left over from AFE2 project)

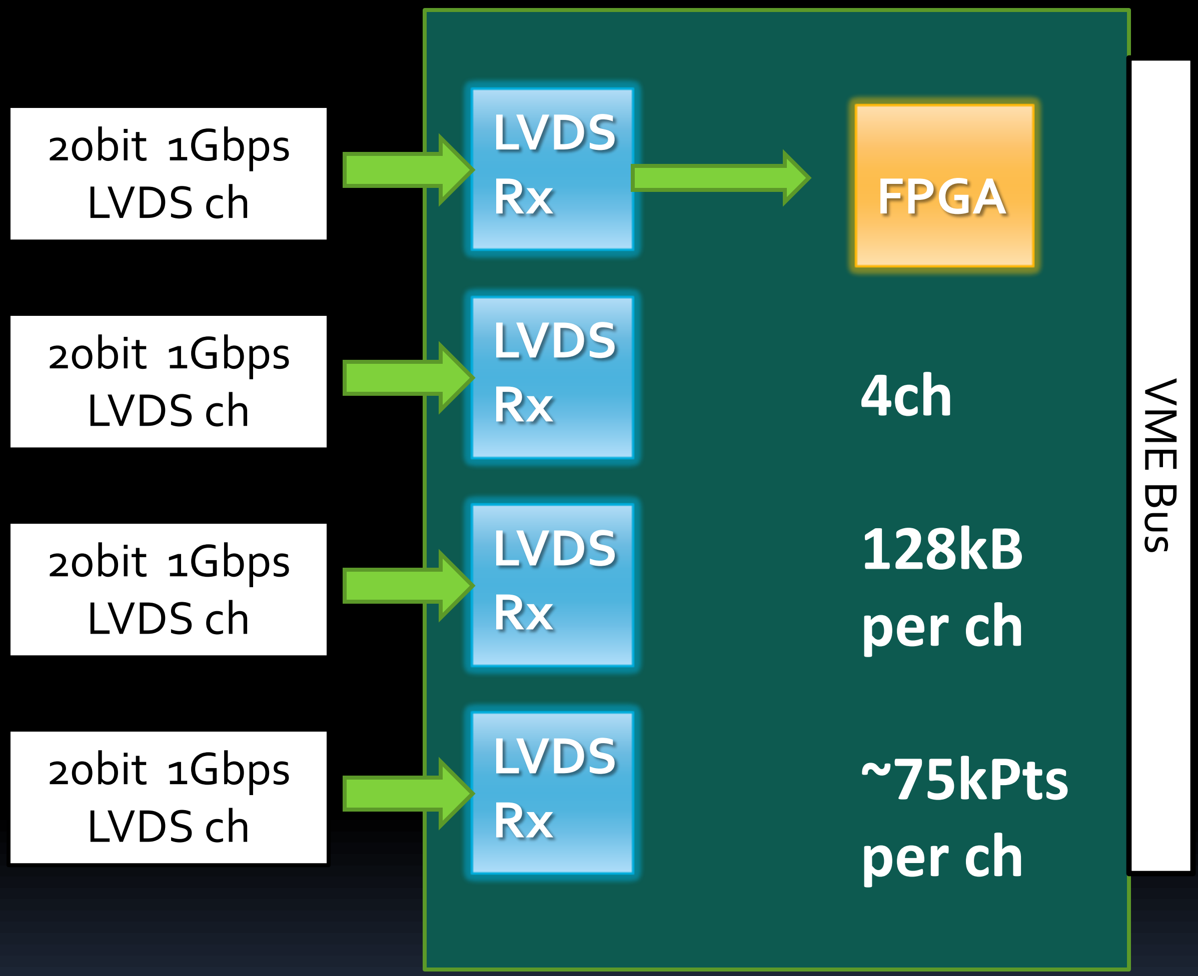



ADC
14bit,
210MBPS
ADC
14bit,
210MBPS
ADC
14bit,
210MBPS
ADC
14bit,
210MBPS
TB4: memory = 4kpts/ch → 20uS
trig
clk
Commands
Data
2.8Gbps/ch
11Gbps per TB4
USB
Internal bus


8170
8160
8150
8140
8130
8120
8110
8100
0
10
20
30
40
50
60
70
80
90
100
110
120


ADC
MOTHERBOARD
44Gbps
DB → MB
2 x 50ohm inputs
2 x 50 ohm outputs
Commands
Data
USB
2 Gbps
LVDS
to
VLSB
100 Mbps
Ethernet
(UDP)

VLSB



VLSB can buffer 300k Samples

Numerology

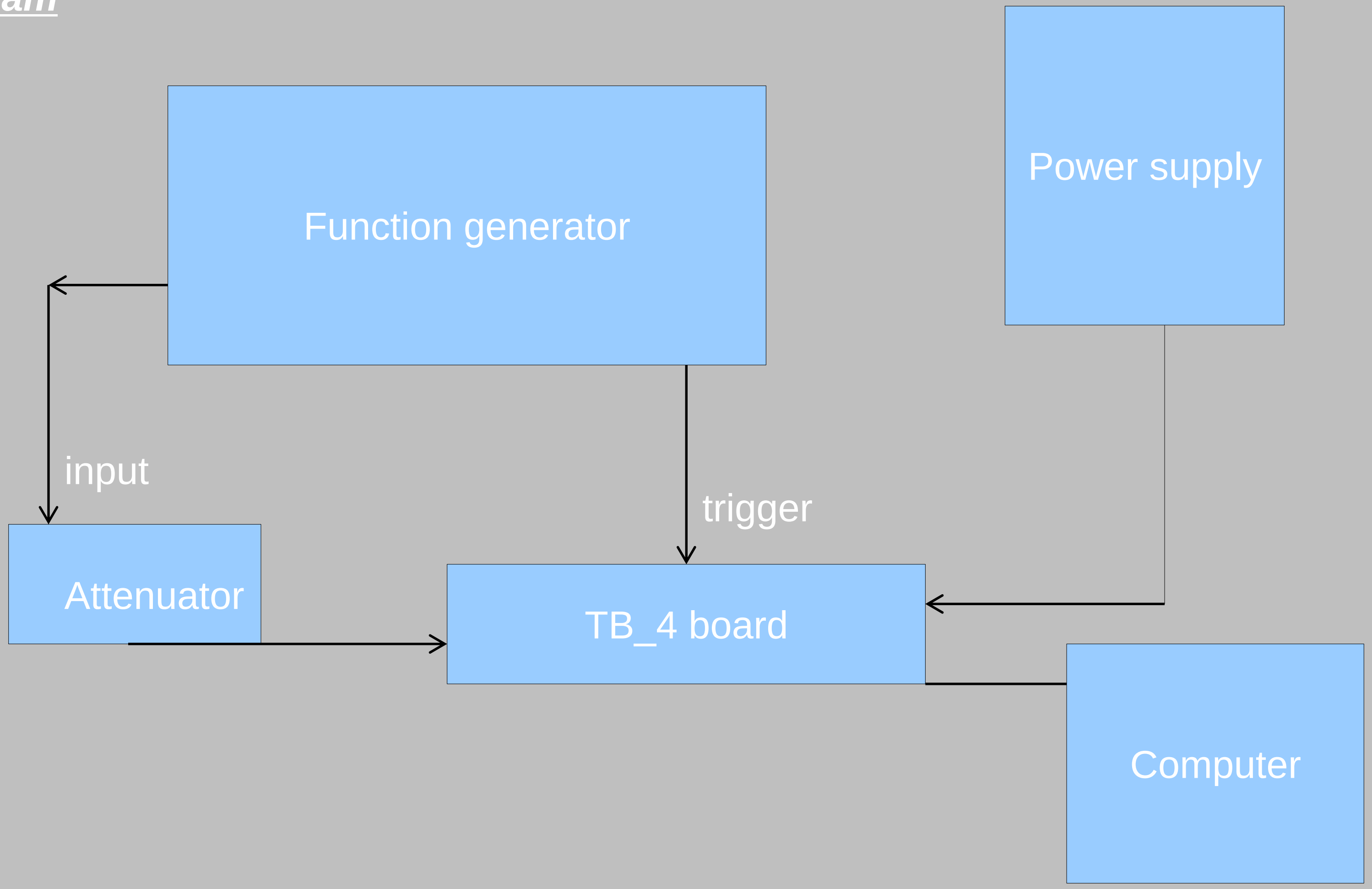
- Realistically for TB:
  - 16ch → 1MB
  - ~100 pts per trig storage
  - 1 MB and 1 VLSB with 2 links
  - Can store about 180 triggers
  - read only between spills
- Worst case
  - Assume ~200 pts/ch per trig
  - 2 Motherboards per VLSB (means VLSB can buffer 45 trig)
- Decent readout during spill (~10MB/s over VME32) to get ~100Hz rate required

Needs and next steps

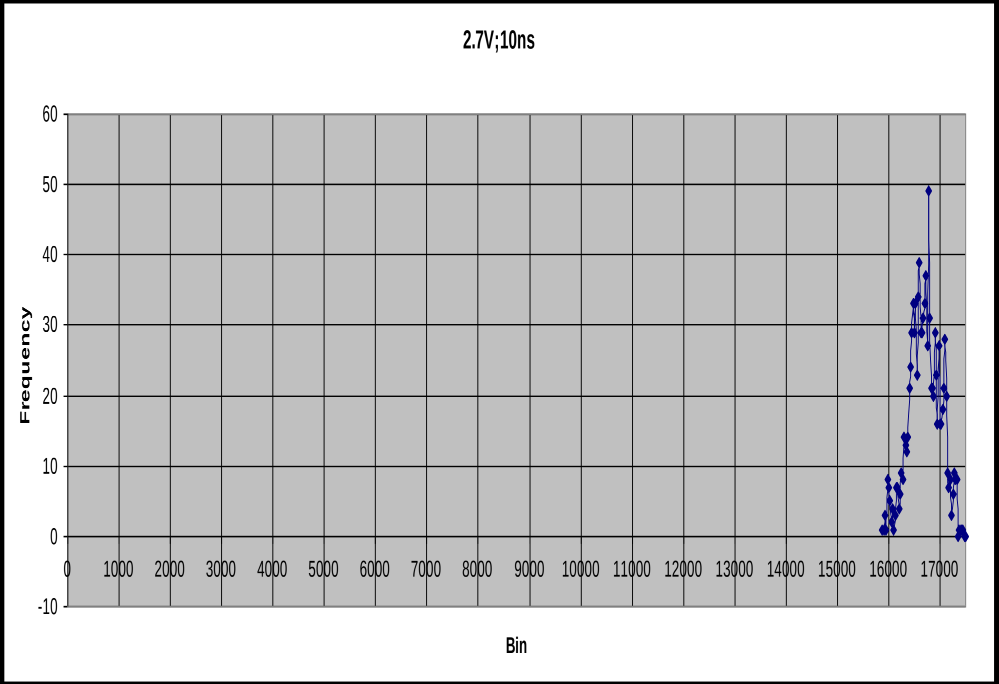
- Muon beam, by its nature, is easy to share
  - We need to reach out to other potential users
- Complete MOU with Fermilab TBF
  - Formalize our needs and institutional responsibilities

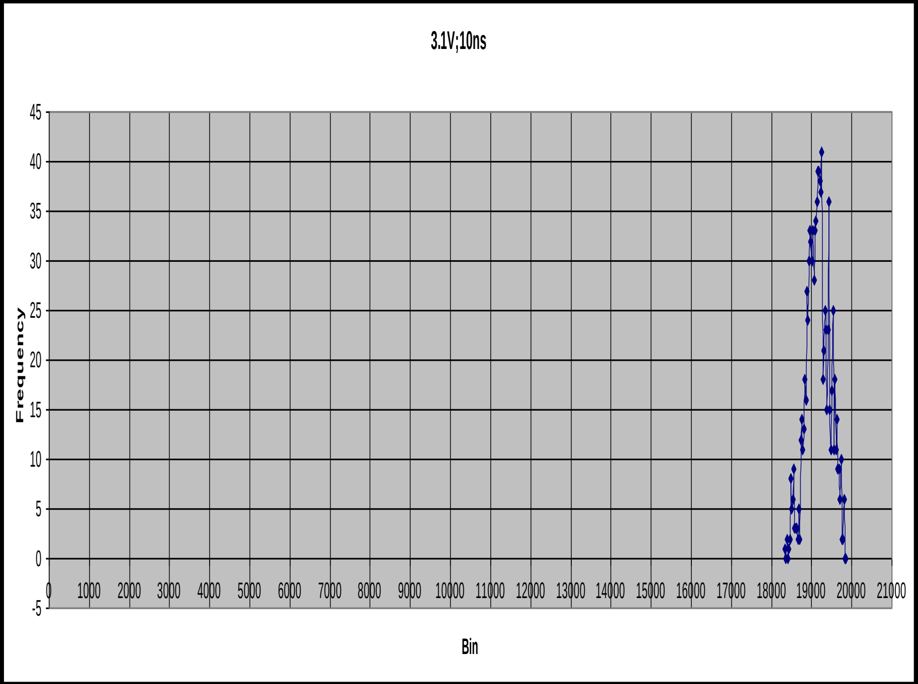
END
OF
TALK

Block Diagram

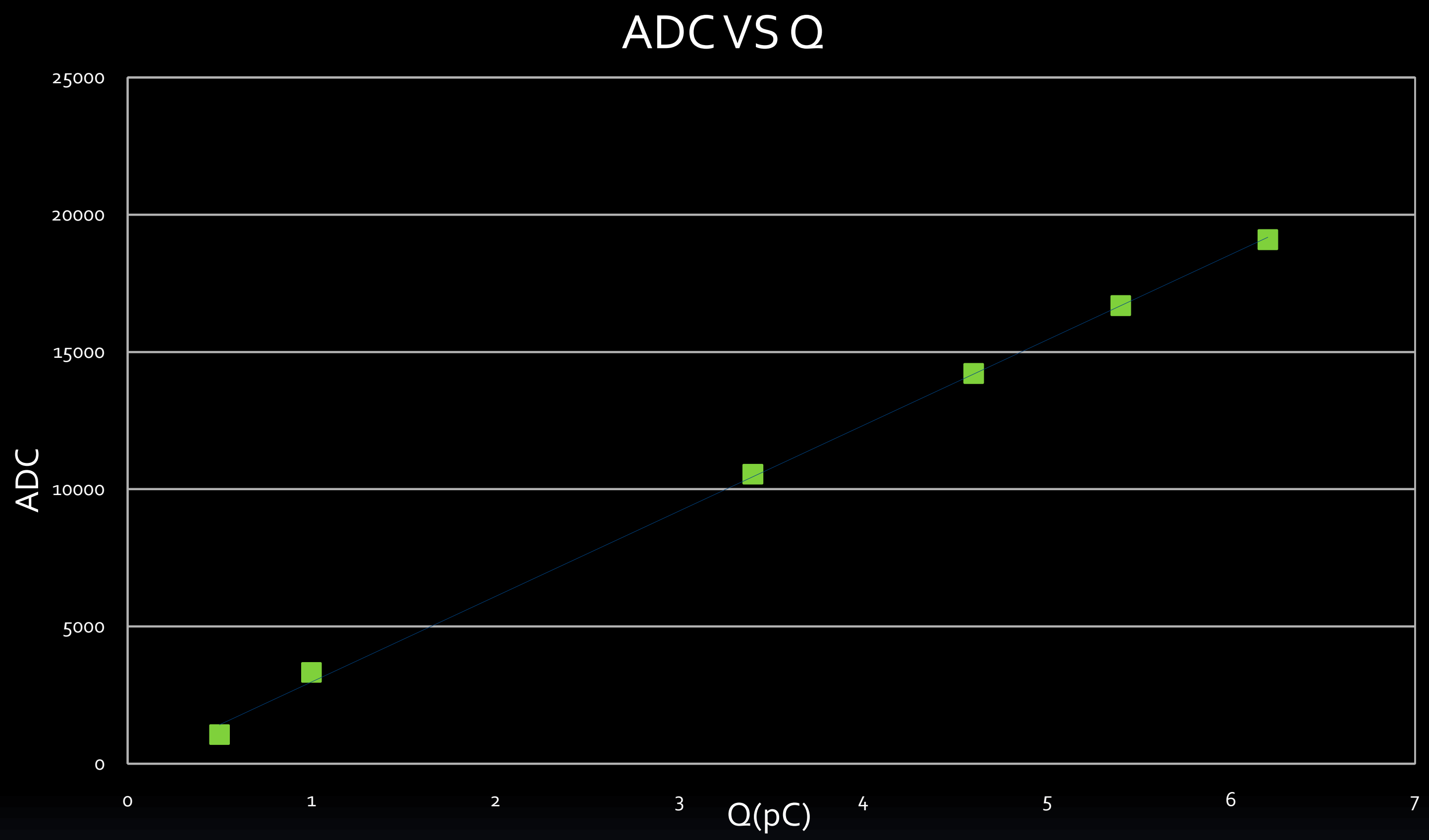


Function Generator: Tektronix AFG 3252
Power Supply : Kenwood





Amplitude (V)	Input Charge (pC)	Mean charge Counts (ADC)	1ADC (fC)
0.25	0.5	1057.00	0.331
0.5	1.0	3324.15	0.300
1.7	3.4	10550.00	0.322
2.3	4.6	14216.00	0.323
2.7	5.4	16688.50	0.323
3.1	6.2	19094.50	0.324

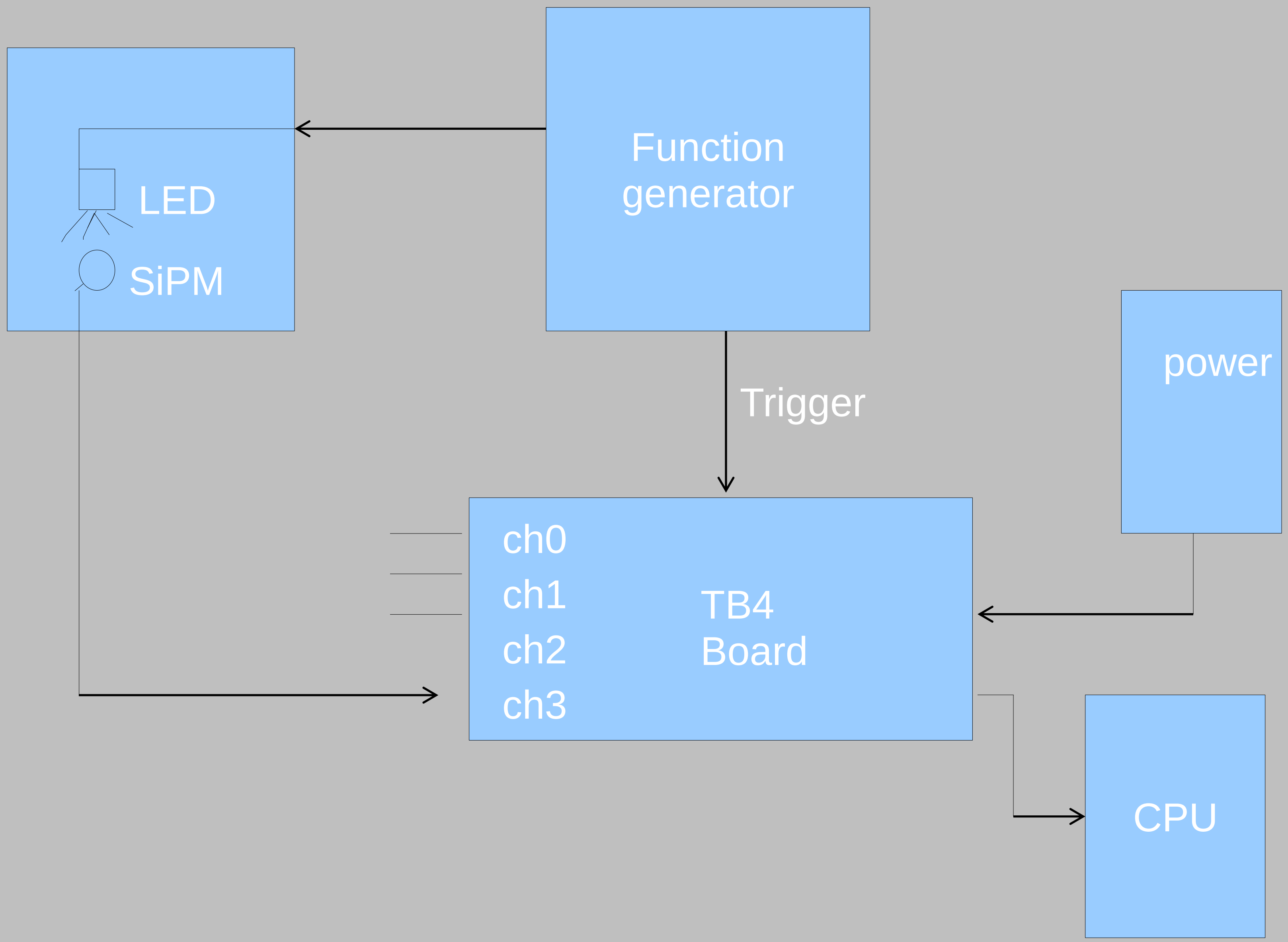


Inverse of the slope gives charge per channel

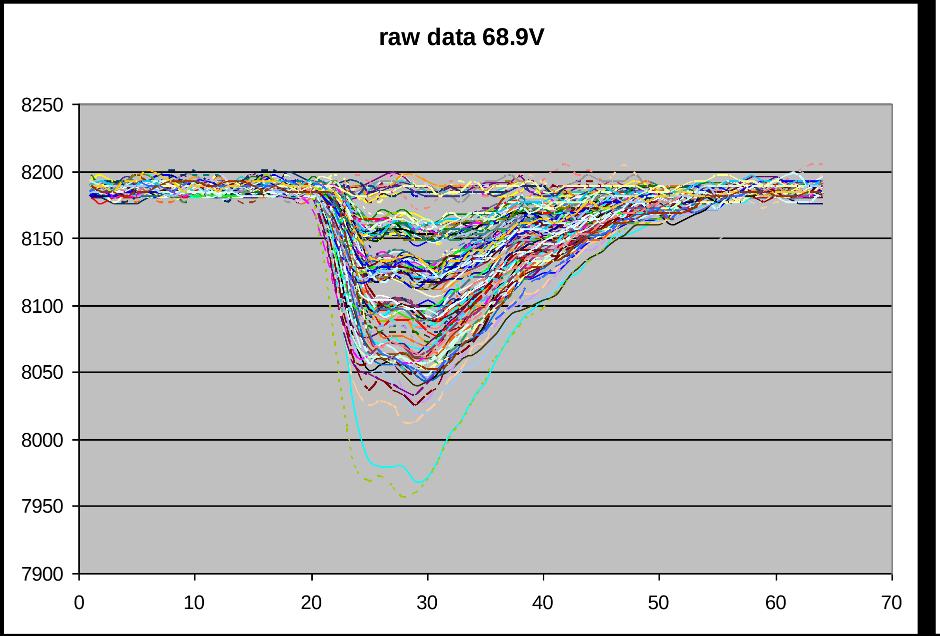
(slope)^-1 = 0.329fC/Channel

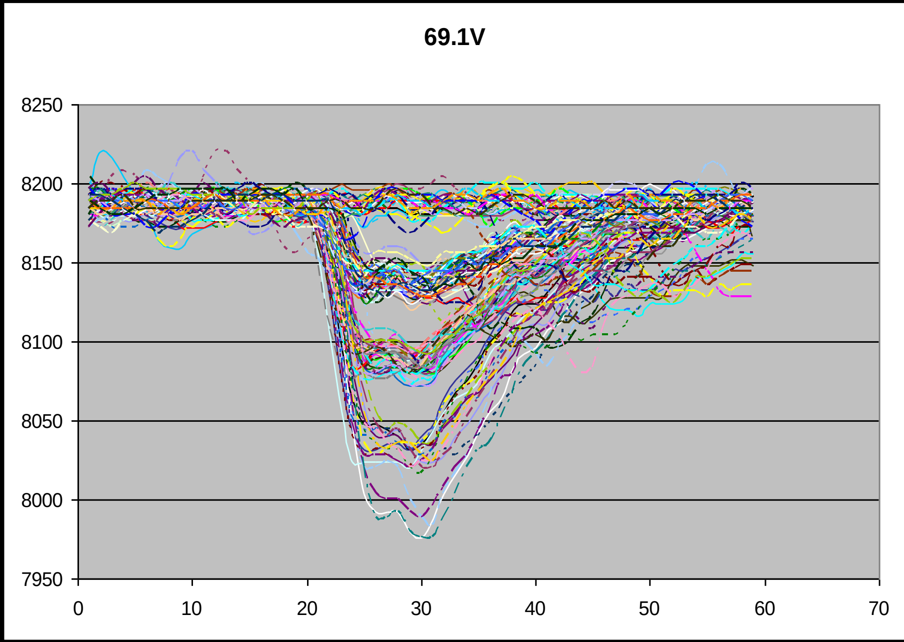
Therefore, 1ADC count = 0.329fC

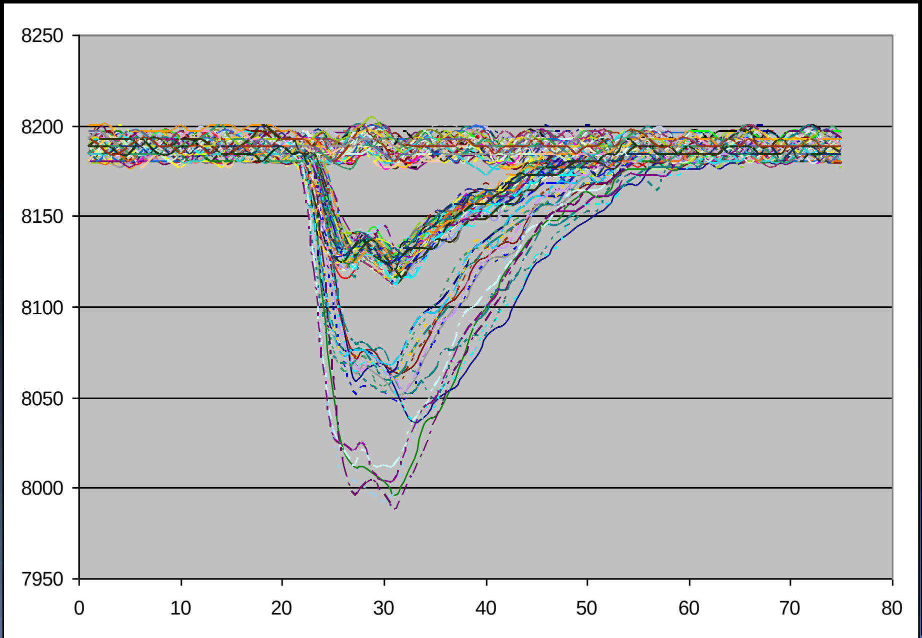
Block Diagram

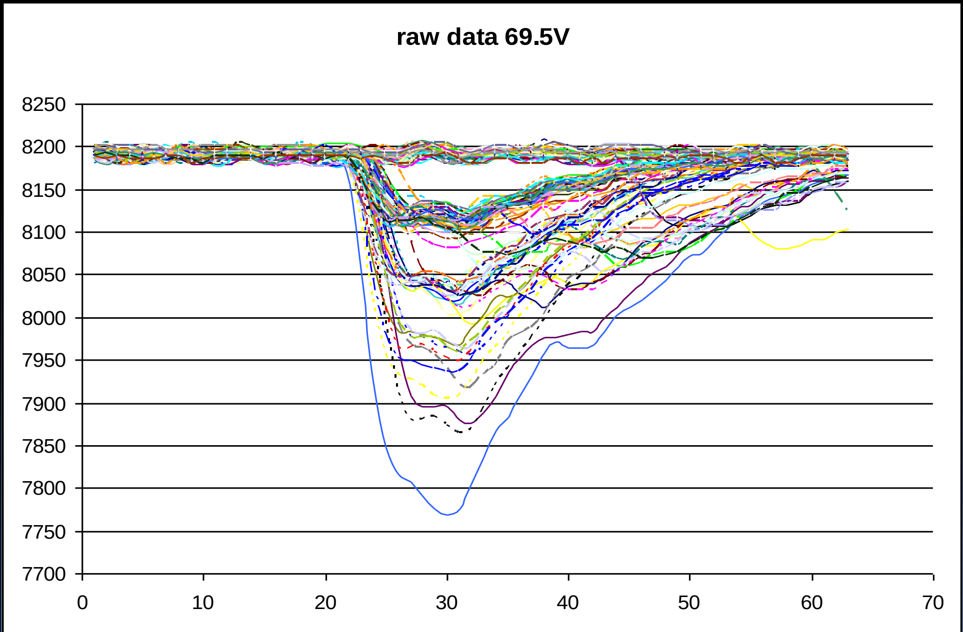


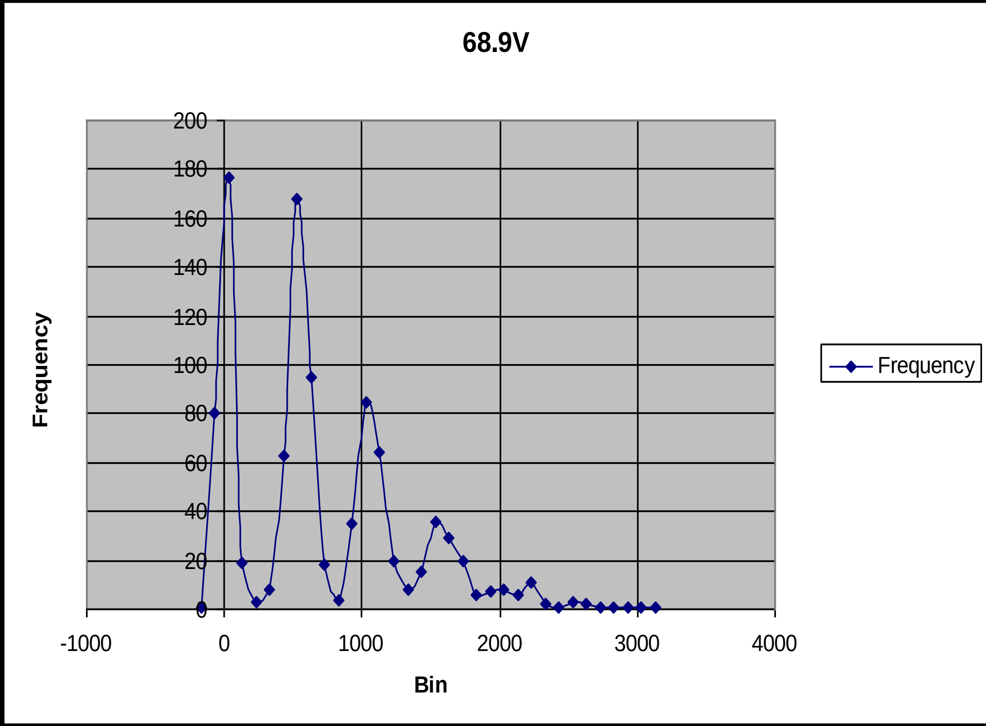
Hamamatsu100 SiPM Plots and Gain calculations

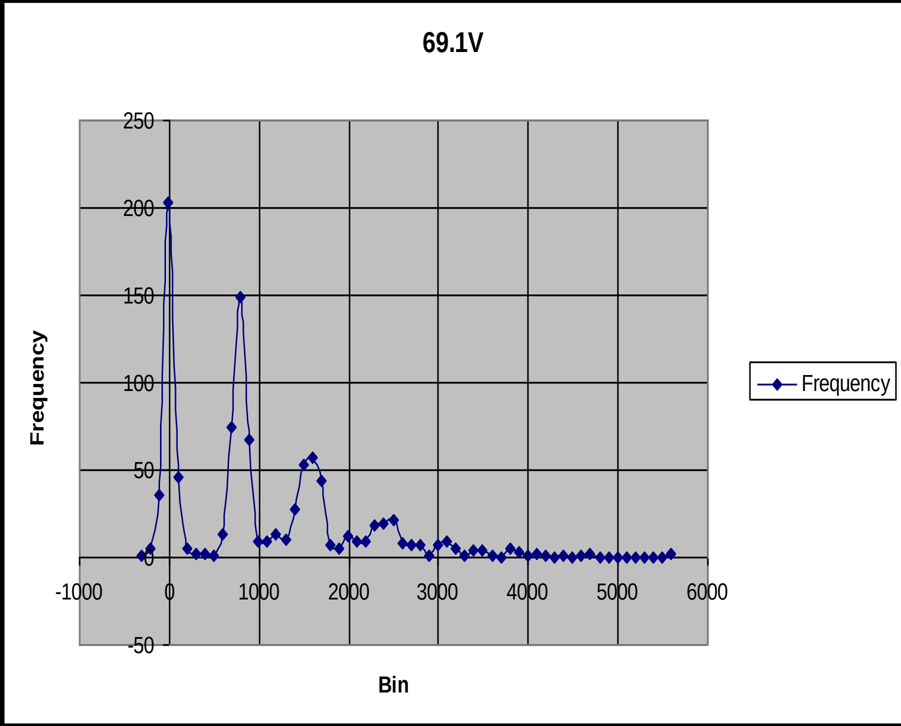


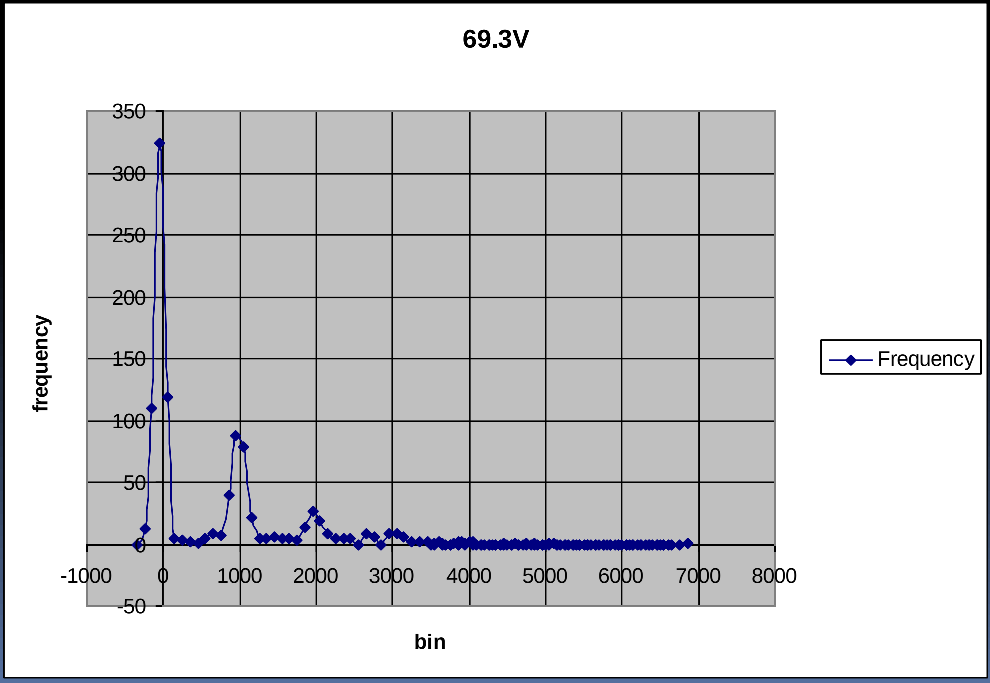


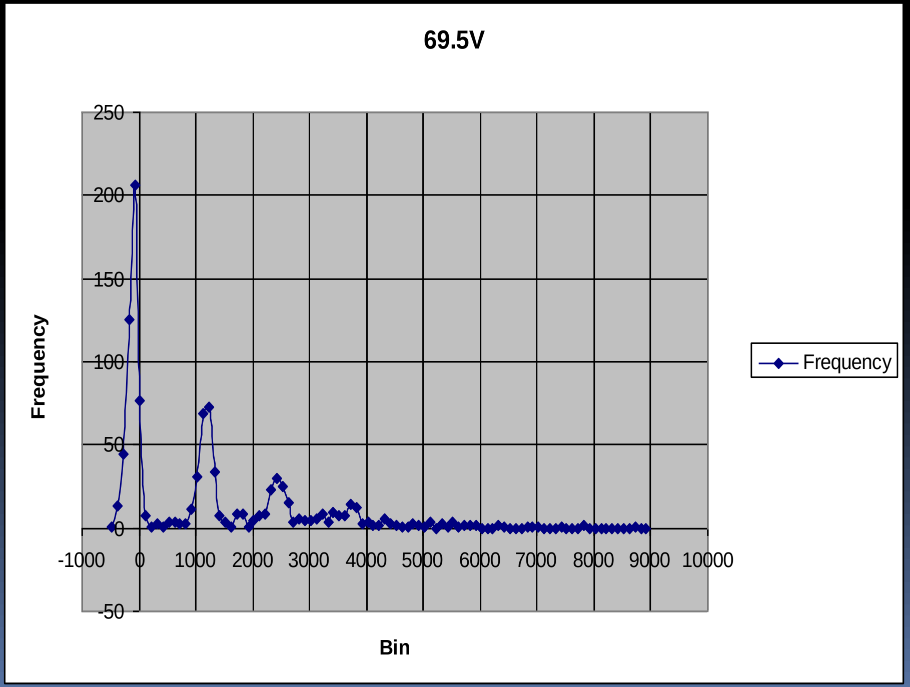


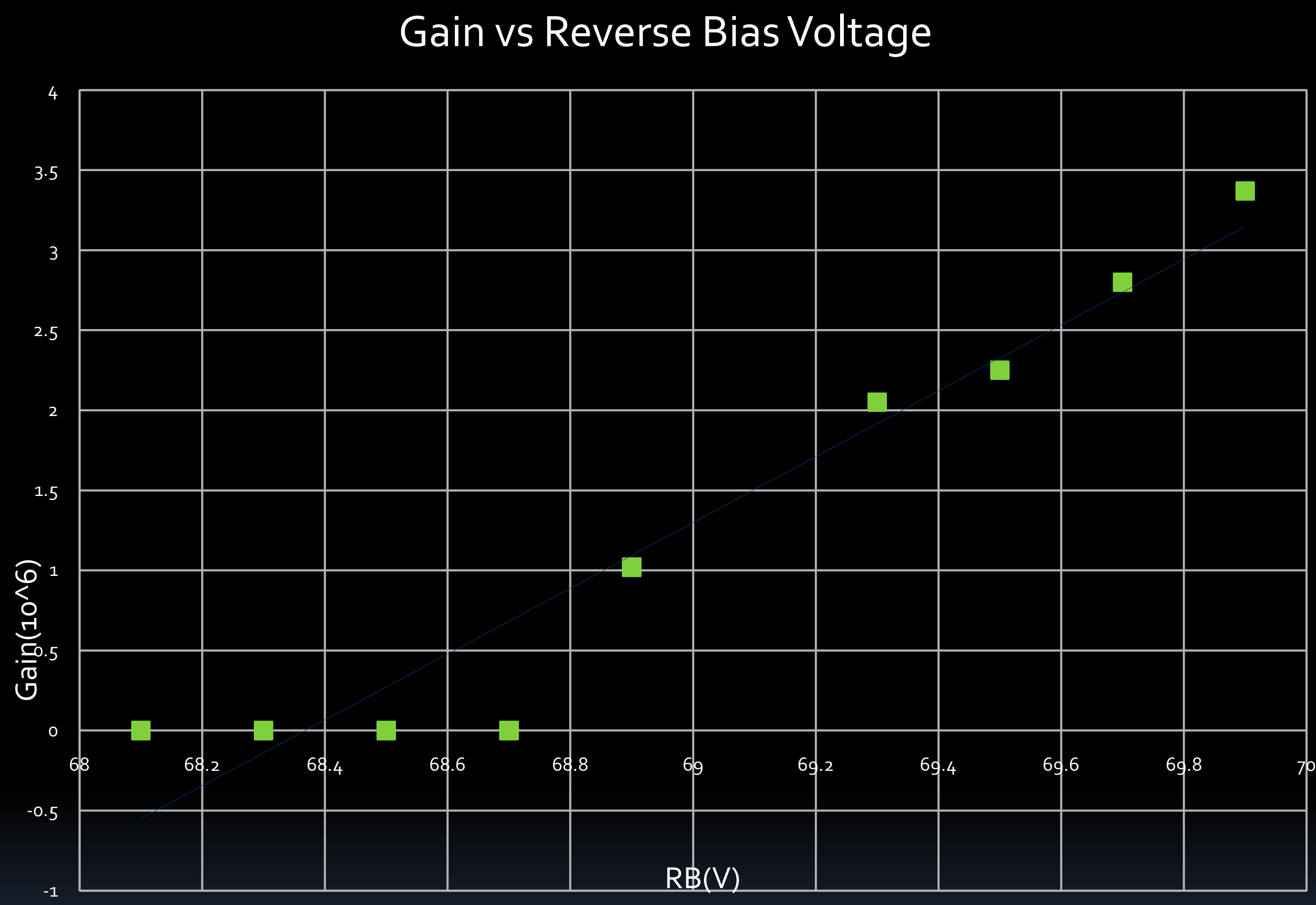



68.9V
Frequency
Bin
Frequency
200
180
160
140
120
100
80
60
40
20
0
-1000
0
1000
2000
3000
4000

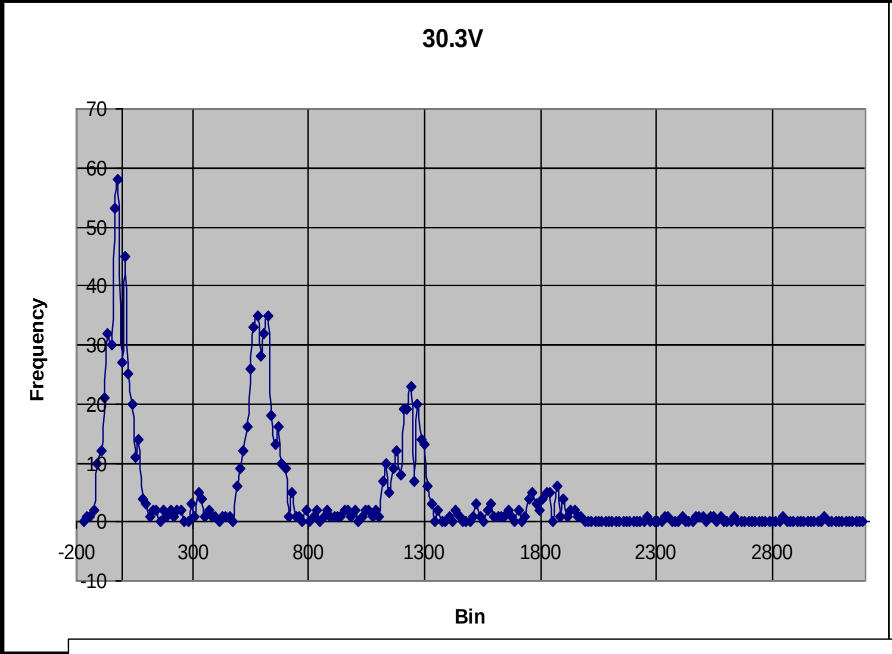

69.1V
Frequency
Bin
Frequency
250
200
150
100
50
0
-50
-1000
0
1000
2000
3000
4000
5000
6000

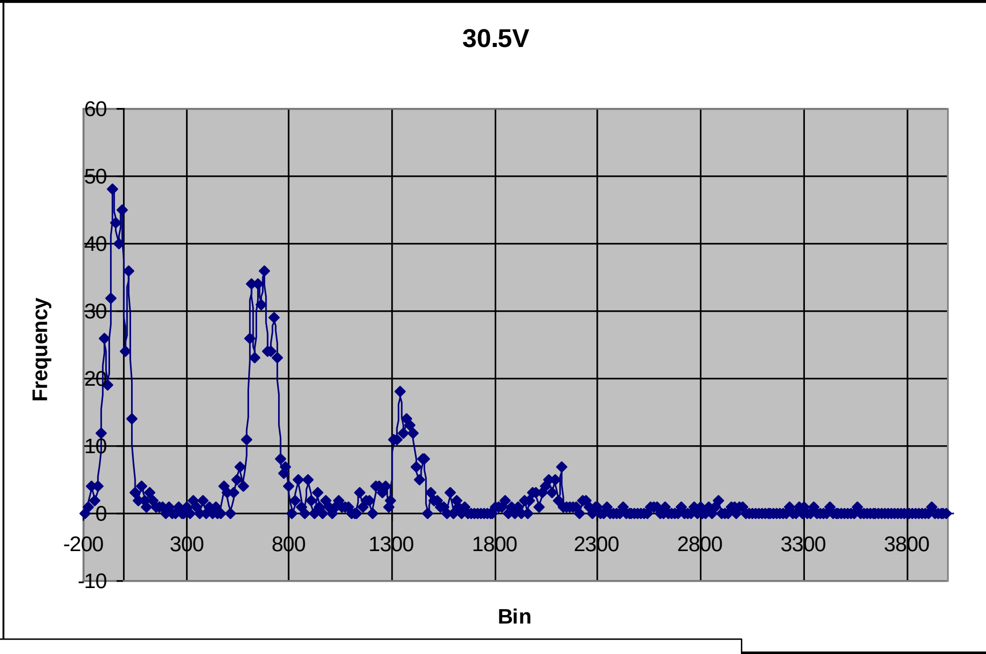

69.3V
frequency
bin
Frequency
350
300
250
200
150
100
50
0
-50
-1000
0
1000
2000
3000
4000
5000
6000
7000
8000

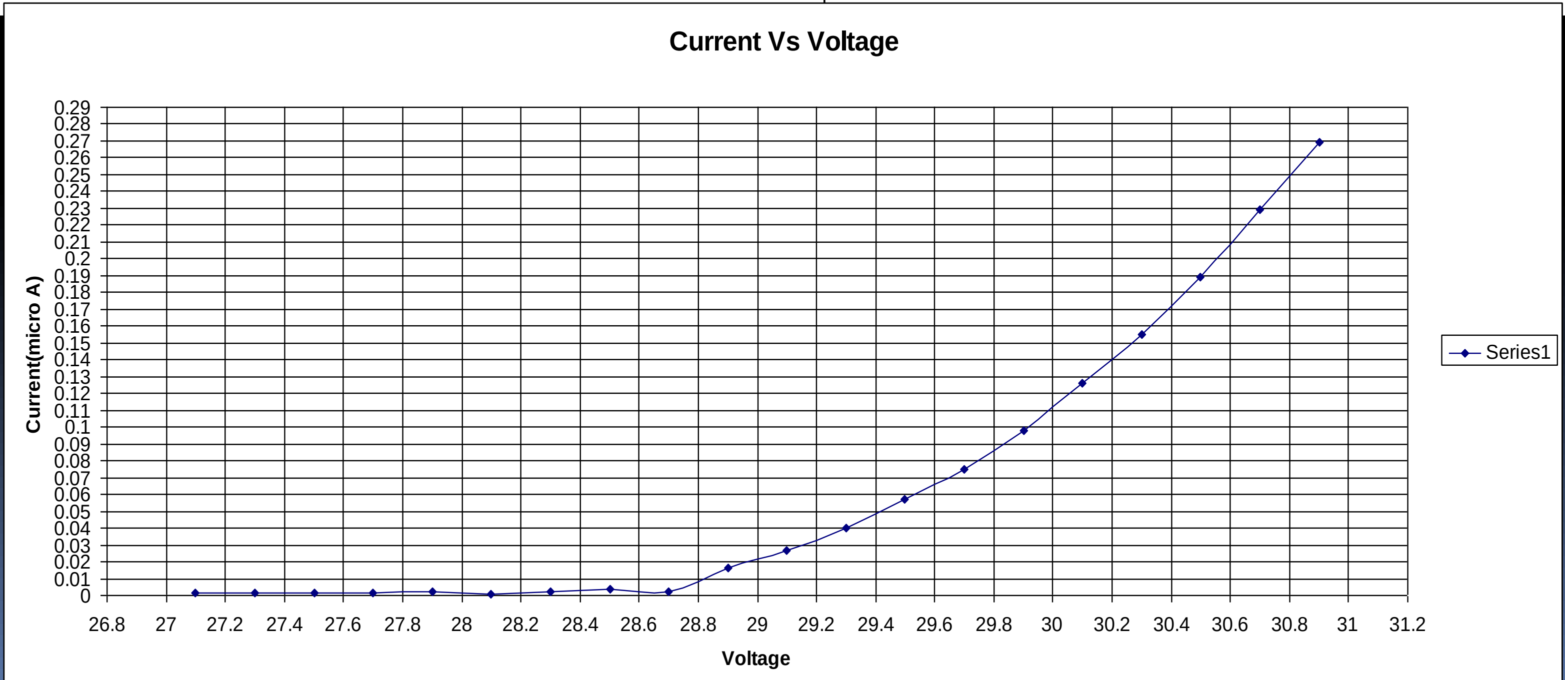

69.5V
Frequency
Bin
Frequency
250
200
150
100
50
0
-50
-1000
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000


Gain vs Reverse Bias Voltage
Gain(10^6)
RB(V)
4
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
-1
68
68.2
68.4
68.6
68.8
69
69.2
69.4
69.6
69.8
70

SenSL devices (1mm x 1mm)

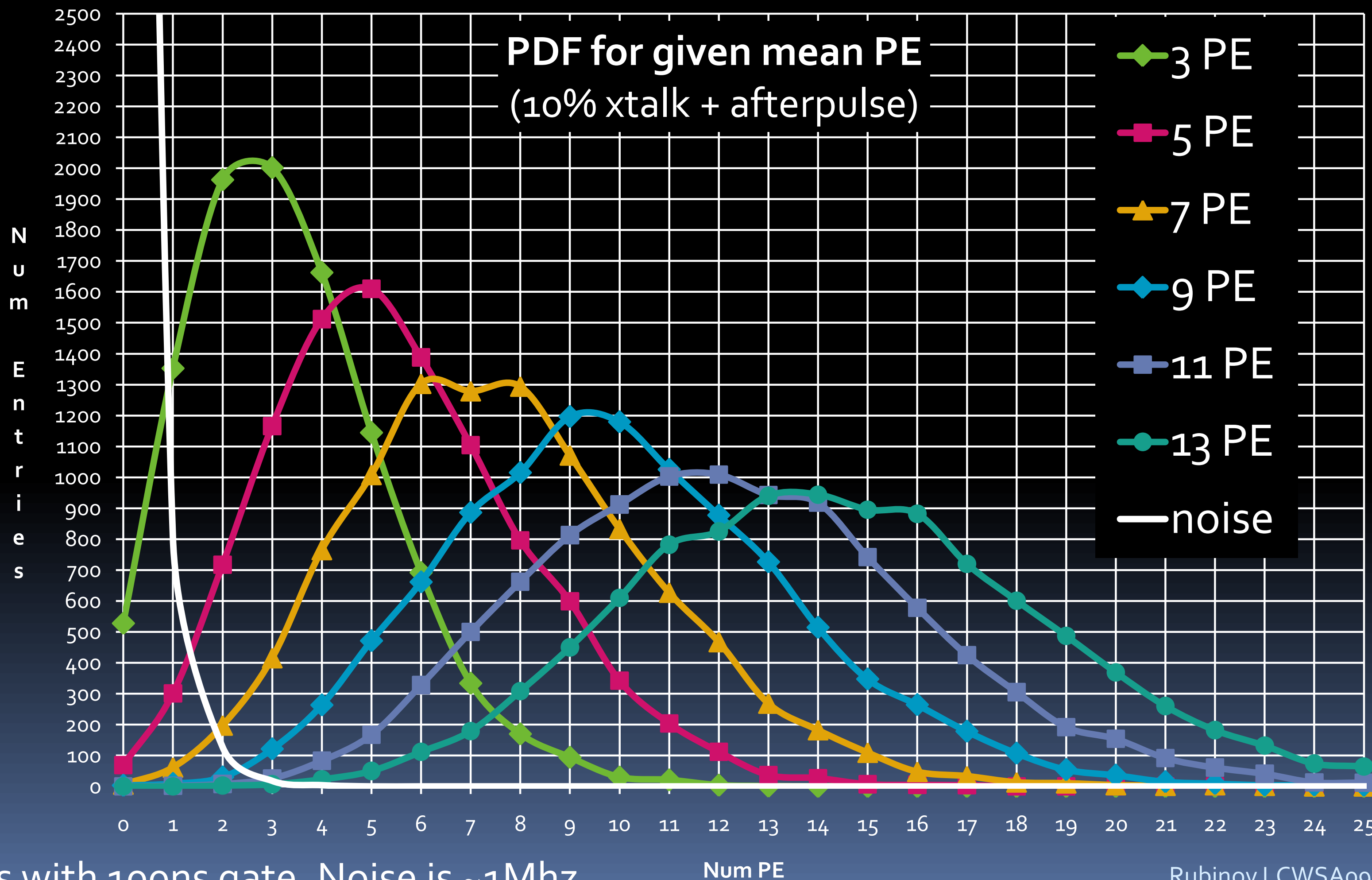






Photon Statistics

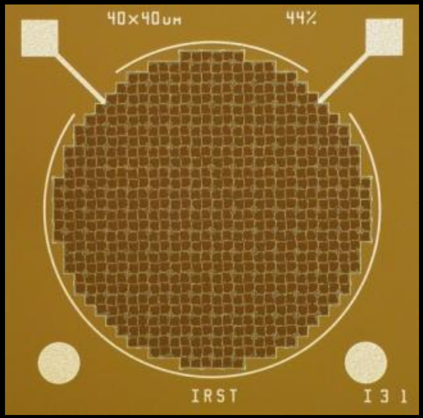
- This is the ultimate limit for noise/efficiency



This is with 100ns gate. Noise is ~1Mhz

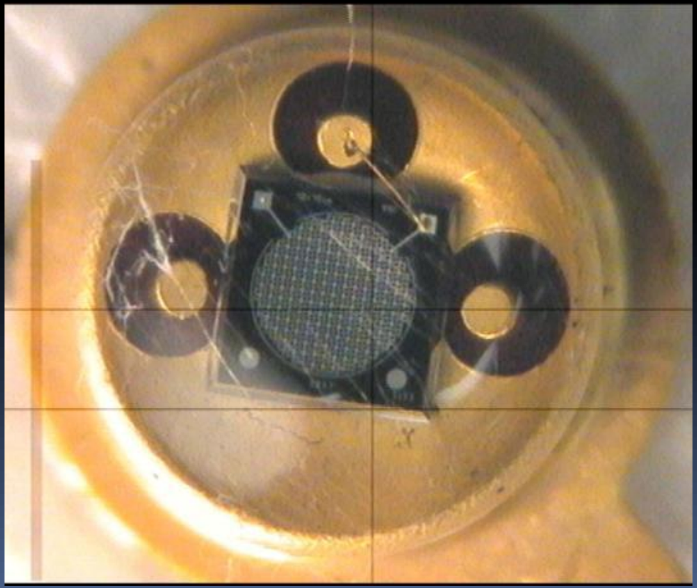
IRST SiPMs for muon-counter/tailcatcher application study at FNAL

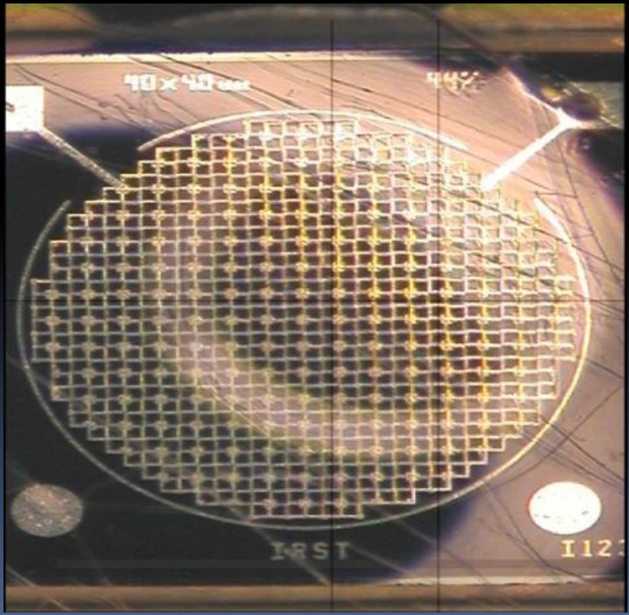
On commission from INFN Udine/Trieste, SiPMs have been produced by FBK-IRST (Trento, Italy) for this application.



Geometry: circular
diameter: 1.2 mm
Microcell: 40 x 40 μm
Improved fill-factor (44%)
Breakdown voltage ~30.5V

They are presently packaged (To18) with photocathode protected by epoxy(glob-top)

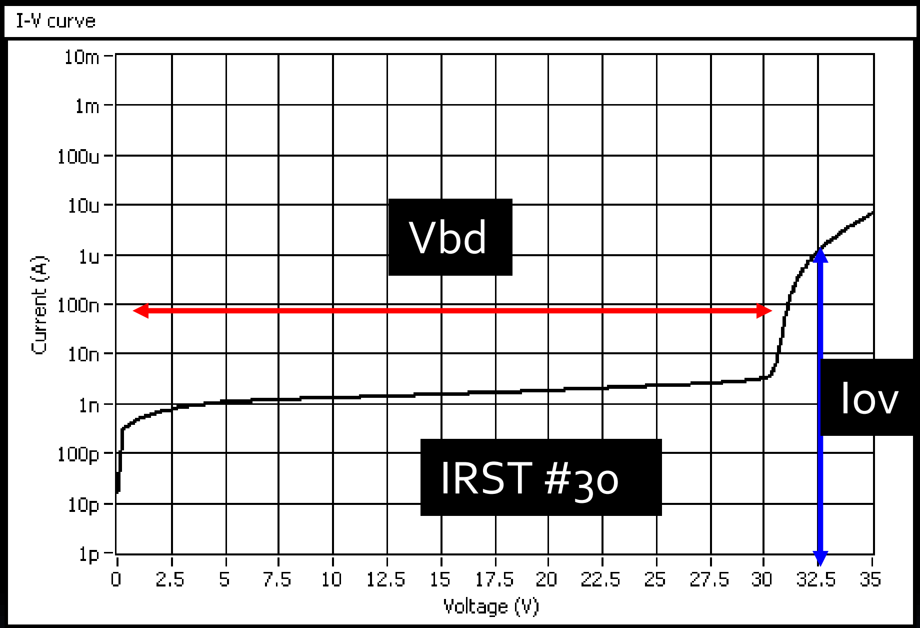




Bench Tests

reveal :

- Low operating voltage (~30V)
- Relatively large operating range (5V)
- very uniform characteristics



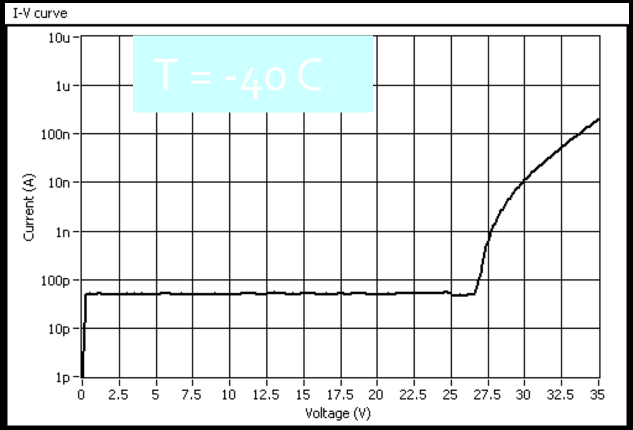
SiPM #	Vbd (V)	Iov (uA)
30	30.4	4.7
31	30.4	3.5
32	30.5	3.2
33	30.6	3.9
34	30.5	3.8
35	30.5	3.7
36	30.6	4.7
37	30.5	5.2
38	30.3	4.6
39	bad	bad
40	30.4	4.3
41	30.6	2.2
42	30.6	1.8
43	30.7	3.5
44	30.7	3.2
45	31.7	4
46	30.3	1.9
47	30.3	2.7
48	30.3	2.8
49	30.4	1.7
50	30.3	4.9

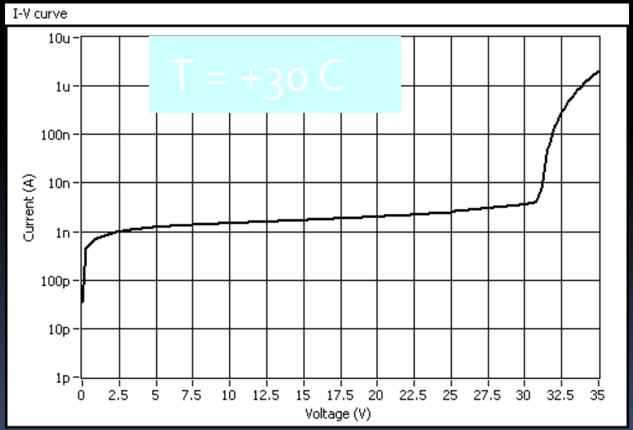
Test beam (fnal: T956)

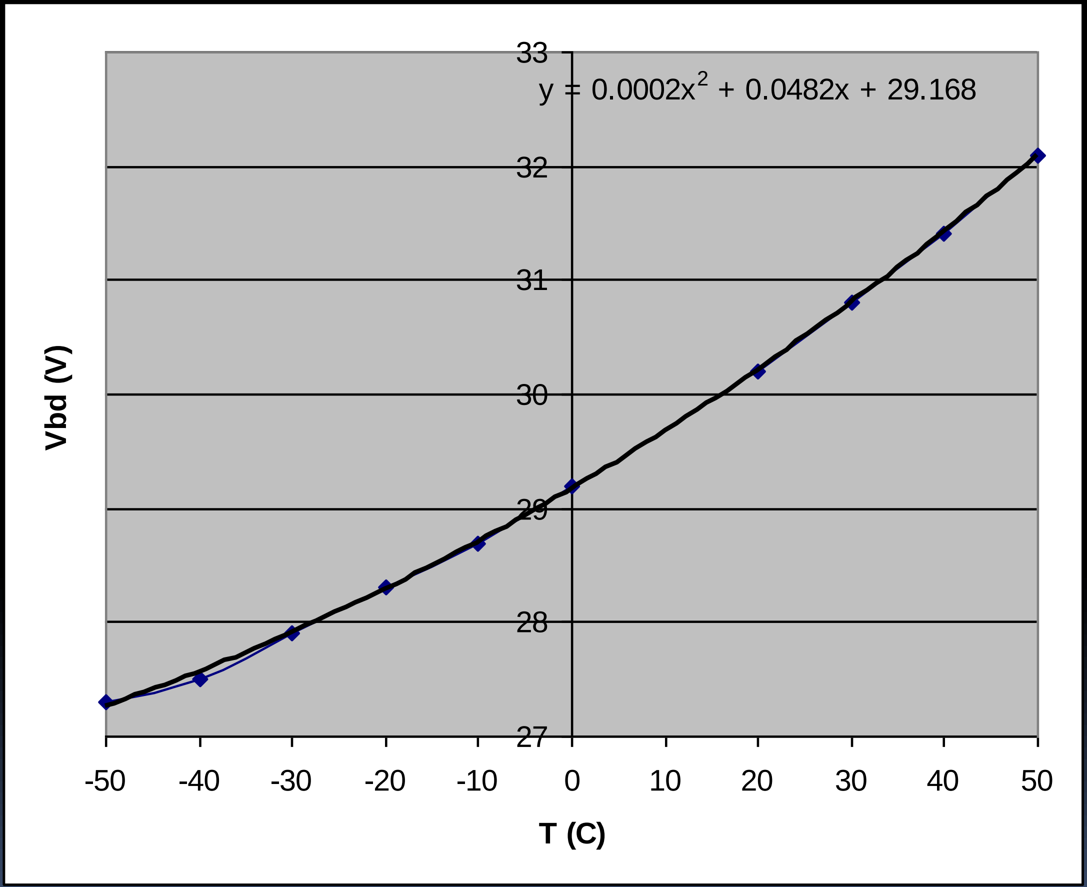
~20 p.e./mip from T956 extrude scint. bar read out by wls fiber.

Detailed characterization, under controlled climactic conditions reveal:

- A low , well-behaved break-down voltage V_{BD} varying with temperature as illustrated below

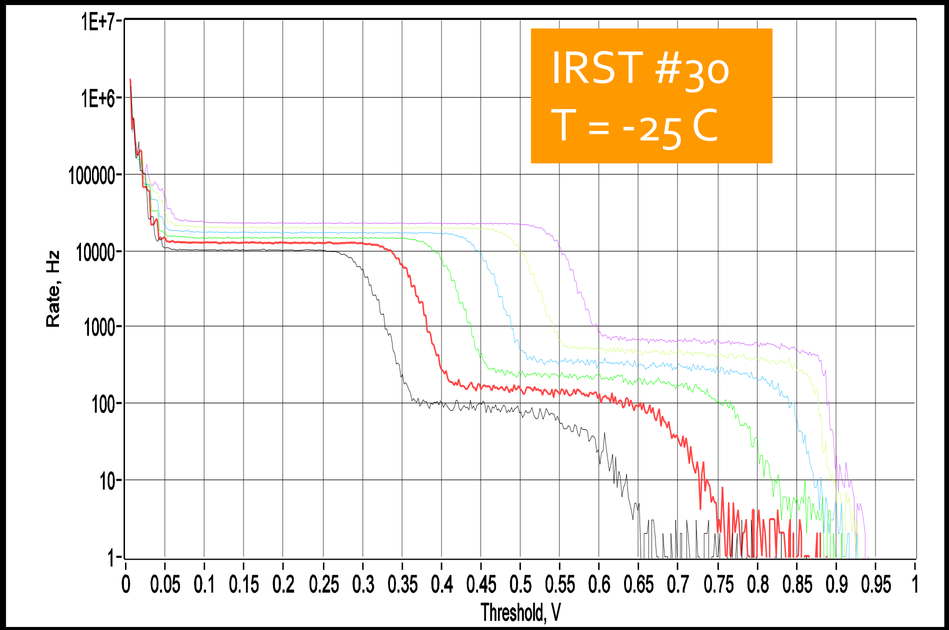


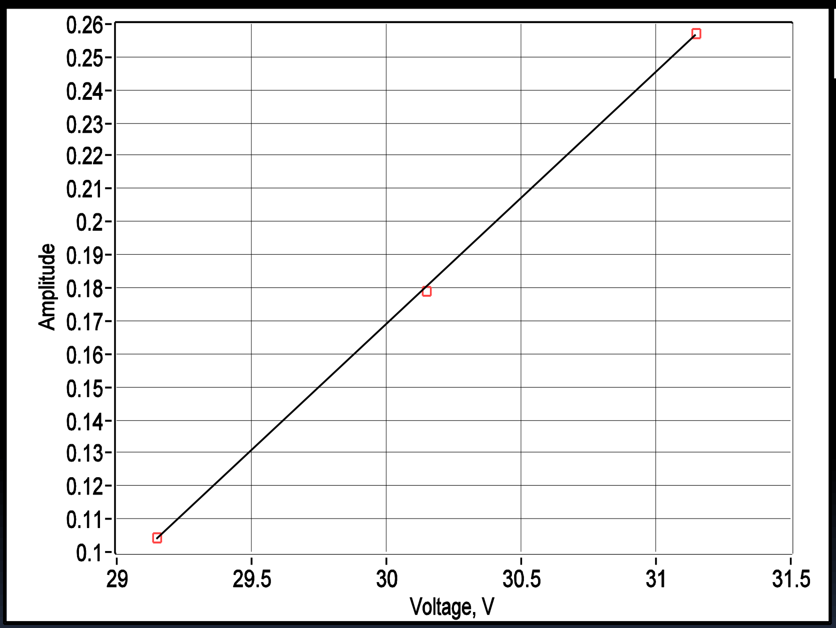




-- a dark count ranging between

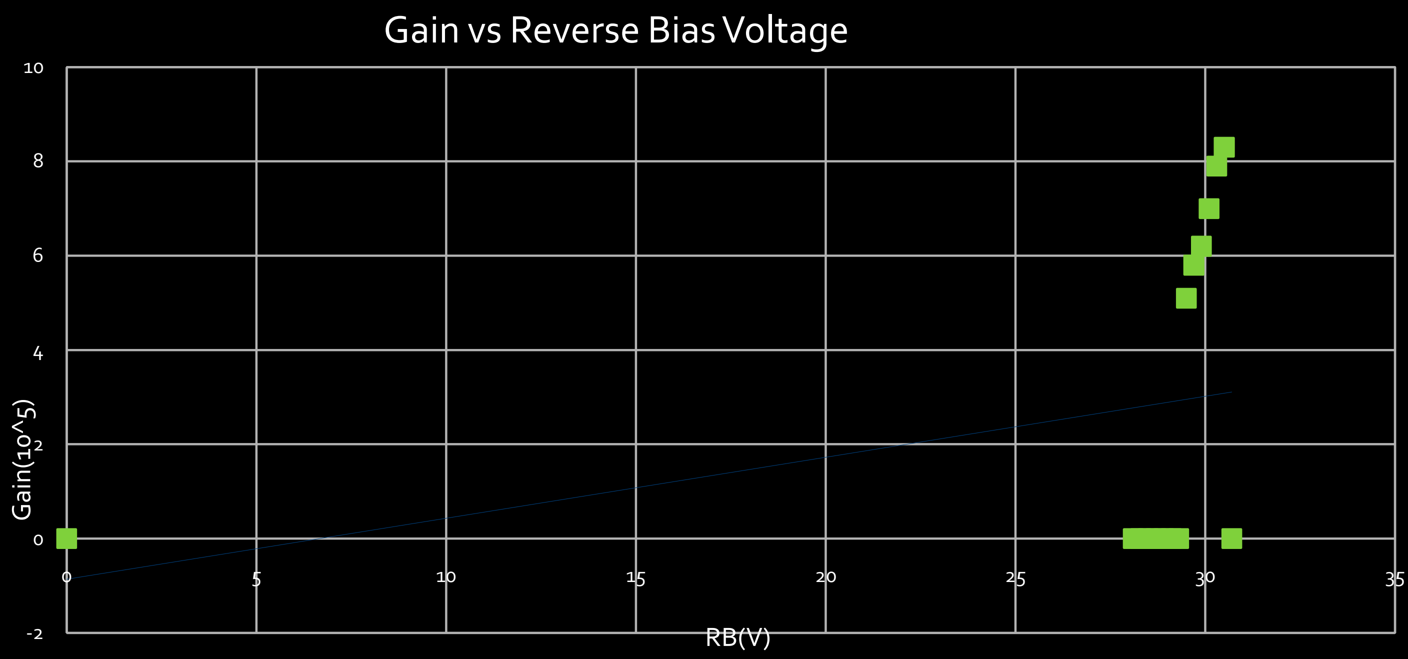
$\sim 10^4$ Hz at low temperatures and
$\sim 10^6$ Hz at at ambient temperatures

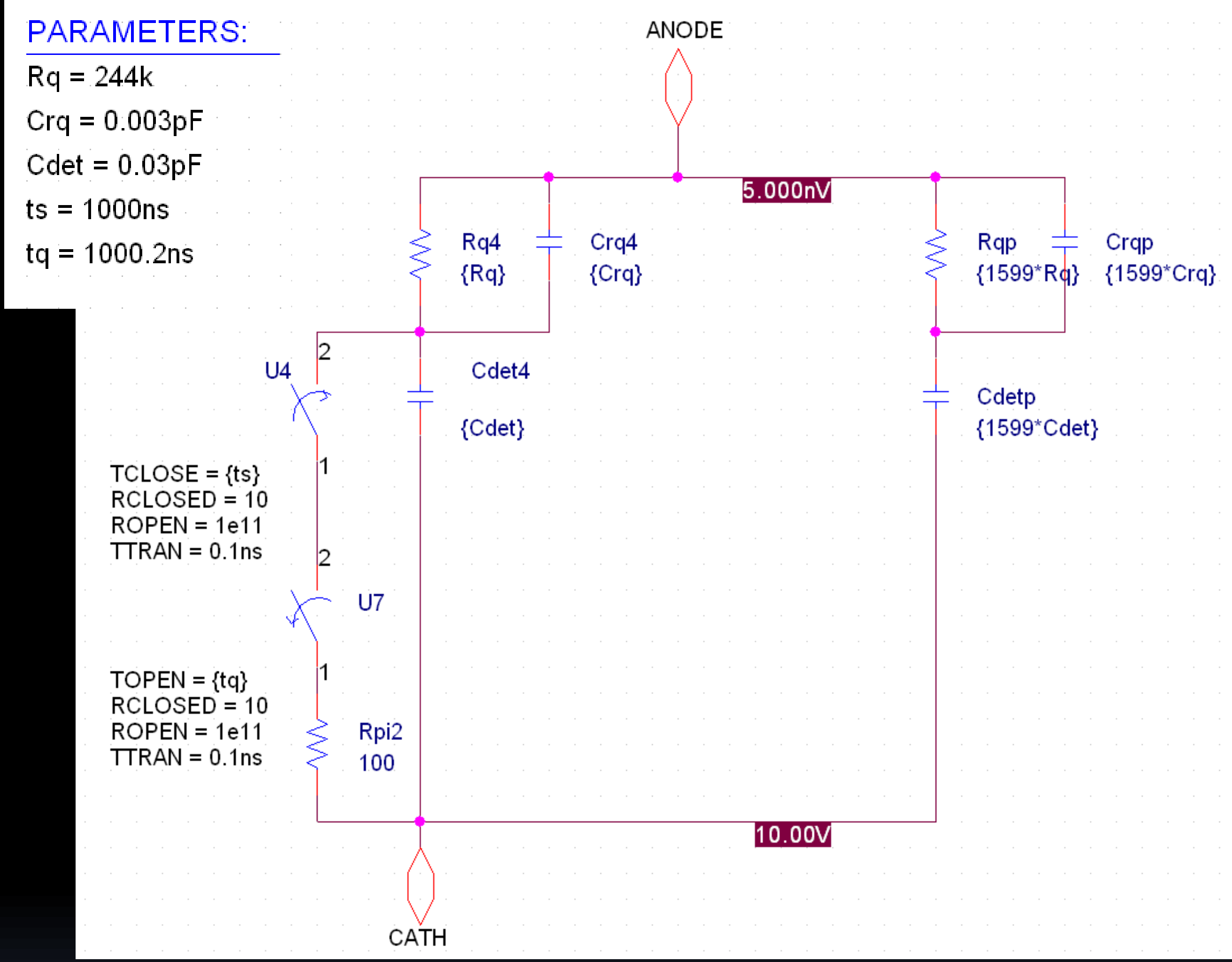




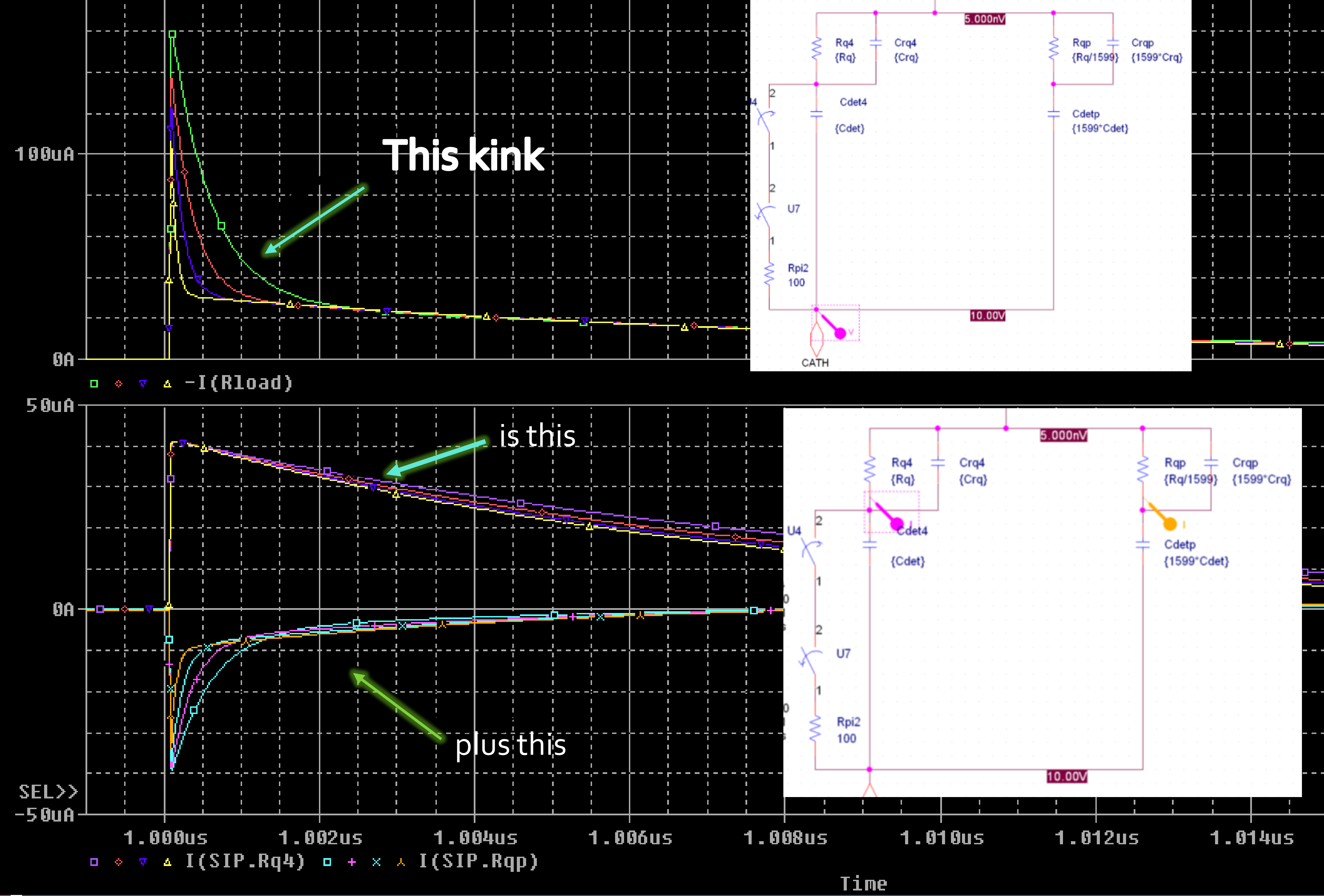
-and a gain of ~ 10^6 at ambient temperatures which varies linearly with bias voltage

The effects of γ and neutron radiation have also been studied and, as expected are not of concern at the larger radii occupied by the neutron counters

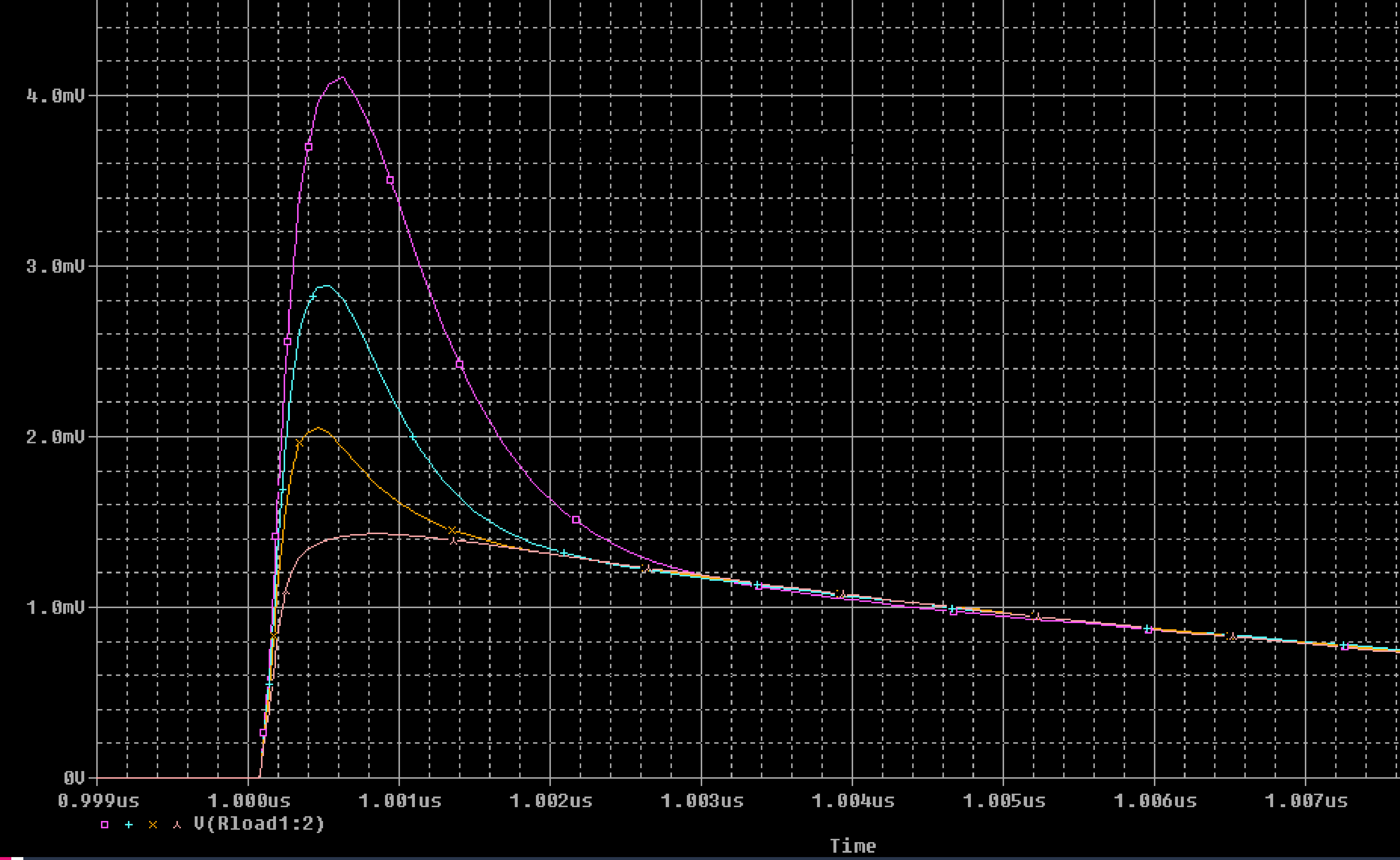

Gain vs Reverse Bias Voltage
10
8
6
4
2
0
-2
Gain(10^5)
0
5
10
15
20
25
30
35
RB(V)



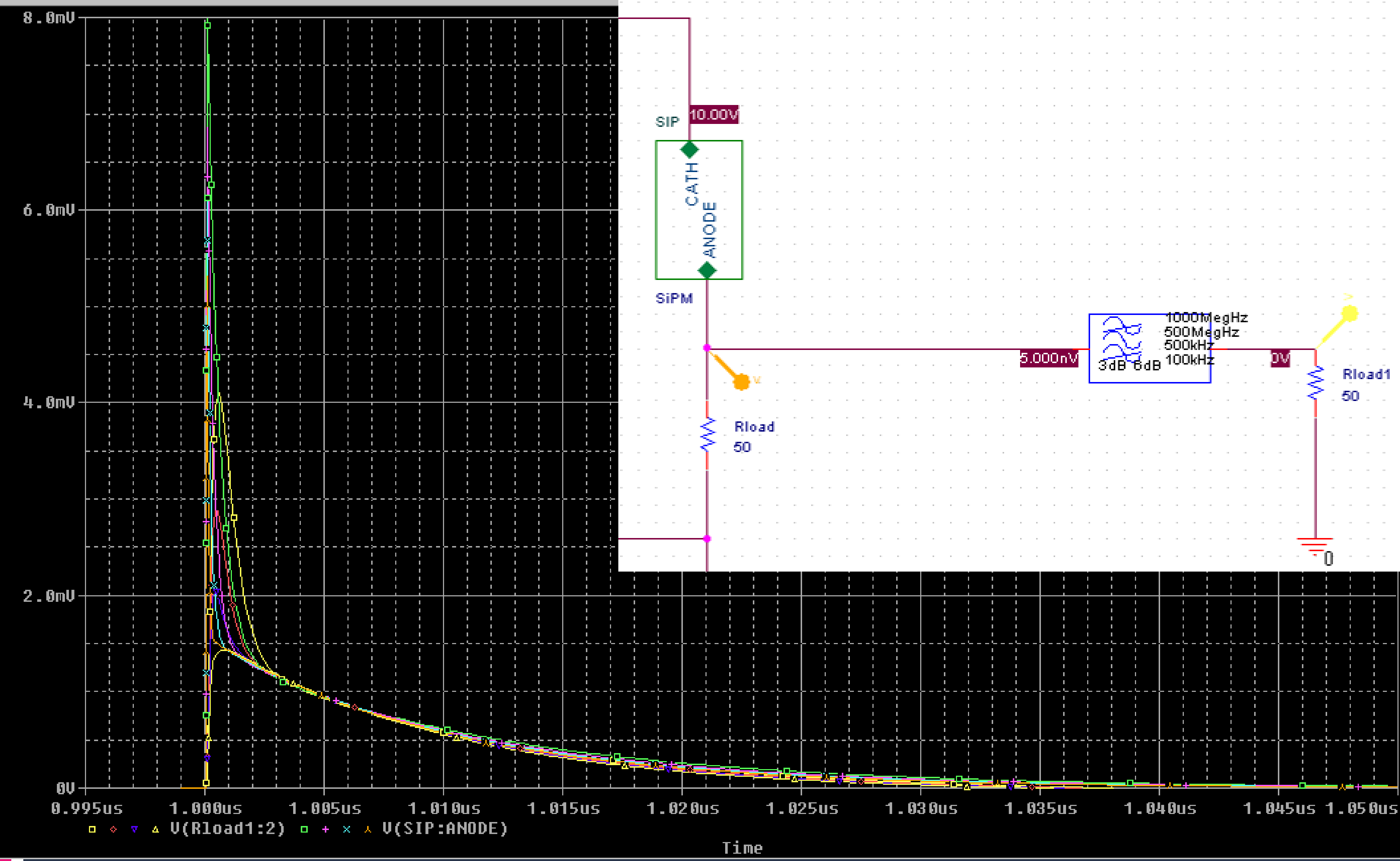
- This is the model I use. I got it from talks by C. Piemonte and others.
- Where available, I use parameters measured by Adam and co.
- Where not available, I guess and fiddle
- In my view, this sort of work is useful to develop a feel for things, and guide studies. Good predictions require a lot more work.



There are 4 values of Crq from 1 to 10 fF. So Crq is important for “spike” but not “tail”



- The shape of the spike depends critically on the shaping function of the amplifier – you can also get “ripples”



- I think it makes sense to "integrate" this spike away before digitizing waveform

Readout of the SiPM

- I have seen the future of SiPM readout
  - Readout electronics will be integrated into the SiPM!

  because
  - SiPM is an inherently digital device
  - We digitize the signal from the SiPM
  - So why do we have an analog step in between?!?
    - Because we want to get started!