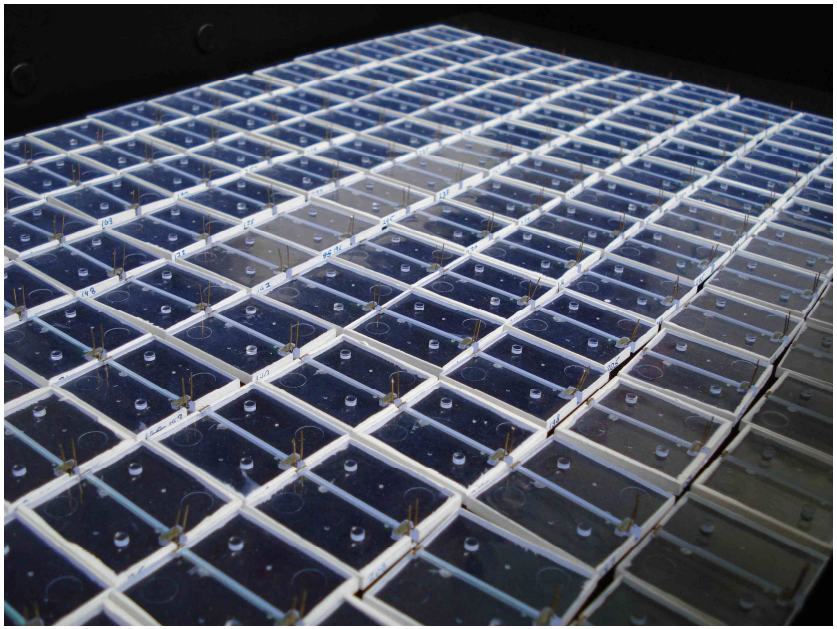
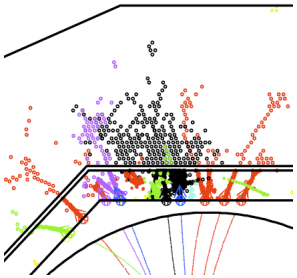
Scintillator HCAL hardware status and plans



Felix Sefkow

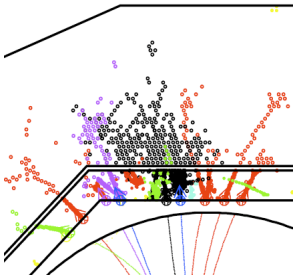
ALCPG 2009

Albuquerque, New Mexico, October 1, 2009



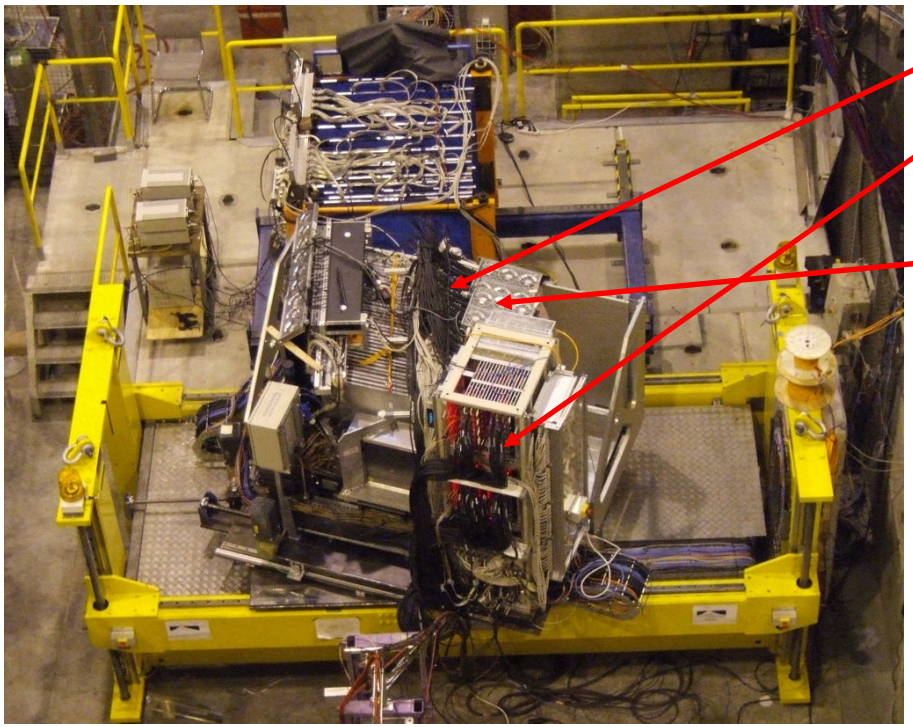
Outline

- Technological prototype overview and goals
- Mechanical structures
- Electronics integration
- Scintillator options

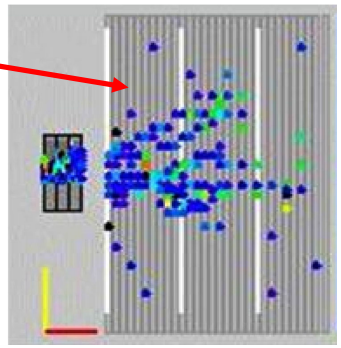


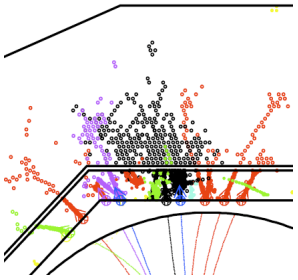
The task

- We have only half-way realized the integration potential of the novel SiPM technology for highly granular detectors
- What needs to be done:

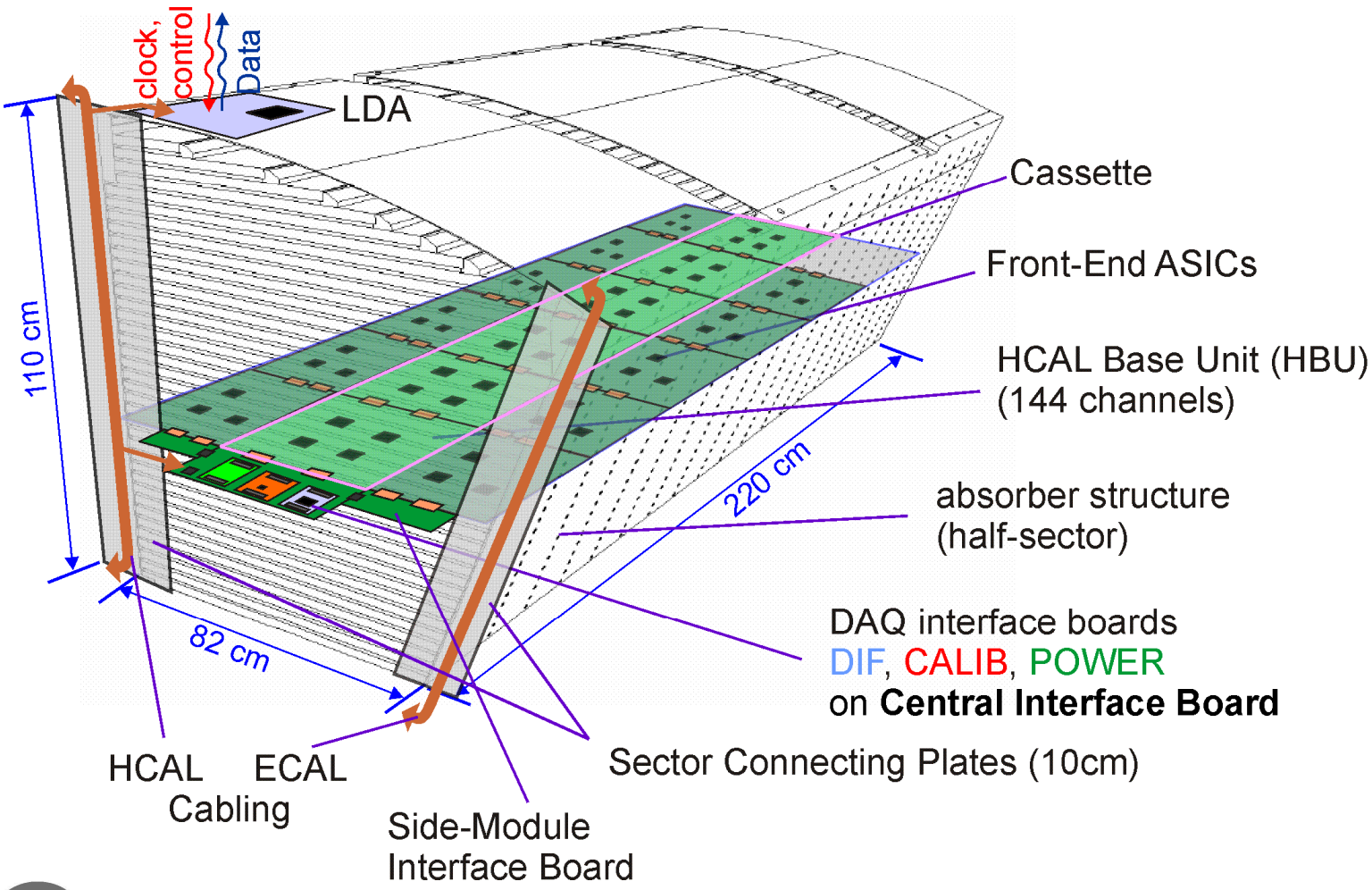


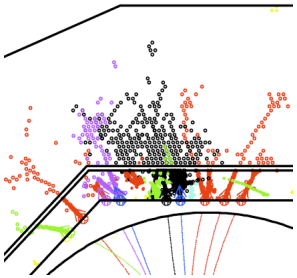
- ASICs into volume
- DAQ in barrel endcap gap (or barrel coil gap)
- Eliminate FE cooling with power pulsing
- On-detector zero suppression





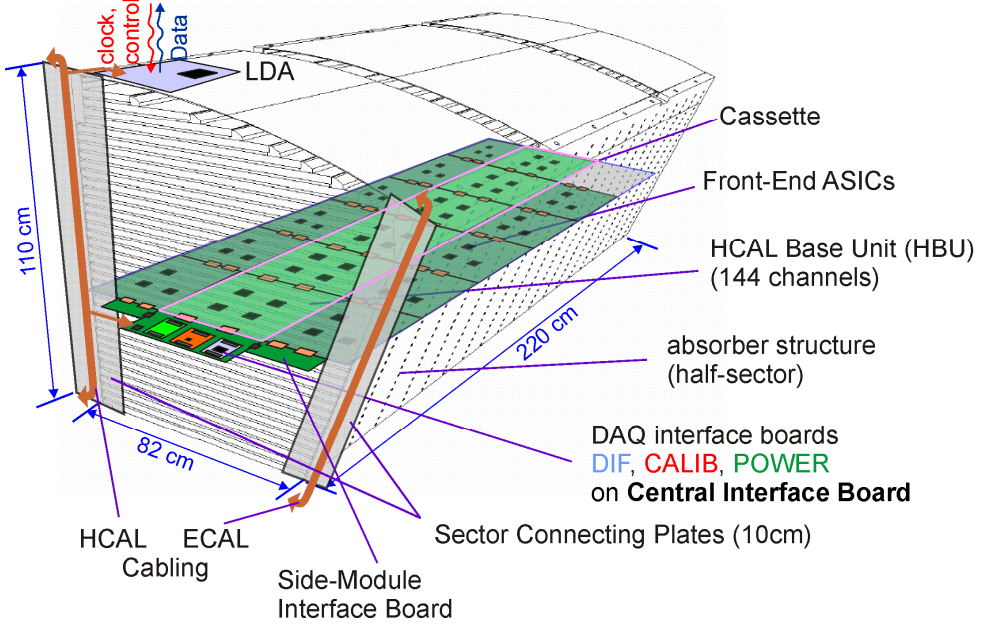
Overview

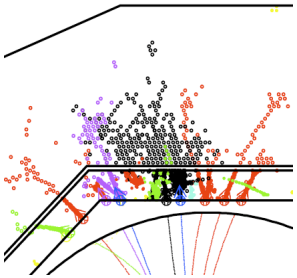

clock, control
Data
LDA
Cassette
Front-End ASICs
HCAL Base Unit (HBU)
(144 channels)
absorber structure
(half-sector)
DAQ interface boards
DIF, CALIB, POWER
on Central Interface Board
Sector Connecting Plates (10cm)
110 cm
82 cm
220 cm
HCAL
ECAL
Cabling
Side-Module
Interface Board



Goals

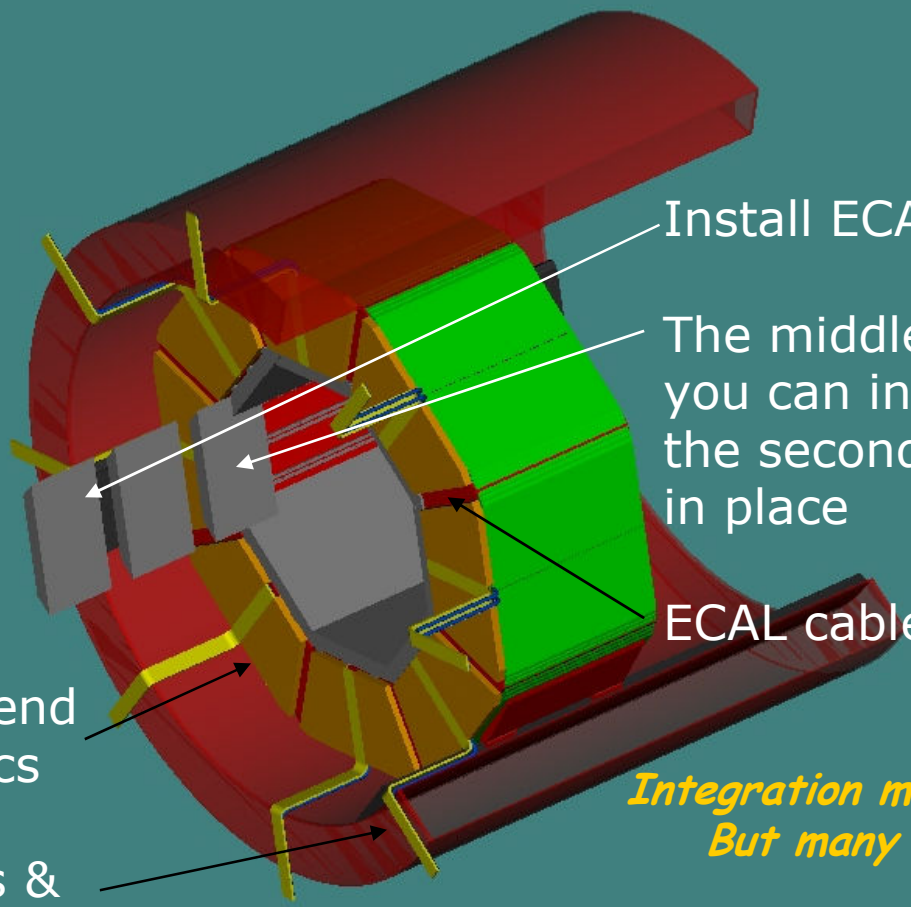
- Compact and hermetic mechanical structure, minimum dead spaces
- Economic solution with tight tolerances
- Read-out layer integration
- Compact interfaces
- Establish operational stability with power pulsing and on-line thresholds





Mechanical overview

Sli



Install ECAL modules

The middle modules you can install only with the second AHCAL half bar in place

ECAL cable slot

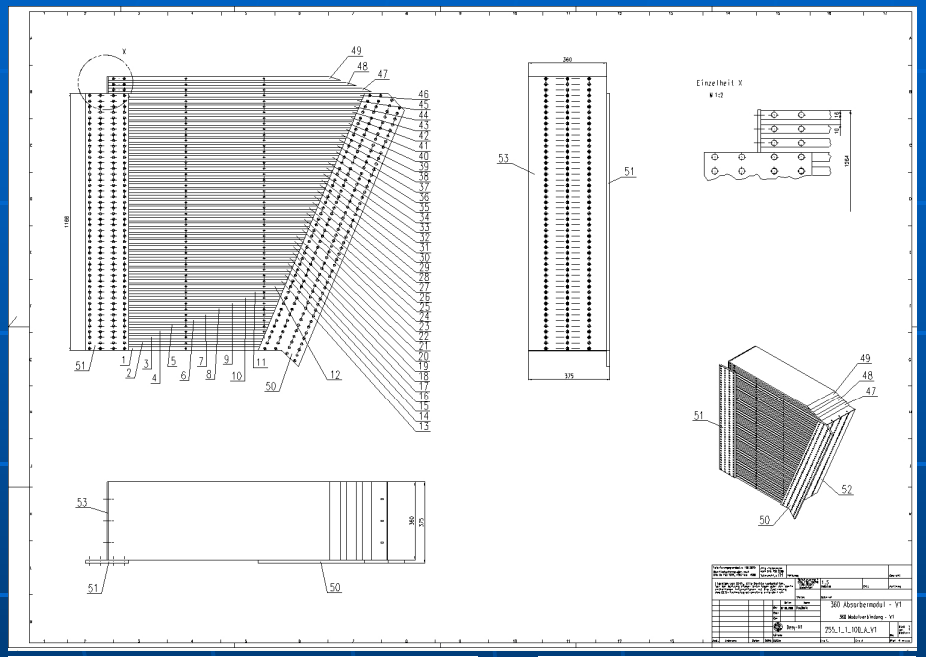
HCAL front end electronics

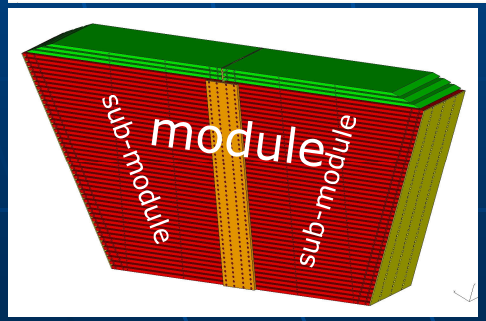
HCAL cables & cooling

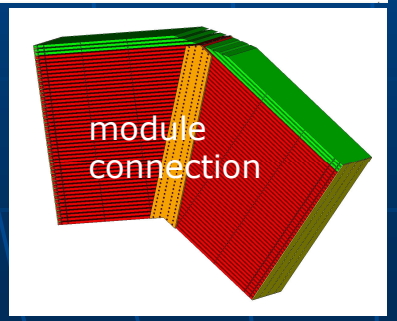
Integration motivated by ILD, But many generic issues

real size test setup vertical

K.Gadow







2 short length (360 mm) absorber sub-modules mounted to a short length module

360 mm = 1 HBU length

- **delivery tolerances**
  flatness, thickness
- **machining**
  tendering, processing, handling, tolerances, costs
- **sub-module mounting**
  stacking and shape tolerances, module interconnection, stability
- **sensitive layer installation**
  handling, tolerances, vertical and horizontal layer connection, cabling and cooling routing

real size test setup vertical

360 mm sub-module

K.Gadow

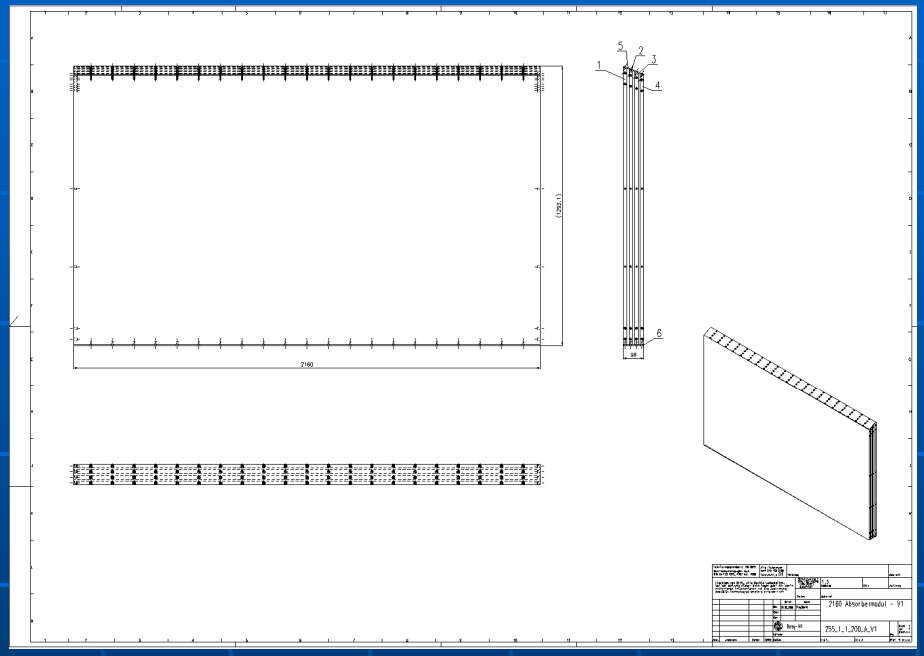
- flatness measured of 4 raw plates 3000 mm x 1500 mm Order 2 batch 1 (not roller leveled)
- order 2 batch 1 water cut to individual plate size
- flatness measured for each plate before machining
- sub-module Nr.1 mounting in horizontal position
- gap size measured in horizontal position (front)
- sub-module Nr.1 turned vertical
- gap size checked by cassette prototype

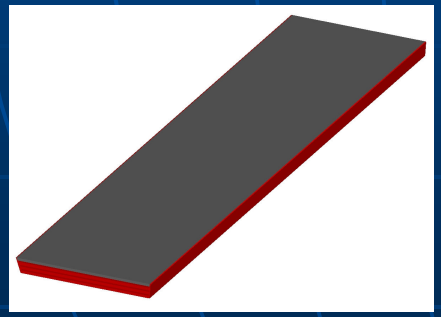
- 2 positions where the cassette does not fit into the gap
- gaps must be measured also in depth
- plate position must be measured

- flatness measured of 4 raw plates 3000 mm x 1500 mm Order 2 batch 2 (roller leveled)
- production finished of sub-module Nr.2
- mounting started

real size test setup horizontal

K.Gadow





4 full length (2160 mm) absorber plates mounted to a fraction of a sub-module

2160 mm = 6 HBU

outer position = broadest plates (~ 1300 mm)

- **delivery tolerances**
  flatness, thickness
- **machining**
  tendering, processing, handling, tolerances, costs
- **sub-module mounting**
  stacking and shape tolerances, module interconnection, stability
- **sensitive layer installation**
  handling, tolerances, vertical and horizontal layer connection, cabling and cooling routing

real size test setup horizontal

K.Gadow

2160 mm sub-module plates layer 43 to 46

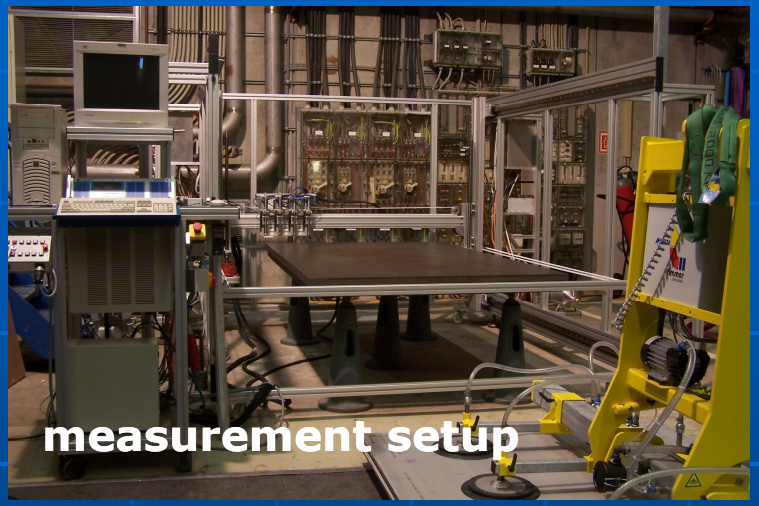
- flatness measured from 4 raw plates 2500 mm x 1500 mm Order 1 batch 1 (not roller leveled)
- order 1 batch 1 water cut to individual size
- plate flatness measured
- roller leveling done
- plate flatness measured
- horizontal mounted

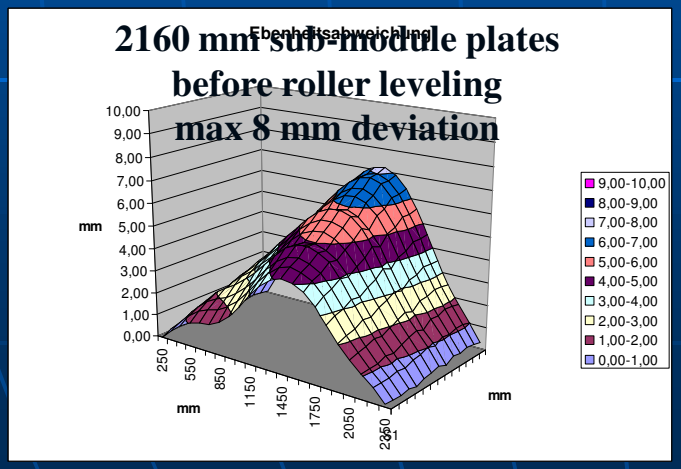
K.Gadow

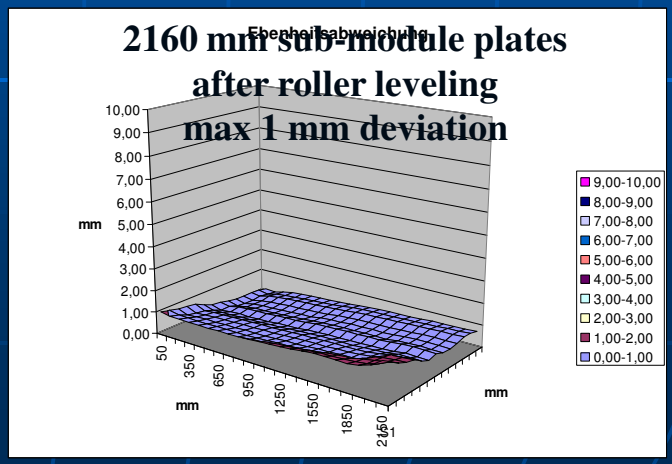
plate measurement

measurement of flatness and thickness deviation according EN10029 (steel plates t >=15<25 mm

- **flatness class N, steel group H**
  - L(1000): max 10mm
  - L(2000): max 13mm
- **thickness class B**
  - min: -0,3 mm
  - max: +1,6 mm
  - measured at the edges only







Roller leveling

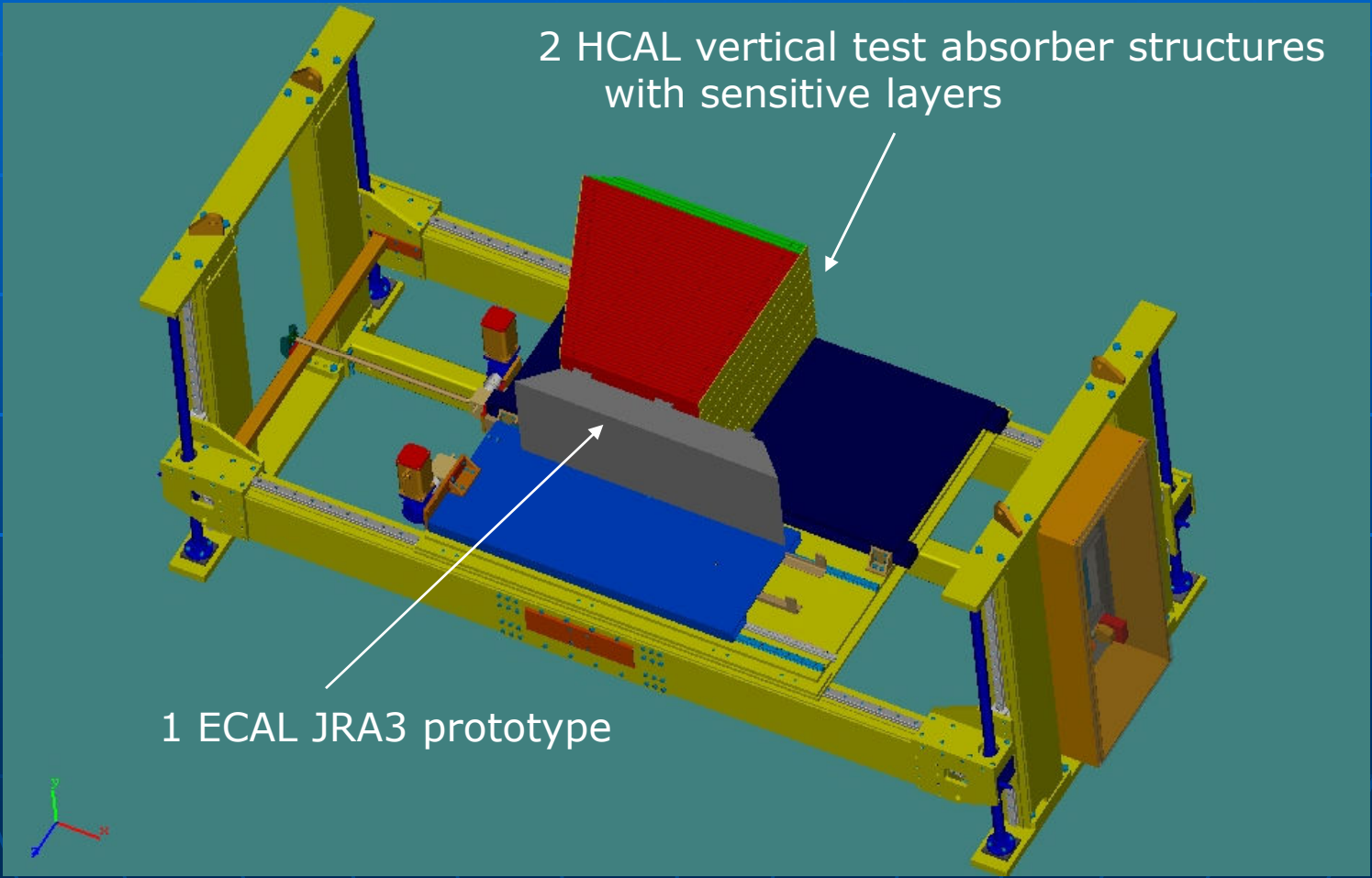
K.Gadow

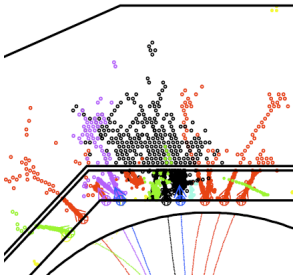
FlatMaster from company arku

capacity: t <= 50 mm
flatness: +- 1 mm

K.Gadow

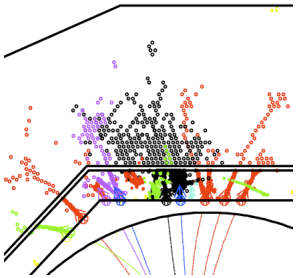
Test beam setup V2





Mechanics status:

- Economic solution for achieving 1mm flatness tolerances without machining found
- Prototypes available to experimentally test whole barrel stability
- Realistic environment to address electronics integration
  - Large area
  - Multi-layer
- Scalable towards a full-size integrated test beam set-up

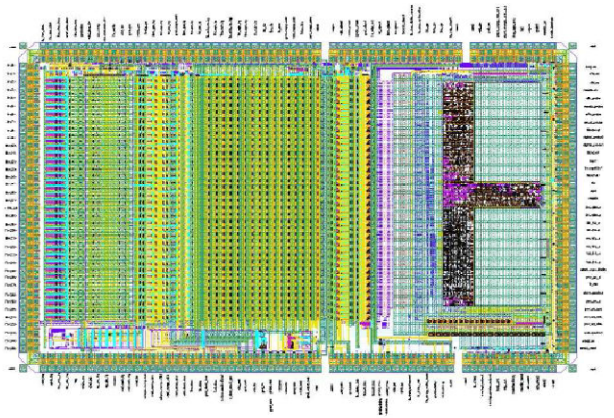


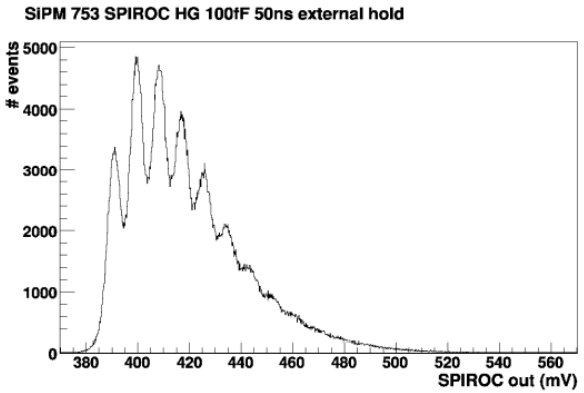
New ASICs: SPIROC

- Electronics is the key
- See R.Poeschl's talk on 2nd generation ASIC family
- Power pulsing: 40 μW / channel
- Auto-trigger
- Analogue pipeline
- ADC and TDC integrated
- Shown to work with SiPM
- Digital part tested with DHCAL

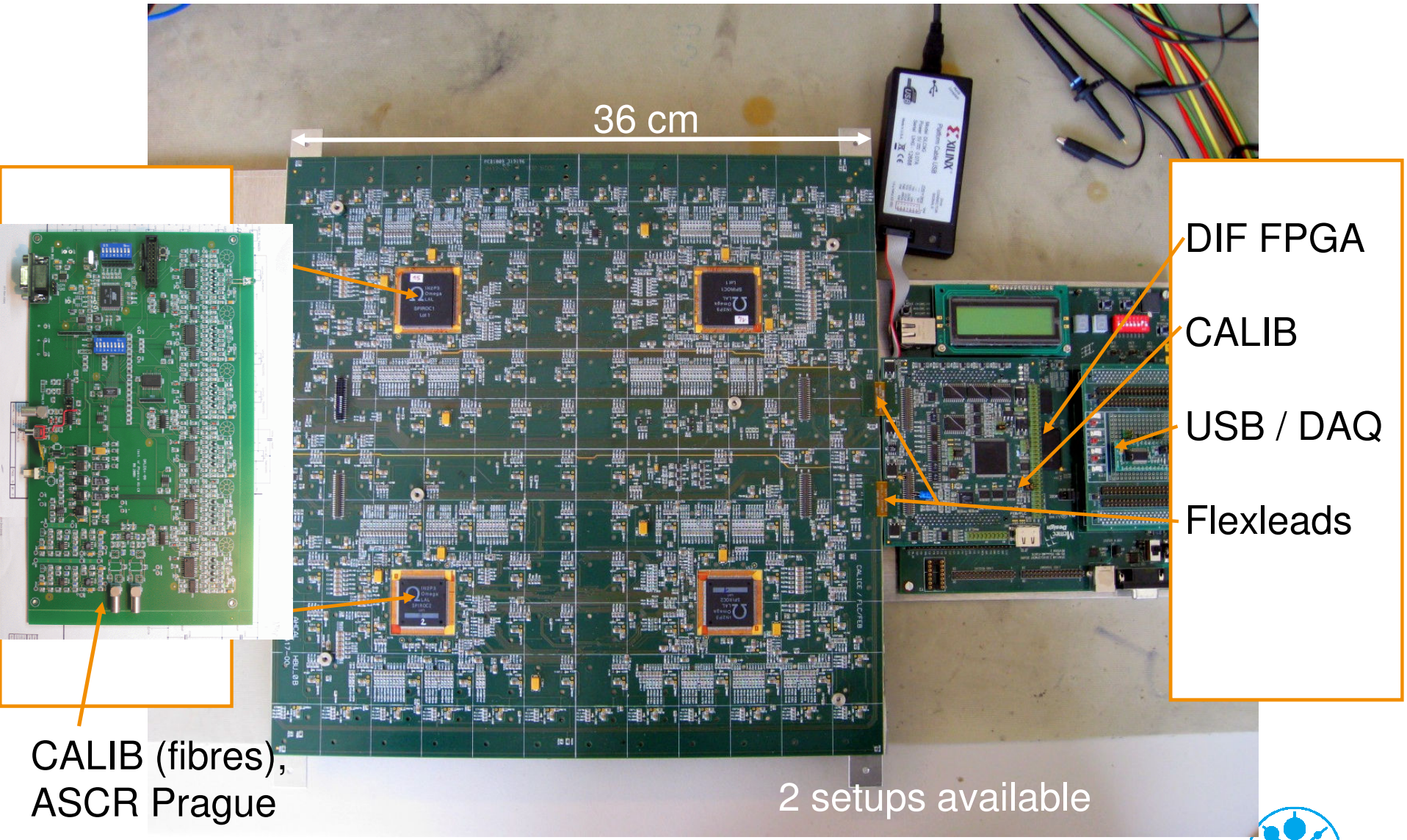
➔ Major challenges

- Establish full readout and calibration chain
- On-detector zero suppression requires on-line control of thresholds



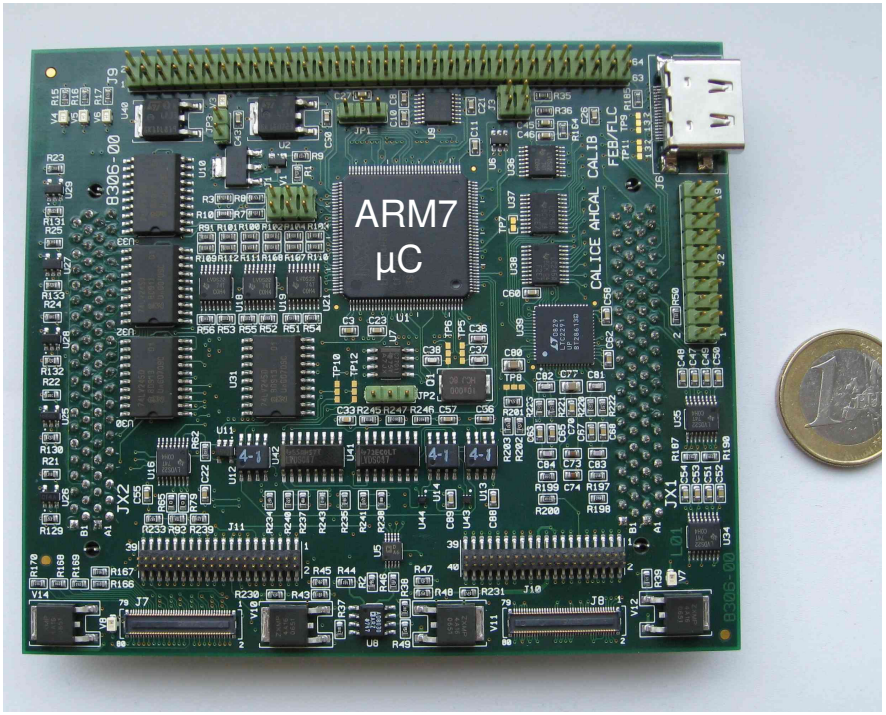


Electronics Integration

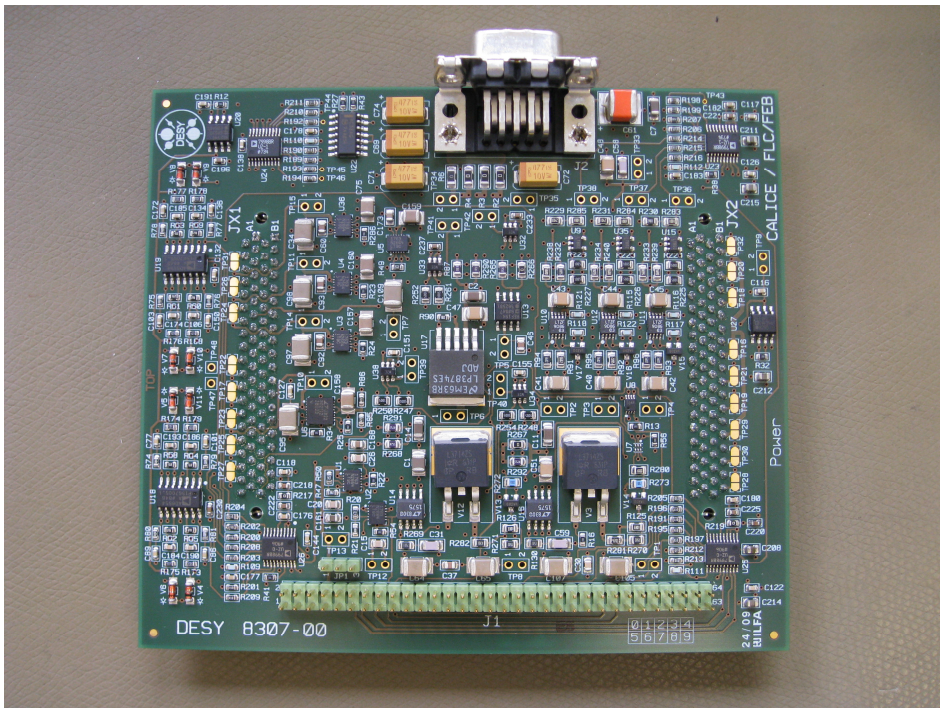


CALIB and POWER Modules

CALIB module: 11 x 10 cm²



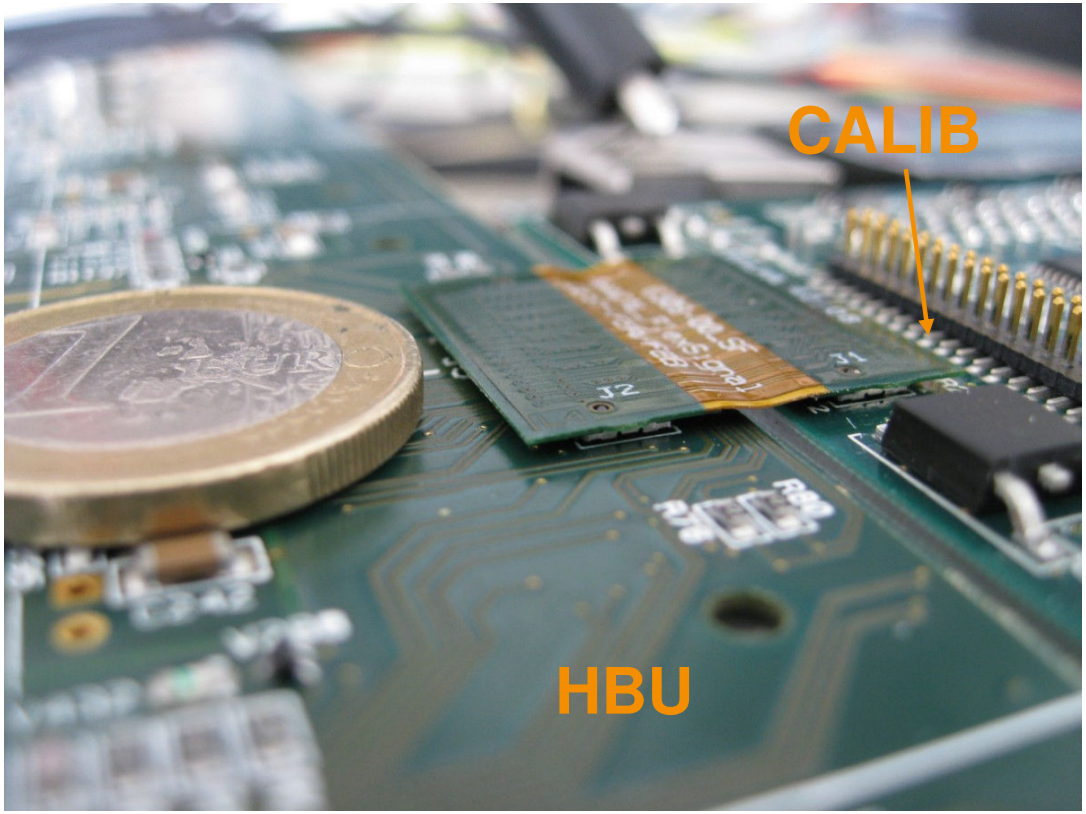
POWER module: 12.5 x 11 cm²



> 4 Modules of both types finished, in operation.
> First tests successful.

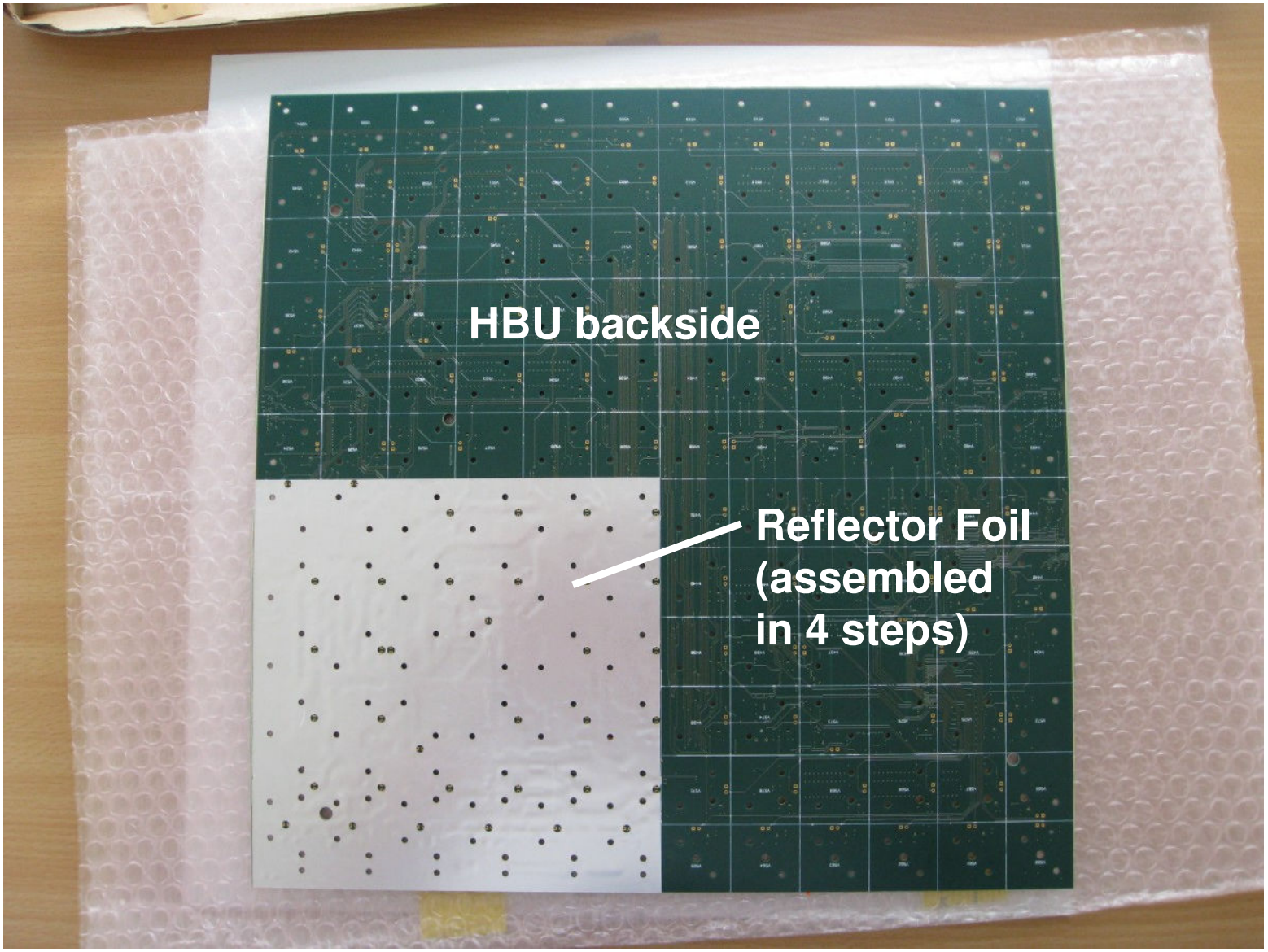
Sizes and heights: To be adapted to ILC mechanics later.

Flexleads – SIGNAL and POWER

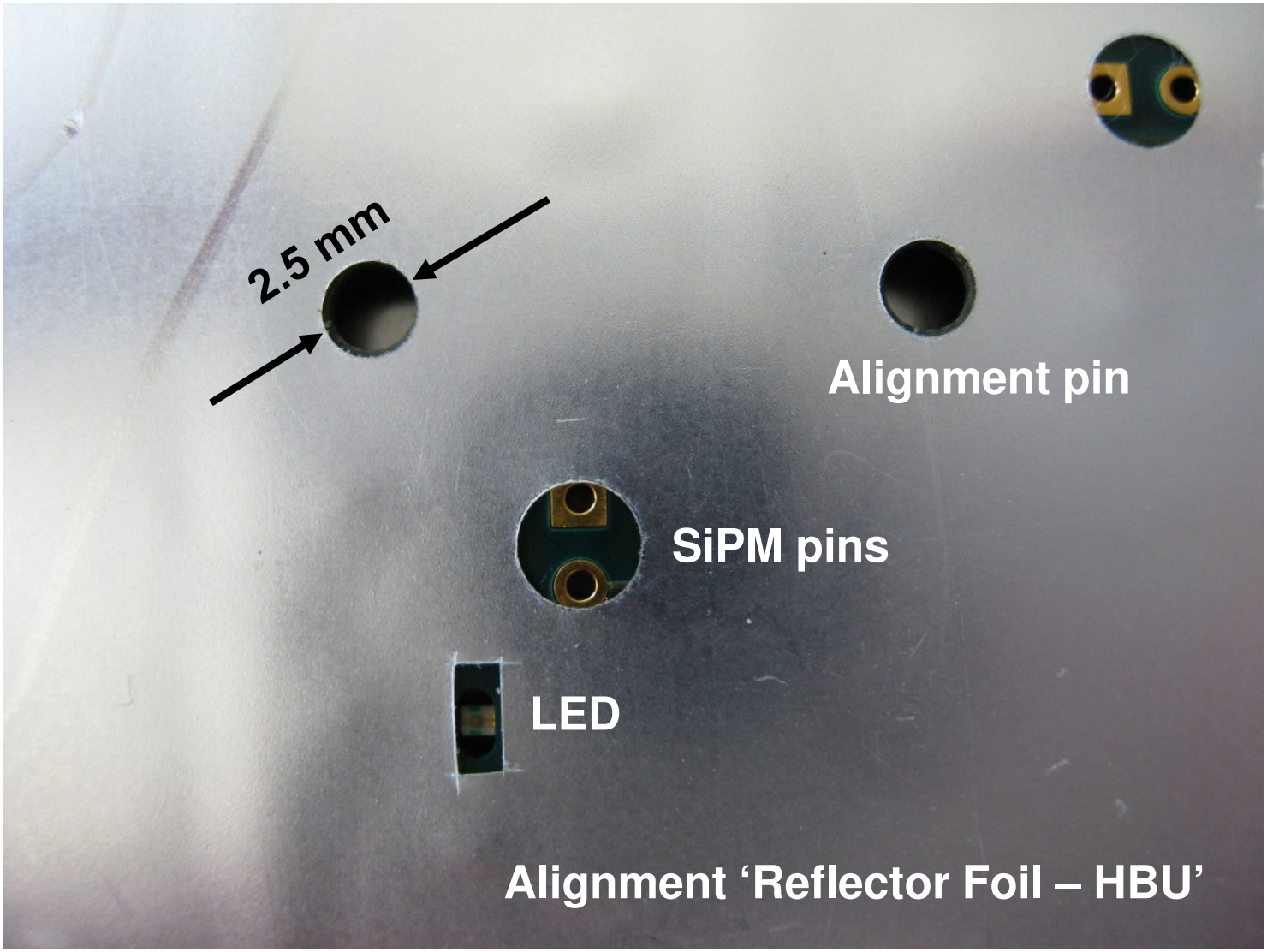


- About 80 connection cycles up to now - still ok.
- Compensate HBU misalignments in distance.
- Fulfill AHCAL height requirements.
- Tests ok concerning:
  - Signal allocation
  - Signal quality
  - Resistance for power

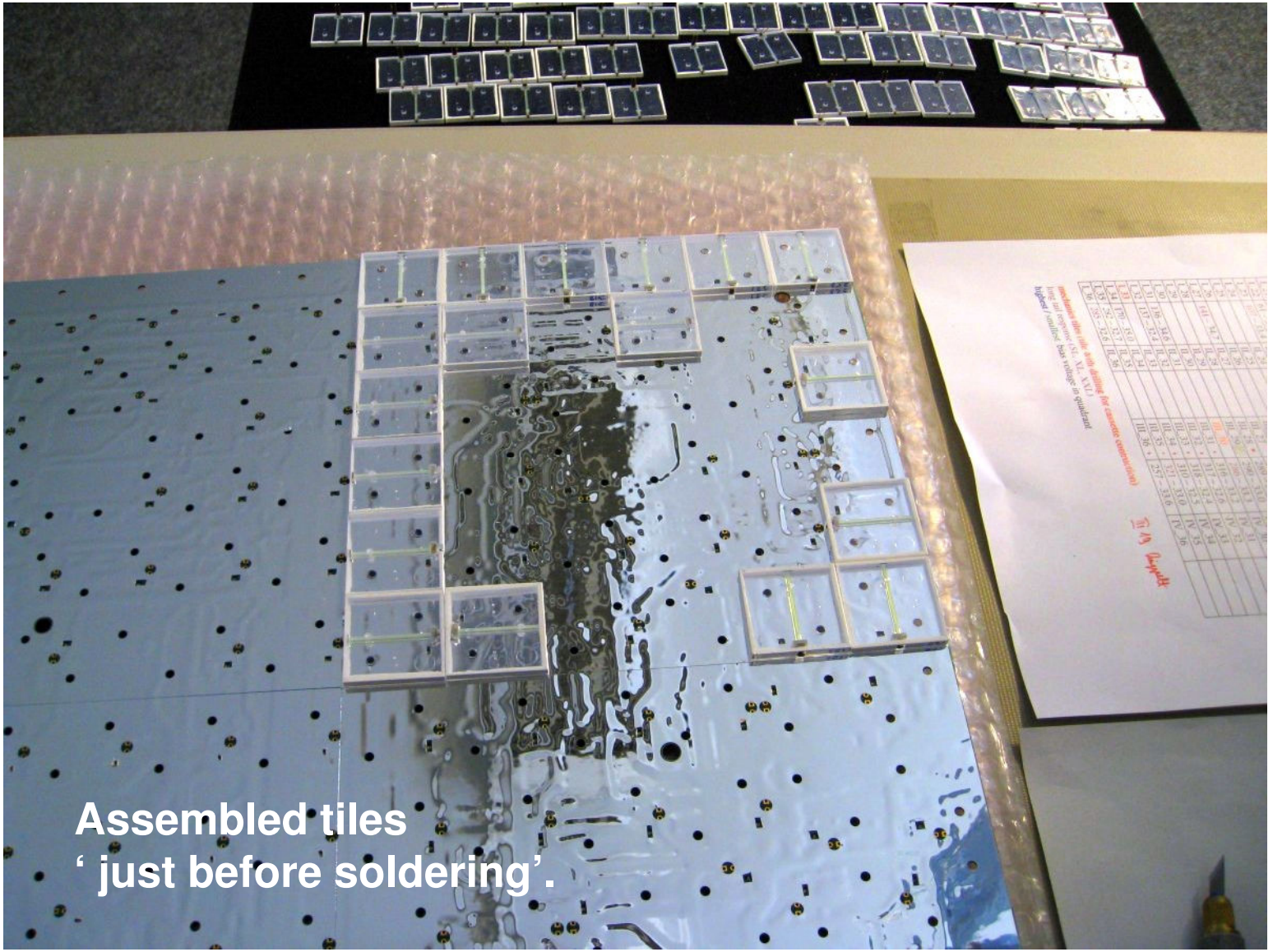
Reflector Foil Assembly



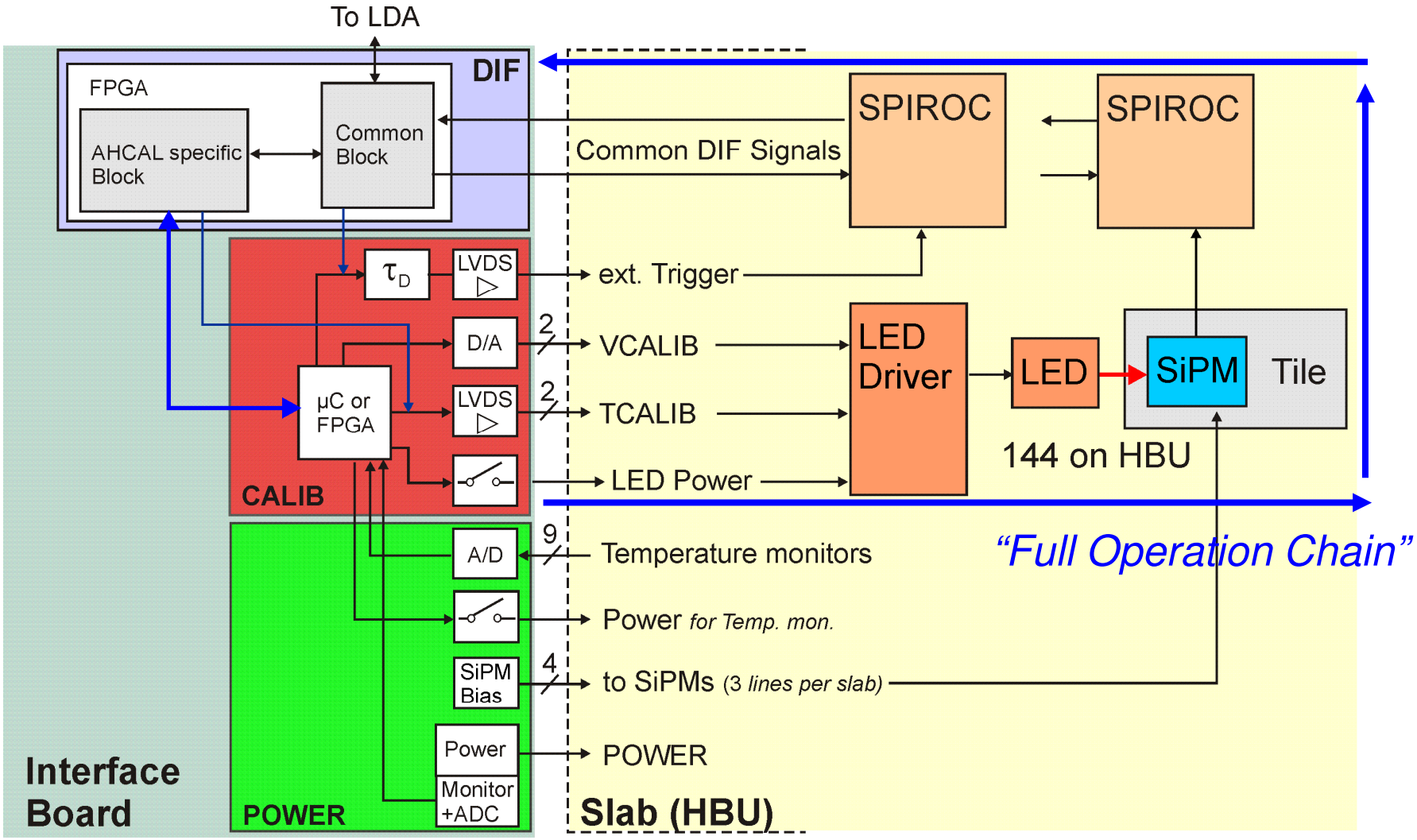
Reflector Foil Assembly



Tile Assembly (the first 18)



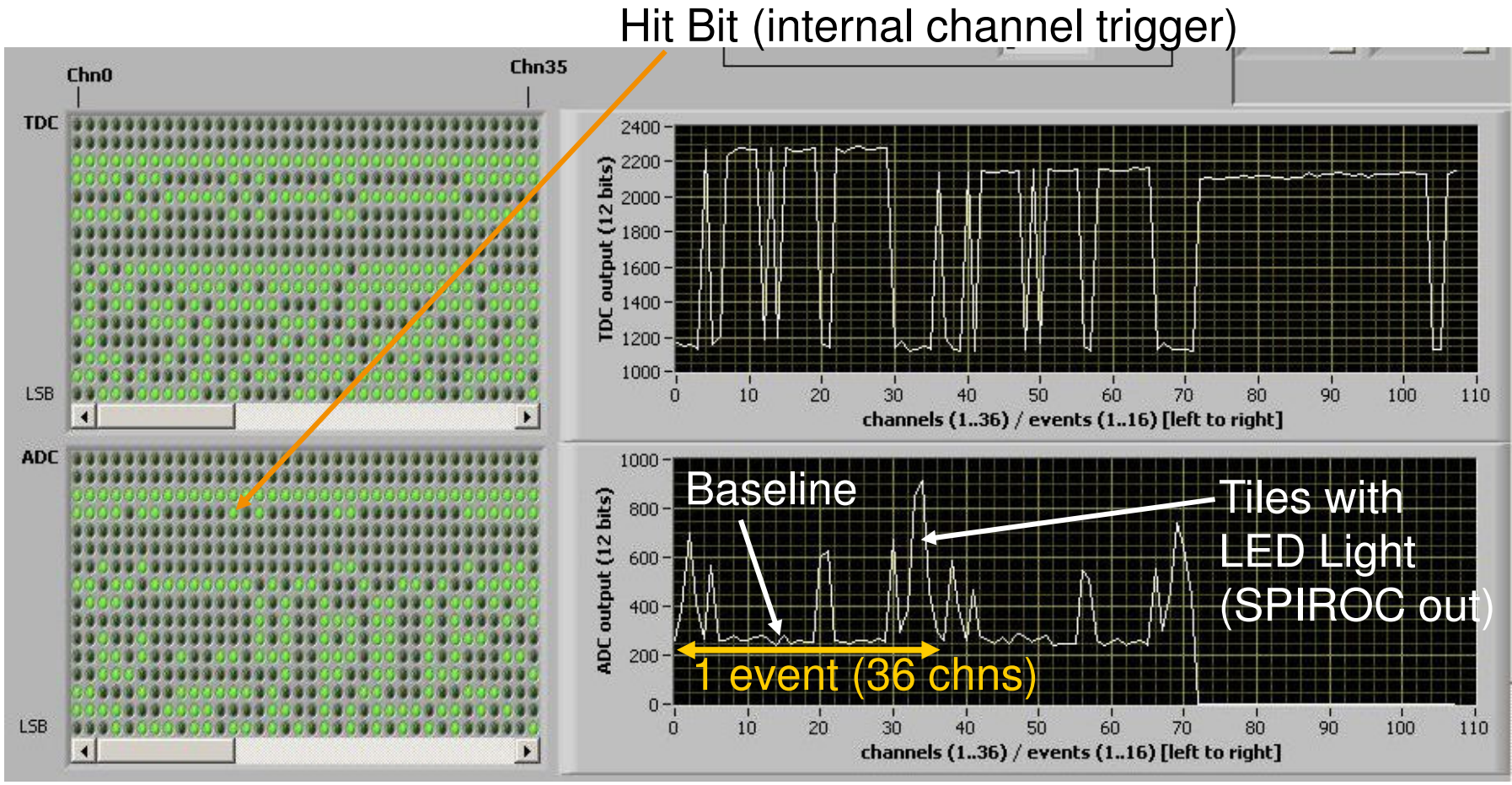
Commissioning – Signal Chain for LED operation



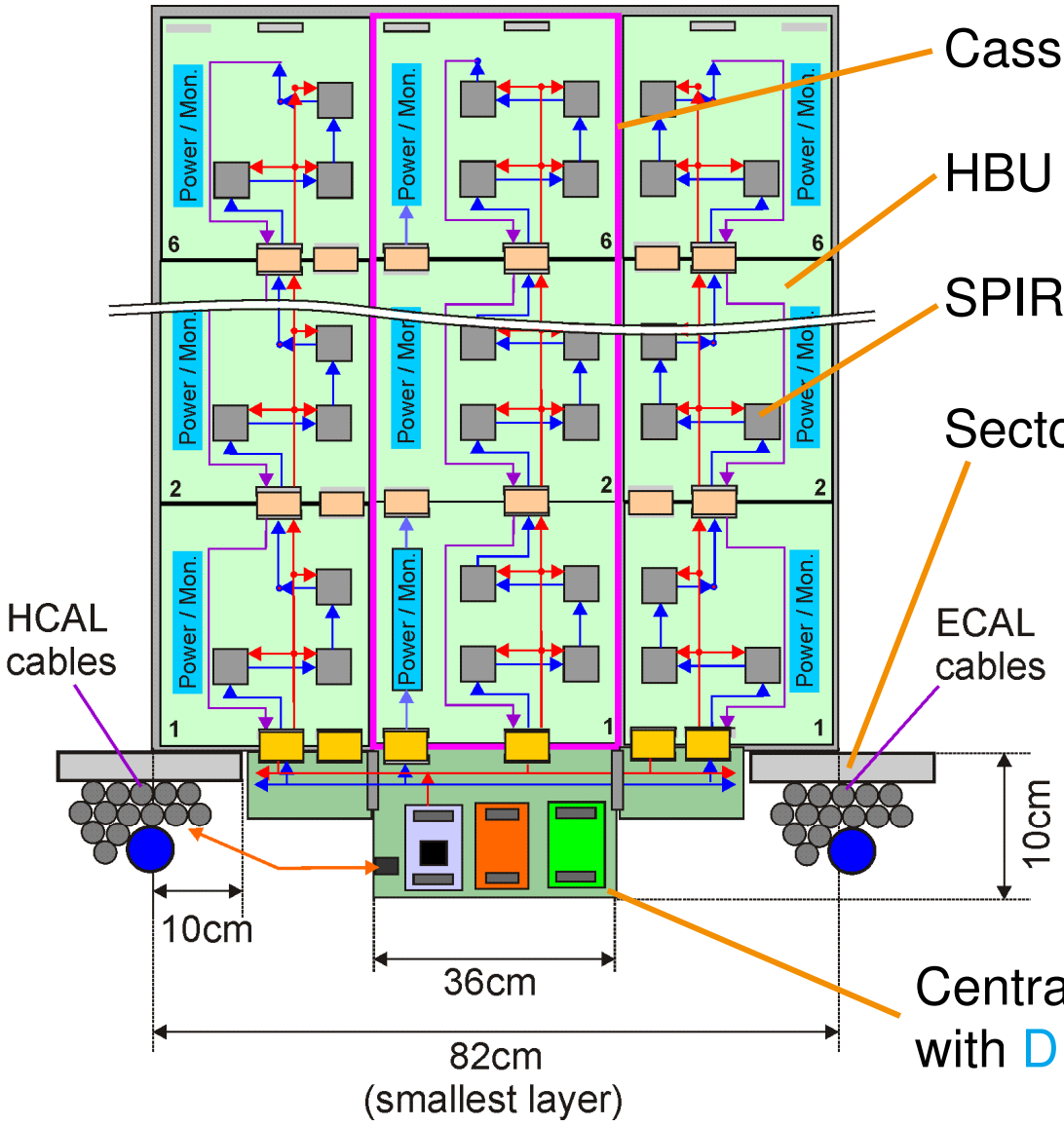
Concept : December 2007

Commissioning (status last Friday)

SPIROC2 output: LEDs firing, 3 events (triggers), 18 tiles assembled



The Next Generation



Cassette (=slab)

HBU

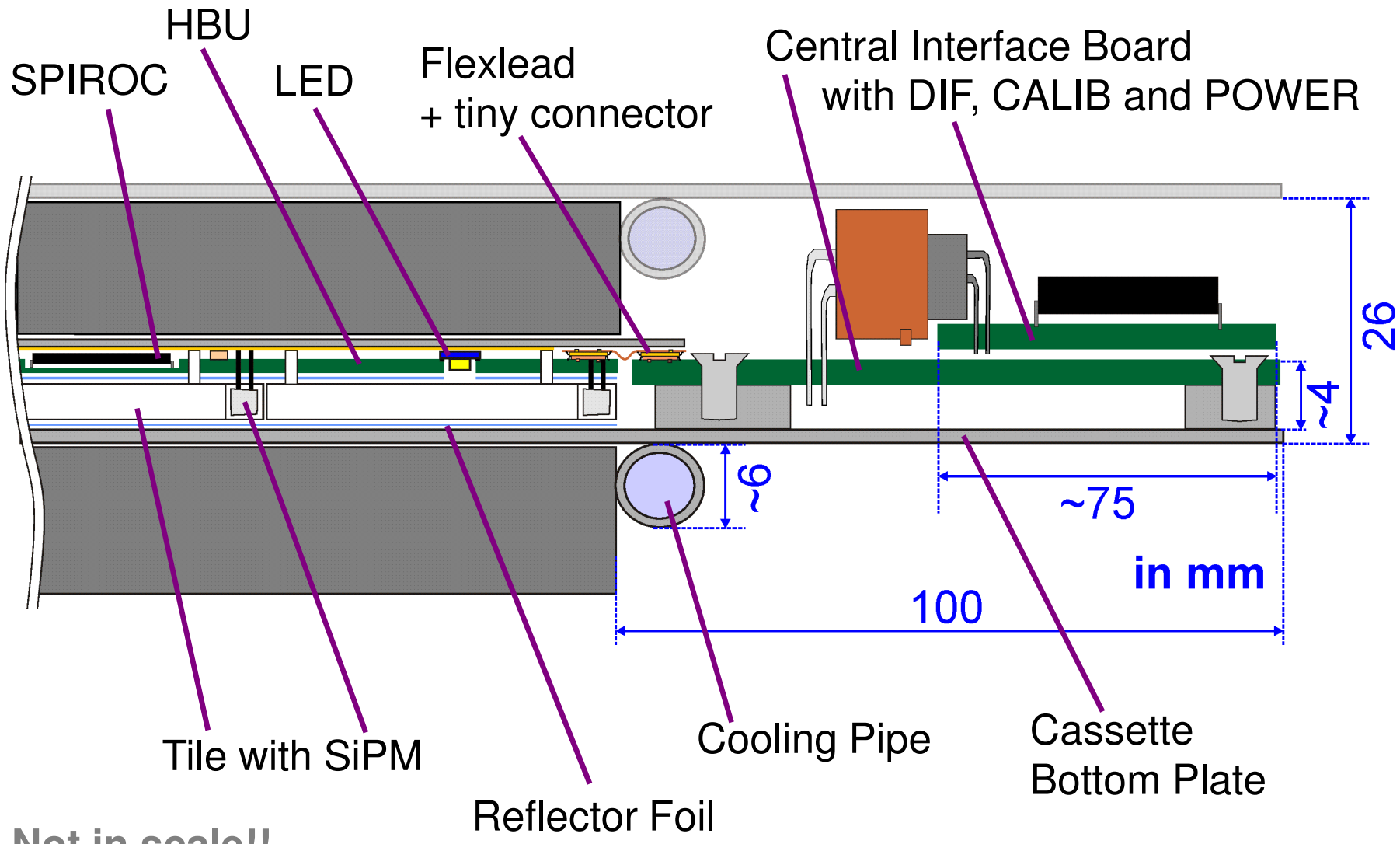
SPIROC

Sector Connecting Plate

Not in scale!!

Central Interface Board with DIF, CALIB and POWER

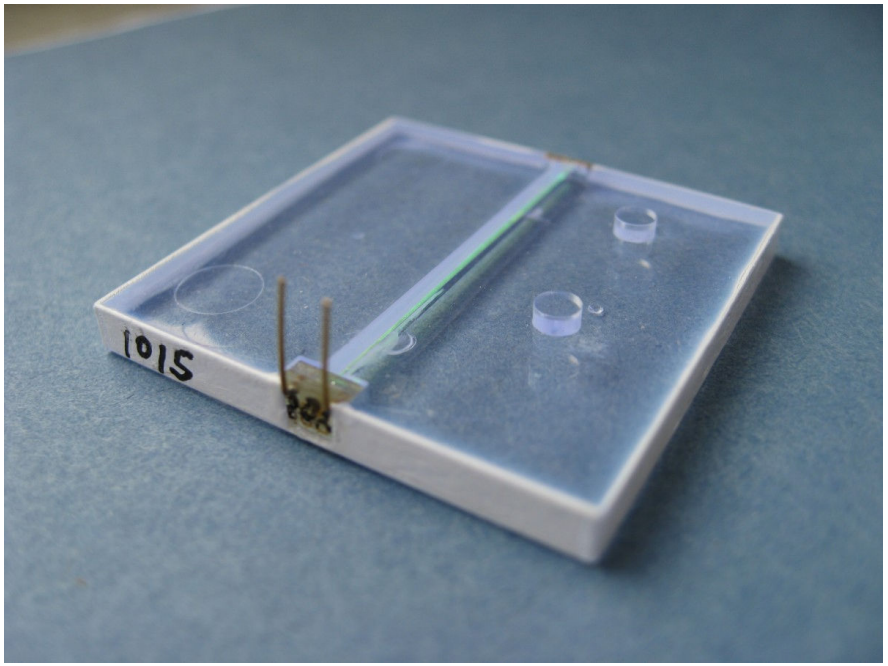
The Next Generation

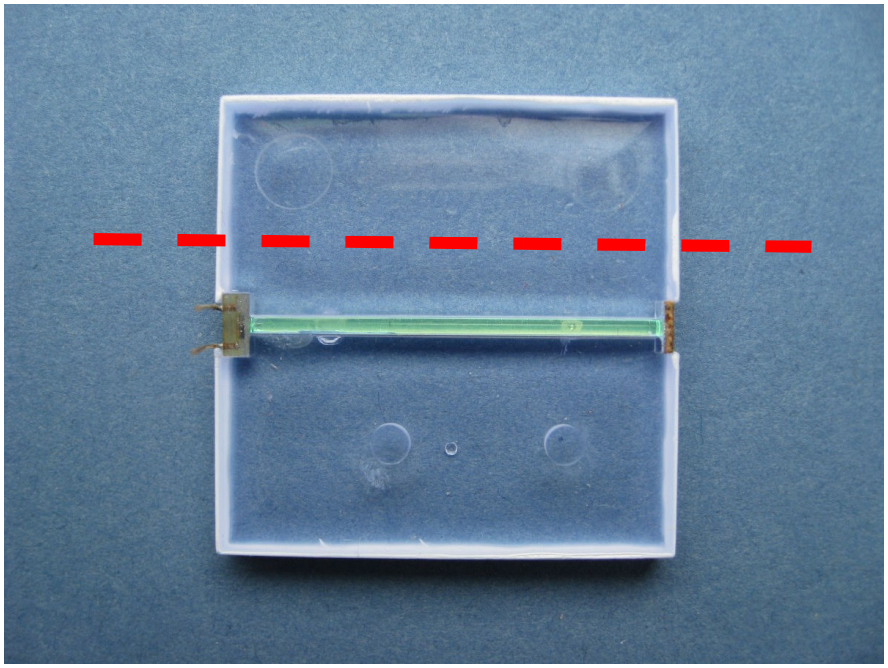


Not in scale!!
To be minimized

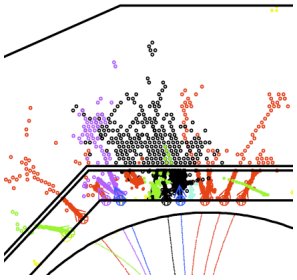
EUDET Tiles

12 tiles of new generation arrived from ITEP





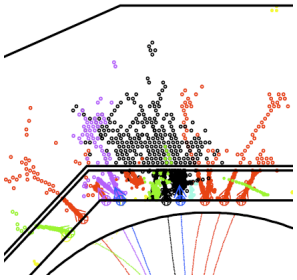
Tiles can be cut to accommodate varying layer width without affecting PCB grid



Electronics status and plans:

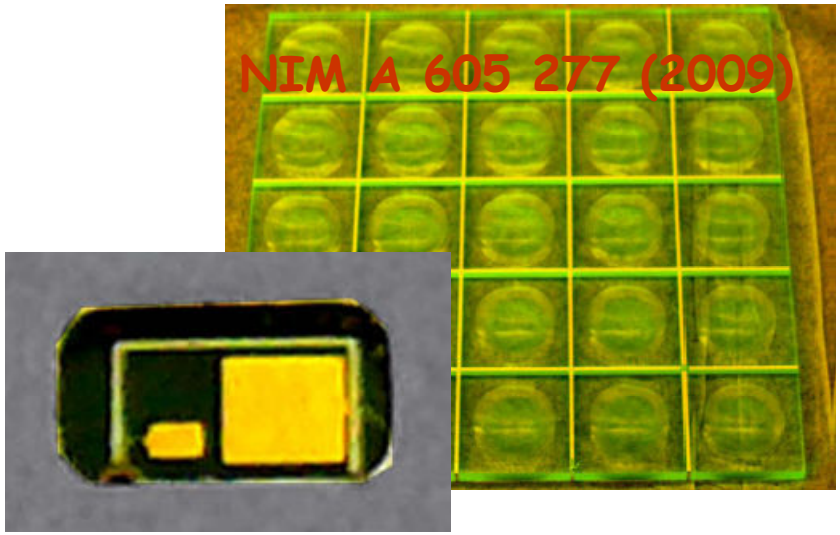
- Readout chain established with LEDs
- First base unit ready for beam test
- DAQ preparations underway (still USB based)
- Will adapt EUDET scheme following DHCAL commissioning

- 2010: Full slab (6 HBUs) tests within horizontal absorber structure
  - Requires new HBU layout with SPIROC-2
- 2011: equip em. shower size volume (12 layers, single HBU) for electron beam tests
  - Requires redesign of layer end interfaces
- Extension to hadronic volume possible if funded

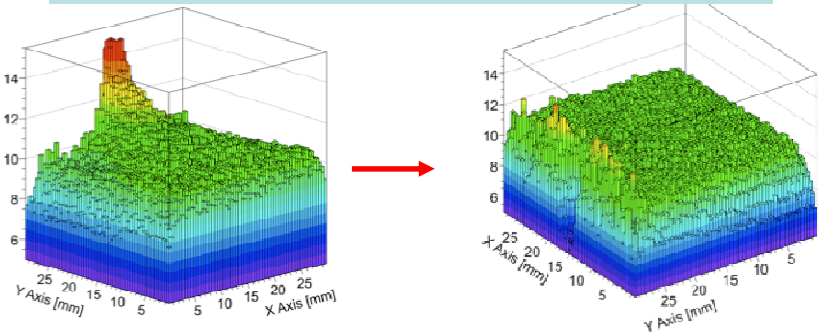


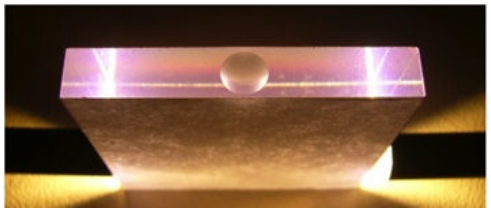
Other coupling schemes

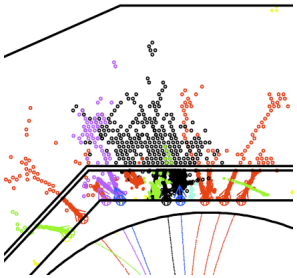
- Surface-mounted MPPCs
- Scintillator cells with dimple to compensate non-uniformity
  - See NIM paper by NIU group and D.Chakraborty's talk
- Strips a la Sci ECAL
- New idea from MPI group
  - Dimple for direct coupling from the side



All require no or minimal modification to electronics board







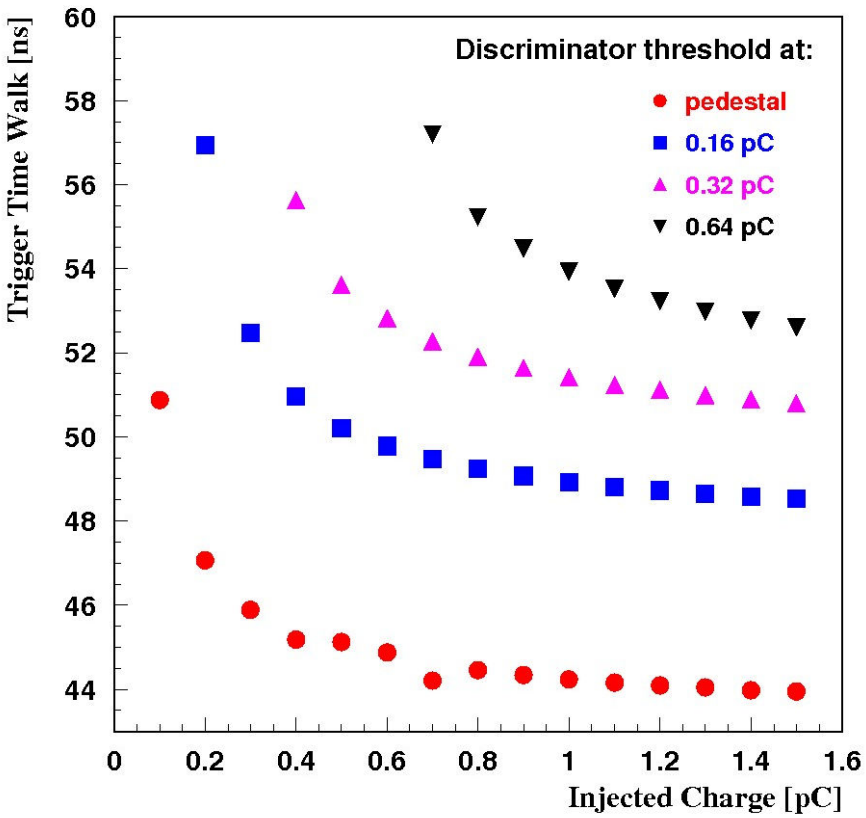
CLIC issues

- Density: jet energy performance at high energy limited by leakage ➔ study denser absorber material: tungsten
  - Test G4 simulation including neutron timing
  - Particle flow with different λ / X_0 testure
  - Even more aggressive integration demands
  - ➔ see talk by C.Grefe for further discussion

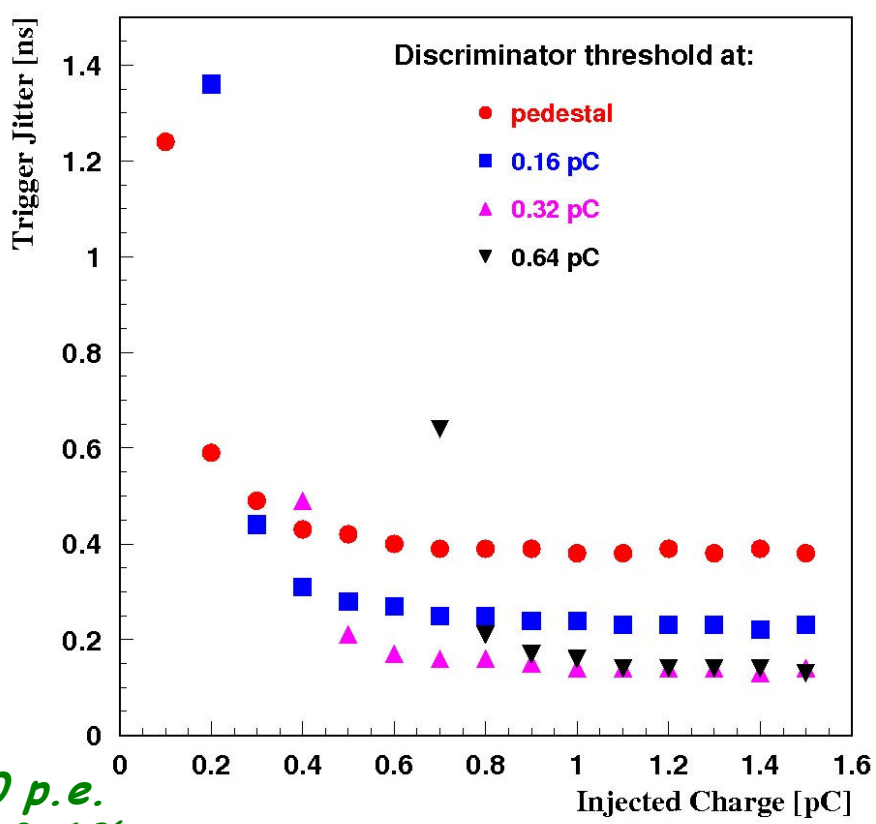
- Time stamping
  - SPIROC TDC provides O(ns) resolution
  - Scintillators and sensors to be optimized

SPIROC1 Analogue Tests

Trigger time walk



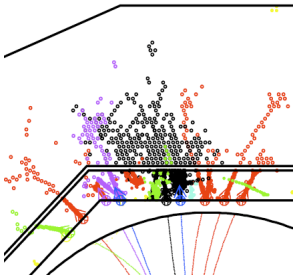
Trigger jitter



10 p.e.
@ G=10⁶

Large time-walk at small charges
=> Problematic in calibration mode

Results consistent with Orsay



Summary

- After end of physics prototype beam tests, integration issues move into focus
- Technological prototype components are available - mostly
- Put them together and make system work – exciting commissioning phase just started
- Staged prototype roadmap
- High energy issues to be tackled next