R&D toward an Integrated Readout Layer for a scintillator-based calorimeter

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Talk outline

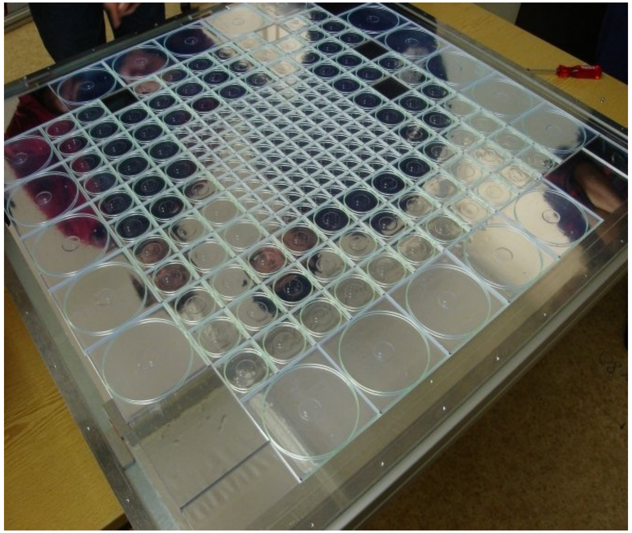
- Objective
  - Make a scalable active layer suited to large-scale production and assembly for a scintillator-based PFA-driven calorimeter.
- Challenges
  - Scintillator-photodetector coupling for millions of volume elements.
  - Signal transport without compromising hermeticity.
- Proposed solution
  - Direct coupling – eliminate the fiber.
  - Integrate photodetector and FE electronics into layer support structure.
- R&D status
- Summary and outlook

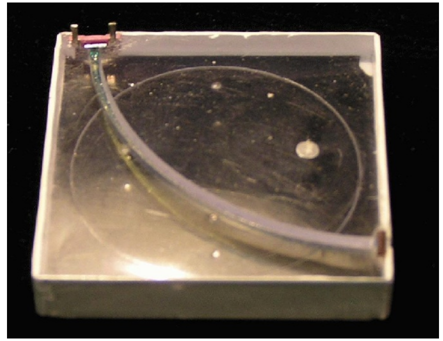
Objective and Challenges

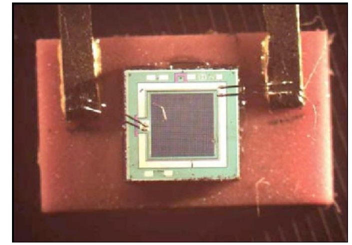
- Beam tests have demonstrated that small scintillator tiles read out with SiPMs satisfy the performance specs for a PFA-driven Hcal.
- The next step is to build a scalable physics prototype with an active layer suited to large-scale production and assembly.
- Embedding WLS fibers in scintillators and mating the fiber end to mm^2-sized SiPMs for millions of channels is quite a challenge.
- A PCB adjacent to the scintillator layer could be used to provide mechanical support, carry signal & bias traces to/between SiPMs FE electronics (ASICs & FPGAs for processing, LVDS for transmission out of the detector) and calibration LEDs – everything on the PCB.
- Mounting the SiPMs flat on this board offers clear assembly advantages.

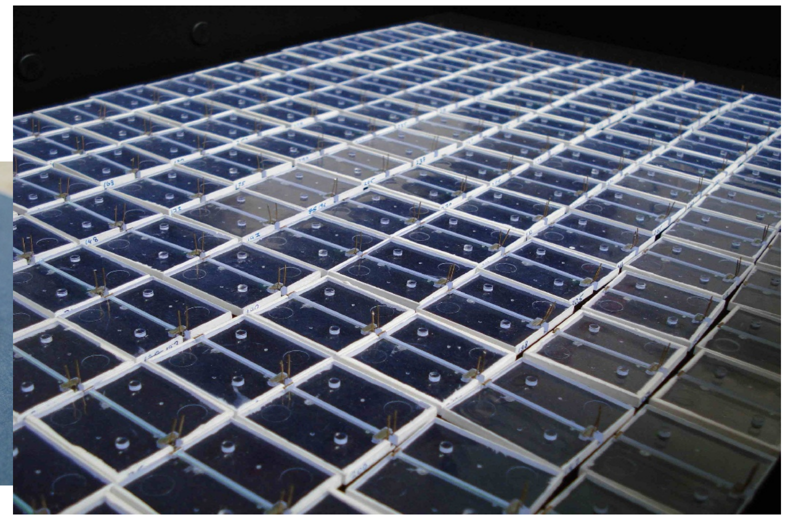
Objective and Challenges (contd.)

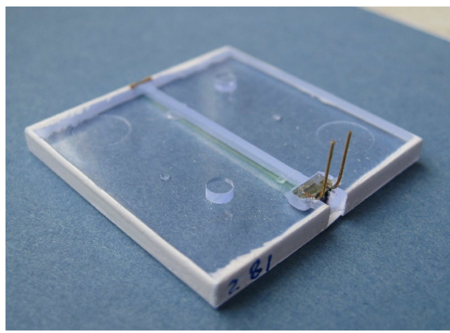
- CALICE Scint HCal employing WLS fiber tested in beams, and newer version:











An alternative solution

- Eliminate the fiber
- Concerns and answers
  - Need blue-sensitive photodetectors or WLS-doped scintillator. Blue-sensitive MPPC's are available. Signal strength is not a problem.
  - Uniformity of response over the cell volume. “Flat”-faced cells show considerable non-uniformity, but we have been able to solve the problem by making a depression on the cell in front of the SiPM.
- This scheme also allows for easy mounting of the SiPMs on a PCB that lies between the active (scintillator) and the absorber layers.
  - ASICs and FPGAs to do the front-end signal processing, the LVDS transcievers+connectors for routing the processed signal, as well as the calibration LEDs will be mounted on this PCB.

An alternative solution (contd.)

- Variants of direct coupling are being investigated independently
  - e.g. "edge-mounting" by MPI – see talks by Boudry & Sefkow at this workshop.
  - In communication, helps side-by-side comparisons, complementarity, cross-fertilization of ideas. MPI has verified and adopted the "dimple" solution developed by NIU to improve uniformity.
- Studies presented here – the first-generation "face-mounting" option - are carried out as a NIU-Fermilab collaborative project.
- Planes of next generation will be beam-tested in the CALICE/EUDET stack.

R&D status

Uniformity scan of a 3 cm x 3 cm x 0.5 cm flat-faced square cell with direct coupling.

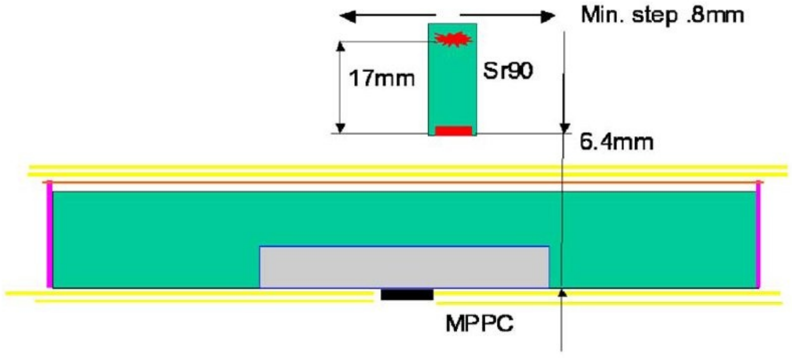
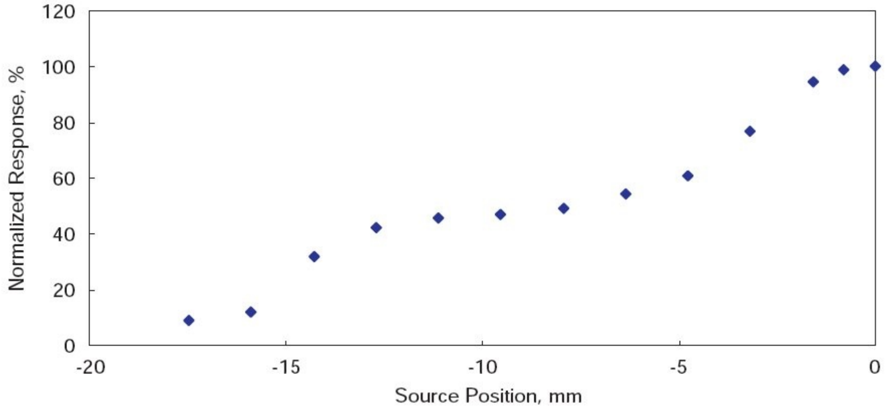
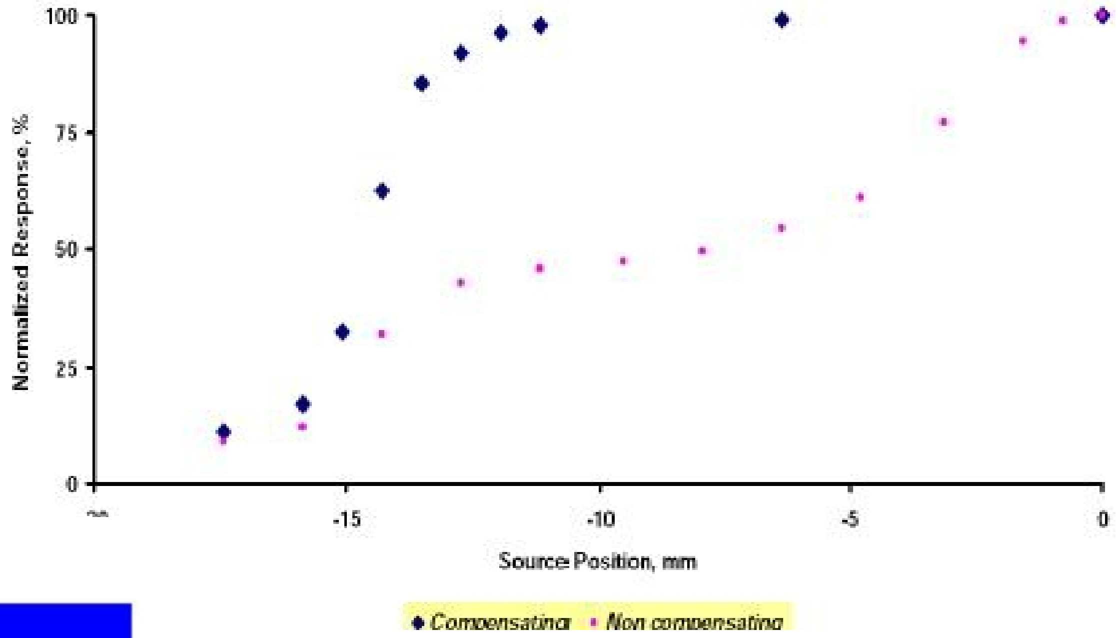
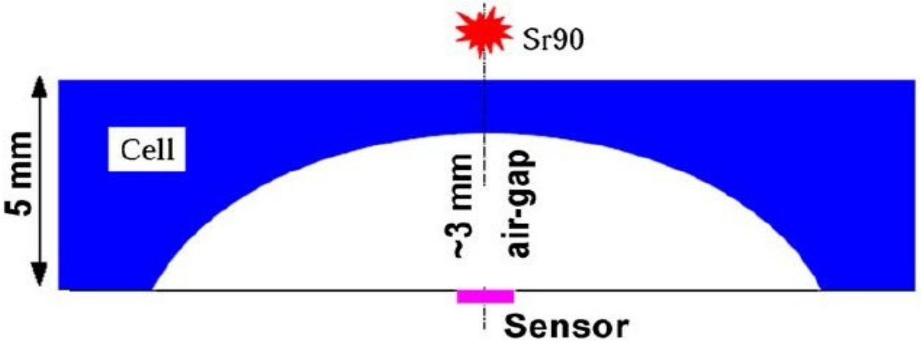


Fig. 1. Tile uniformity scan schematic (not to scale).

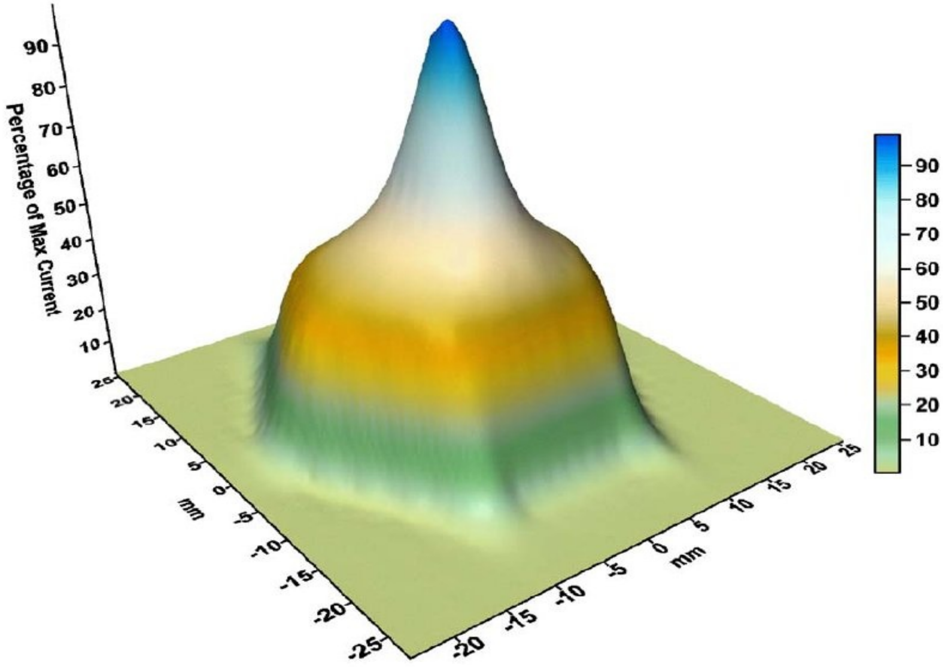


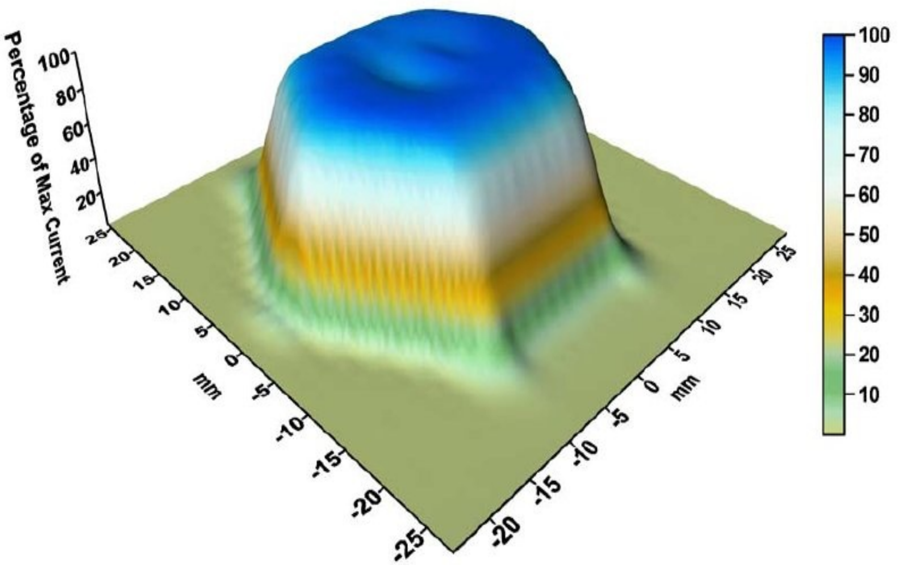
Uniformity improved by machining a depletion on cell face



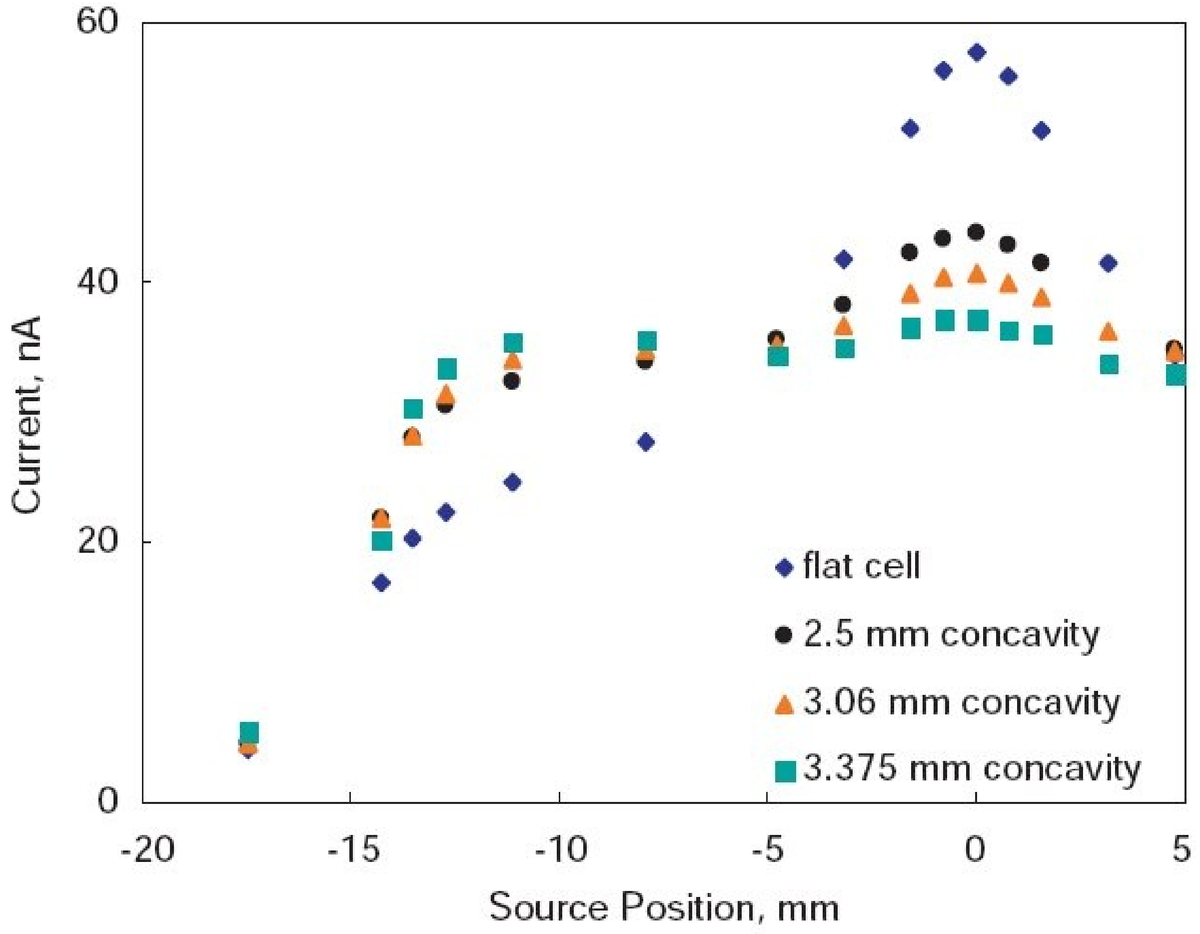


Comparisons between "flat" and "concave" cells





Optimization of "concave" cells



MIP response of a "concave" cell

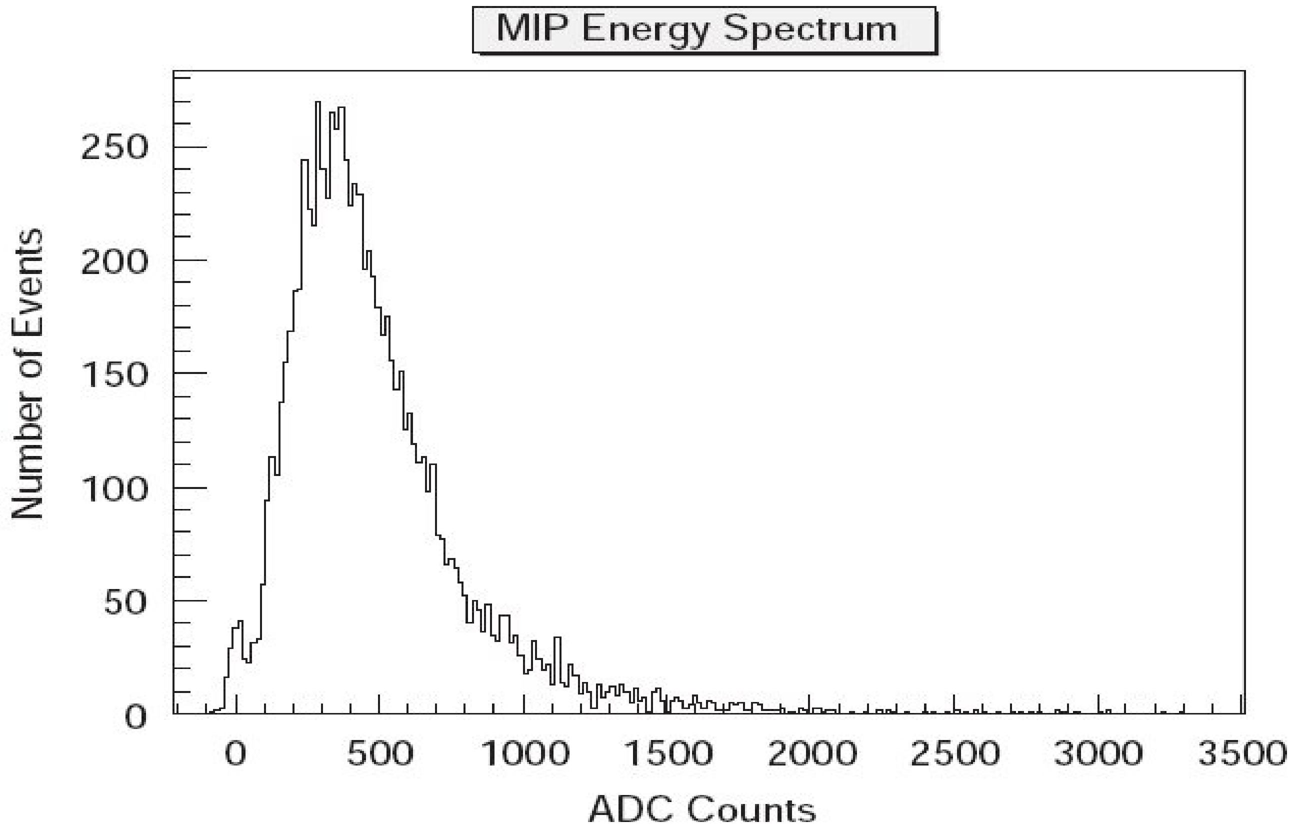
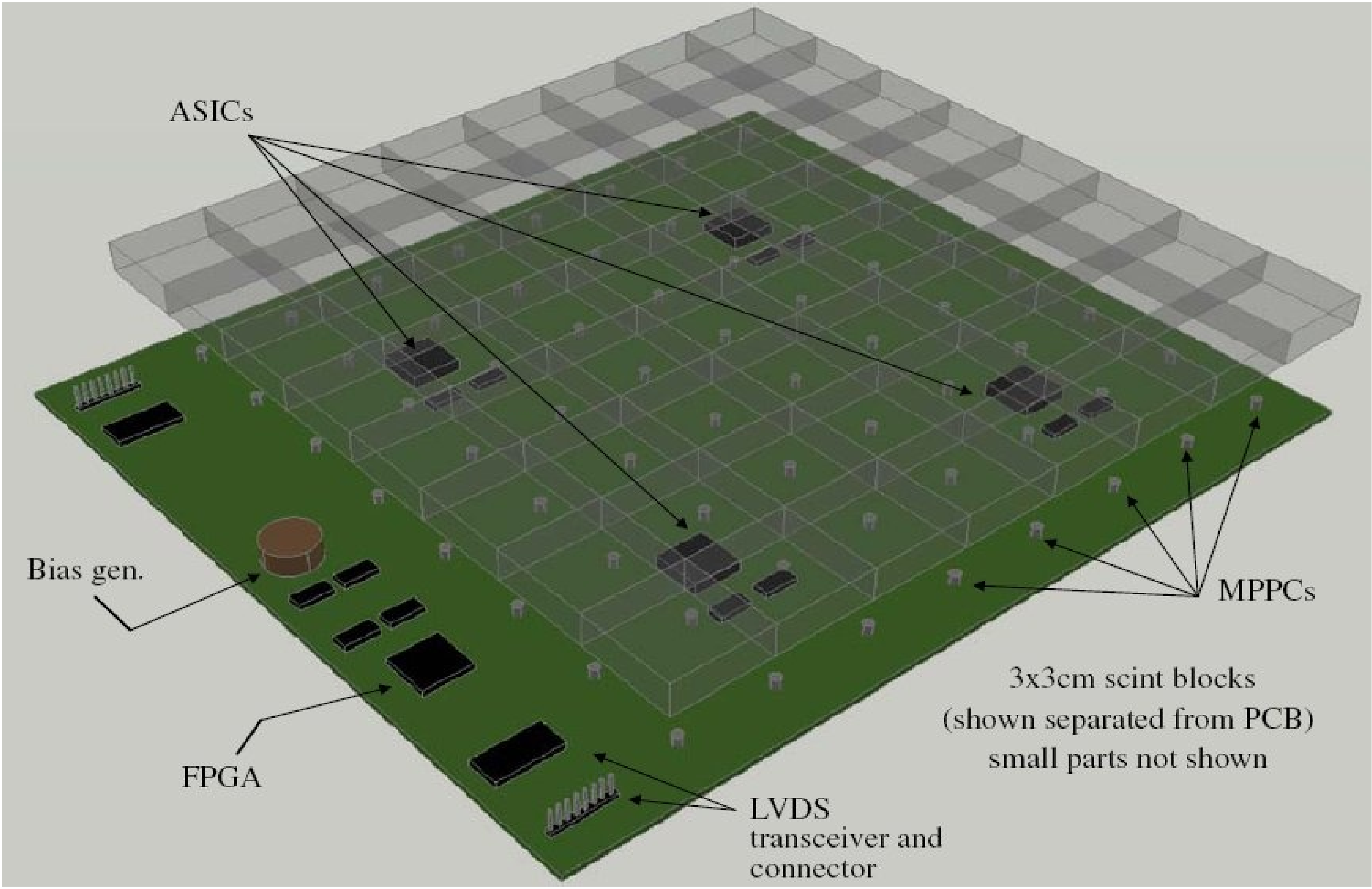


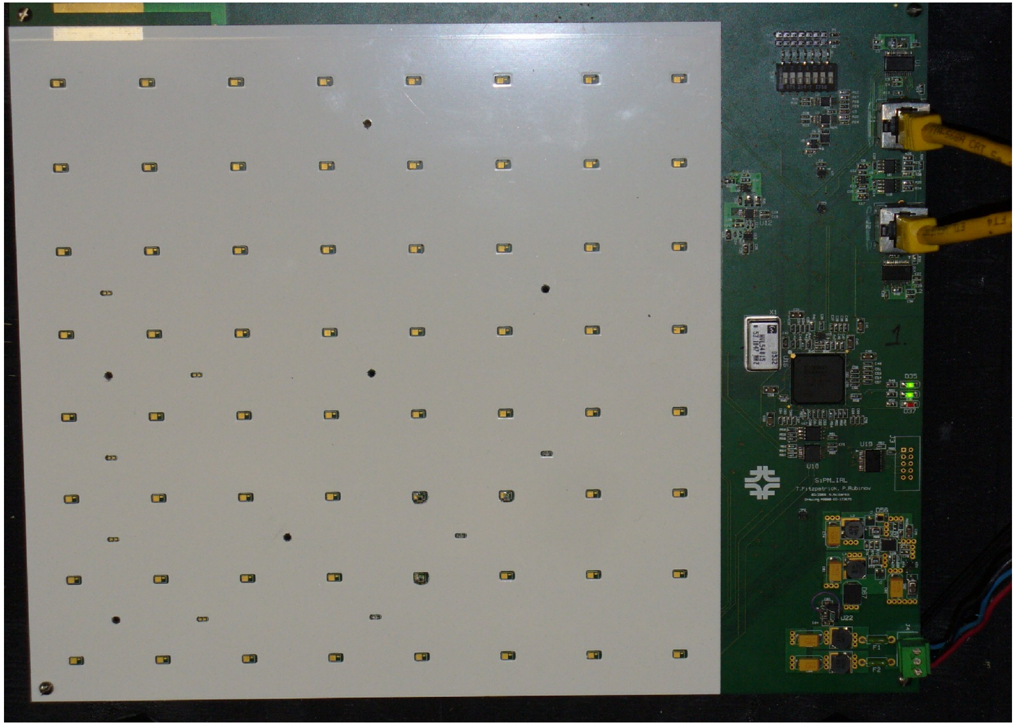
Fig. 9. Response of a directly coupled concave tile to cosmic ray muons.

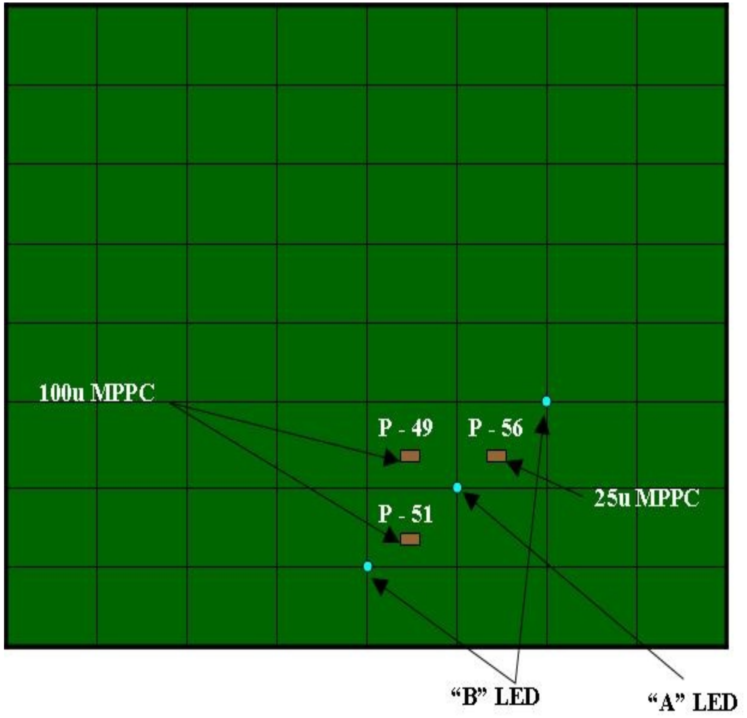
The Integrated Readout Layer (IRL)



Elements of the IRL

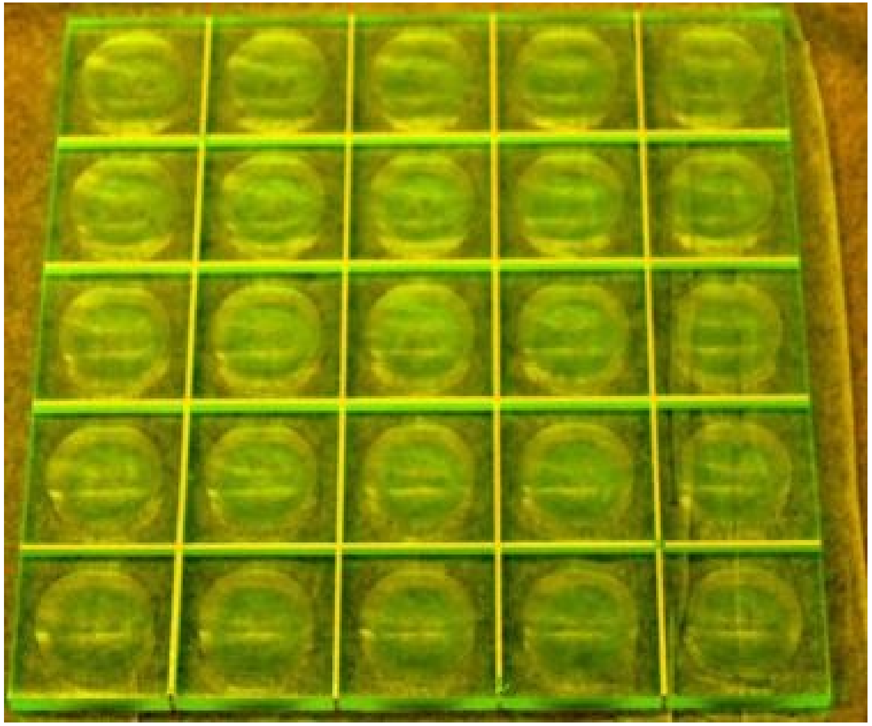
- The IRL board has 64 slots for SiPM's. Each slot has a high gain and a low gain channel. This board has 8 places for calibration LED's.
- Designed and produced by Fermilab





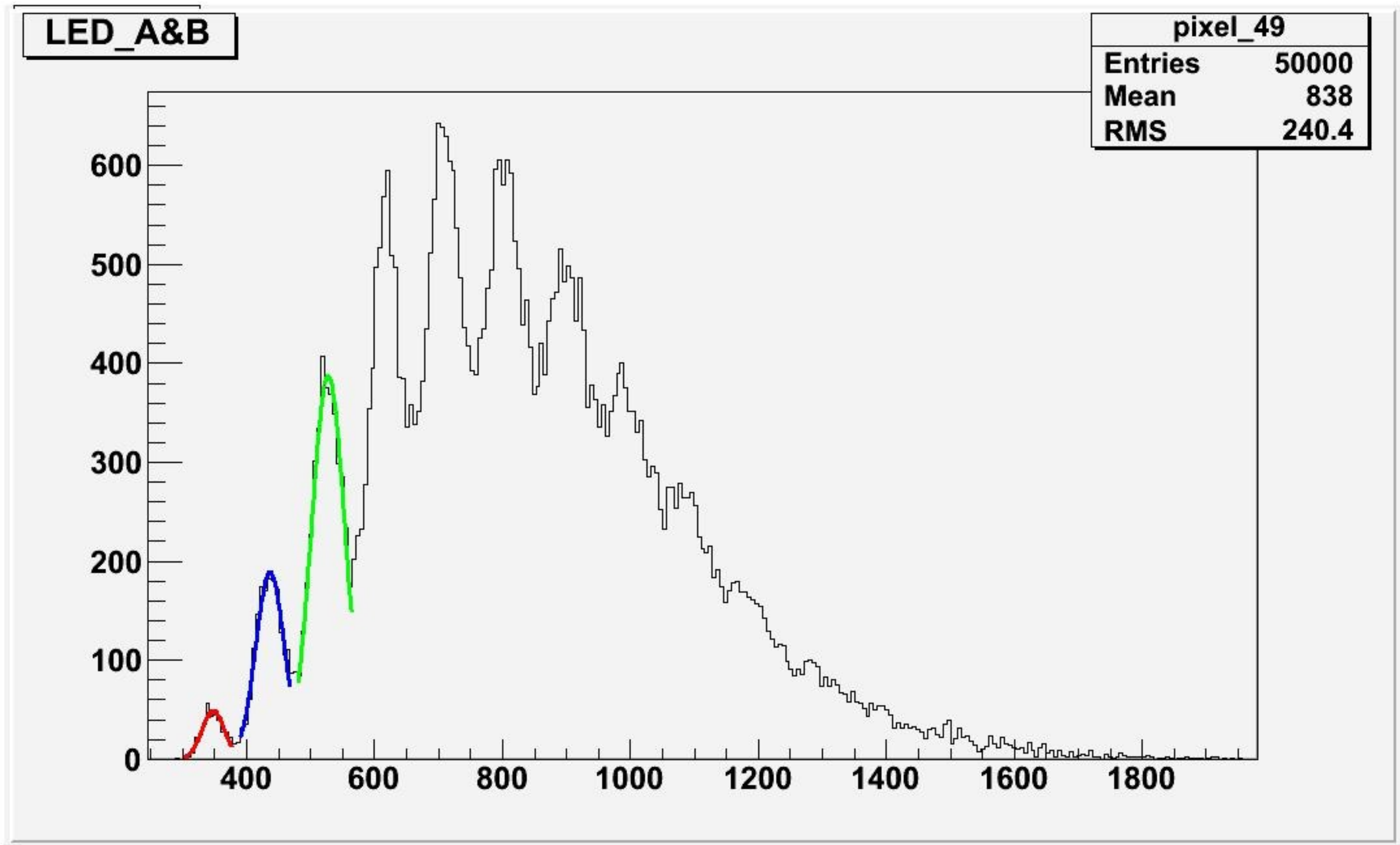
Elements of the IRL (contd.)

- The scintillating megatile placed over the SiPMs and calibration LED's. The SiPMs are "directly" coupled to the 5x5 array.



Testing the IRL

- The IRL shows the PE peaks in a low-gain channel.



Testing the IRL (contd.)

Calibration: Light is generated by one surface-mount LED at the corner of 4 tiles. Percentage deviations are w.r.t to the mean calculated from all four tiles.

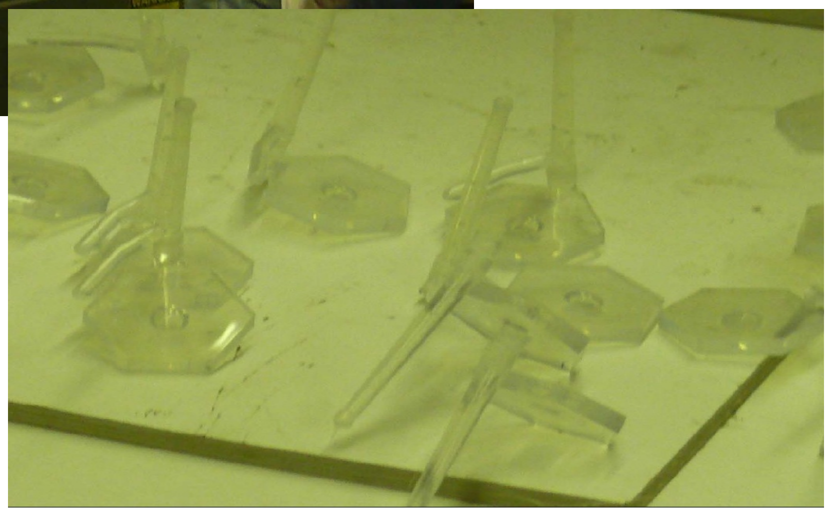
	Light Distribution			
	P49	P51	P53	P56
Measurement 1	7.77%	5.57%	-12.31%	-1.04%
Measurement 2	8.49%	7.32%	-13.21%	-2.60%
Measurement 3	7.13%	2.03%	-8.27%	-0.89%

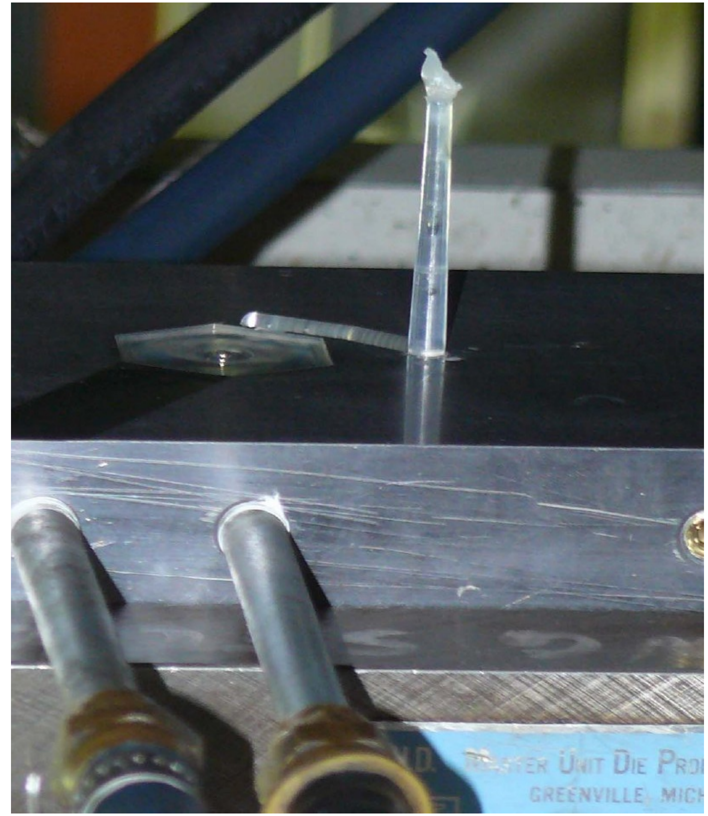
Low gain mode

	Light Distribution			
	P49	P51	P53	P56
Measurement 1	9.19%	5.49%	-7.65%	-7.03%
Measurement 2	8.97%	5.96%	-7.57%	-7.37%

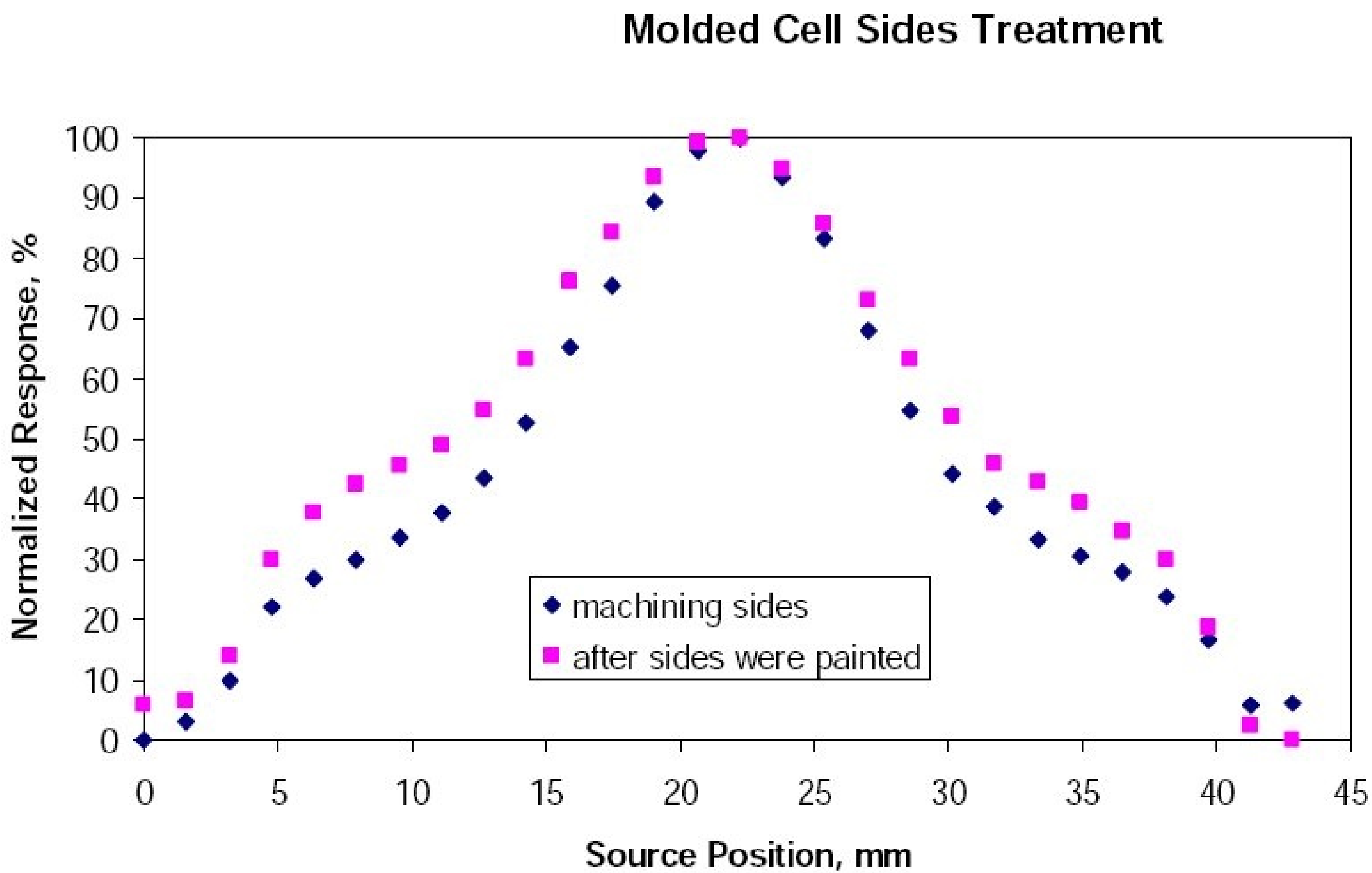
High gain mode

Injection molding of tiles





Tests of injection-molded tiles



Summary

- Direct coupling works.
  - MPPC's offer adequate signal response with nice PE resolution.
  - Concave cells afford excellent uniformity of response.
- The Integrated Readout Layer concept with SiPM's, calibration LEDs, FE electronics mounted on the board has been shown to work.
  - Much more work is needed toward a physics prototype.
  - Easier fabrication of megatiles, e.g. using injection molding remains to be investigated.
- In principle, the idea should be applicable to ECal as well.
- See NIM A **605** 277 (2009) for more details.

Plans

- Fully characterize and investigate tolerances associated with the current IRL prototype.
- Use this experience to design and prototype the next generation IRL.
- Test a few planes in the CALICE/EUDET test beam module.

Back-up slides

Testing the SiPMs

- Need to bias large number for long periods

Proposal:

•Use elastomeric connectors (e.g. Fujipoly) to make contact to a large number of chips with simple electronics to do simple, DC tests : I-V curve

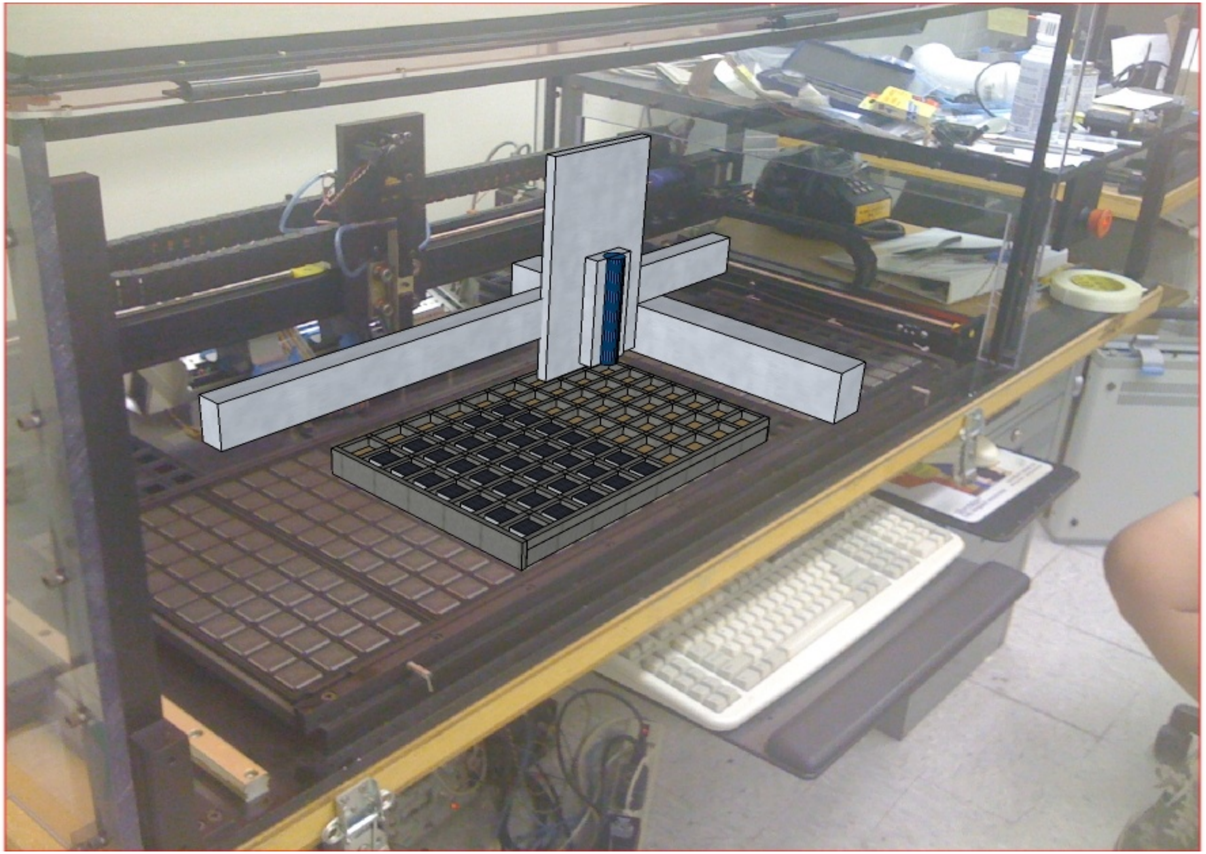
or pogo pins or temporary die attach or….
Depends on what exactly the units under test look like

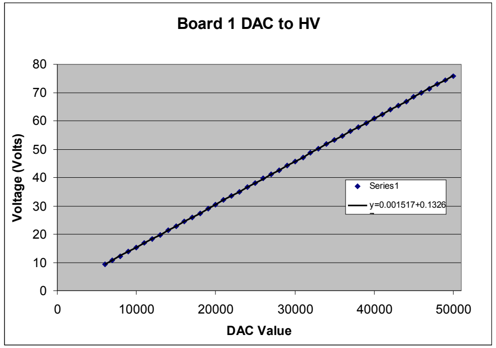
•Use a flying head to move a light source, more complex, high speed electronics to an individual chip for more detailed testing (gain, eff, etc.)

•Enclose everything in a light-tight, temperature-controlled box.

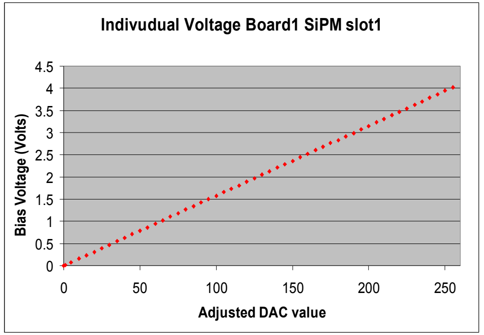
Testing the SiPMs (contd.)

- Fermilab has used a chip-testing robot for many projects

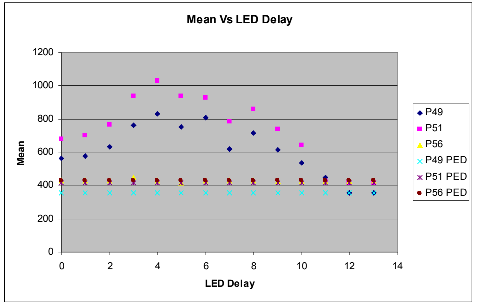




Board 1 DAC to HV
Voltage (Volts)
80
70
60
50
40
30
20
10
0
0
10000
20000
30000
40000
50000
DAC Value
Series1
y=0.001517+0.1326



Indivudual Voltage Board1 SiPM slot1
Bias Voltage (Volts)
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
50
100
150
200
250
Adjusted DAC value



Mean Vs LED Delay
Mean
1200
1000
800
600
400
200
0
0
2
4
6
8
10
12
14
LED Delay
P49
P51
P56
P49 PED
P51 PED
P56 PED