IR Transparent Si microstrips

(alignment optimized Si sensors)

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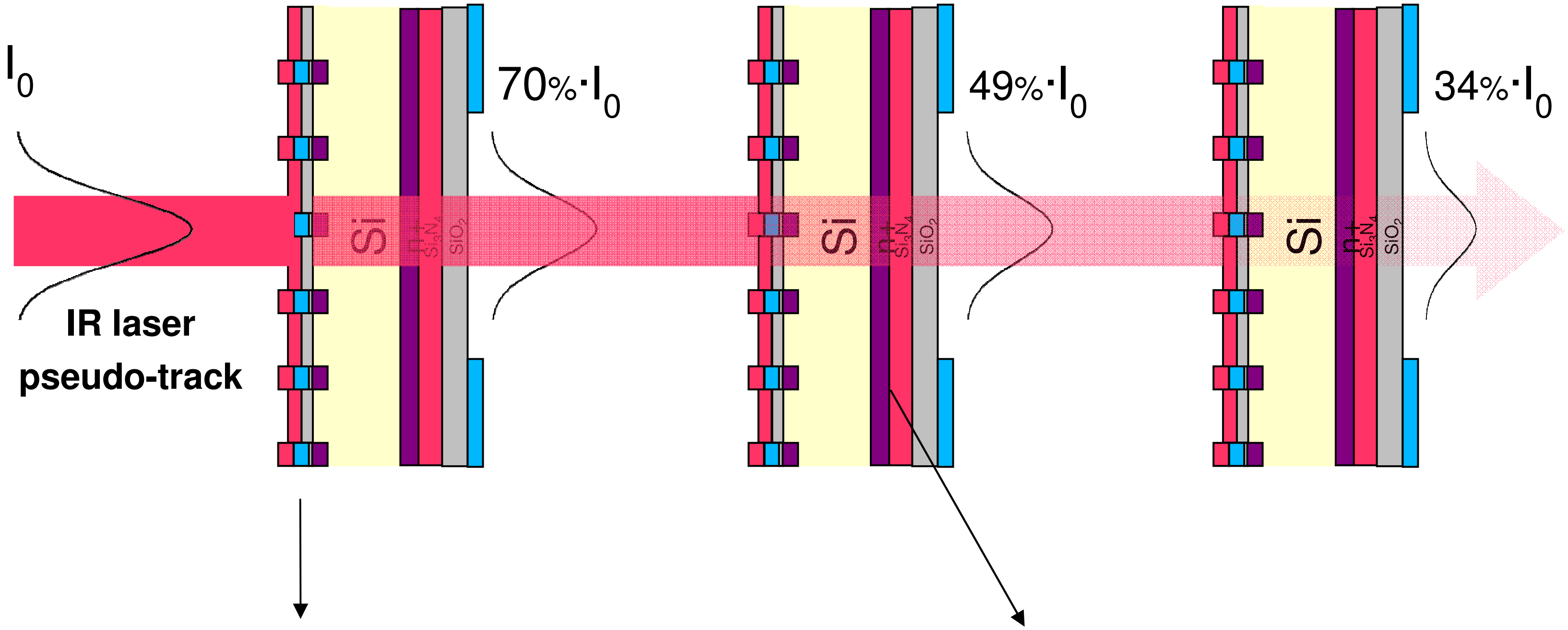
IR track alignment

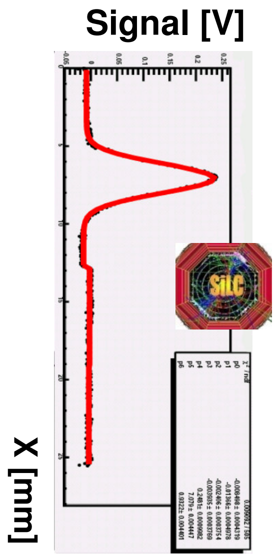
- Aim: align Si microstrip sensors using IR laser tracks



IR laser pseudo-track

IR light is partially absorbed by Si

φ~1 mm opening in Al allows beam-through



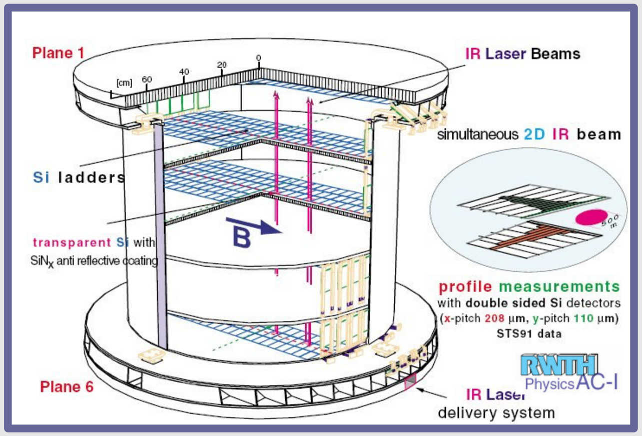
P. Kvasnicka

- Higher %T ⇒ simpler implementation of the system:

Transmittance	90%	80%	70%	60%	50%	40%
Traversed	30	15	10	7	5	4

- System features:
  - Laser intensity~200 MiPS ⇒ **sharing same DAQ as Si detector**
  - Silicon modules are directly monitored, **no external fiducial marks**

An idea that works ...



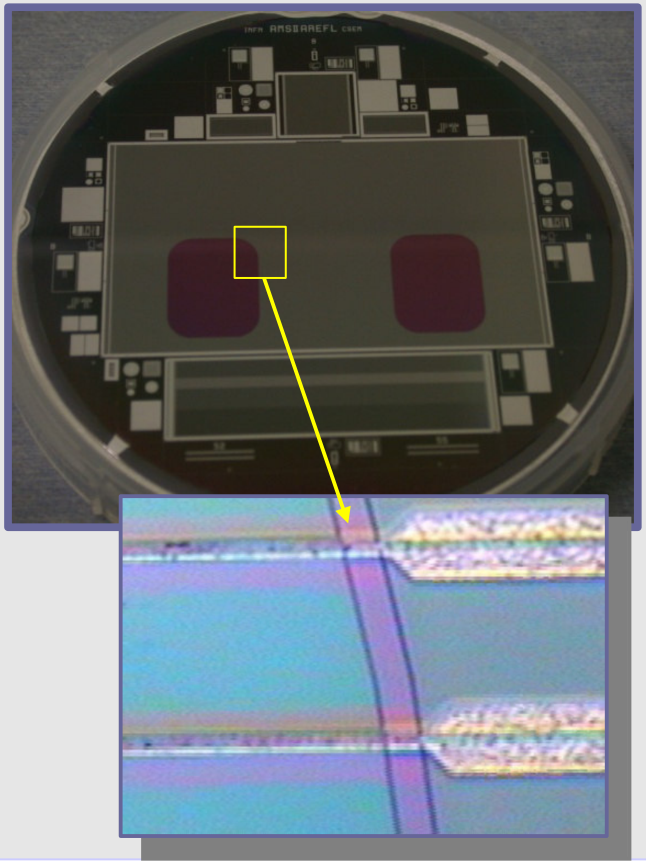
AMS-01 innovation (W. Wallraff)

λ = 1082 nm, 110 µm RO pitch

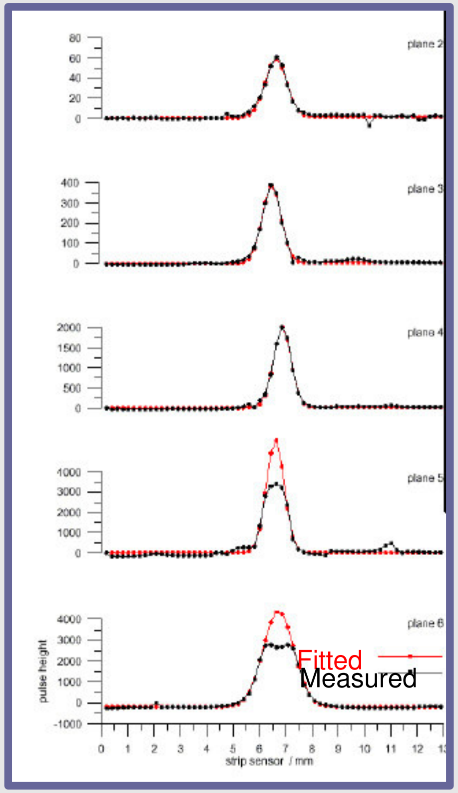
IR “pseudotracks”

1-2 µm accuracy obtained

Transmittance~ 50%



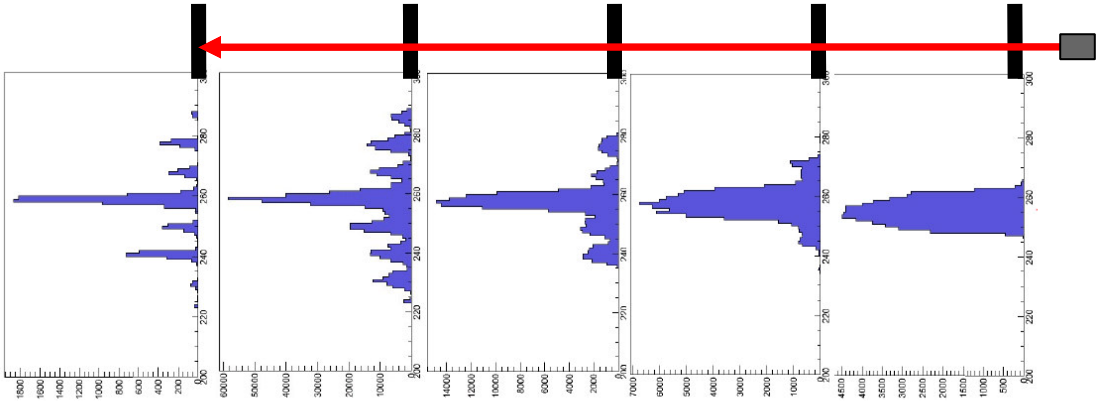
Up to 4 ladders traversed



CMS
TEC

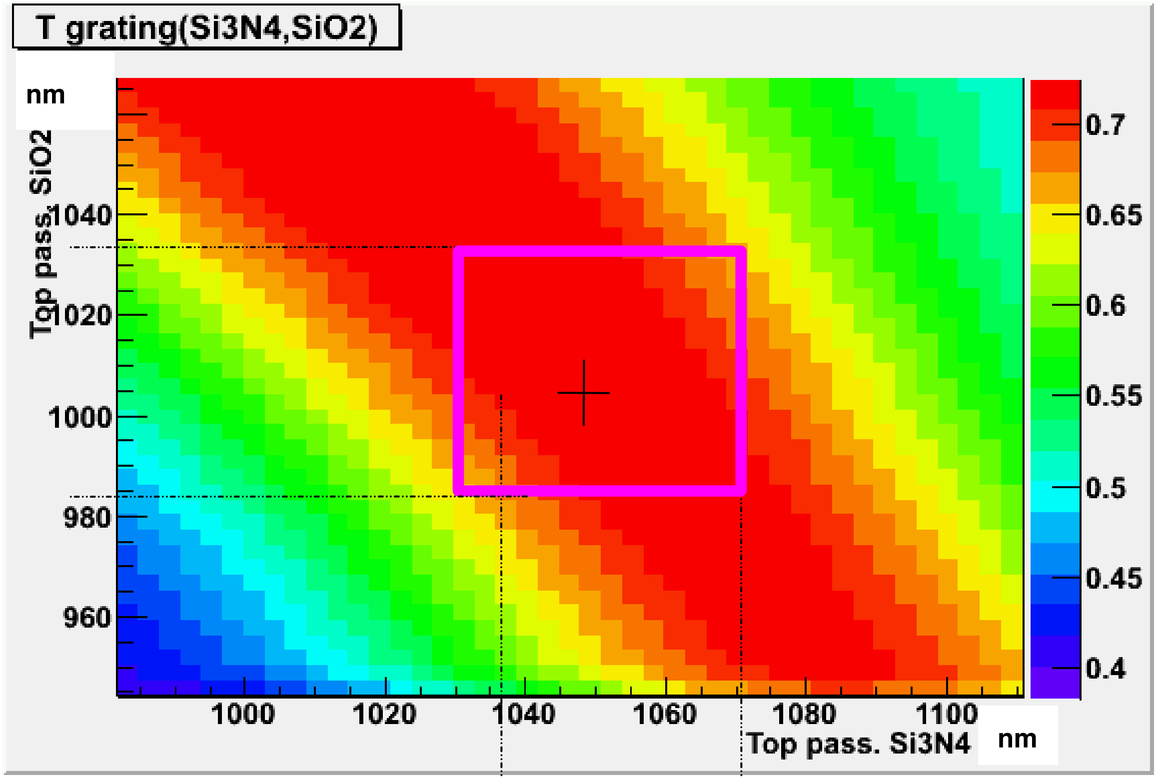
λ = 1075 nm

- Optimization of sensors not included from beginning of sensor design ⇒ **lower transmittance** ~20%
- Some sensors need to be operated in saturation
- 100 µm reconstruction error needed for L1 trigger



Constraints for maximum %T

- Developed full simulation of light propagation through sensor multilayer. Diffraction by strips taken into account (first time such detailed simulation has been done)
- Transmittance depends mostly on pitch over strip width
- Idea to boost %T:
  - Choose optimal layout (sw/pitch=10%)
  - Use passivation as an AntiReflection Coating (ARC)
- Recipe for production process:
  - Deposit each layer (thickness tolerance ≤5%)
  - Correct last Si3N4 layer if needed, according to plots like:



Si3N4	1046	X
SiO2	1006	Y
Al	950	
SiO2 (FO)	1000	
295 µm Si + implants		
SiO2	1020	
Si3N4	1005	

λ=1085 nm

CNM sensors (GICSERV08)

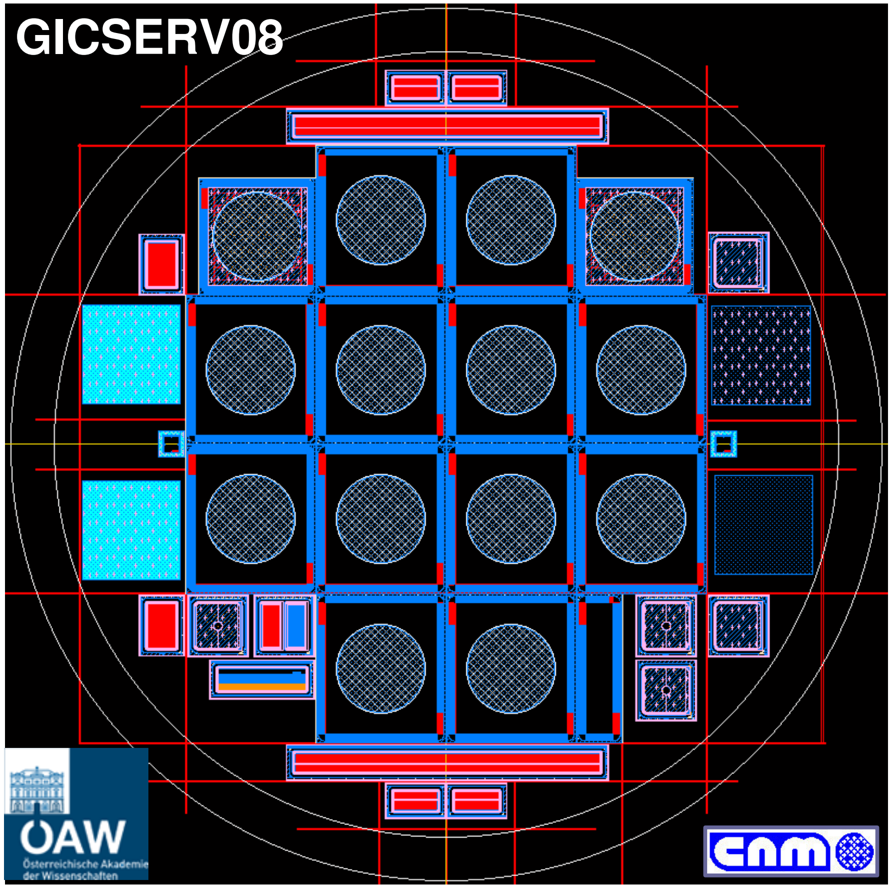
- Prototypes built by CNM-Barcelona (Spain)

- Aims:

— Test %T vs multigeometry

— Use optical test structures (continuous layers) to extract refraction index and control deposition

— Test of electrical test structures



- 5+1 wafers
- 12 μstrip detectors per wafer (6 with intermediate strips, without metal contacts)
- 50 μm RO pitch (25 μm interm. strip)
- 256 RO strips
- 1.5 cm length varying strip width (3,5,10,15 μm)

- Mask designed by **D. Bassignana** (CNM)
- Electronic test structures designed by **M. Dragicevic** (Vienna) including:

  CAP TS AC, CAP TS DC, CMS Diode, MOS, GCD, Sheet
- Optical test structures available (Si, Si+p^+,SiO_2, SiO_2+passivation)

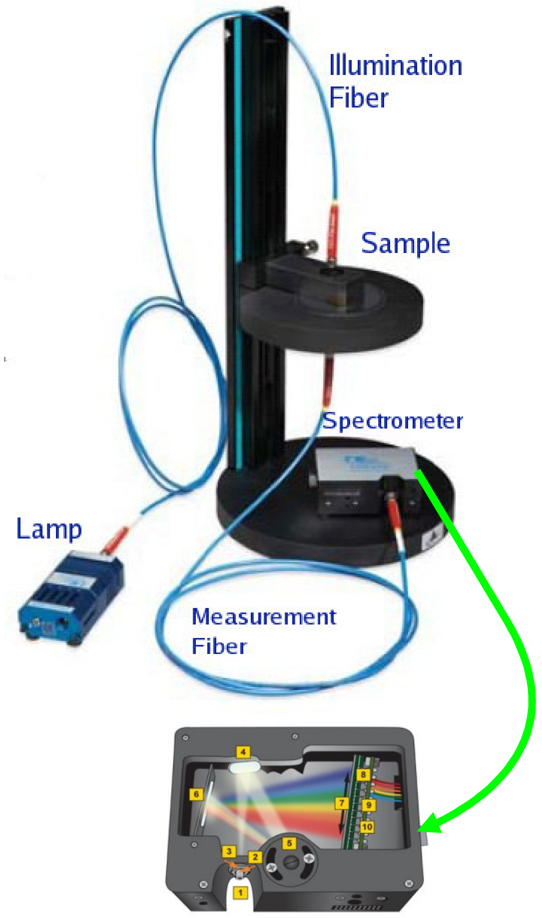
Production progress

- Production started on 11th of May 09
- All processes done until deposition of 1st passivation layer (end of July 09)
- Thickness of all layers measured after each deposition

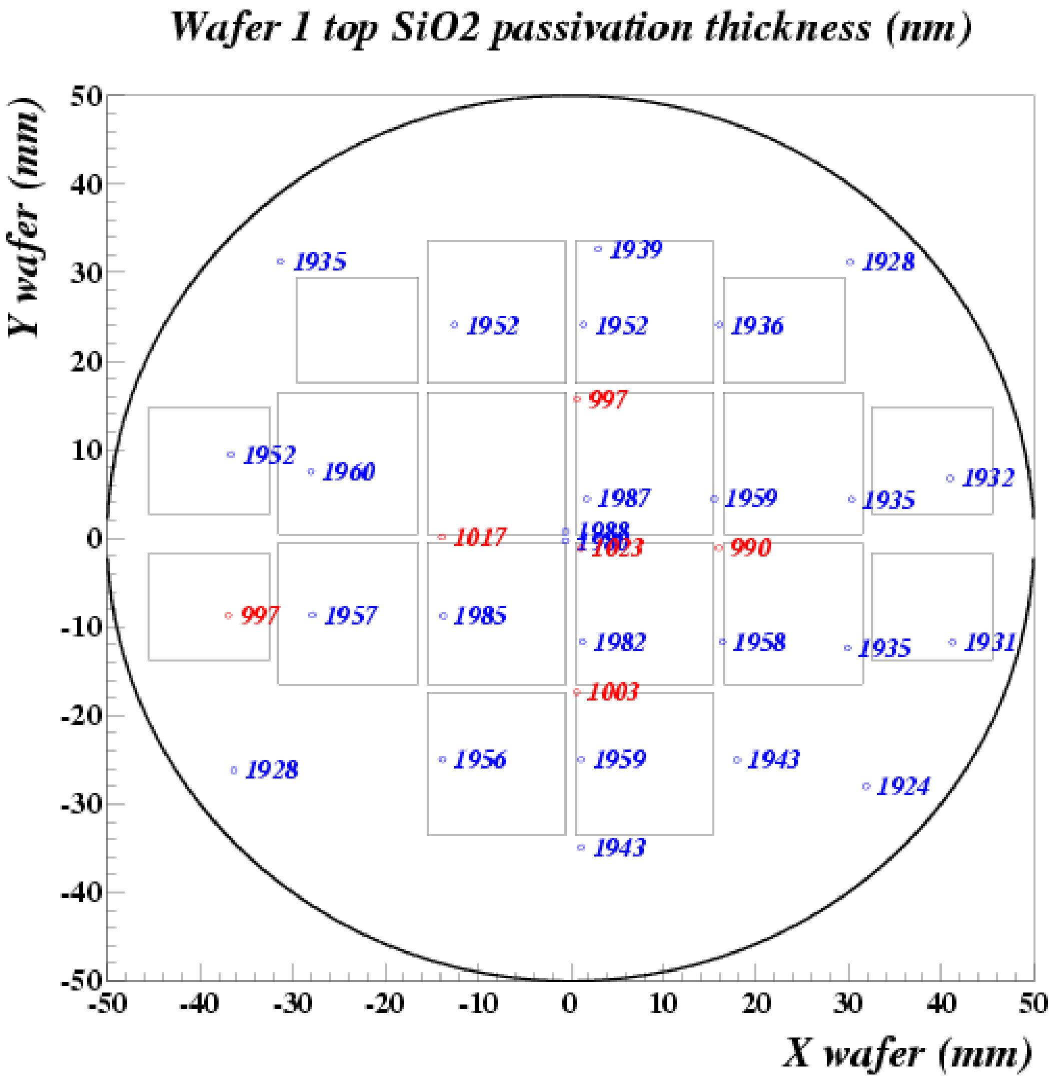
- For the 1st batch, we decided to hold the production just before deposition of the last passivation layer. Like this we can measure the wafer at an intermediate step

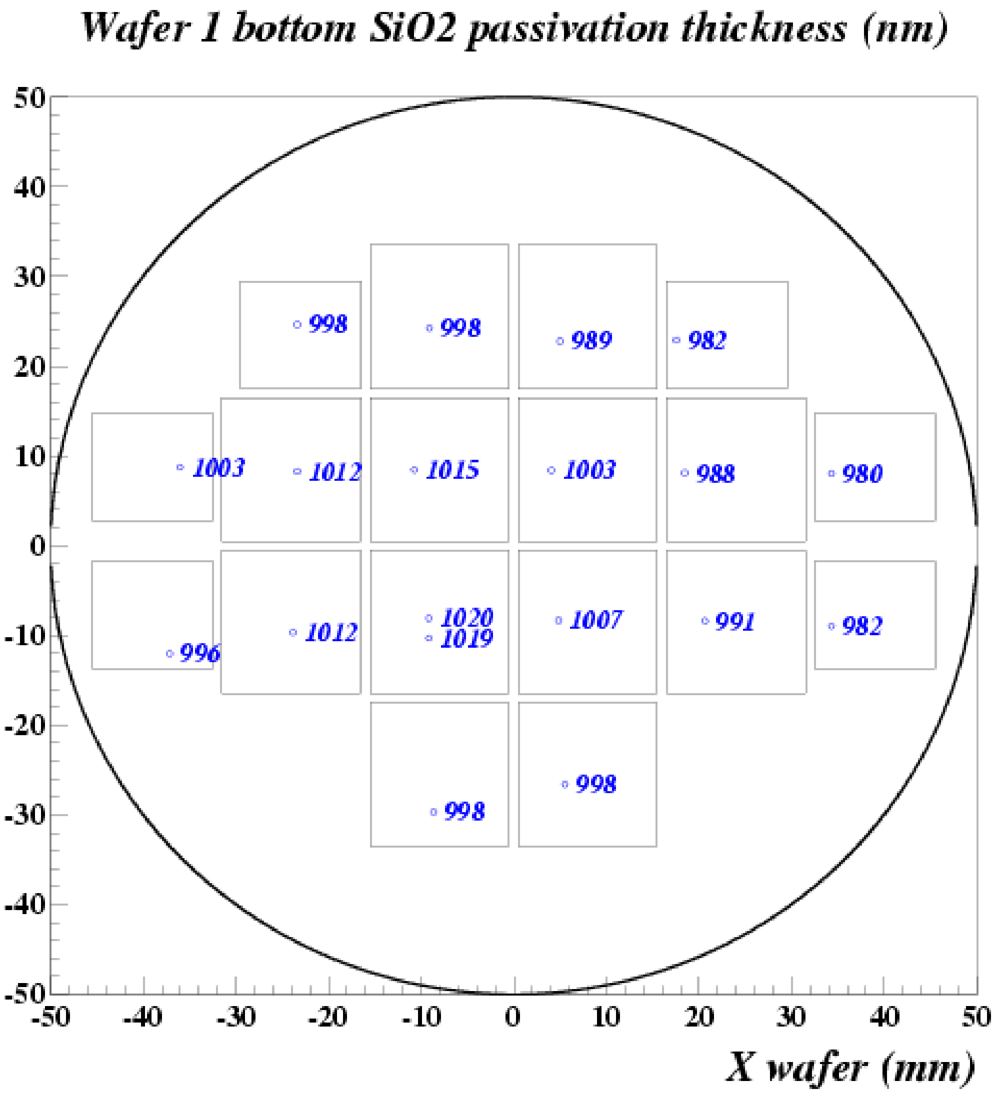
- Optical measurements were taken by end of July
  - — Test structures (no internal structure)
  - — Sensors (strips ⇒ diffraction)

- NIR spectrophotometer used for Optical measurements
  - — %T : Measures spectrum with sample in/out
  - — %R: Comparison against calibrated reflector



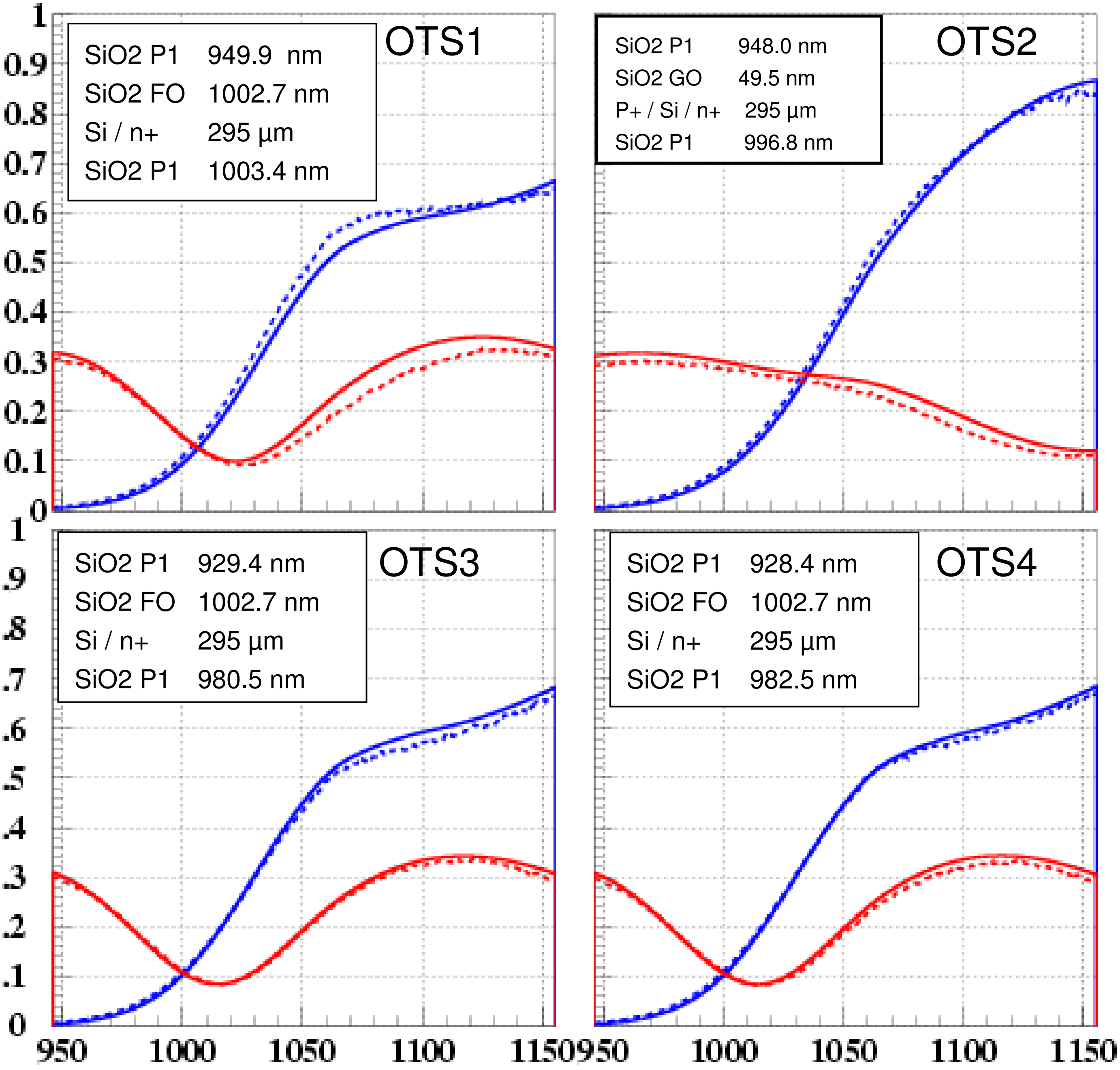
Top and bottom SiO2 passivation thickness measurements





- Aluminum (not shown) also measured
- All materials within requested 5% tolerance thickness

WAFER 1: Measured optical test structures vs simulated



- Test structures simulated (no fit involved)
- n⁺ and p⁺ taken optically identical to Si

Observed differences not due to thickness measurement error (<1 nm)
Not sensible to ~5 µm change in Si thickness.

- **New parametrization** for SiO2 refr. index used !!!

┅ %T meas
━ %T sim
┅ %R meas
━ %R sim

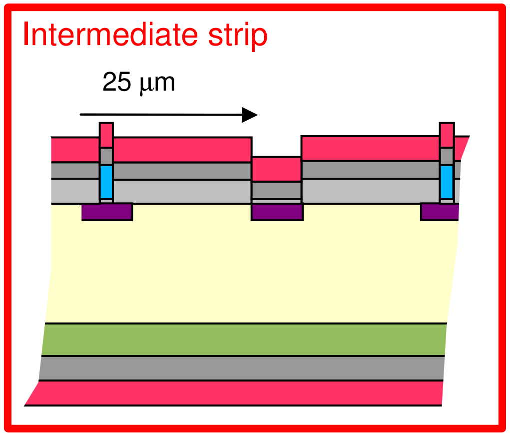
Photometric measurements of transparent microstrip detectors prior to last Si3N4 deposition

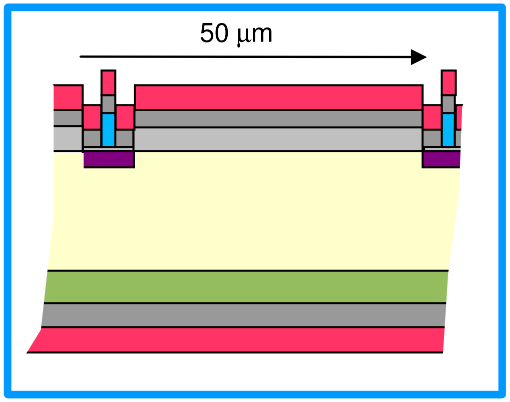
This is a control measurement before completion of sensor

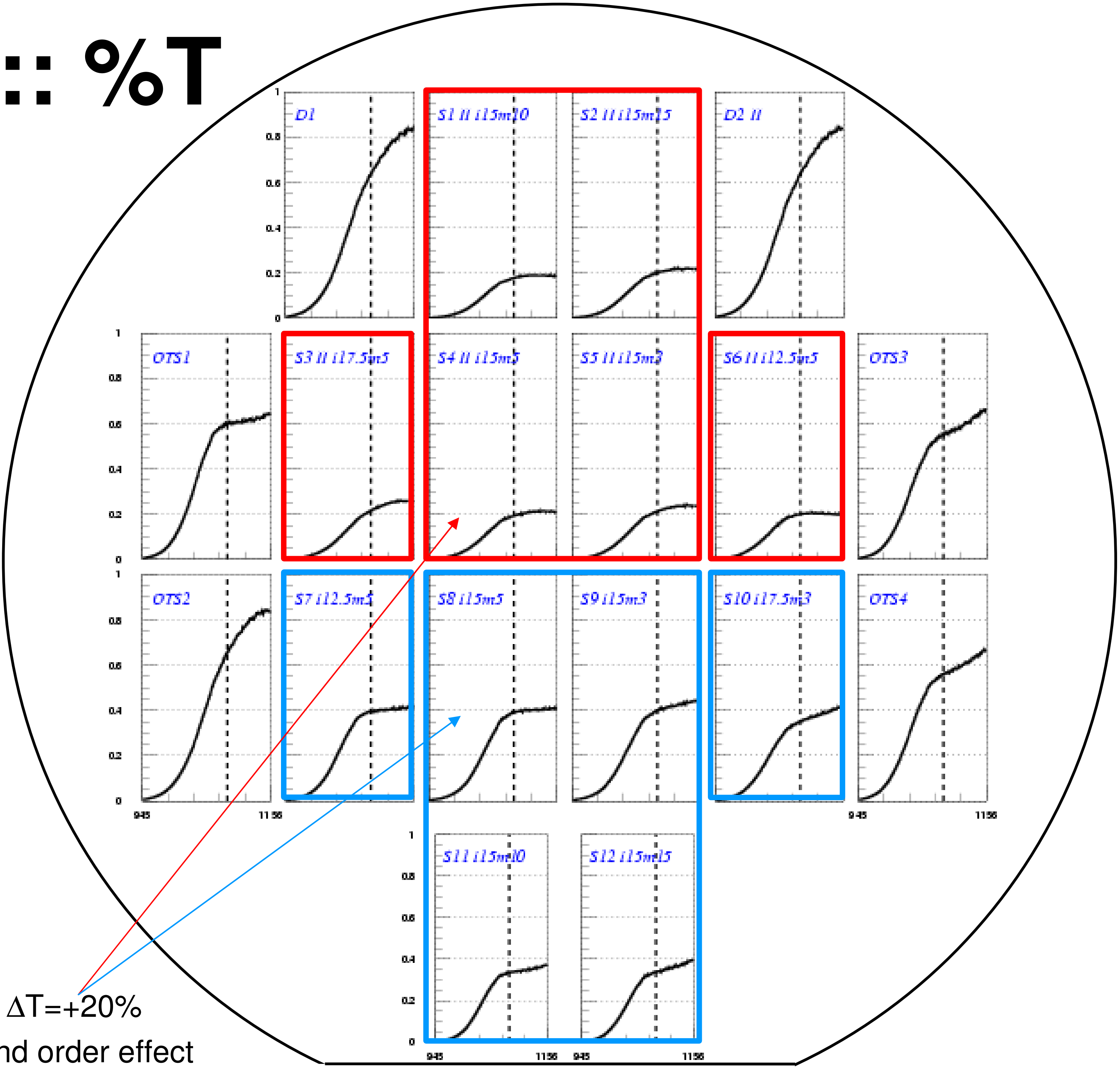
Last passivation layer(s) top and bottom Si3N4 determine overall transmittance

Wafer 1:: %T

measured

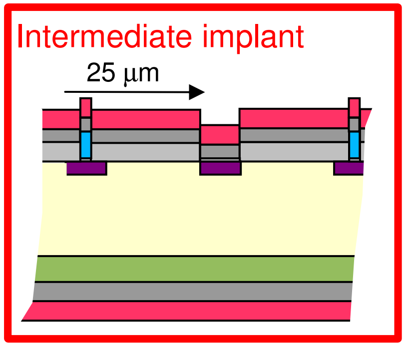


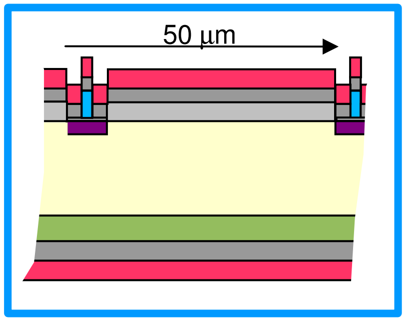


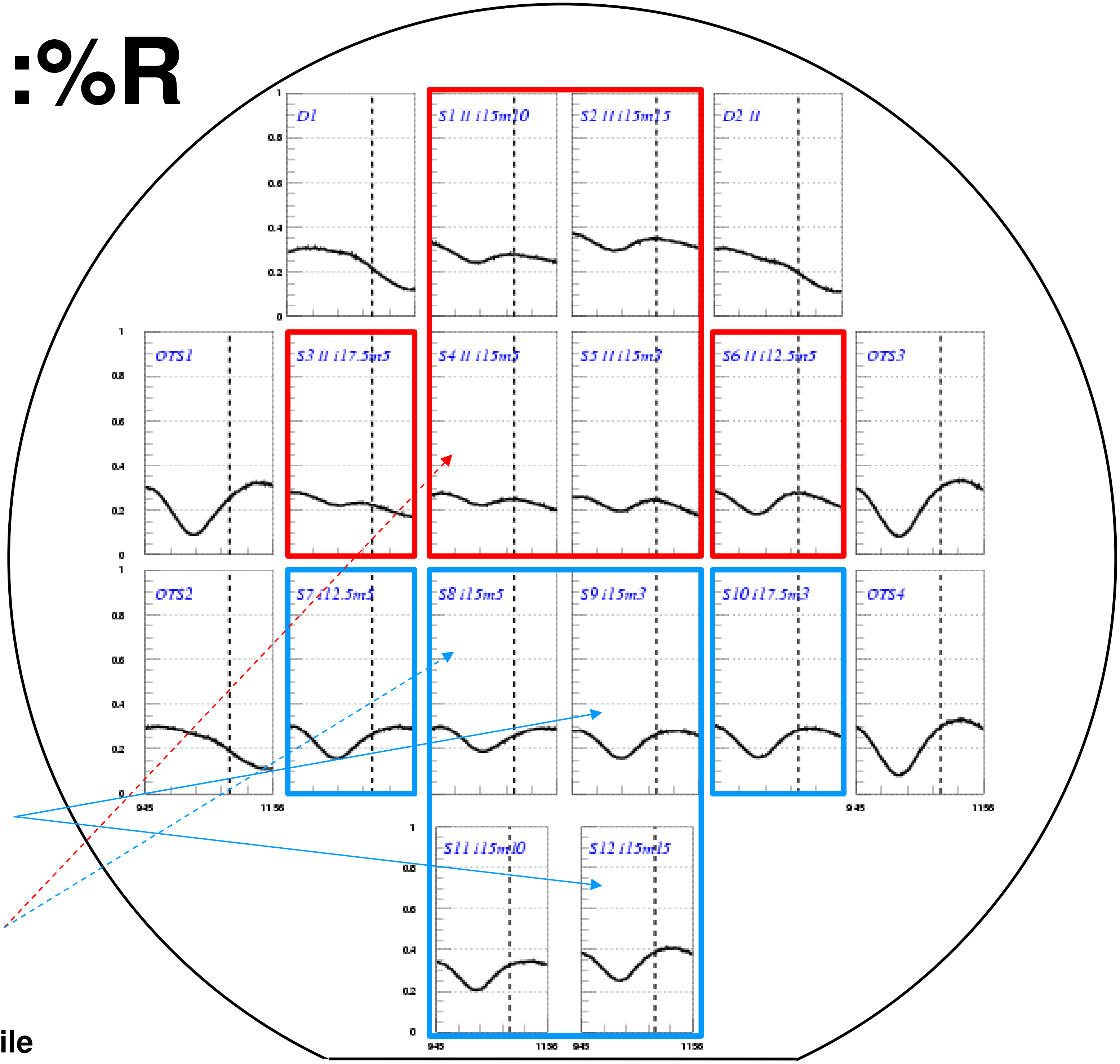


- T~70-80% test structures
- No intermediate implant ⇒ ΔT=+20%
- Metal width [3-5] µm: second order effect
- Metal width >10 µm: ΔT≤-5%

Wafer 1::%R measured







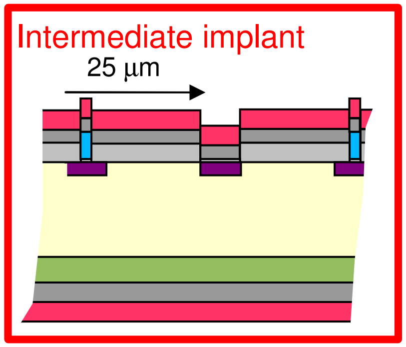
- Metal width has higher influence in reflectance: ΔR=10% between [3-15] µm

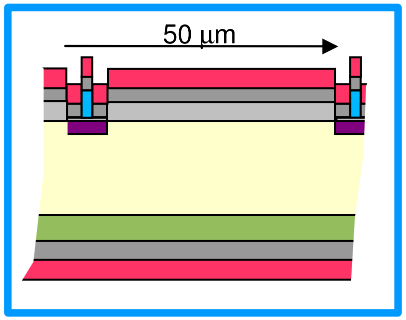
- Removal of intermediate implant does not reduce %R

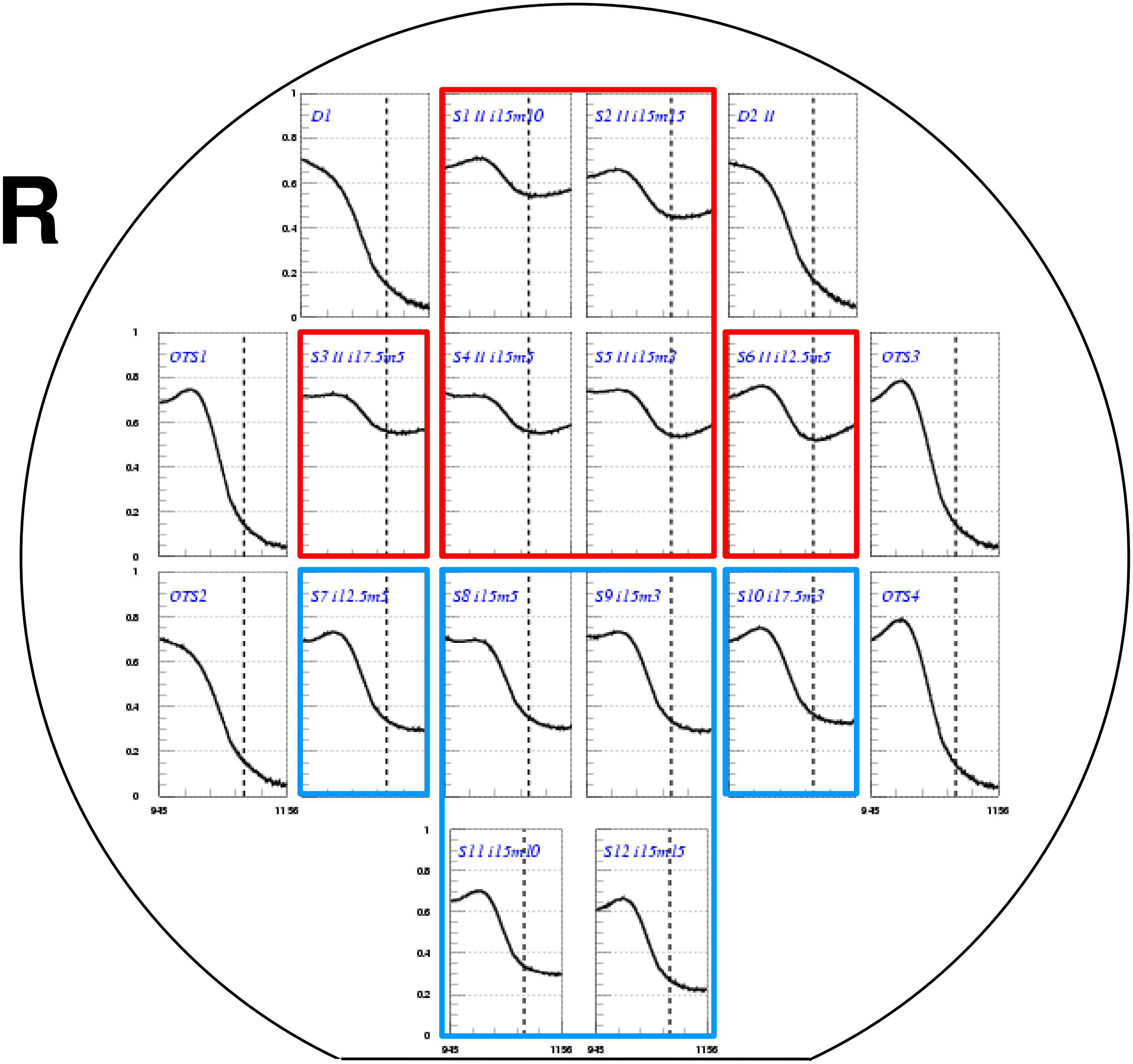
- **%R linked to Al width while %T related to uniformity**

Wafer 1

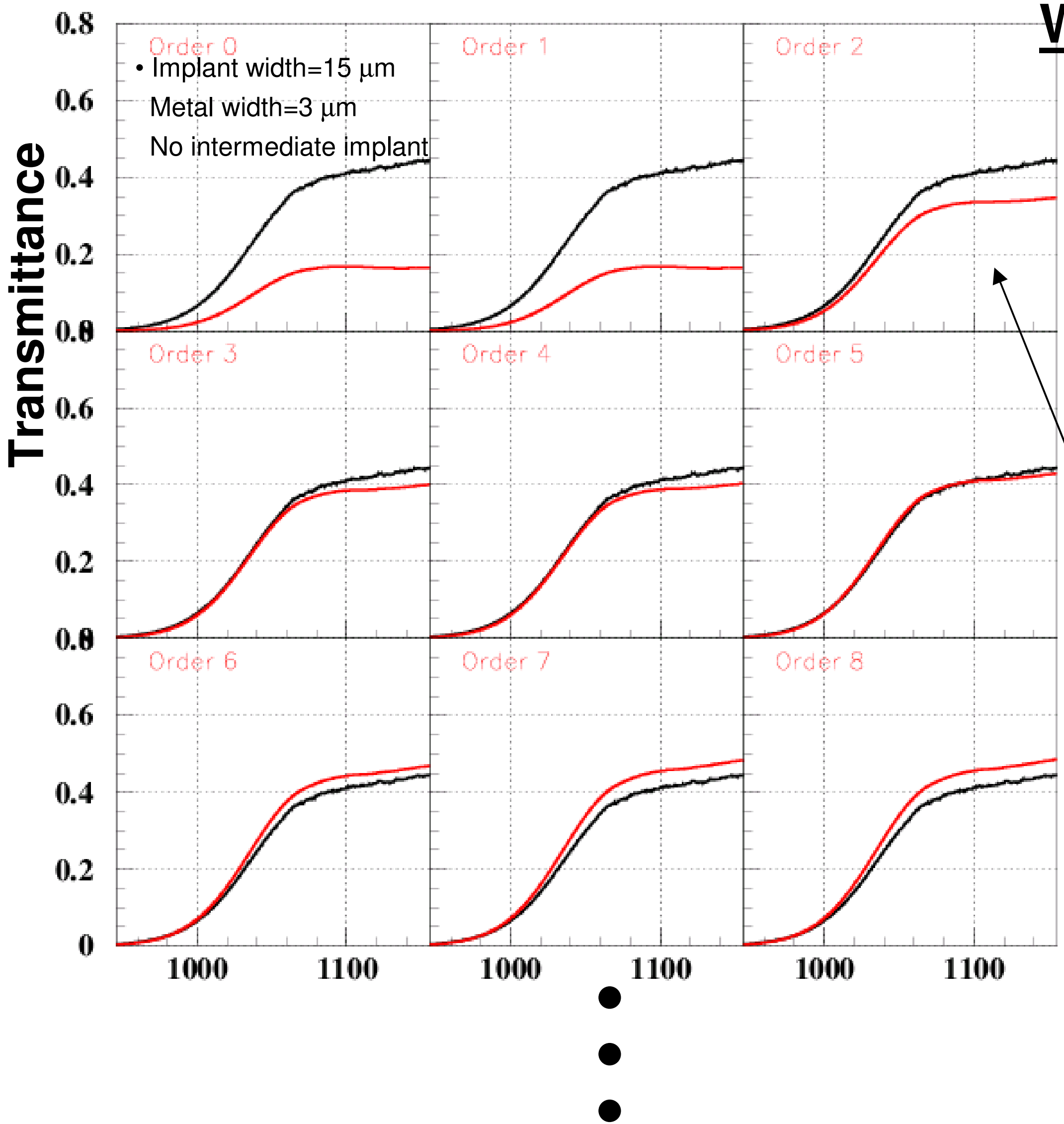
%A=1-T-R


Intermediate implant
25 µm


50 µm

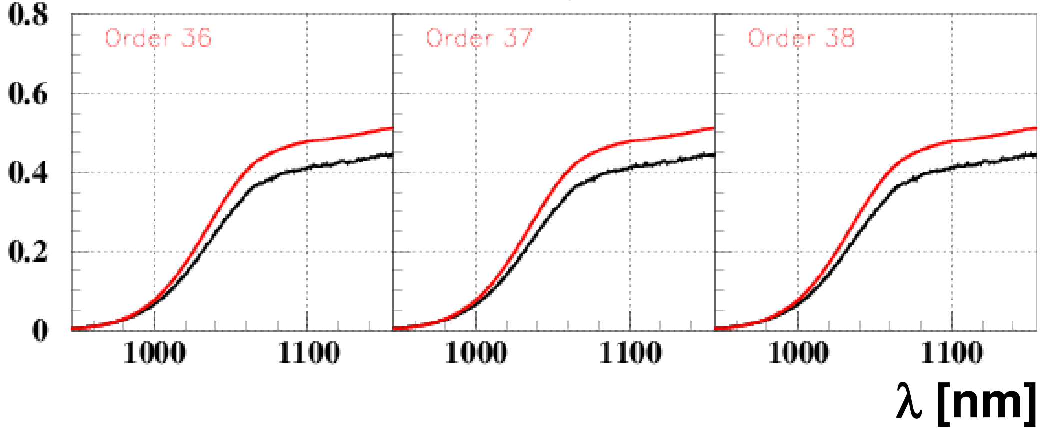

D1
S1 II i15m10
S2 II i15m15
D2 II
OTS1
S3 II i17.5m5
S4 II i15m5
S5 II i15m3
S6 II i12.5m5
OTS3
OTS2
S7 i12.5m5
S8 i15m5
S9 i15m3
S10 i17.5m3
OTS4
S11 i15m10
S12 i15m15
1
0.8
0.6
0.4
0.2
0
945
1156

WAFER 1: Measured sensor vs simulated

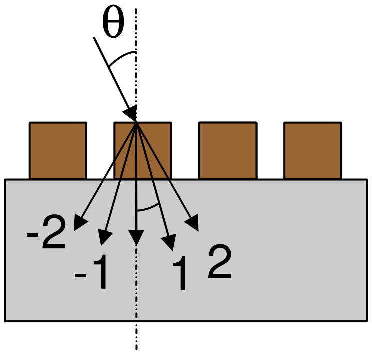

- Implant width=15 µm

Metal width=3 µm

No intermediate implant



- Diffraction orders:



- Plots show cummulative %T distribution up to 38 diffraction orders. For example: T[3]=T[order 0]+T[o=±1]+T[o=±2]+T[o=±3]

- Our calculation overestimates %T. Why? Geometrical acceptance problem. Due to limited size of our optics not all radiation is captured ⇒ Update simulation to account for this effect (work in progress)

▬ %T meas

▬ %R sim

Summary

- IR tracks useful to align selected sensors. Higher %T needed to simplify system

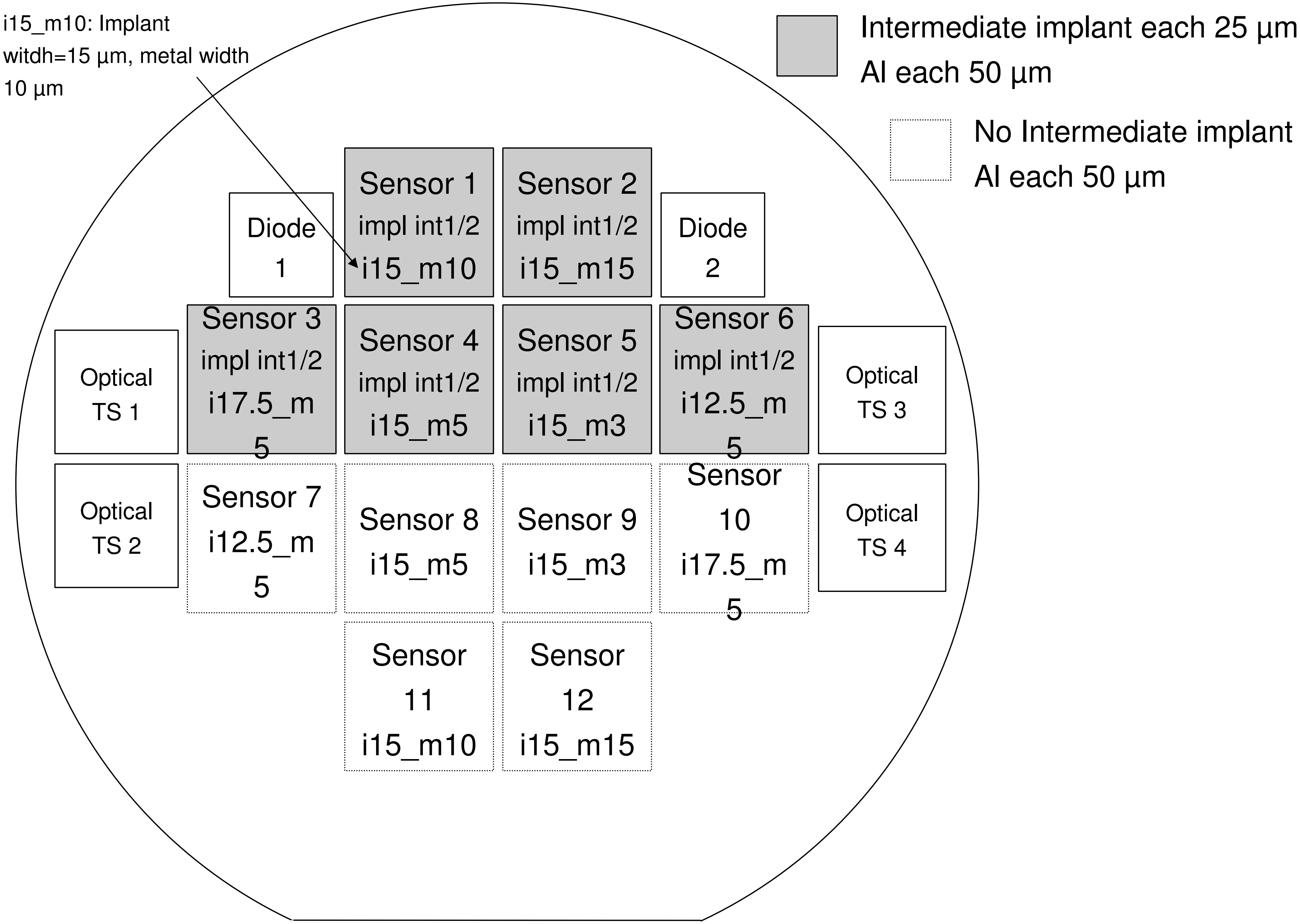
- We are after a simple production process that can be easily implemented by large scale producer
  - Passivation=ARC
  - Layers deposited to 5% thickness tolerance

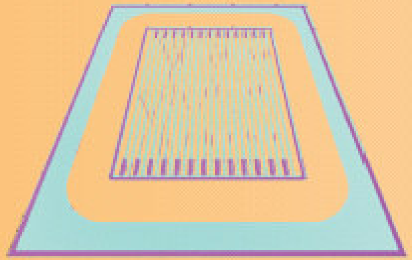
- 5+1 wafers with multigeometry sensors produced. Production stopped (foreseen) for control
  - New SiO2 parametrization was needed

- Deposition tolerance at CNM is remarkable. Better than 5% in almost all layers

- Measurements of %T and %R were done
  - Simulated continuous optical test structures very close to measurements
  - Working on full sensor simulation

BACKUP

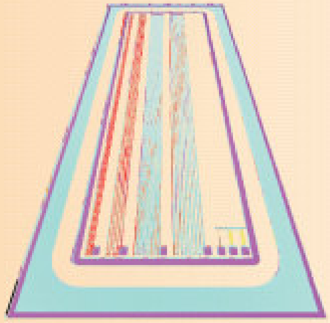

i15_m10: Implant witdh=15 µm, metal width 10 µm
Intermediate implant each 25 µm
Al each 50 µm
No Intermediate implant
Al each 50 µm
Diode 1
Sensor 1 impl int1/2 i15_m10
Sensor 2 impl int1/2 i15_m15
Diode 2
Optical TS 1
Sensor 3 impl int1/2 i17.5_m5
Sensor 4 impl int1/2 i15_m5
Sensor 5 impl int1/2 i15_m3
Sensor 6 impl int1/2 i12.5_m5
Optical TS 3
Optical TS 2
Sensor 7 i12.5_m5
Sensor 8 i15_m5
Sensor 9 i15_m3
Sensor 10 i17.5_m5
Optical TS 4
Sensor 11 i15_m10
Sensor 12 i15_m15



TS-Cap

TS-Cap connects 26 p+ implanted strips to a bias ring. Each implant is separated by a dielectric structure from a layer of polysilicon which is connected to the aluminum readout strip above.
We measure the electric strength and the capacitance of the thin readout dielectric.

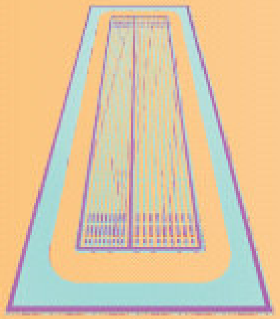
Measured parameters
C_{ac} : Coupling Capacitance
IV_{diel}: Dielectric Breakdown



Sheet

Seven superficial meander-like strips of different widths and materials. From left to right: p+ (red) with 10 µm and 20 µm width, aluminum (blue) with 12 µm and 22 µm width, polysilicon (yellow) with 6 µm width, 2x meander-like polysilicon with 5 µm width .

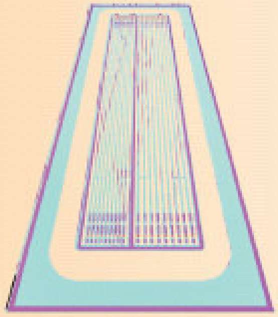
Measured parameters
ρ_{p+}, ρ_{alu} : p+ and Aluminum Resistivity



Cap-TS-AC

2 sets of 9 detector like strips with a pitch of 80 µm (left) and 120 µm (right). The 3 outermost strips on each side of the two sets are shorted. The capacity between the centermost strip and its two neighbours is measured.

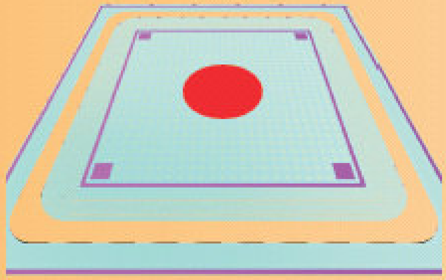
Measured parameters
C_{int} : Interstrip Capacity



Cap-TS-DC

A similar structure as Cap-TS-AC, but the strips are not connected to the bias ring while each p+ strip is directly connected to its aluminum readout strip and polysilicon in between. The resistance of the silicon oxide between the centermost strip and its two neighbours is measured.

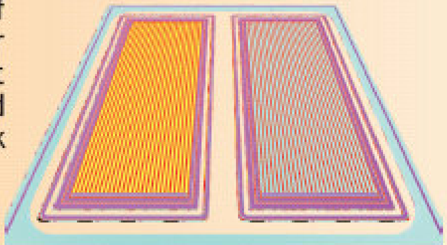
Measured parameters
R_{int} : Interstrip Resistance



Diode

A large diode with a multiguard structure around it. The large hole in the centre of the aluminum enables irradiation with laser or particles from a radiation source (not used). We can calculate the resistivity and the carrier concentration in the silicon bulk from measurements on this structure.

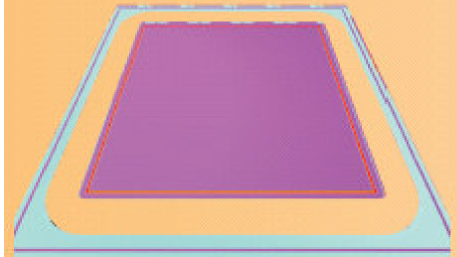
Measured parameters
IV_{diode} : Dark Current
V_{depl} : Full Depletion Voltage



GCD

The Gate Control Diode consists of two comb-like structures: A diode intertwined with a MOS structure made of polysilicon (left) or aluminum (right). The materials are separated by a thick dielectric (SiO_2).
We can assess the quality of the thick gate oxide and its interface to the silicon bulk.

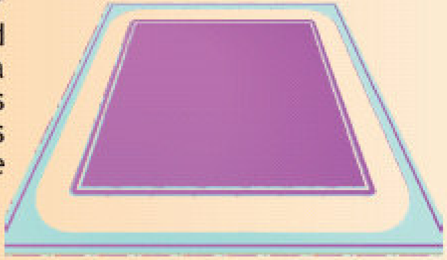
Measured parameters
I_{surf} : Surface Current
V_{fb} : Flatband Voltage



MOS1

The first Metal Oxide Semiconductor structure is a capacitor with p+ implant and polysilicon as electrodes separated by a dielectric. The polysilicon electrode is coupled to the aluminum layer which serves as contact pad. The dielectric between the electrodes is formed with the thin oxide.

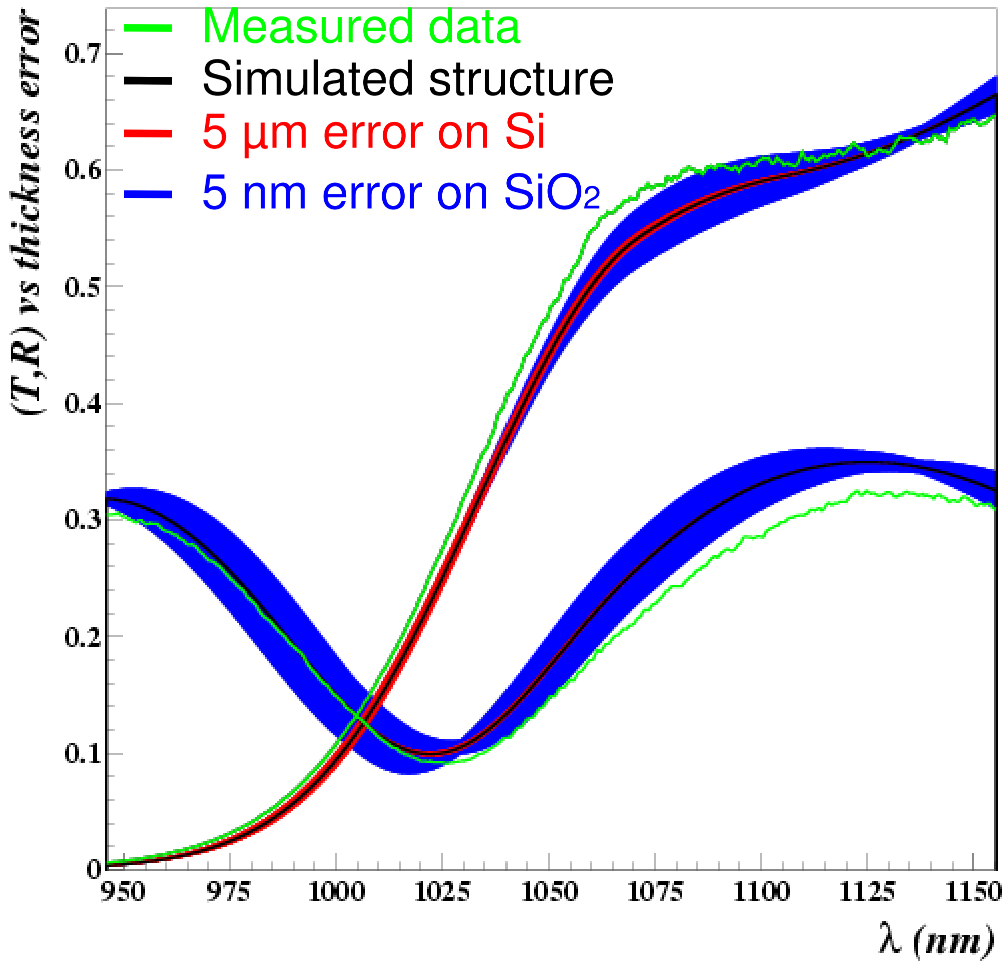
Measured parameters
C_{MOS1}: MOS1 Capacity



MOS2

The second Metal Oxide Semiconductor structure consists of a thick layer of oxide above the silicon bulk and an aluminum electrode on top.
We can assess the quality of the thick oxide by measuring the flatband voltage .

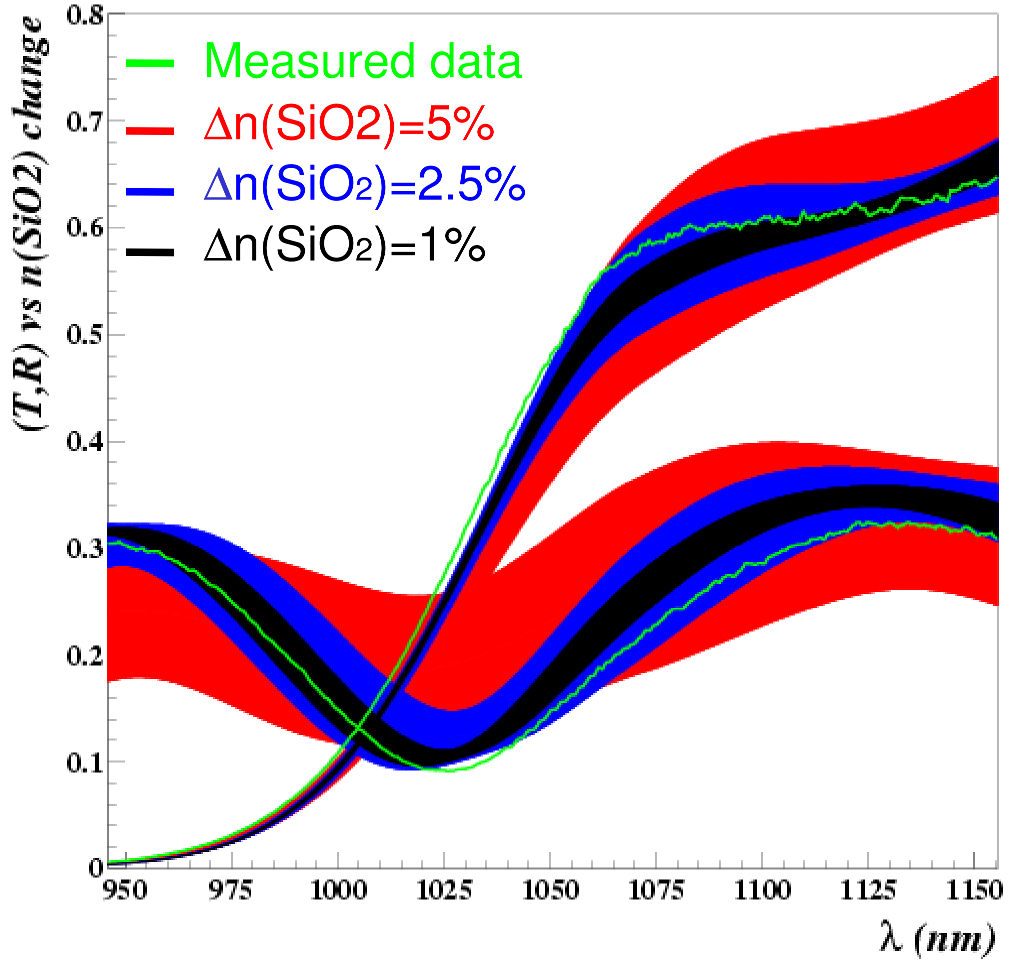
Measured parameters
V_{fb} : Flatband Voltage
C_{ox} : Oxide Capacity



Can observed difference be due to thickness measurement error?

No (as long as measurement error < 5 nm)

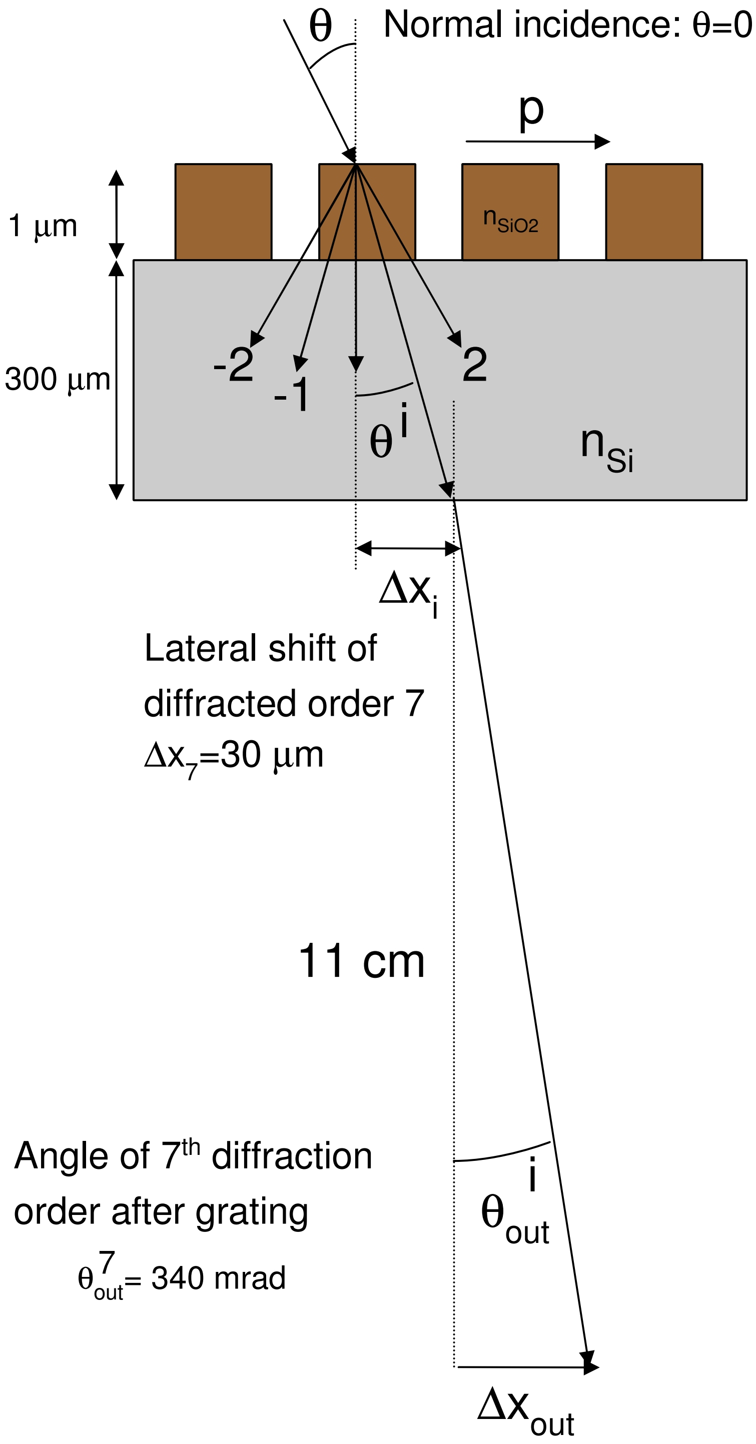
Observed that 5 nm error on SiO2 influences much more than 5 µm error on Si



Can observed difference be due to refraction index scaling?

Maybe...

(if we allow n(SiO_2) change of 2.5%)



Normal incidence: $\theta=0$

Propagation angle of diffraction order i: θ_i

$$\sin\theta_i = \sin\theta + i\,\lambda/(n_{SiO2}p)$$

Lateral shift of diffracted order 7

$\Delta x_7 = 30\ \mu m$

Angle of 7th diffraction order after grating

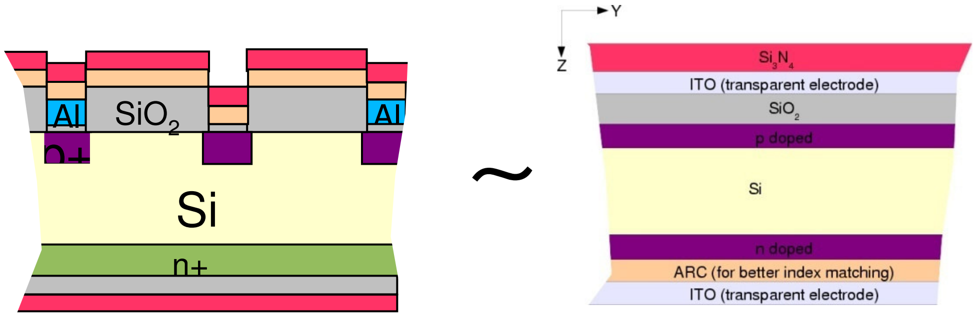
$\theta^7_{out} = 340$ mrad

Lateral shift of diffracted order 7 in measurement plane: $\Delta x_{out} = 4$ mm !!

Notes:

- First diffraction order falls 5.3 mm away from normal
- We have a 1.5 mm diameter pinhole at the measurement plane

Simulation of planeparallel structures



- **Simple simulation**: **multiple reflections** ⇒ interferences ⇒ Calculation of (T,R)

  — Refraction index either tabulated or modeled using dispersion relations

  $$n(\lambda),k(\lambda),d_i \Rightarrow \mathbf{T_{calc}}, \ \mathbf{R_{calc}} = f[\, n(\lambda),k(\lambda),d_i \,]$$

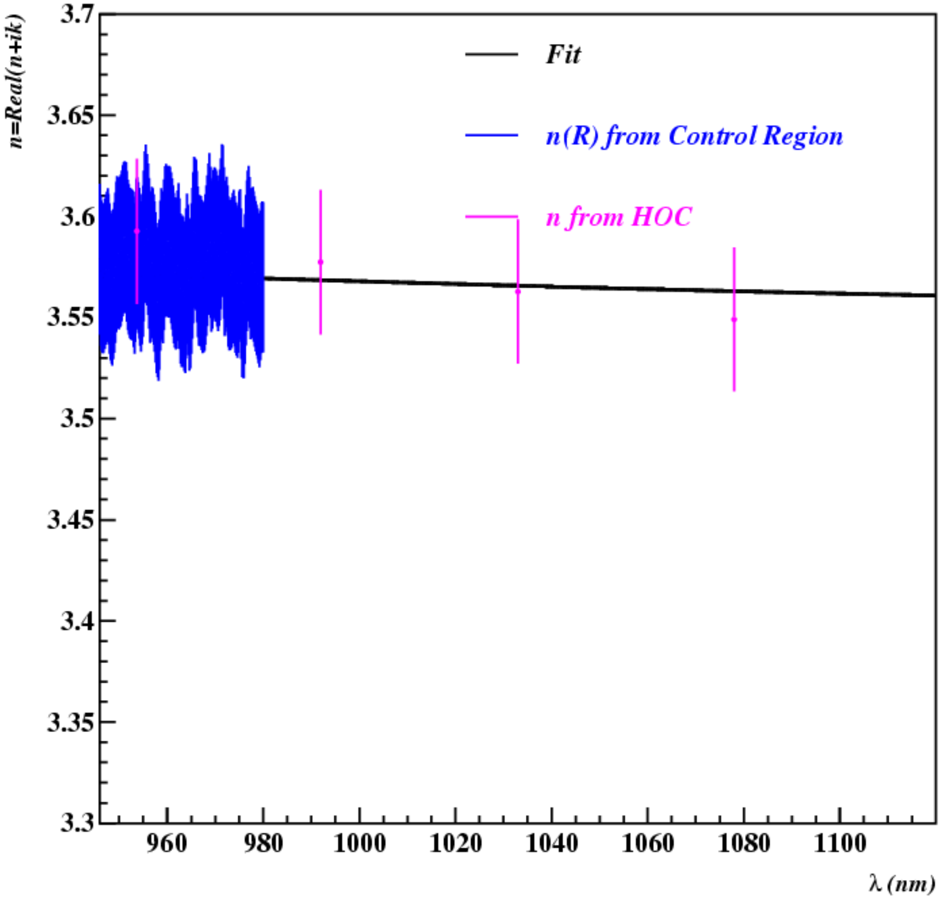
  (i=1...Number of layers)

  — Or solve the **inverse problem**:

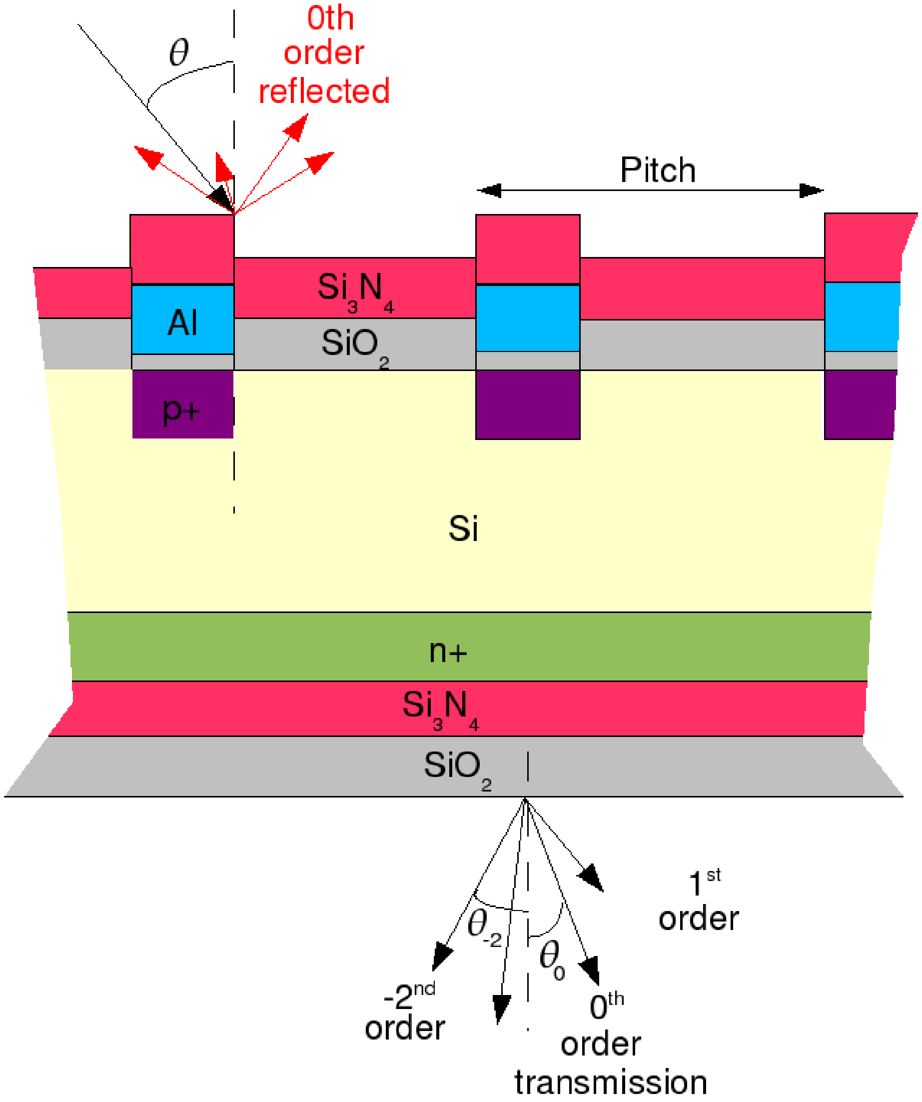
  $$\mathbf{T_{meas}}, \ \mathbf{R_{meas}} = f[\, n(\lambda),k(\lambda),d_i \,] \Rightarrow n(\lambda),k(\lambda),d_i$$

  using non-linear least squares fit

- **Inverse method** used to characterize material <u>samples from CNM</u>



Full optical simulation



- Microstrip layer is not continuous.

- Interferences alone do not describe measured spectra. Needed to account for **diffraction**

- Fresnel and Fraunhoffer approximations for diffraction not applicable here, because some layers are transparent..

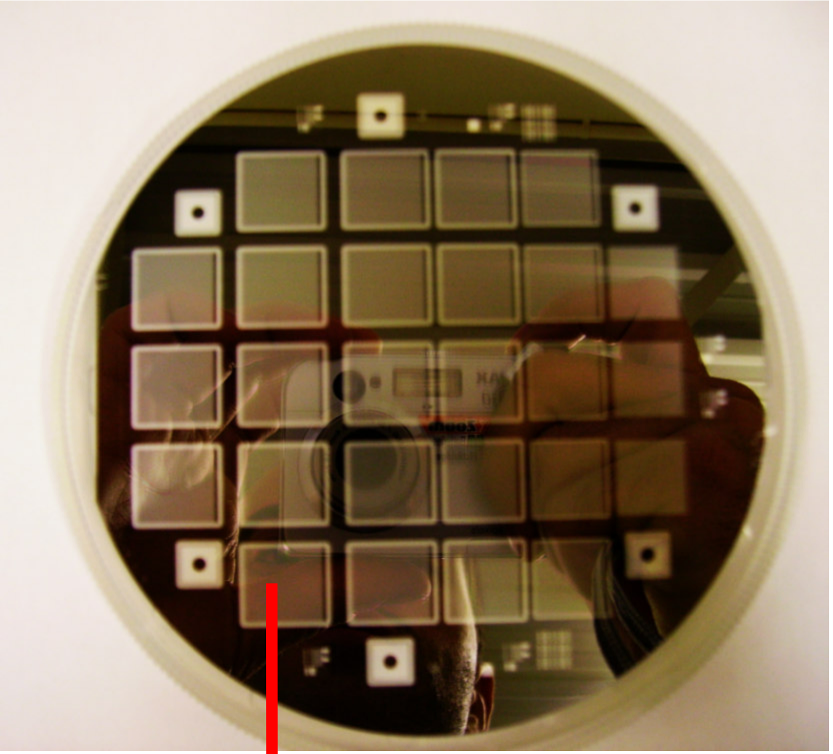
Then:

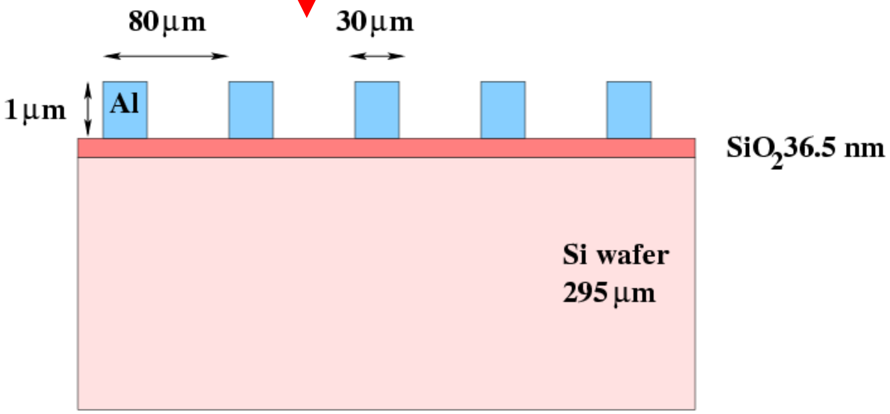
- Solve **Maxwell** equations **rigorously**

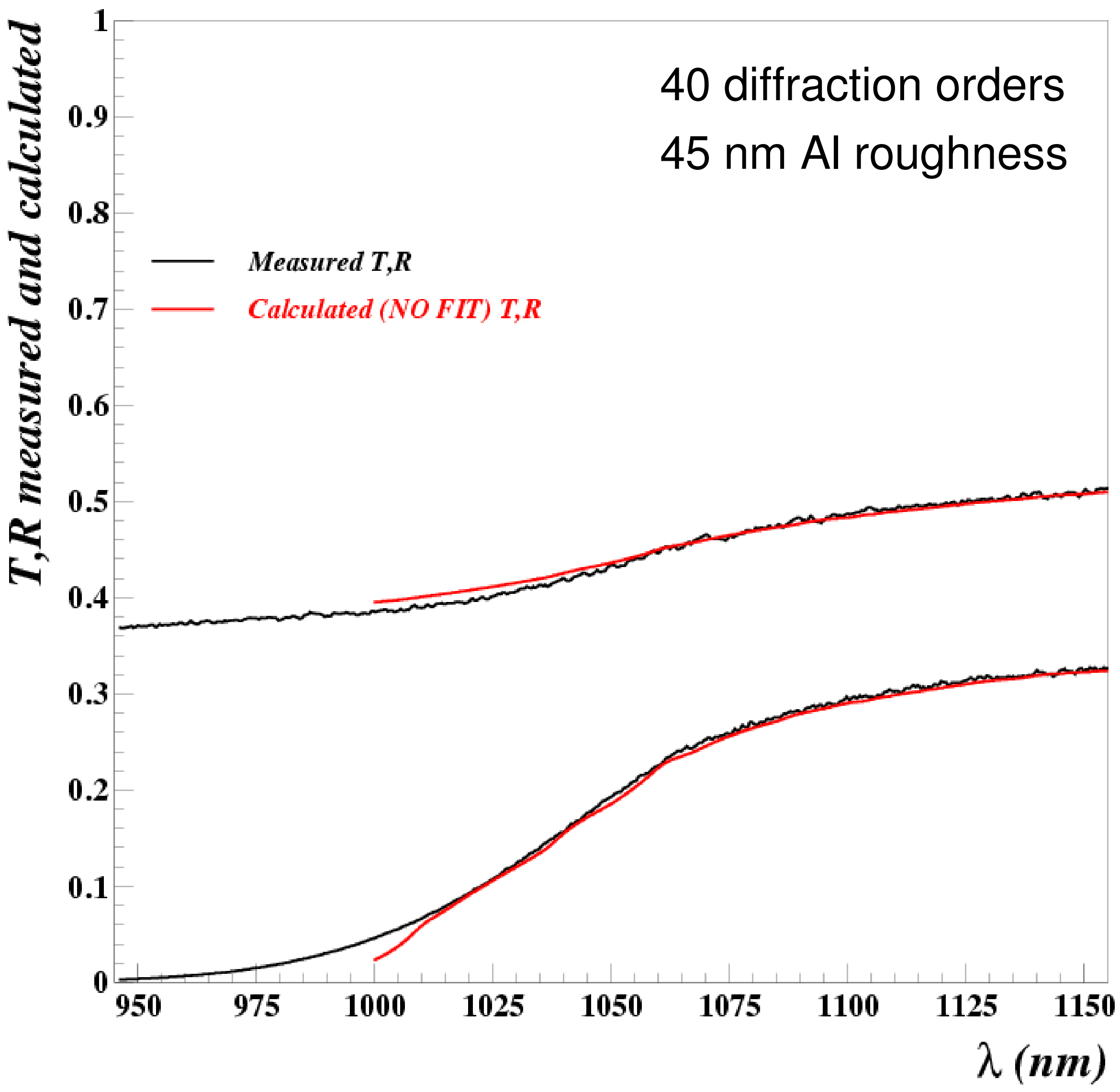
- Using **RCWA method** (see EUDET-memo-2008-37):
  - — Fields expressed as Fourier expansions
  - — RODIS software for diffraction efficiency at any order.

Measurement of CNM diffraction sample

- CNM produced a simple wafer to test the simulation, using GICSERV07 access.







Optimization constraints

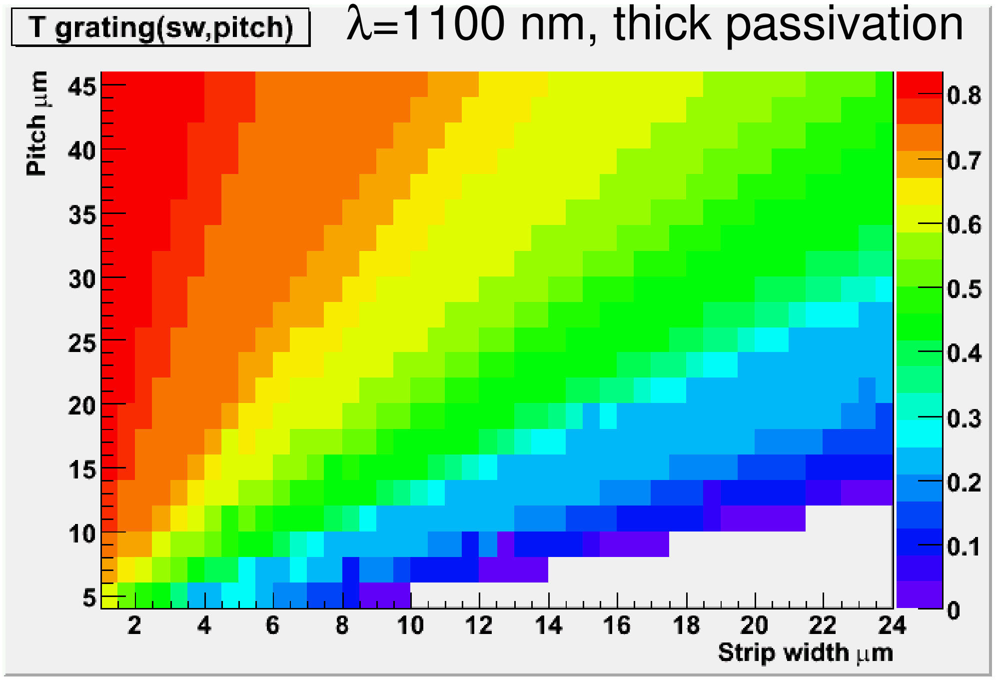
- Study done at **2** different **wavelengths**:

  1) Readily available IR laser wavelength **λ=1085 nm**

  2) longer (exotic) wavelength **λ=1100 nm** (higher transmittance of Si).

- Fixed readout **pitch** (SiLC baseline+Beetle chip) is **50 µm**. One intermediate strip

  What is the best strip width?



— For fixed pitch:

Wider electrode width ⇒ smaller %T

— Bigger pitch ⇒ higher %T

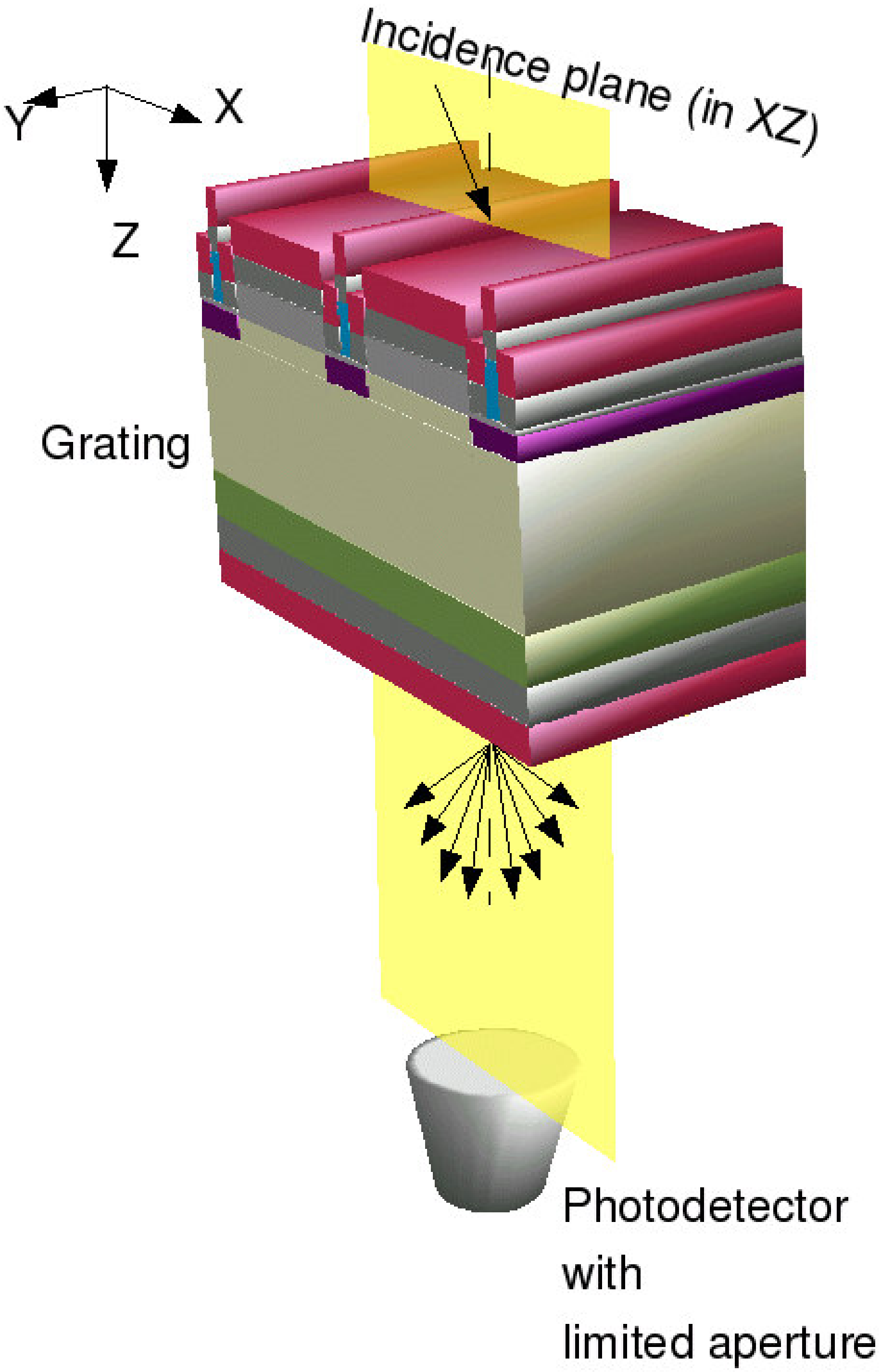
— **We will produce sensors of different strip widths** to test it

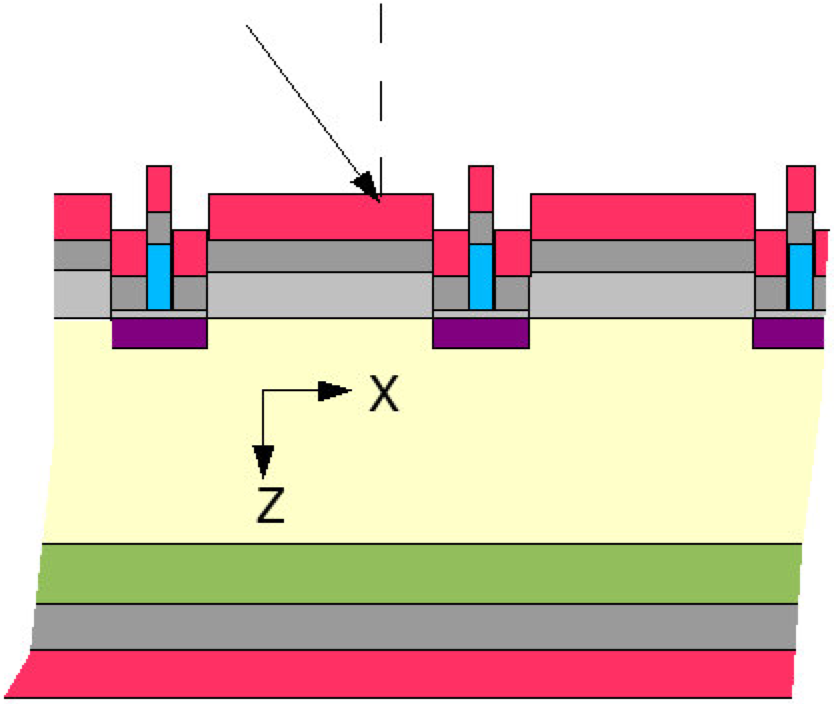
- Field oxide is a key parameter for CNM:

Field Oxide thickness= 1 µm

Al thickness= 950 nm

- **Repeatability** on the deposited thickness of a material **is a percentage of its thickness**. So the thicker the material is, the worse accuracy on thickness achieved


Incidence plane (in XZ)
Y
X
Z
Grating
Photodetector
with
limited aperture


X
Z