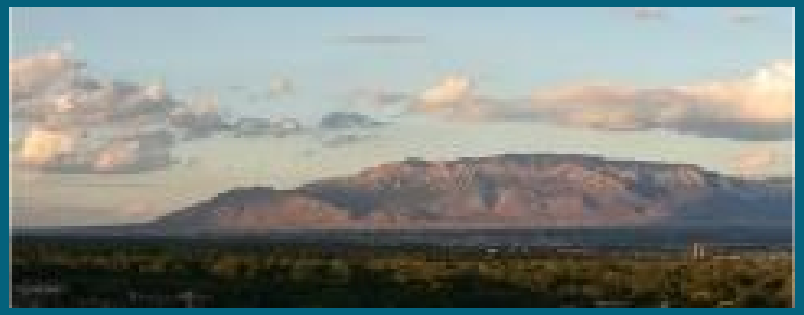
Latest from the SiLC R&D Collaboration: achievements & perspectives

Bruce Schumm (UCSC-SCIPP) & Aurore Savoy-Navarro (LPNHE-UPMC/CNRS)
On behalf of the SiLC R&D collaboration



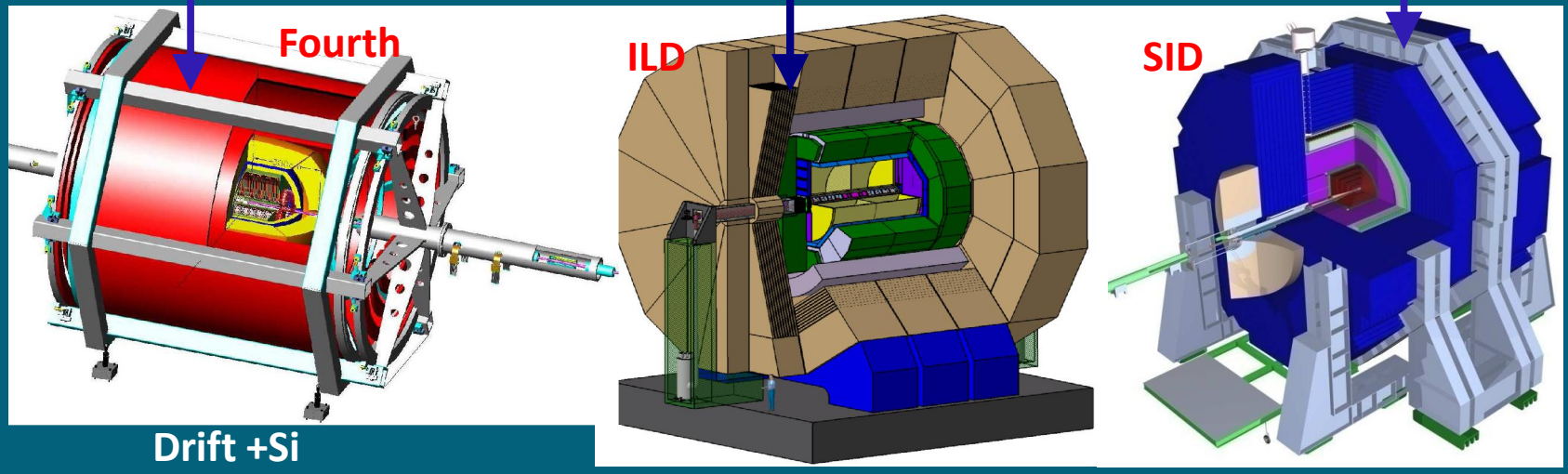
2009 Linear Collider Workshop of the Americas
September 29-October 3 2009
Albuquerque, New Mexico

Outline

The work & results reported here are those obtained since last year, by the ongoing R&D activities of the SiLC R&D Collaboration. The aim of this generic R&D collaboration is to develop the next generation of large area semi -conductor trackers for the Future Linear Collider (LC).

- The SiLC R&D collaboration present status
- The basic R&D activities and current status on:
  - sensors
  - associated FEE
  - related mechanical issues
- Applications to LC tracking concepts and Integration issues
- Synergies and perspectives in the after LOI period.

SiLC (Silicon tracking for Linear Collider)



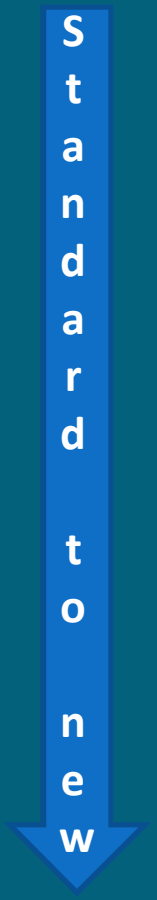
3 LOIs have been submitted March 09 & 2 tracking strategies: Hybrid versus All Si.

Generic & horizontal R&D *Collaboration applied to the 2 tracking concepts*
Goal: *To develop the next generation of large area Silicon trackers*
Strong synergy *with the construction of* ***LHC Si trackers & their upgrades***
Opening since last year to the ***CLIC case*** ***(see later)***.

SiLC*: U. Michigan, U. of Barcelona, UMB-CNM/CSIC, U. Helsinki & VTT, Karlsruhe U., Moscow St. U., Obninsk St. U., LPNHE-UPMC/CNRS-IN2P3,Charles U. Prague, SCIPP&UC Santa Cruz, IFCA-CSIC & U. Cantabria, U. S. Compostela, Seoul Nat U., Korea U., Yonsei U., SKKU-Seoul, Kyunpook Nat. U., INFN Torino & Torino U., IRST-Trento U., IFIC-CSIC, HEPHY-Vienna, HPK-Japan.*

The R&D on sensors: the roadmap

- The microstrip sensors
  - => Standard planar strips
  - => Alignment-friendly strips
  - => Edgeless planar strips
- 3D technology based sensors
  - => SOI Edgeless strip sensors
  - => 3D short strips
  - => 3D pixels



The sensor baseline: strip sensors

In 2007 SiLC launched an effort on new single sided strip sensors:

GOALS = get the industrial firms to produce:

- **Larger wafer (6''to 8''), thinner 200 µm, smaller pitch (50µm)**
- **decreased non-active edge (from a few hundreds down to 10-20 µm)**
- **direct connection of FEE onto the strip sensor (see later).**

AND:

Because of gained expertise for LHC (HEPHY in CMS):

Test structures included for detailed characterization and further studies (many different options added this way for testing improved features)

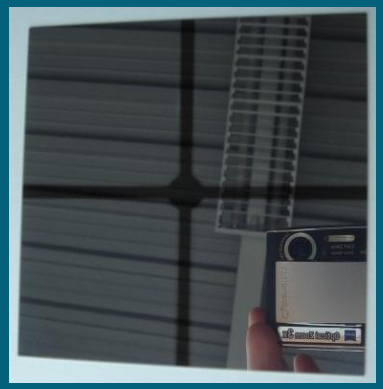
AND:

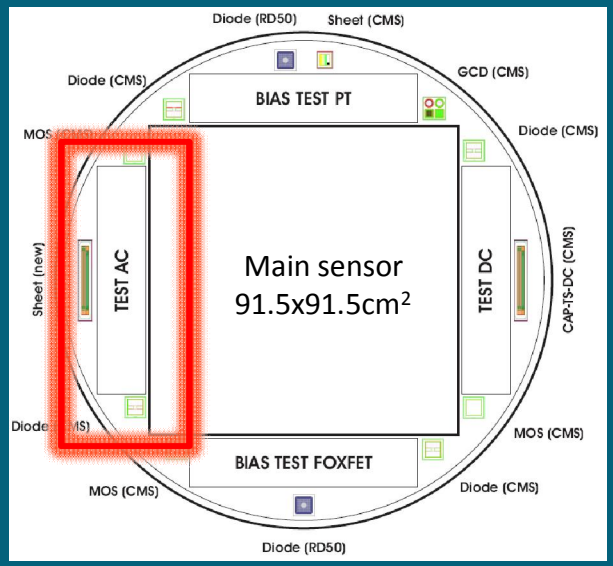
Alignment special treatment for some of them

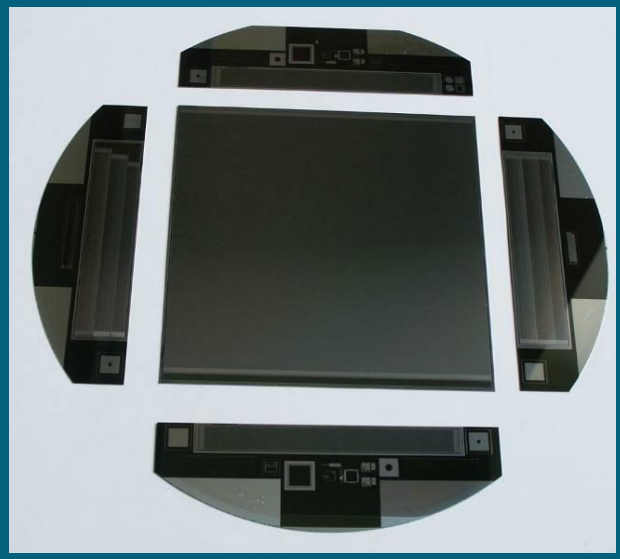
SiLC Sensor order to HPK (end 2007)

SiLC Collaboration ordered at Hamamatsu (HPK):

- 30 pieces single-sided 6” wafer
- 5 pieces. alignment sensors of same layout, but hole for laser in backplane metallization





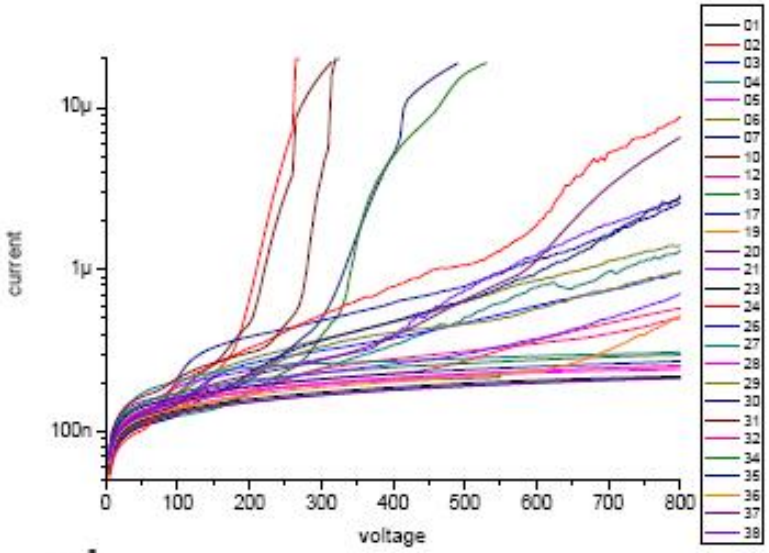


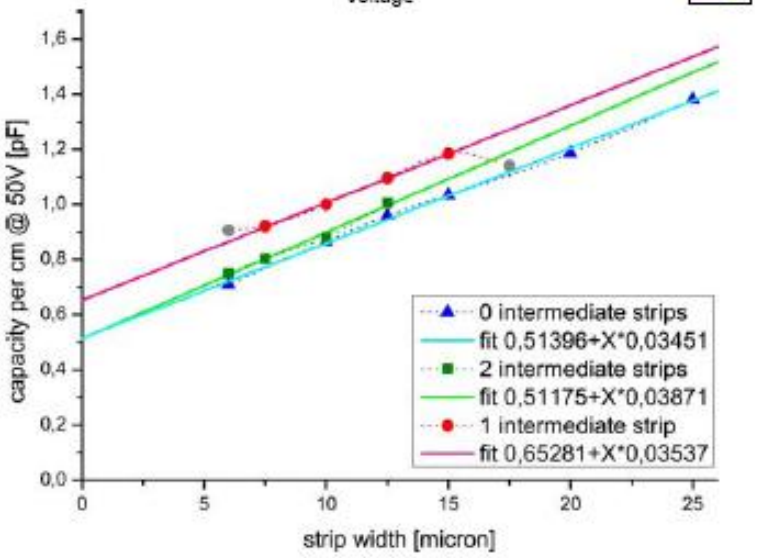
Specifications:

- Wafer thickness : 320 μm
- Depletion voltage around 75V
- 1792 AC-coupled strips, individually biased via poly-Si resistor (20MOhm)
- Strip pitch: 50 μm pitch,
- Strip width: 12.5μm
- No intermediate strips
- Additional test structures around the wafer

HPK strip sensors electrical characterization

- sensors have been intensively tested in Vienna
  - IV curves on all sensors
  - CV curves to determine full depletion voltages (approx 50-65V)
- measurement of the inter-strip capacitance reveal different values for each zone:
  - capacitance scales linearly with strip width
  - different offset for region with one or two intermediate strips

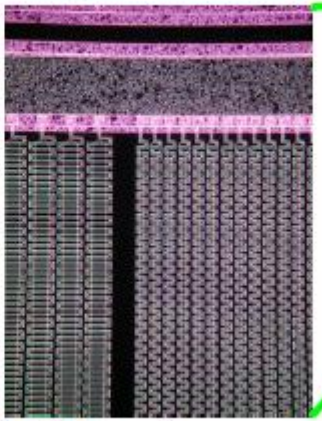




THE HPK STRIPS TEST STRUCTURES (HEPHY)

Mini Sensor Layout

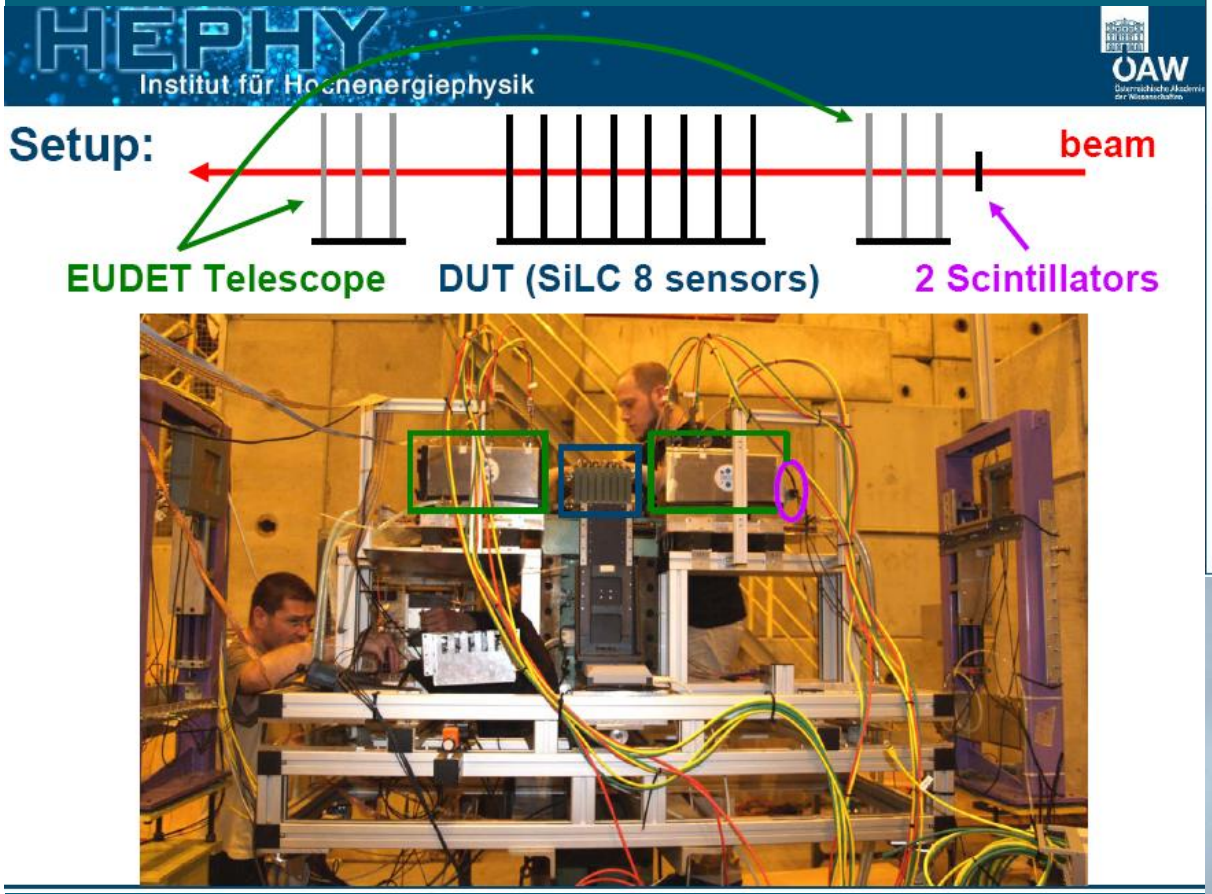
- produced by HPK Japan
- single-sided AC coupled strips
- thickness: ~ 320 µm
- active area: ~ 15 x 64 mm²
- depletion voltage around 65 V
- number of strips: 256
- biasing scheme: poly-Si resistor (20MOhm)
- readout pitch: 50 µm
  - 3 different regions with no, one or two intermediate strips
  - In total 16 zones **(separated by missing strip):**
    - **consisting of 16 strips each**
    - **different strip widths in each zone**

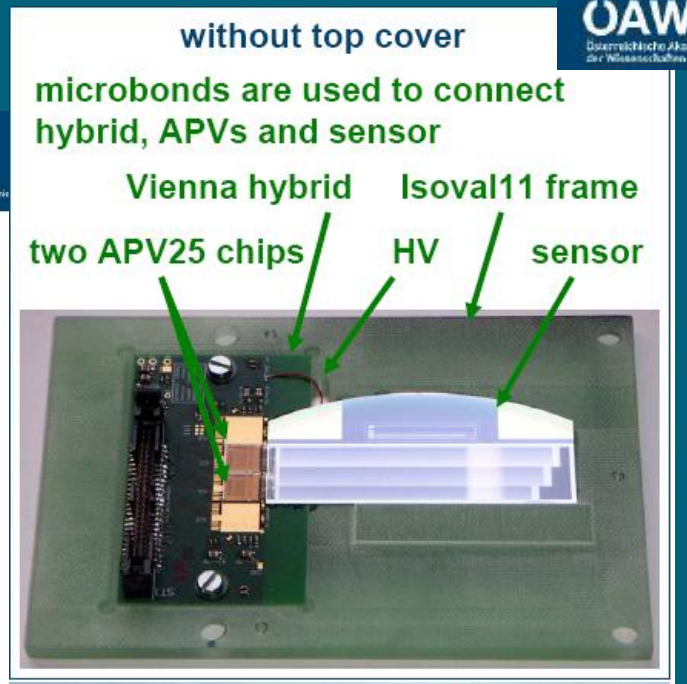


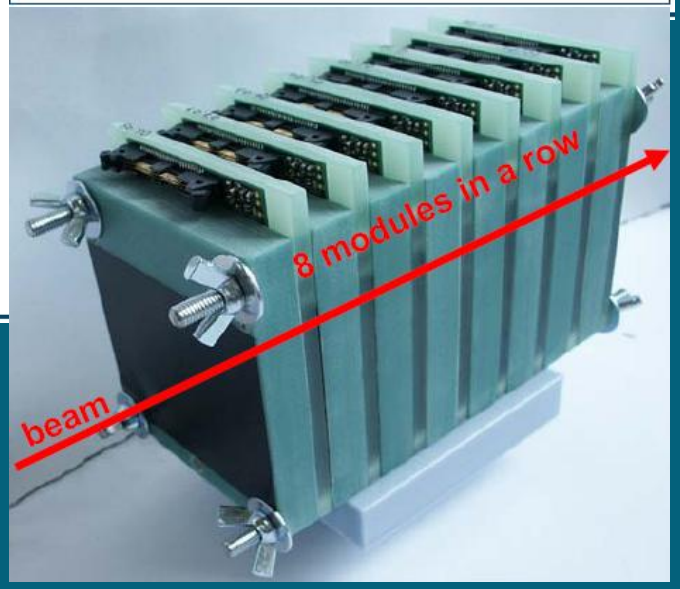
zone	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
strip width [µm]	6	10	12,5	15	20	25	6	7,5	10	12,5	15	17,5	6	7,5	10	12,5
# int. strips	0	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2

Test beam on HPK test structures

See W. Mitaroff's talk)





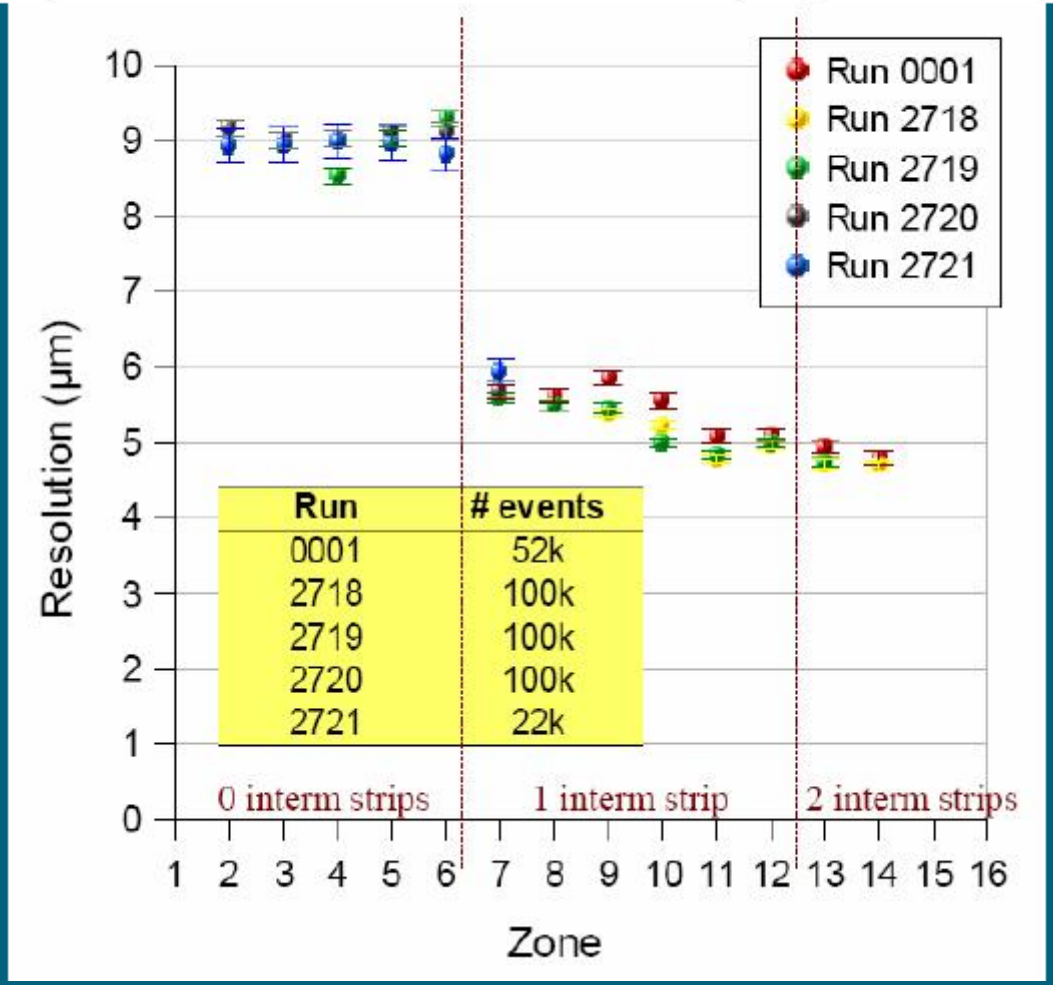


Performed on H6B SPS-CERN in June2008.
New series of test beam in the same test beam line August 15-31, 2009 (see W. Mitarof's talk)

2008 test beam on test structures: results

CU Prague

Spatial resolution vs strip geometry



Run	# events
0001	52k
2718	100k
2719	100k
2720	100k
2721	22k

TESTAC:

strip width [μm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

Interesting result:

9μm resolution if no intermediate strip

5 or 6μm resolution if 1 or 2 intermediate strip

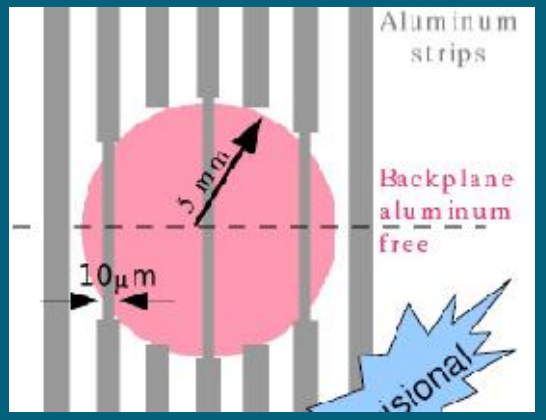
HPK strip sensors for alignment

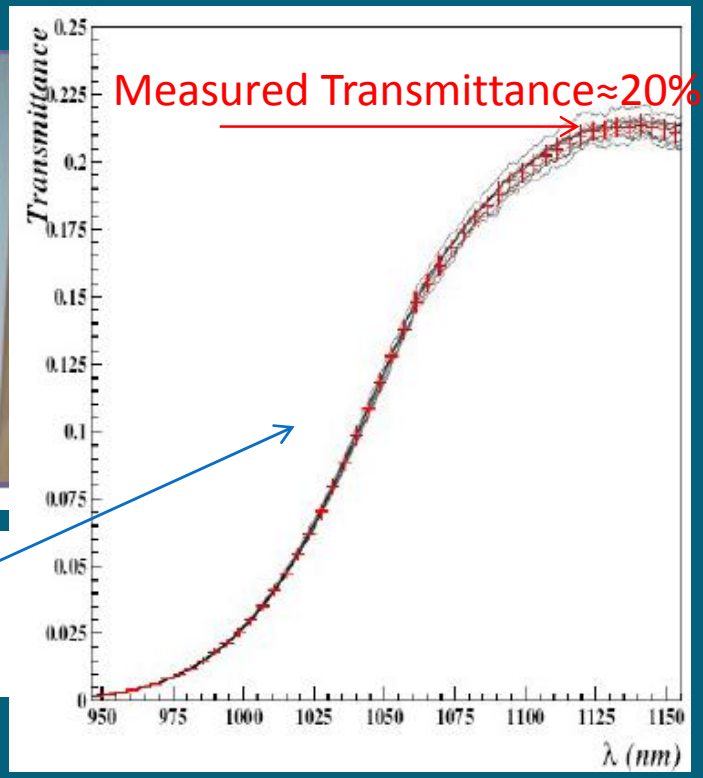
Implemented:

- ∅~10 mm window where Al back-metalization has been removed

Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)

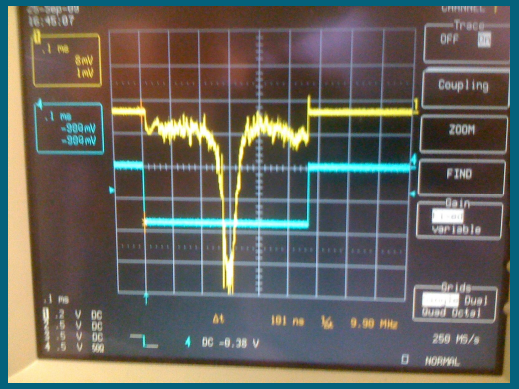




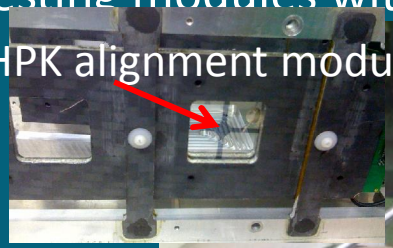
- They are alignment friendly, but not optimized for transmittance: no Anti-Reflection Coating (ARC).

Alignment test set ups (here with HPK equipped modules)

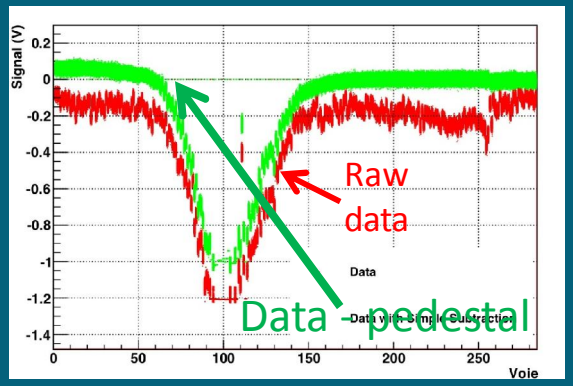
HPK alignment friendly (AF) sensors characterized at HEPHY test bench and test at SPS beam (Aug'09). Set up (LPNHE) for testing modules with any A.F. Sensors with laser or beamtest.

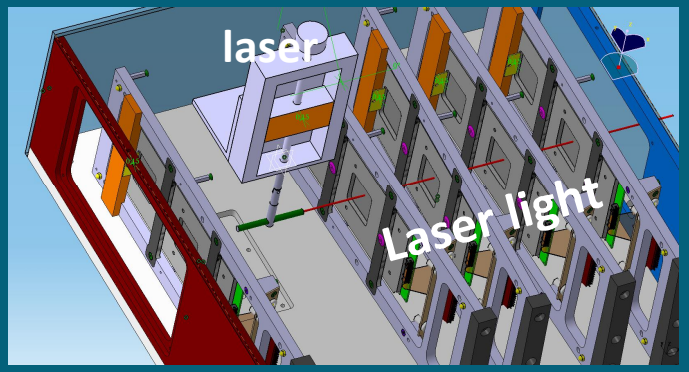


HPK alignment module



Laser response of the A.F. Equipped modules: reconstructed from data (bottom) ; oscilloscope (top)





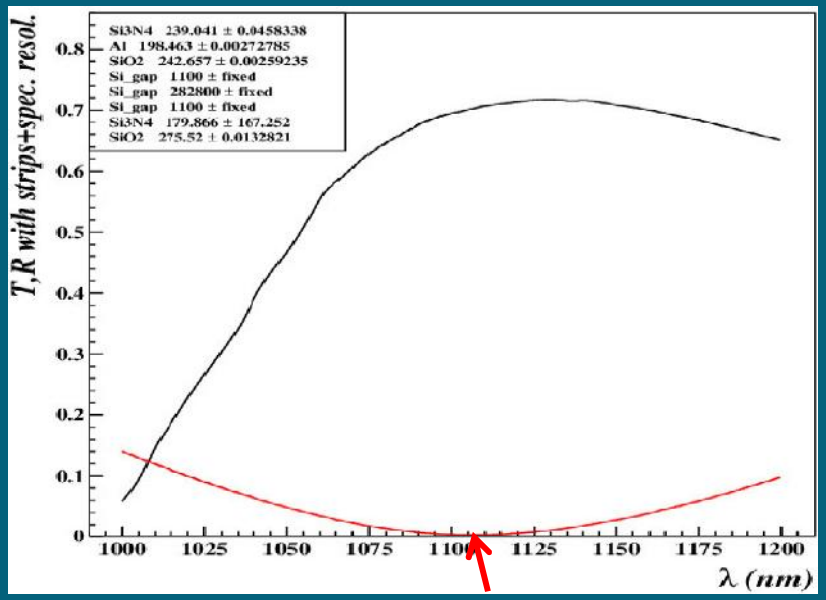
Standalone test system: Faraday cage with 3 modules equipped with 2 HPK A.F+2 standard HPK modules for test at beam or Lab.

R&D on new IR transparent detectors

Goal: Transmittance up to 70%

In the framework of SiLC & EUDET, an R&D is conducted for developing IR transparent sensors with transmittance T up to at least 70% (*20% for usual alignment sensors*). The higher transmittance the more sensors can be aligned with a single beam.

A detailed simulation study (*the most complete in the field so far*) was performed by M. Fernandez-Garcia (IFCA) for determining the key parameters to increase T.



Key parameters:

1) No need for 3rd party antireflection coating. (ARC). Passivation layers are used as ARC
2) Metal strip width chosen to minimize reflectance (10% of pitch)
3) Thickness of different layers optimized to achieve maximum transmittance. Outcome depends mostly on thickness of outermost passivation layers.

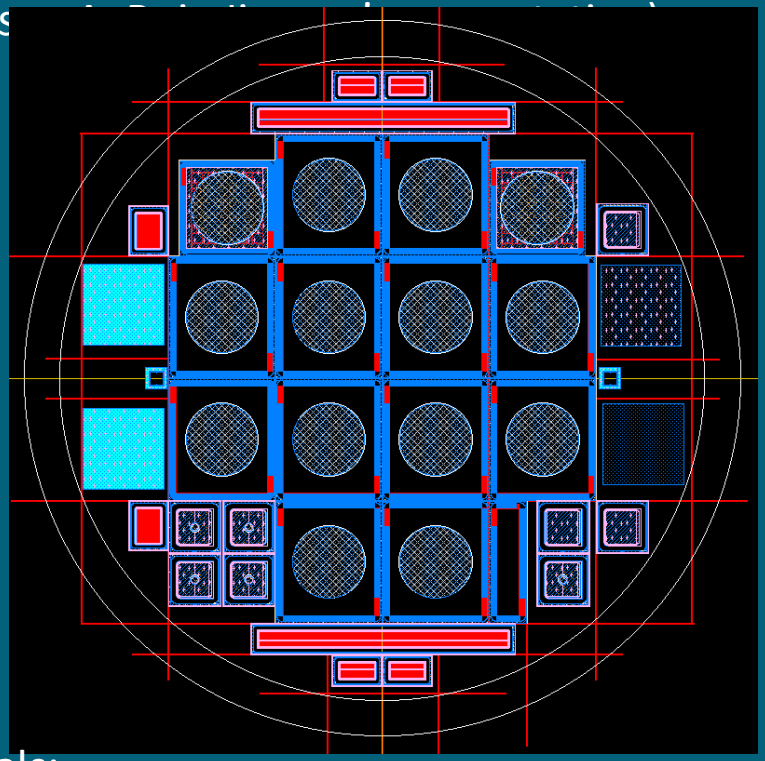
Followed by the fabrication of these new sensors by IMB-CNM (M. Lozano et al.) , before going to industrial transfer (see A. Ruiz-Jimeno's presentation)

R&D on IR transparent detectors

Goal: Transmittance up to 70%

Tests on these new sensors were performed on a preliminary batch end of July at the IMB-CNM production line. The wafers include:

(s



- 12 different detectors
- Common parameters:
- active area= 1.2x1.5 cm^2
- circular window in the back metal (r=0.5 cm)
- 256 readout strips with 1.5 cm length
- 9 guard rings and scribe line with n-well
- 6 detectors completed with floating intermediate strips for improved spatial resolution using the capacitive charge division principle.
- Optical test structures needed to characterize each material
- (see A. Ruiz-Jimeno's presentation)

Goals:

Study of effect of intermediate strip on optical transmittance

Characterization of T,R versus metal and/or implant width

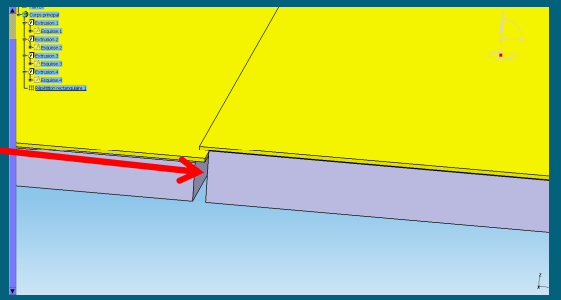
Find best design with optimal standard materials and industrial transfer for large size production

Edgeless strips sensors: Why?

Edgeless sensors decrease the non active edge regions of sensors (usually of a few hundreds of microns) down to about 10 to 20 µm.

Our interest in edgeless or active edge sensors is motivated by:

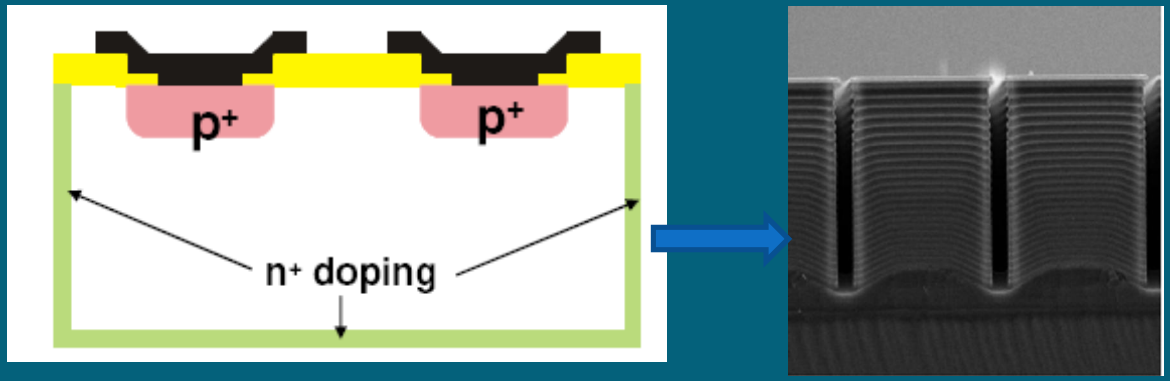
- ✓ allow building large area Silicon trackers seamlessly tiled detector matrices,
- ✓ thus no need for sensor overlap
- ✓ easier to build
- ✓ decrease of the material budget
- ✓ improvement of the tracking performances both in momentum and spatial resolution.



Two solutions based on the edgeless strip based on Edgeless planar and Edgeless SOI technologies are pursued.

Edgeless planar strips (FBK-irst-U. Trento/INFN)

(*Gian Franco Dalla Betta*)



Schematic cross-section (left view) and photograph (right view) of a planar strip detector with active edge on n-type substrate

Collaborative effort with prototyped sensors 2.5x5cm^2 (Trento & Paris)

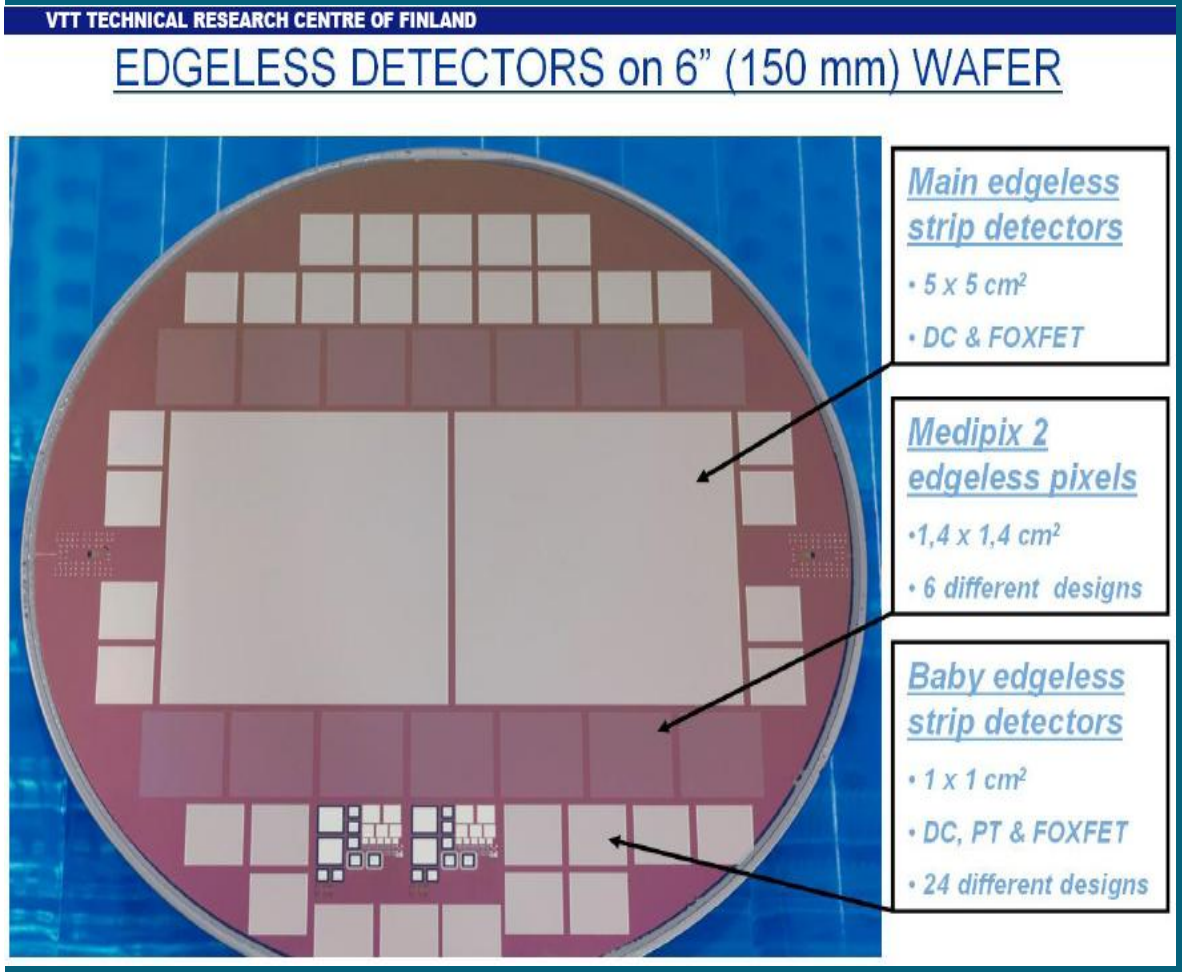
Goal:

Wafer bonding treated (contacts with EDGETEK in France)

Build 5x5cm^2 sensors and read out by VA1' chips

Full characterization at Lab followed by beam test & comparison with standard planar strips (HPK) & SOI based edgeless prototypes (see next)

SOI Edgeless strip detectors



(*courtesy Juha Kalliopuska*)

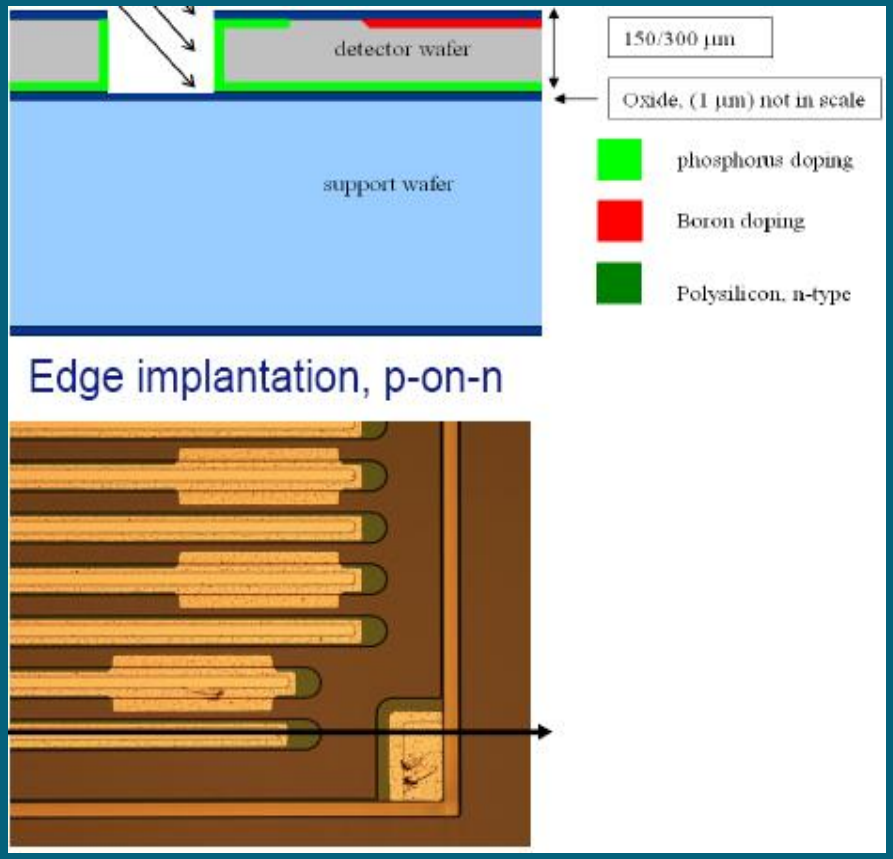
VTT achieved fabricating:

- edgeless strips & pixels sensors
- on 6'' SOI wafer
- based on alternative fabrication process w.r.t 3D processing with poly-Silicon filling
- Proving to be easier and more feasible fabrication line.
- Two different designs produced: p-on-n and n-on-n and
- Electrically characterized: CV, IV and breakdown voltage

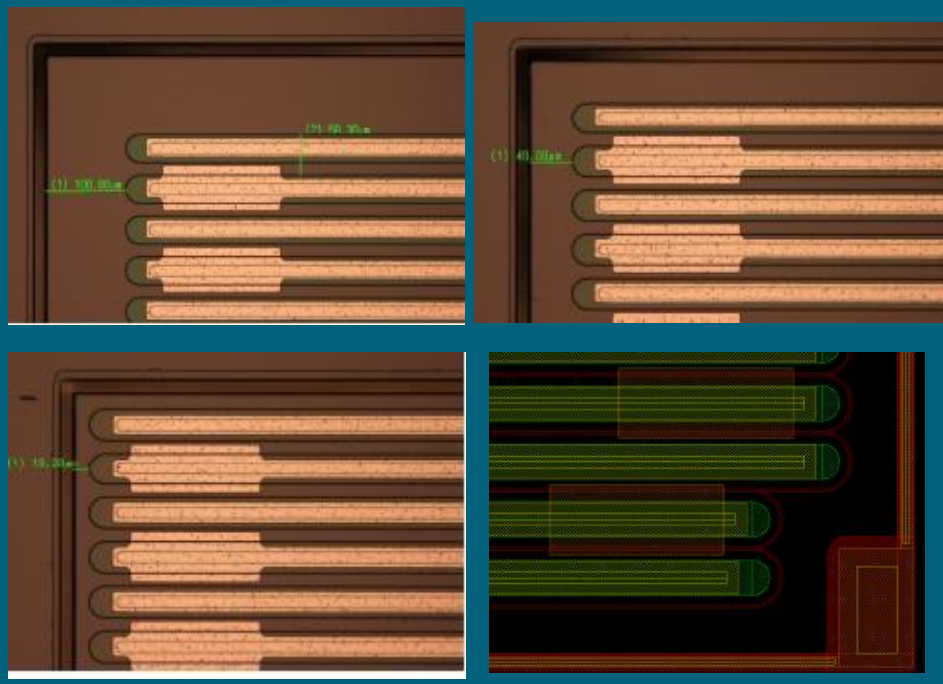
SiLC is going to include these new sensors on their test beam prototype tests

SOI Edgeless strip detectors

New fabrication procedure:



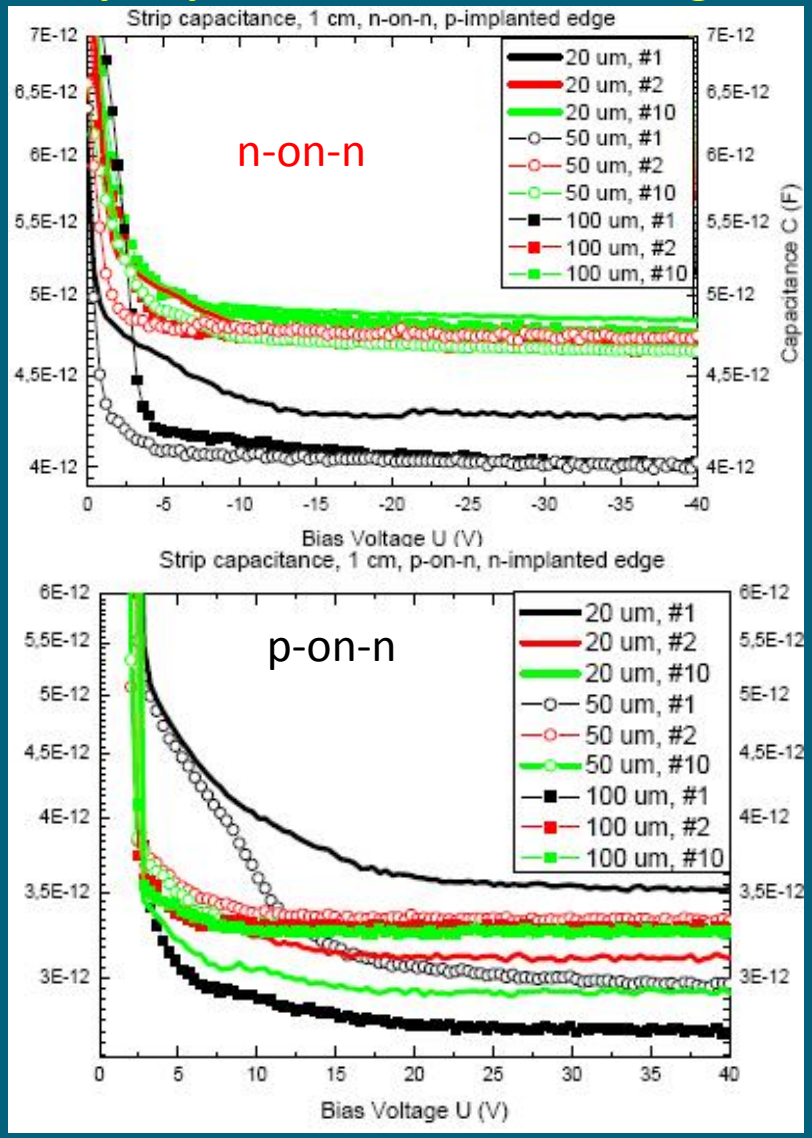
DC strip p-on-p & n-on-n designs with different active edges distances (100, 50 and 20 µm)



- No need for polySi filling, planarization & separate ICP dicing
- Fast process and no bowing of the wafer
- Detector sustain handling – no edge cracking
- Physical inactive edge region ~ 1µm
- Requires non-planar lithography => readiness available at VTT

SOI Edgeless strip detectors: characteristics

Strip capacitance vs Bias voltage:

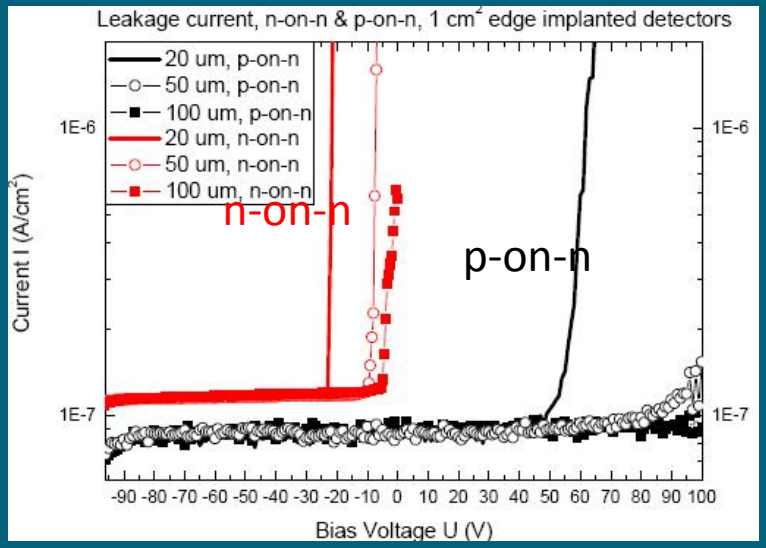


Front-to-backplane depletion: 7V (p-on-n)
4V (n-on-n)

Full depletion: 25-40V (p-on-n)
13-25V (n-on-n)

Strip capacitance of 3 to 3.5pf/cm (p-on-n)
(about 2 to 2.5 worse than planar strips)

Leakage current vs Bias Voltage



Looks promising!

SiLC will compare these two edgeless technos including on prototyped devices at test beams

3D based technology developments: short strips and pixels

Interest for higher granularity &/or thinner devices (examples later)

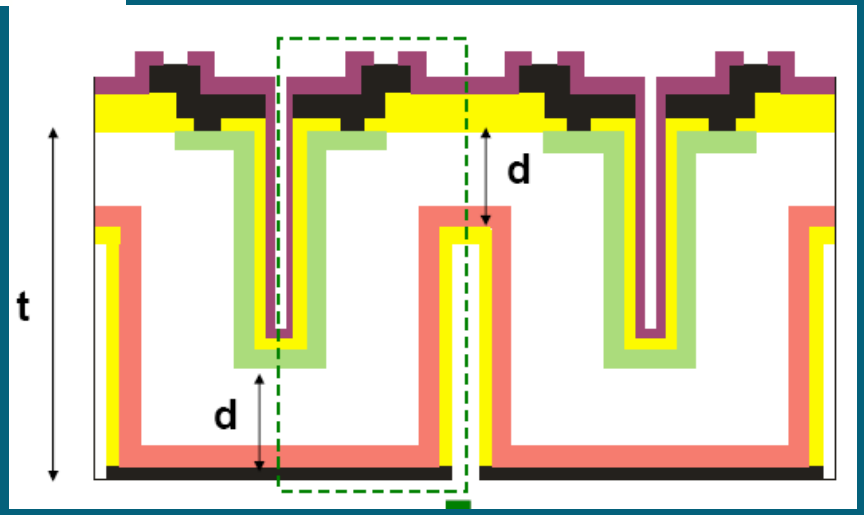
- **3D based short strips (fabricated by FBK-irst)**

Since 2009 collaborative contacts IRST-U.of Trento/LPNHE in SiLC on developments of short strips (1-2cm) based on 3D technology. We can benefit from the advantages of 3D without suffering of the high strip capacitance of these strips.

Goals:

1) Use first the recycled 3D-DTC-2b batch with non passing-through columns (see next slide), to build first short strip based detector area for test beam equipped with VA1' reference read-out.
2) 3D-DTC-3: n-on-p, 250 µm thick substrate, full 3D detectors and passing-through columns.
   New double-sided process defined, no need for support structure, allow dual read-out strip. Available fall 2009, for test in 2010.

3DDTC-2b produced by FBK

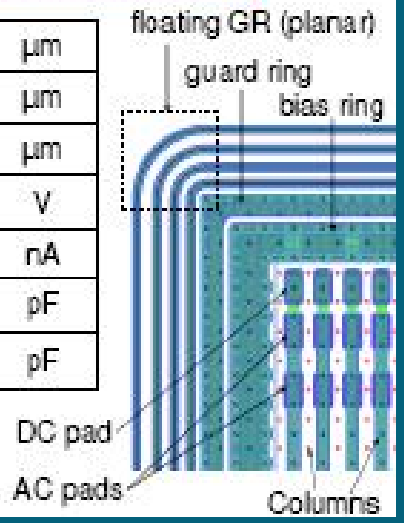


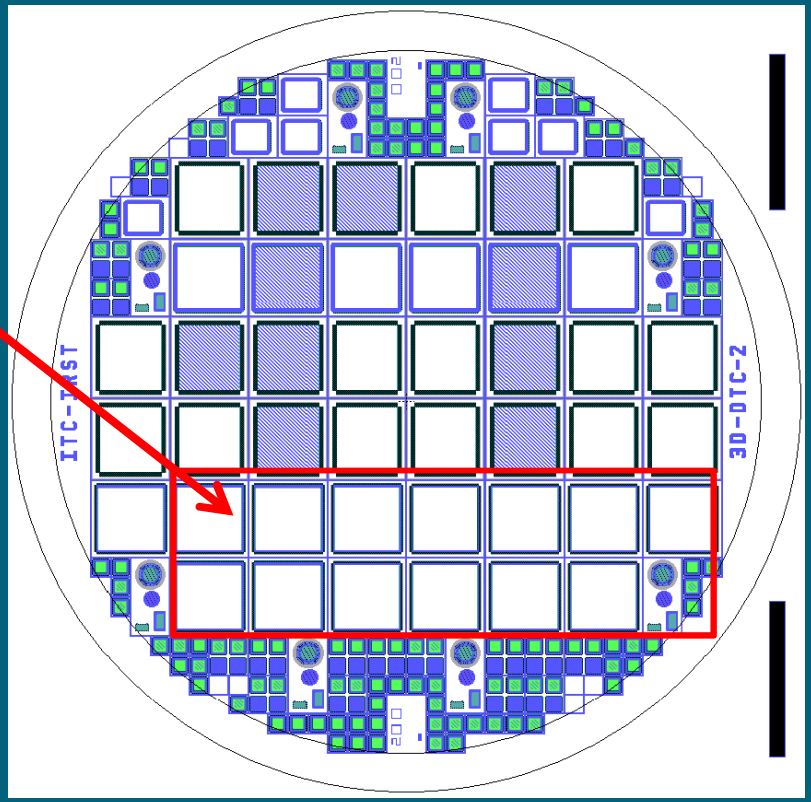
Batch	3D-DTC-2b
Substrate type	p-type
Substrate thickness (μm)	200
Junction column depth (μm)	160-170
Ohmic column depth (μm)	190
Completed by	April 2009

Microstrip detector features

Substrate thickness	220	μm
Junction column depth	120	μm
Back column depth	190	μm
Lateral depletion	~20	V
Strip leakage current	~1	nA
Strip capacitance	~7	pF
Coupling capacitance	50	pF

102 x 102 columns array
80μm inter-column pitch



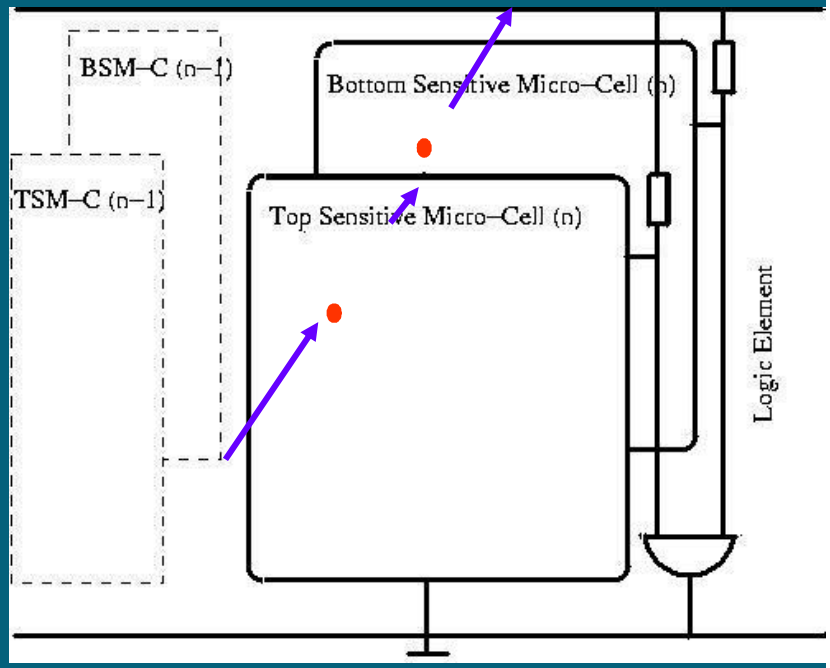


Low material budget & high intrinsic gain 3D pixels

Avalanche Pixel Sensor (APS) for Tracking (OSU)

PRINCIPLE:

The charged particle crosses two identical breakdown mode microcells on top and bottom of the wafer. Two breakdown processes are thus created and produce the output coincidence signal. The quenching elements stop the avalanche processes. Then the microcells recover from the breakdown state.



Courtesy V. Saveliev

Low Material Budget & High Gain 3D pixels:

Main parameters:

✓Pixel sizes: 10x10 up to 100x100 μm^2

✓ Intrinsic Gain (breakdown mode) equivalent ~10^6 :

✓ Thus fully digital device

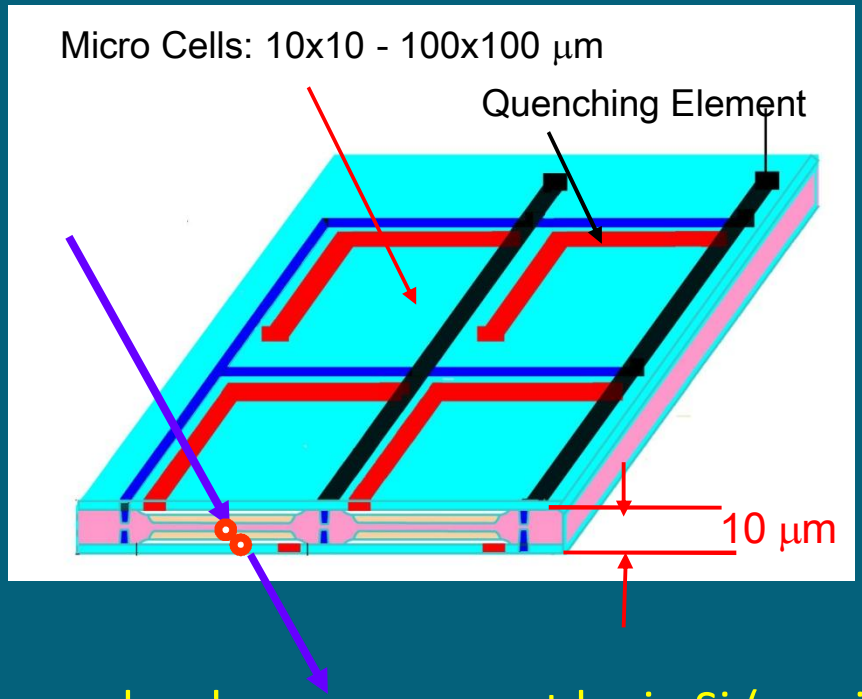
✓Thickness of the detecting structure: 4µm

✓ Operating conditions

- Low Operational voltage ~ 50-60V
- Room Temperature
- Non sensitive to Magnetic Field
- No need for Analogue VFE

✓ Standard CMOS technology

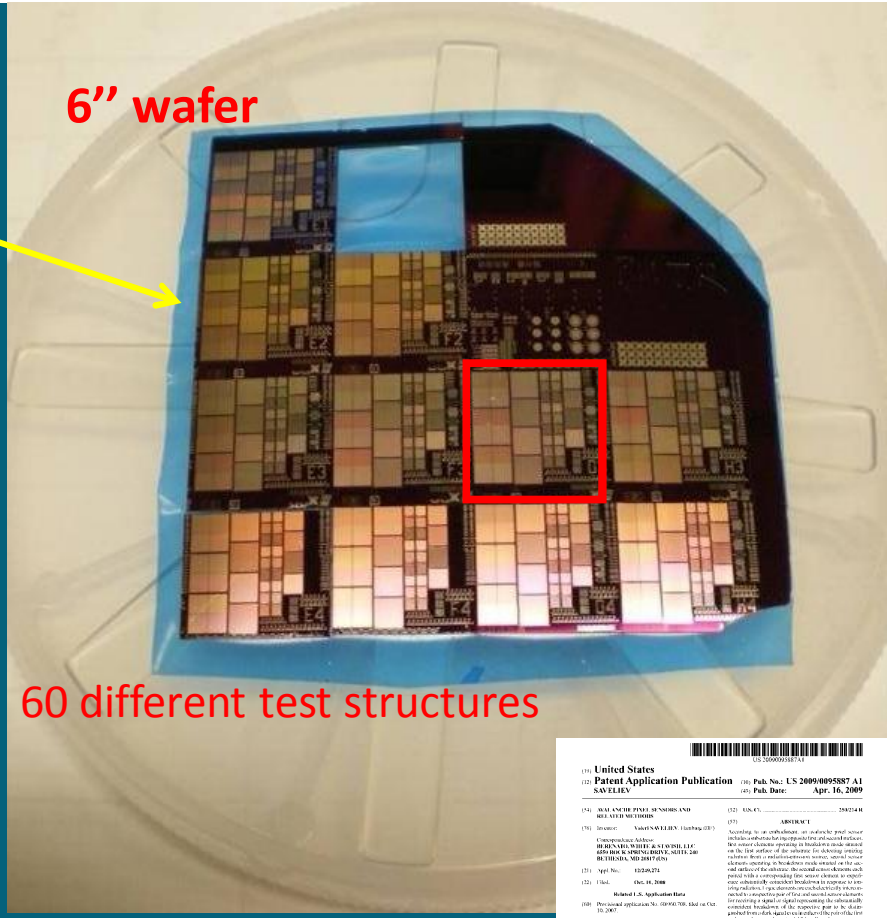
So easy mass production



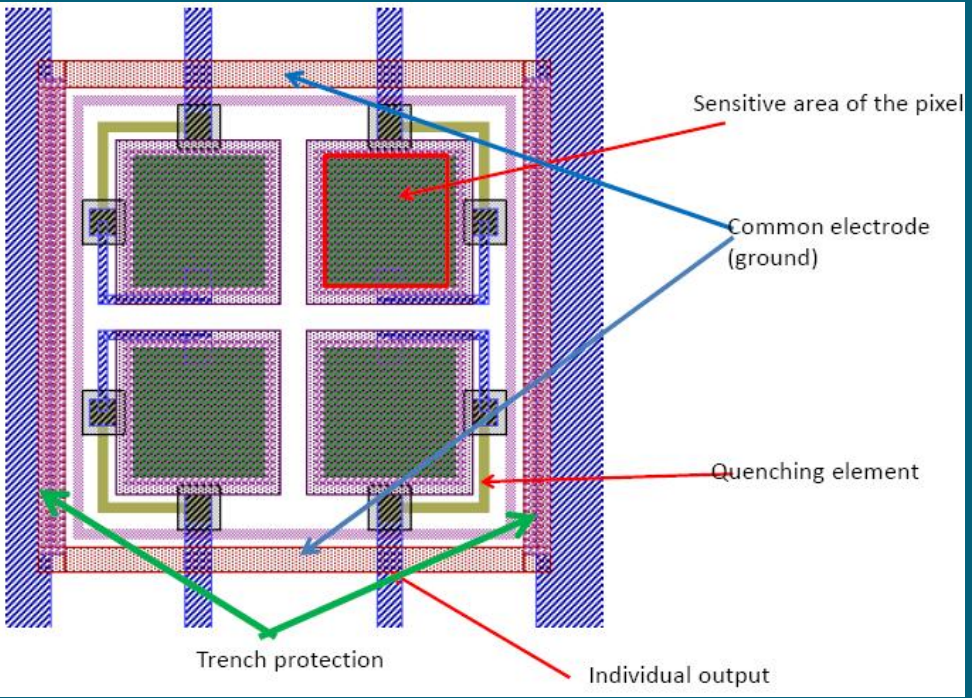
✓ The quenching elements for quenching the avalanche process must be in Si (passive)

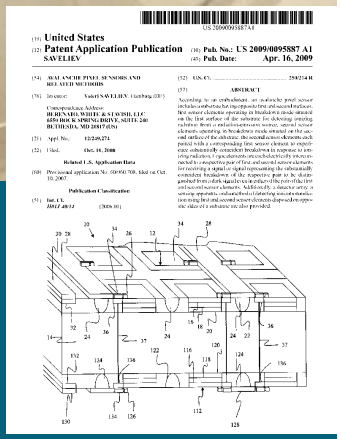
APS Manufacturing by:

KOTURA Inc. Monterey Park Ca (USA)



Ex : test structure made of 4 indpt. pixels 25x25µm²



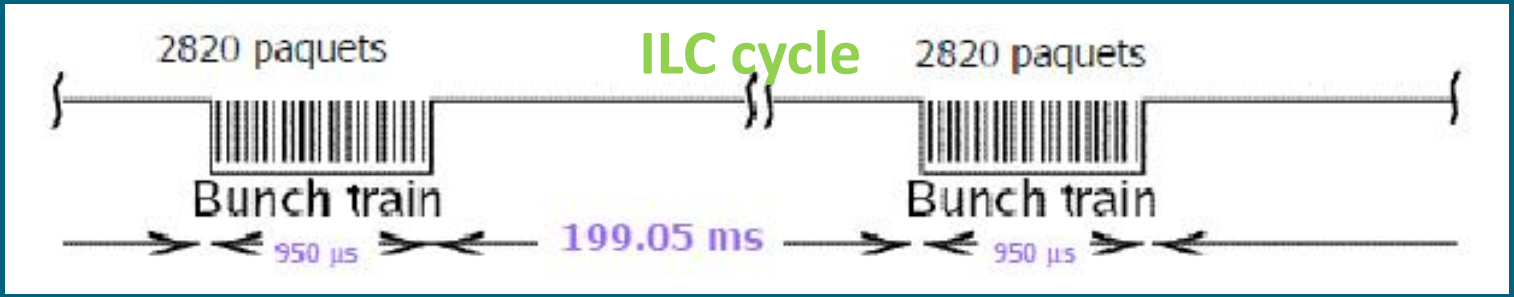


Manufactured APS by KOTURA will be further characterized by SiLC , including test structures both at Lab and test beams (beam telescope prototypes)

R&D on Front End Electronics

The FEE is closely related to the fact 1) that microstrips are currently the baseline for LC sensors and 2) to the cycle of the ILC machine

.



Long shaping time (relatively slow cycle machine)

Power cycling (possible)

Digitization and pre-processing : Take advantage of the time between inter-bunch trains for highly processed, controlled, fault tolerant and flexible readout (fully programmable).

FEE in numbers

- Goal: Integrate 512-1024 channels in 90nm CMOS:
  (but foreseen elementary blocks of 256 channels: multiplexing factor 256:1)

  - Amplifiers : 30 mV/MIP over 30 MIP range
  - Shapers : 500ns–2μs
  - Sparsifier : Threshold the sum of 3-5 adjacent channels
  - Samplers : 4 samples at variable sampling clock period (up to 80ns)
    Event buffer 8 depth
  - Noise baseline : at least as already achieved with UMC 180 nm tech.
    375 + 10.5 e-/pF @ 3 μs shaping, 210μW power
  - ADC : 12 bit-ADC
  - Power dissipation/channel for the overall FE chain: 1mWatt
  - Buffering, digital pre-processing
  - Calibration
  - Power switching (could save a factor of about 70)
  - Total number of readout channels: a few 10^6 channels

Main features of the new circuit (new= currently under design)

128 channels (1 test channel): Preamplifier, shaper, sparsifier, analogue pipeline (4x8 cells), 12-bit ADC

2D memory structure: 4x8/channels

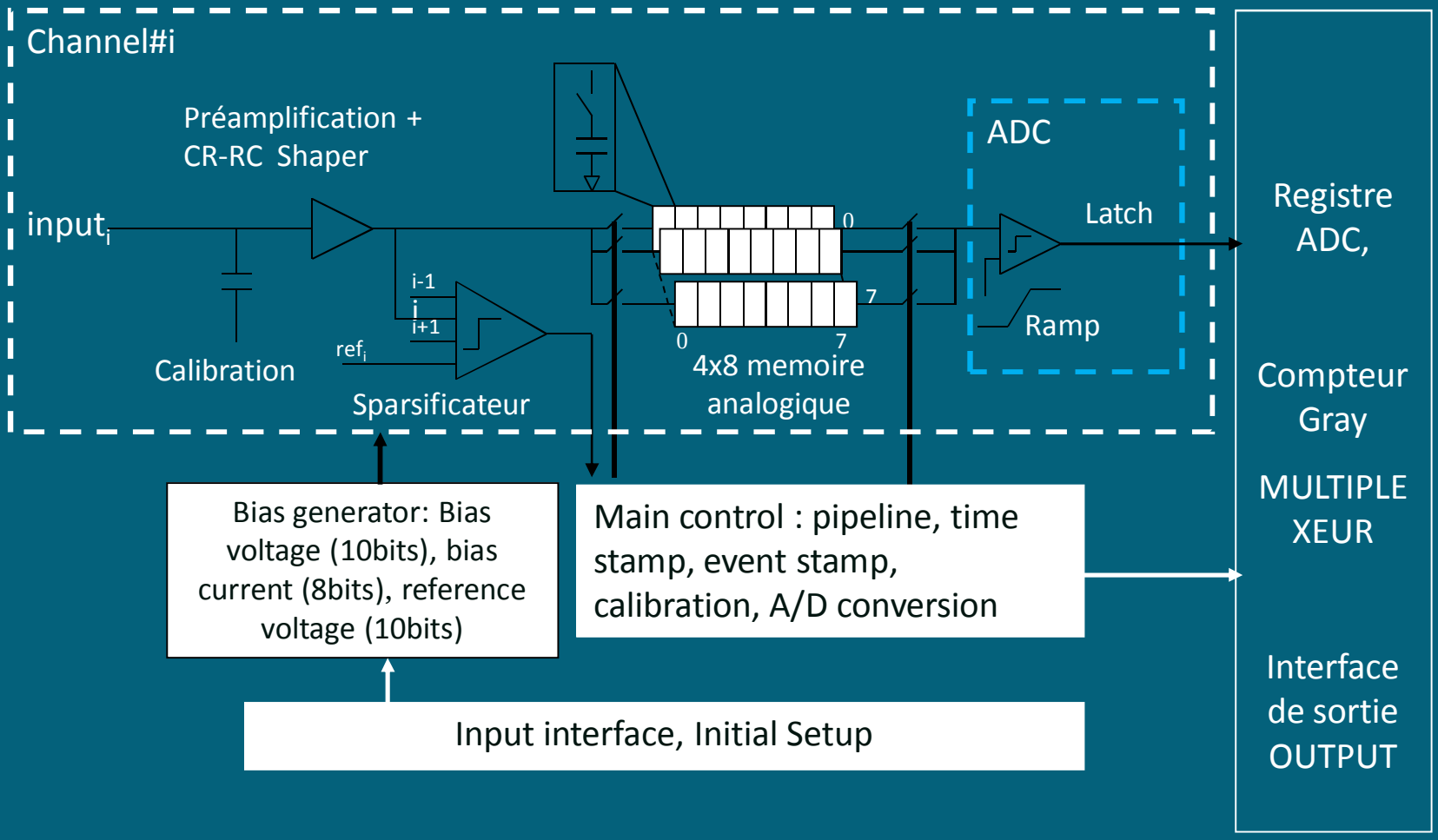
Fully digital control:

- Bias voltage(10-bit) and current (8-bit)
- Power cycling (in optional)
- Shaping time programmable
- Sampling frequency programmable
- Internal calibration
- Sparsifier threshold programmable per channel
- Event tag and time tag generation

.....

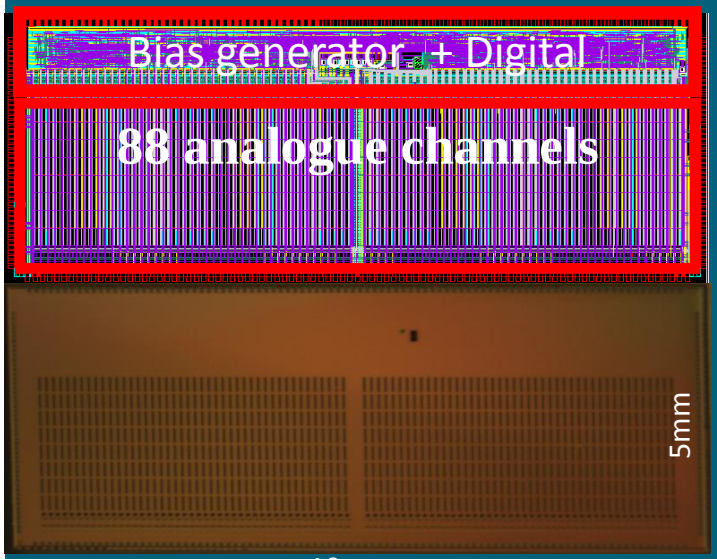
2 Trigger modes: Internal (integrated sparsification)
External (LVTTL) for beam test

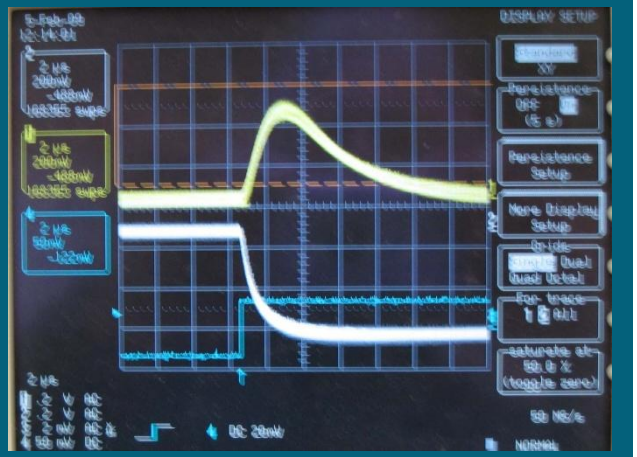
Developing a mix-mode FE readout with pulse-height reconstruction, zero suppression, full digital control (highly fault tolerant, flexible/robust) power cycling, in DSM CMOS technology

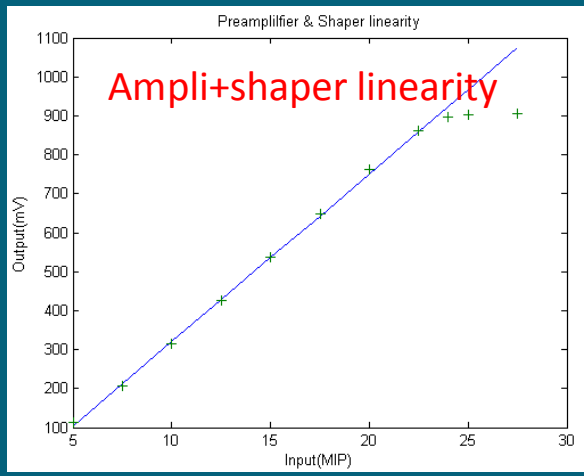


Present status and roadmap

SiTR_130-88: first full mix mode prototype delivered end 2008 and fully tested
analogue part: OK; Problems with digital part







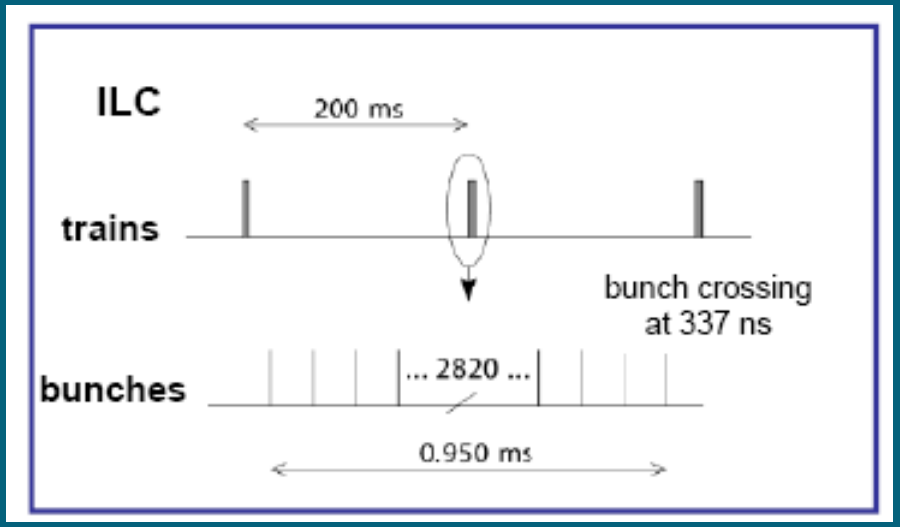
Power dissipation: 1.2 mWatt/channel for full chain

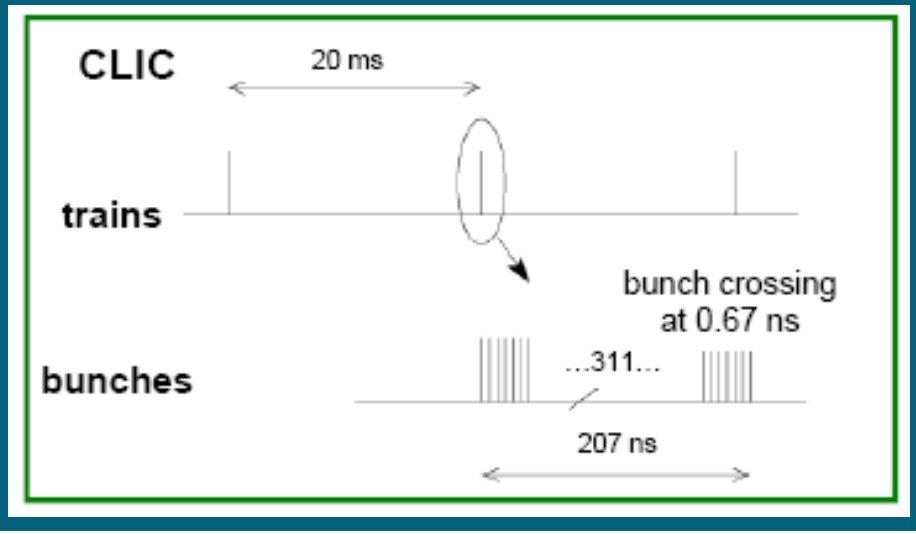
SiTR_130-128 under design for equipping t.b. Prototypes in 2010 and later (several 10^4 ch.)

ROADMAP ON ELECTRONICS

- Go to 256 channels and gather 7x258 in 1 block
- Thinning (50 µm)
- Go to 90nm CMOS techno
- **Direct connection of the FE chip on strip sensor (wire bonding -> bump bonding -> 3D interconnect)**
- Adapting FE to CLIC cycle (complete revisit of FE)
- Bunch tagging at CLIC
- Develop the TOT (B. Schumm's presentation)
- Develop Data processing and data handling (DAQ)
- connectivity & cabling to DAQ

Machine cycle: CLIC vs ILC





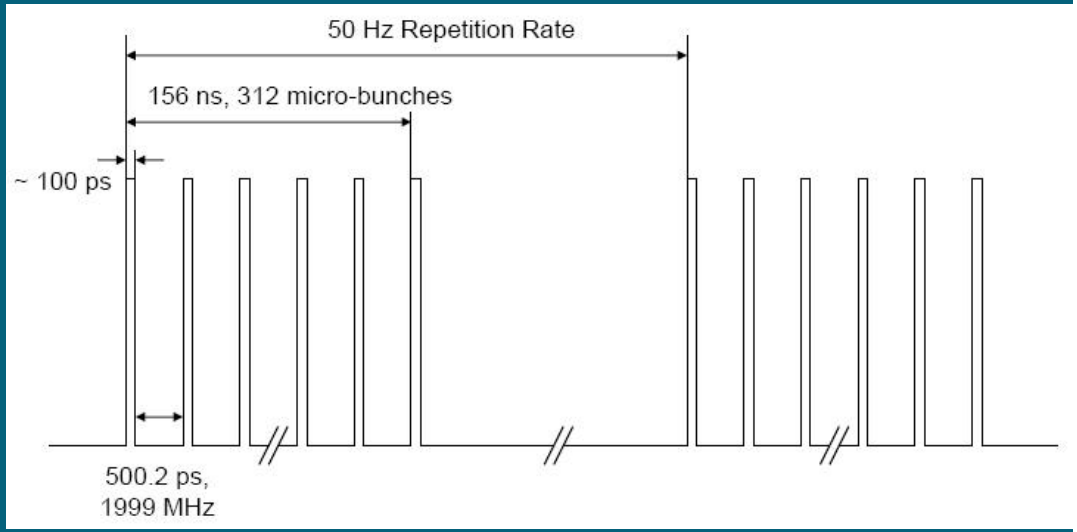
CLIC & ILC: different e+ e- machines (technology, Ecm range)

⇒Thus their cycles are different

⇒ so are the environmental conditions imposed to the detectors & their associated electronics

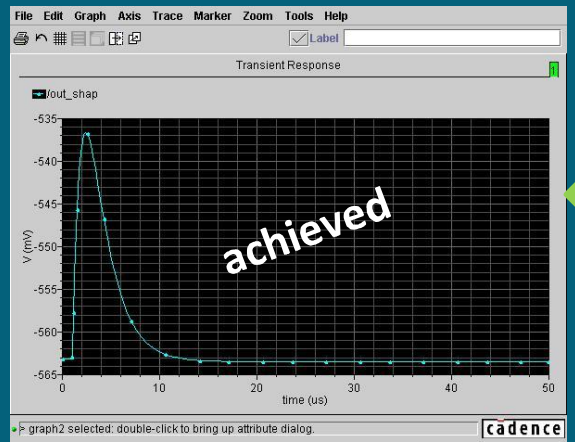
⇒So also are the Physics (going to higher Energy)

This requires new studies: CLIC is NOT a cut-and-paste of the ILC case.



The CLIC case

The ILC VFE output



Adapting strip VFE (preampli+shaper) to CLIC has started.

VFE Paramètres (For CLIC case)	Cahier des charges	Circuit réalisé
Bruit du préamplificateur + shaper (à Cdet = 10pF)	~1000 e^-	856 e^-
Gain en charge en sortie du shaper	30 mV/MIP	27 mV/MIP
Consommation du préamplificateur	< 250µW	240µW
Consommation du shaper	< 100µW	90 µW
Linéarité à 10 MIP	1%	1% (jusqu'à 18MIP)
Linéarité à 20 MIP	2%	3%
Temps de montée en sortie du shaper	10 - 25ns	20ns
Temps de descente en sortie du préamplificateur	< 250ns	250 ns
Temps de descente en sortie du shaper	< 200ns	< 120 ns

Questions:

- Time Stamping O(100ps)?
If needed on dedicated layer?
Or time stamping 10-20ns*
-Pulse shaping at 20ms feasible (?)
-Power dissipation?
could be kept reasonable?

*We have some idea based on our LHC previous experience on how to achieve a fast pulse reconstruction and get a time stamping with O(20-25ns) resolution.

Direct connection sensors-FEE

Major R&D objective: NO MORE Hybrid FEE board +pitch adapter

⇒New module concept under development

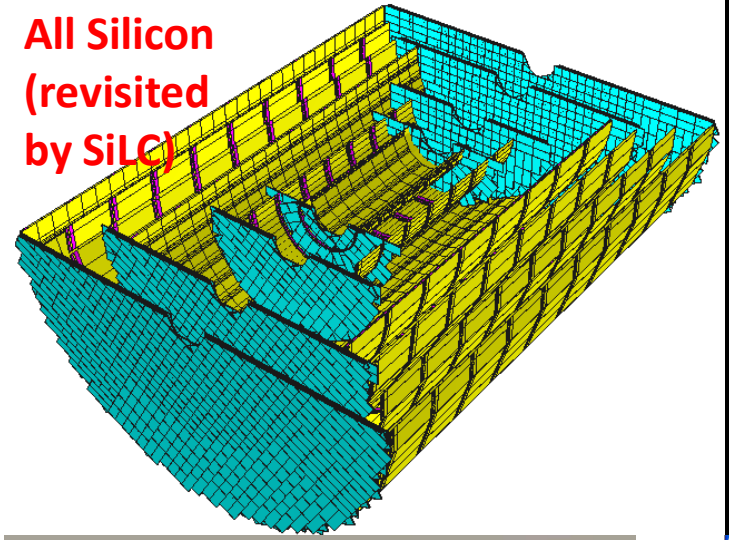
ALL-in-ONE SOLUTION => direct connection of FE chip on the sensor

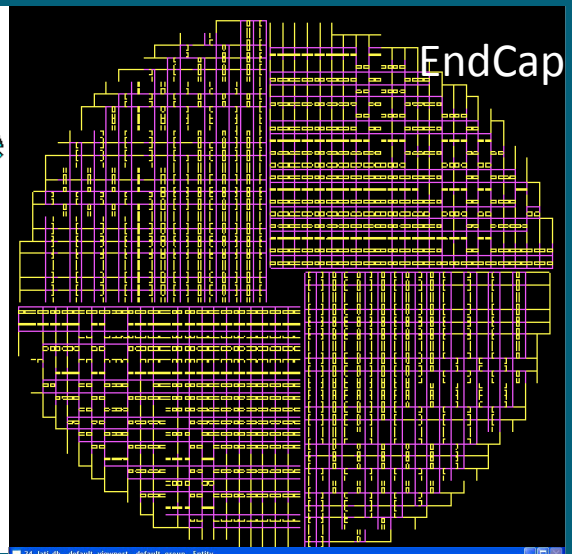
- material budget,
- simplification of elementary module (tile) and
- of overall detector construction (burden put on sensor and FEE chip),
- improvement in performances
- Use high tech advances (cost?)

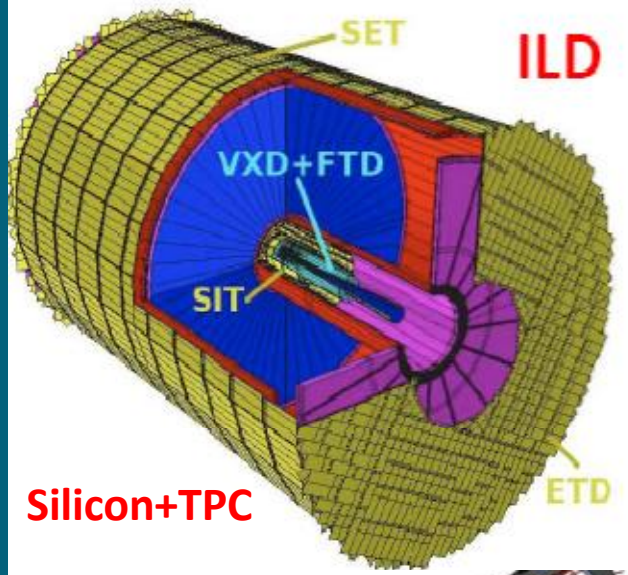
SiLC is pursuing with the different steps: wiring onto the sensors: HEPHY + Polish firm (proto at CERN t.b); bump bonding: HPK+LPNHE (proto sensor+FE chip in 2010); going in // to 3D vertical interconnect (part of the worldwide 3D interconnect effort)

Tracking concepts at LC: All-Si vs Hybrid

All Silicon (revisited by SiLC)

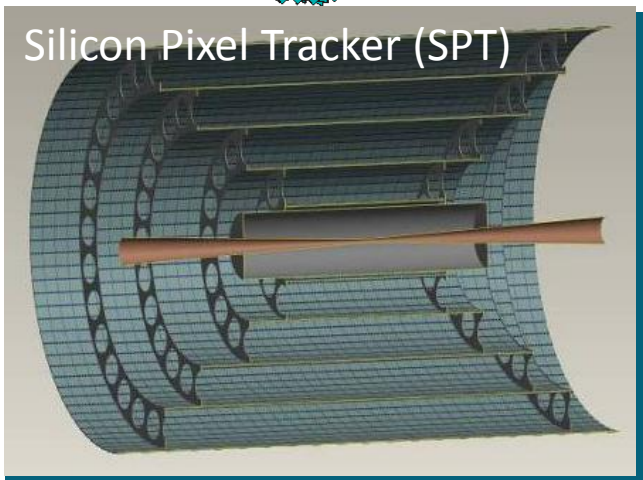


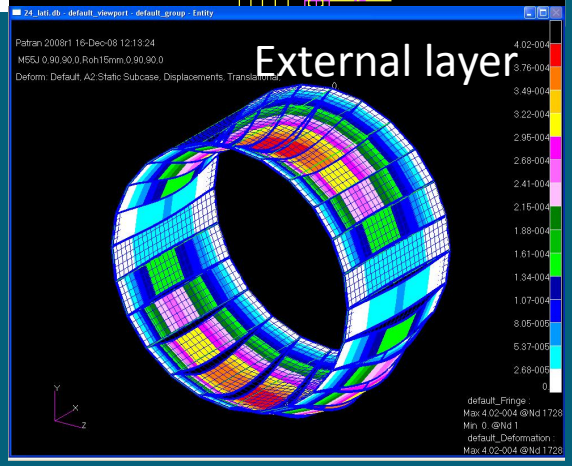




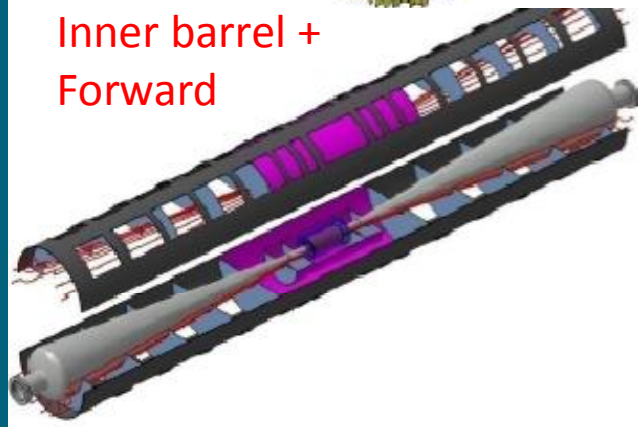
Silicon+TPC

Silicon Pixel Tracker (SPT)





Inner barrel + Forward



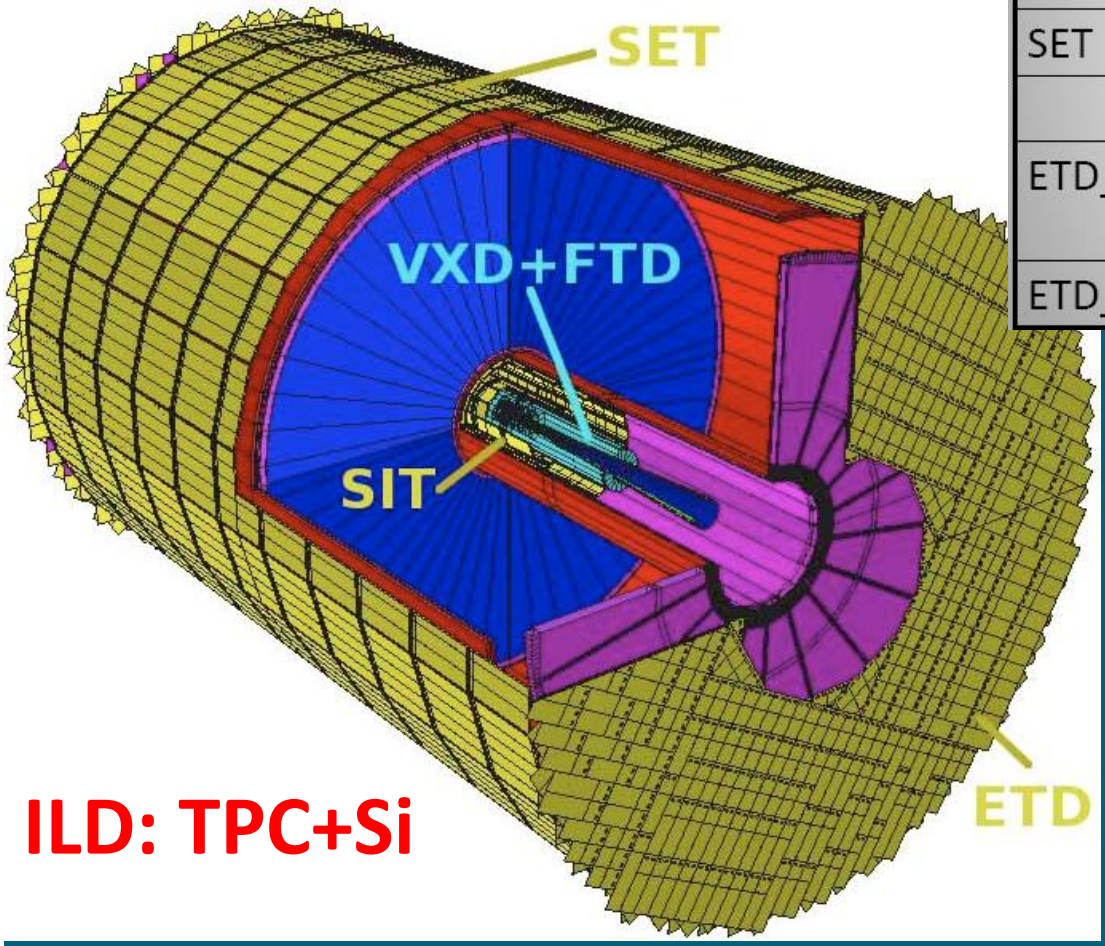
ILCROOT Geant4 based simulation: edgeless strip detectors with a unique sensor type (but SPT)

Detail study performed already for LOIs. Requested a ready -for -construction design end 2012.

ILD Hybrid tracking: *The Silicon Envelope*

(in numbers as currently in the ILD LOI)

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30



ILD: TPC+Si

Total number of channels:

10^6 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)

= **$10 x10^6$ channels**

Total area:

7 (SIT)+110 (SET) +2x30(ETDs) = **180 m^2**

Total number of modules:

500 (SIT) + 2500 (SET) + 2000 (ETDs)=

5000 modules with unique sensor type

(but for FTD) but ***variable strip length*** (10-30 cm) depending module location.

GEANT4 simulation **(here)& mechanical design** (CATIA) in progress

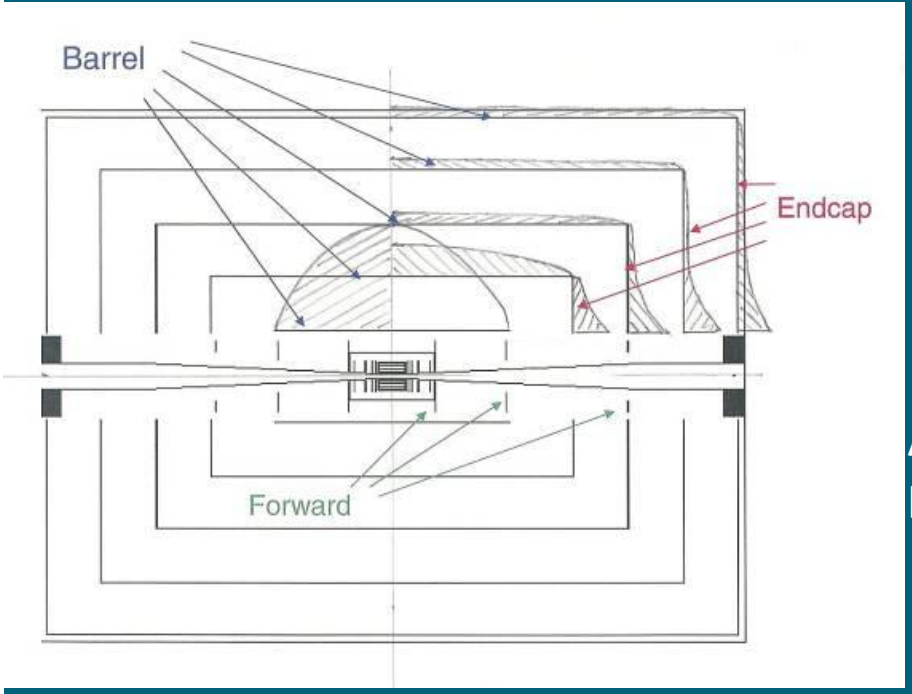
The Silicon Pixel Tracker *(C. Damerell et al.)*

Among the motivations:

- Develop a tracking system of unprecedented **transparency** **(aim: 0.6% X0 /layer)** so that nearly all photons down to 7^o θ_P will convert in the ECAL, and complications due to hadronic interactions in the tracker will be rare.

-Maximise performance: pixels provide unambiguous space points on each layer.

- Basic principle is to strip out all feature that aren't strictly necessary, and which would increase the material in front of the calorimeter

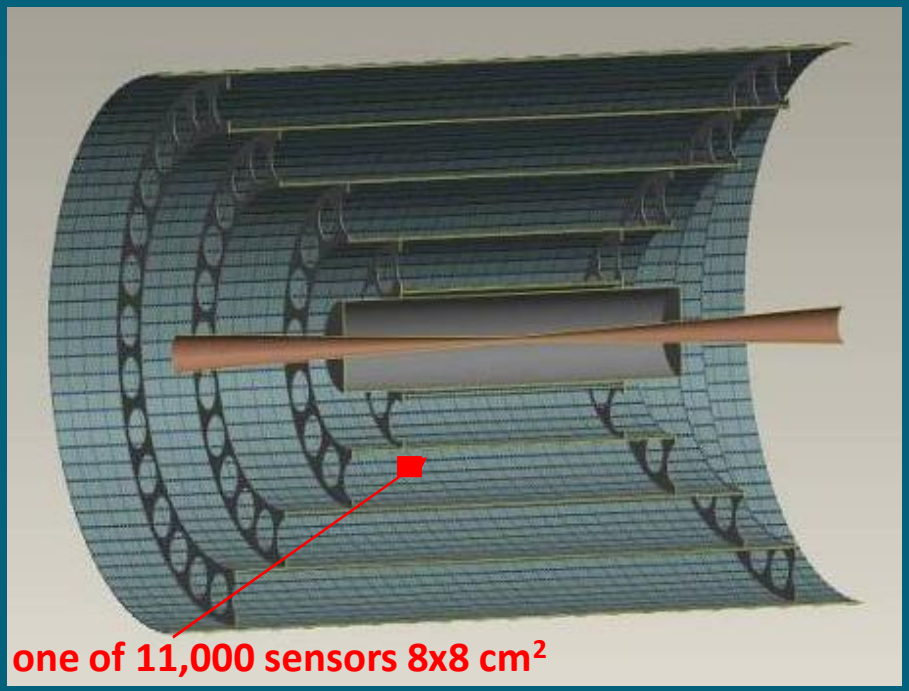


- **Total hit density ranges from 2.5/cm^2/train (layer 1 barrel) to 1/10 of that (outermost barrel) – occupancies in SPT are everywhere < 10^{-4}**
- **Forward disks: densities exceed 600/cm^2 /train, so pixels with short sensitive windows will be needed. But area to be covered is small.**

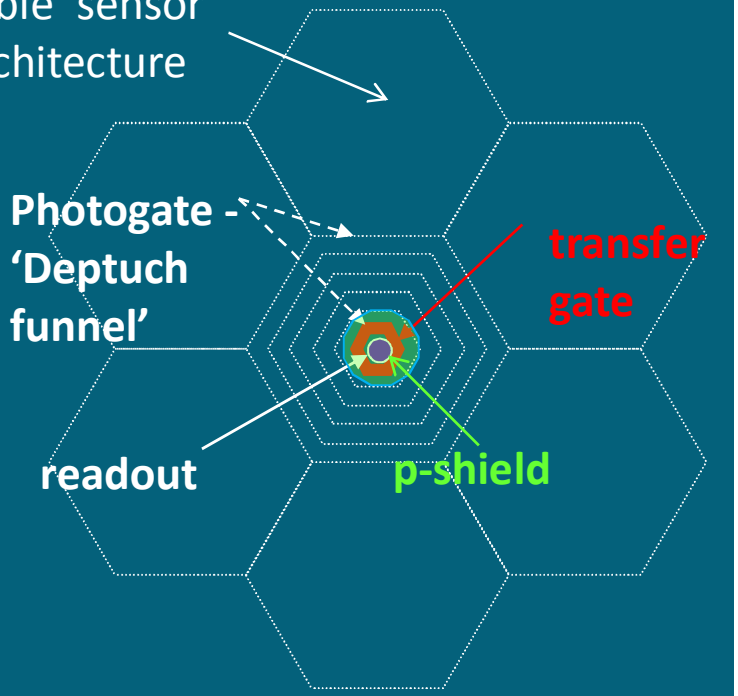
Courtesy C. Damerell et al.

SPT preliminary design *(C. Damerell et al.)*

Techno under consideration: started with CCD's (LCFI R&D) now charge-coupled CMOS pixels.



Possible sensor architecture



The mechanical issues of such a detector design are addressed : again here the expertise from LCFI R&D is instrumental

Some features: ~0.6% X_0 per layer, seems achievable , 3.0% X_0 total, over full polar angle range

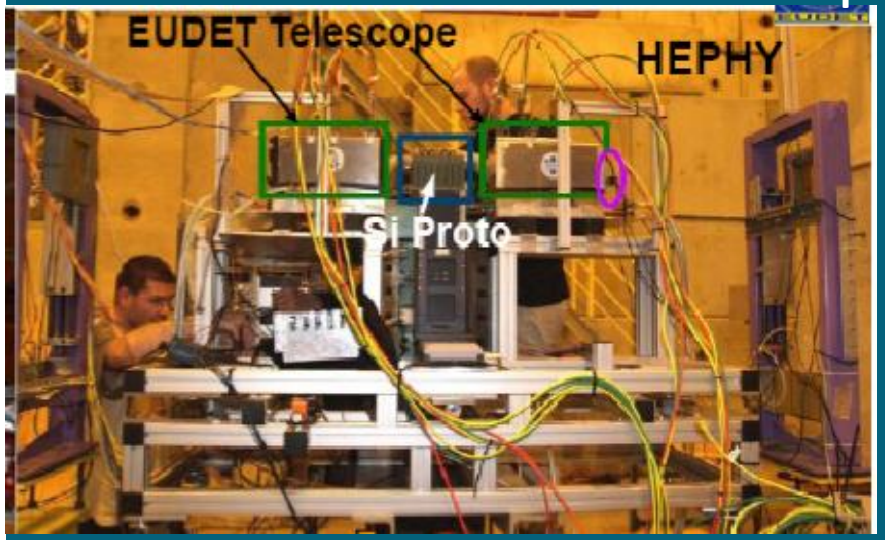
Unique pixel size of 50 µm diameter

30 Gpixels, in line with trends in astronomical wide-field focal plane systems by 2020 ***(multi-Gigapixel focal plane arrays in astronomy (eg LSST))***

SiLC has added this new research line in collaboration with C. Damerell & co-workers

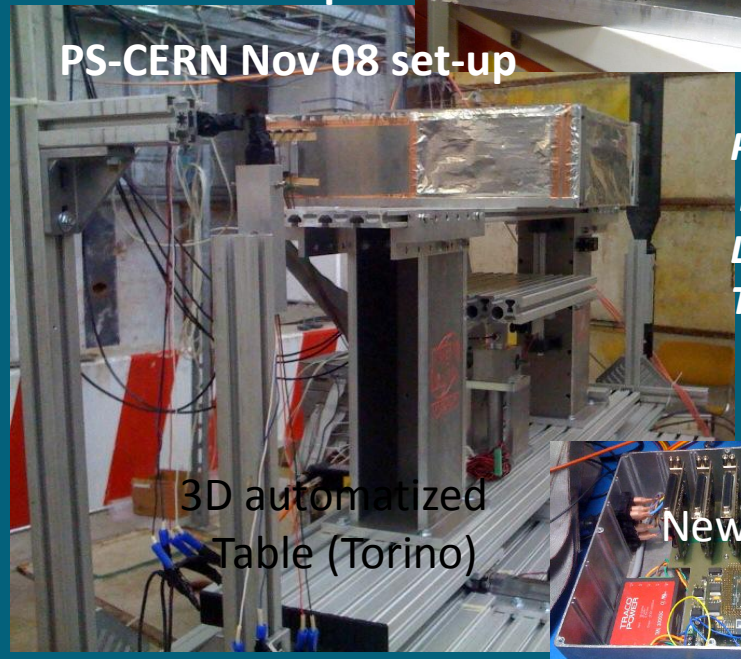
Test beams activities at DESY & CERN 2008-2009

Combined test with EUDET MAPS telescope at SPS.



Multipurpose SiLC standalone test beam set-up

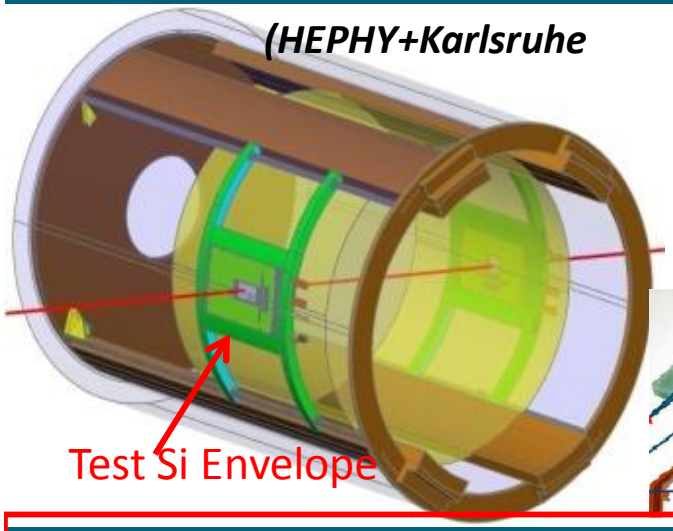
PS-CERN Nov 08 set-up



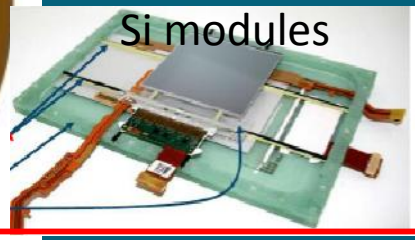
Prague
ICFA
LPNHE
Torino

Combined test beam with LCTPC (DESY)

(HEPHY+Karlsruhe



Mechanical support



In preparation 2010-12: combined test beams with calorimeters
Tests on new FEE, new sensors;
Larger size prototypes

=> Expertise on prototype construction, developed FE, DAQ and analysis for test beams since 07

Conclusion & perspectives

- As for the other major sub-detectors, an active R&D is ongoing on Si tracking for the future LC , driven by a rather hard-line schedule (despite unknowns..): next major milestone in 2012 (a “ready-to-construct” TDR).
- It includes a test beam programme within the FP6-EUDET framework combined with the other sub-detectors (vertex, TPC –both ongoing- and calorimeter, expected to start next year).
- Tracking is a Key issue and semi-conductor based trackers play a major role in both tracking strategies (All Si or hybrid)
- Because unknown on time scale and machine(s), the R&D must provide “very soon” a “*conservative R&D line*” but also keep *an innovative R&D line*; the tracking we are proposing may/will be quite different of what will be built at the end (ex: SPT alternative).
- This applies first of course to the basic R&D objectives: sensors, FEE
- Key words: Synergies with other R&Ds on the field and collaboration with Industry.

Experimented synergies