SPIROC measurements status and proposal for SiPM readout

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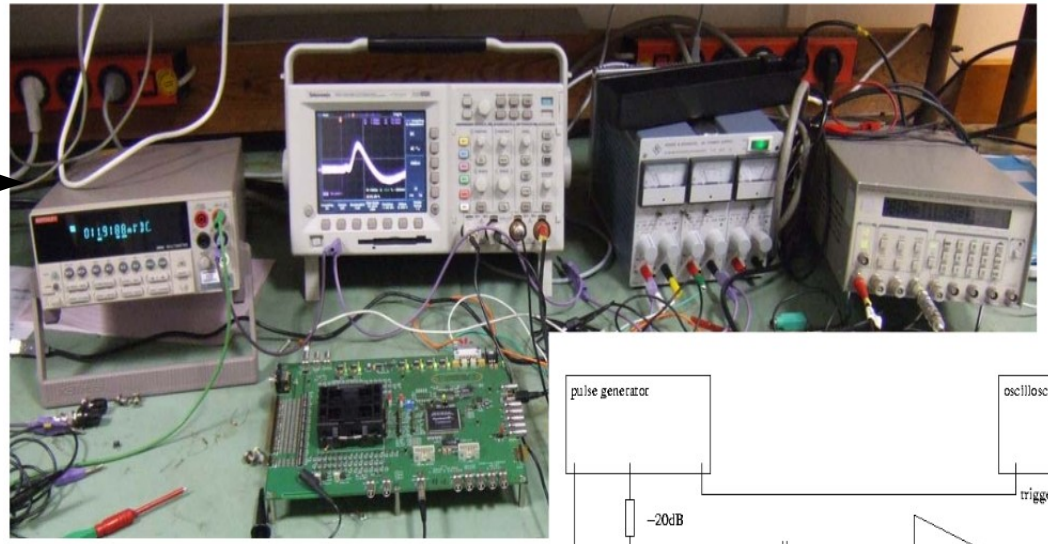
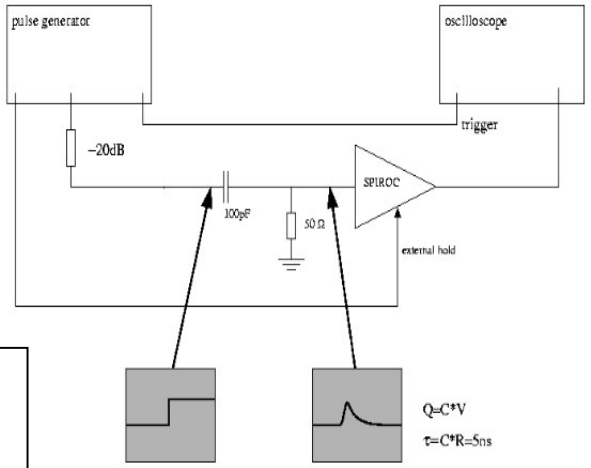
status of measurements – analog part

Test setup:

Pulser + Coupling C +

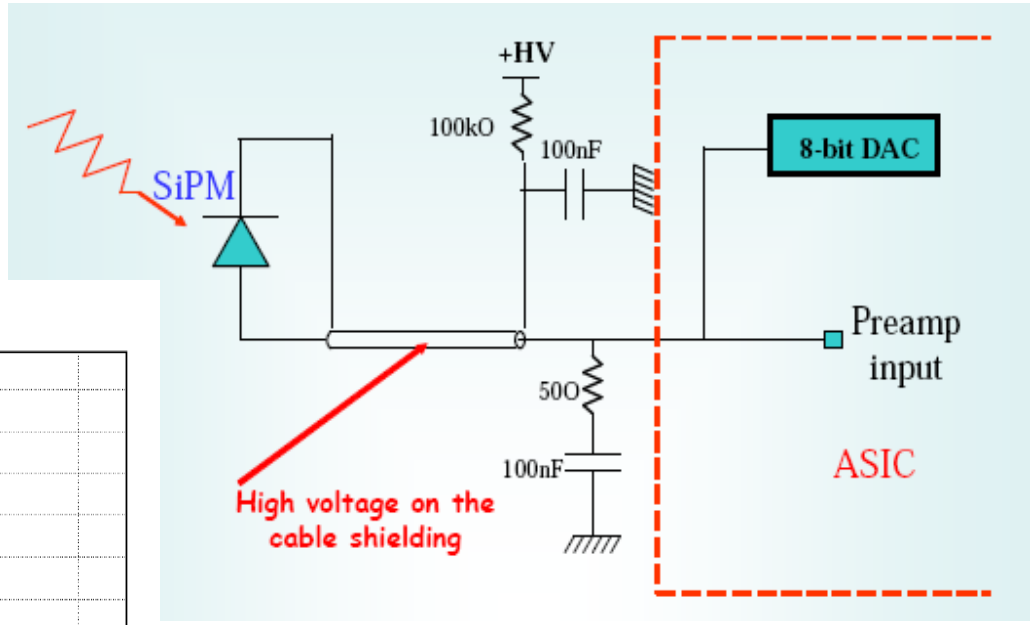
Oscilloscope

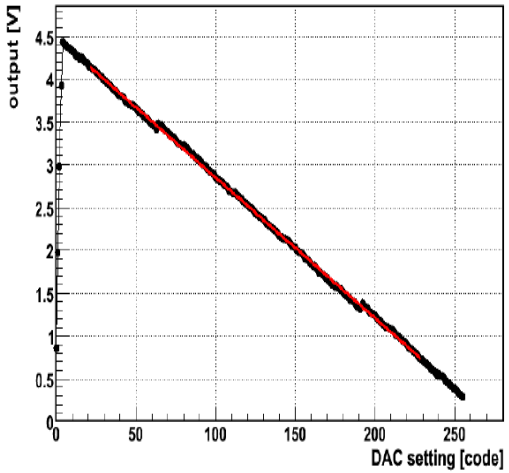


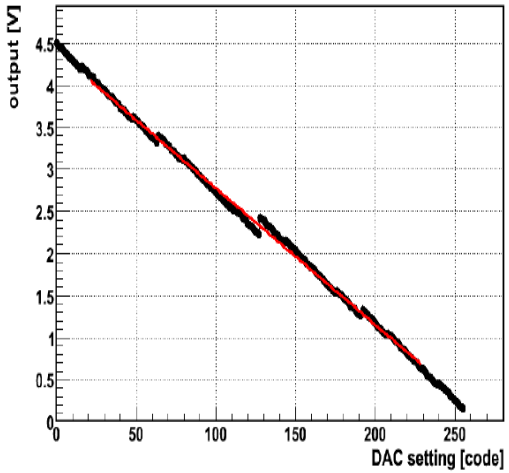


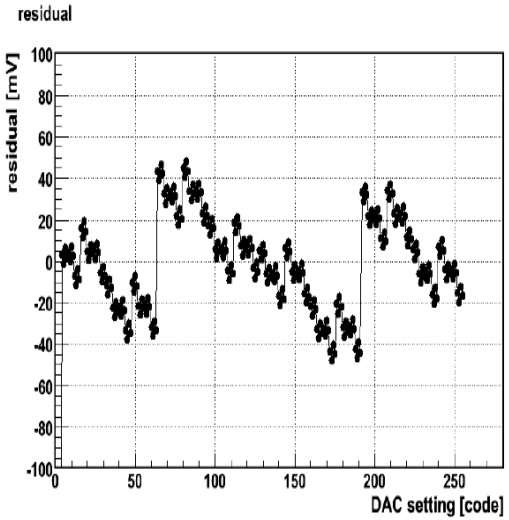
uto-trigger mode

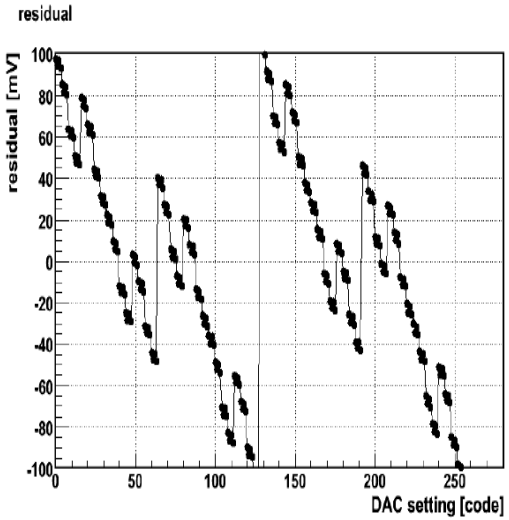
Input DAC





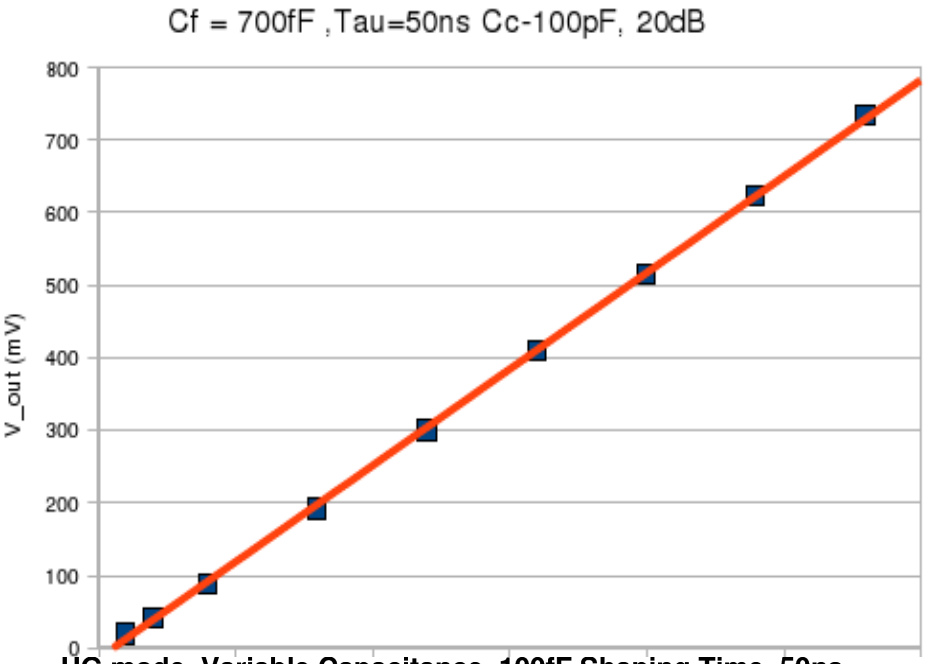


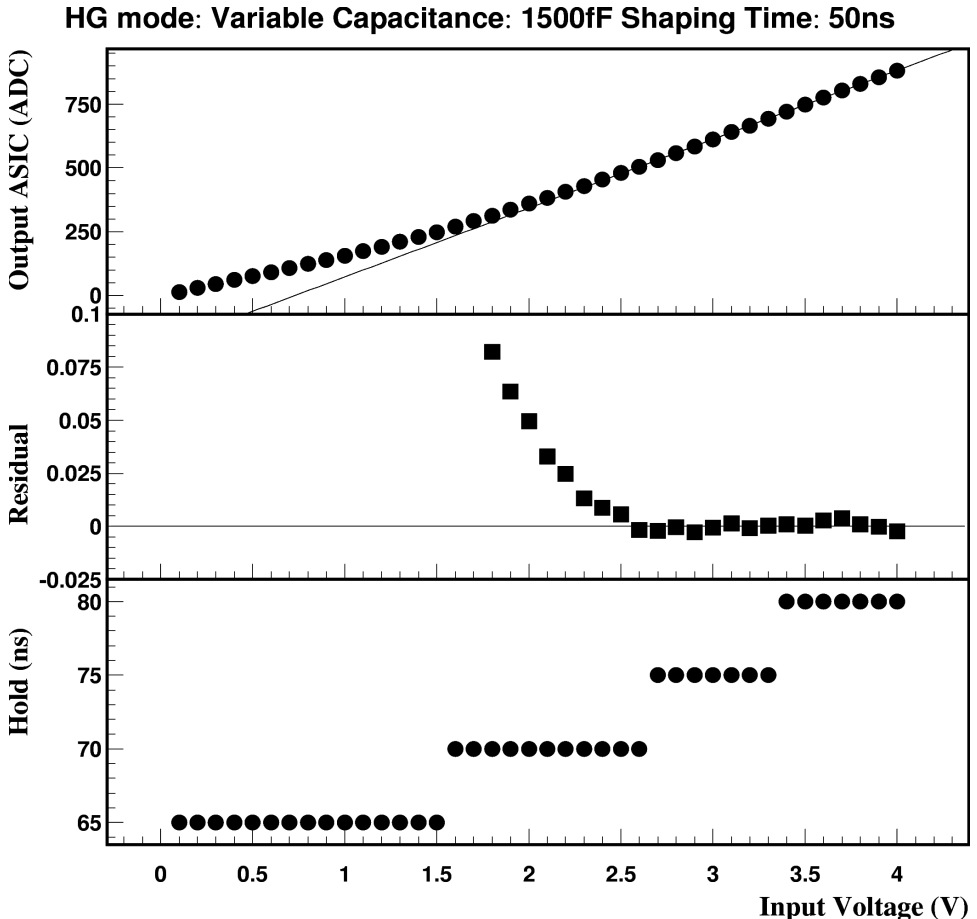


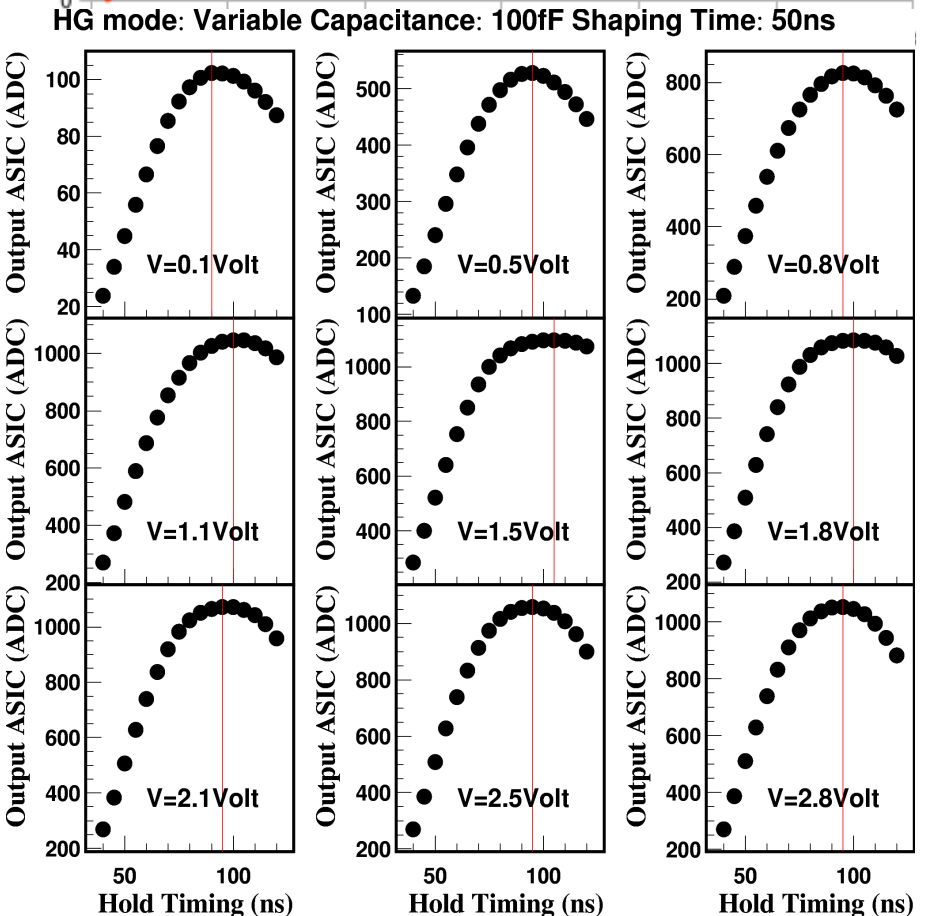


- swing 4.5V
  tune SiPM voltage
- residual :+/-2%
- consistent with Orsay measurements

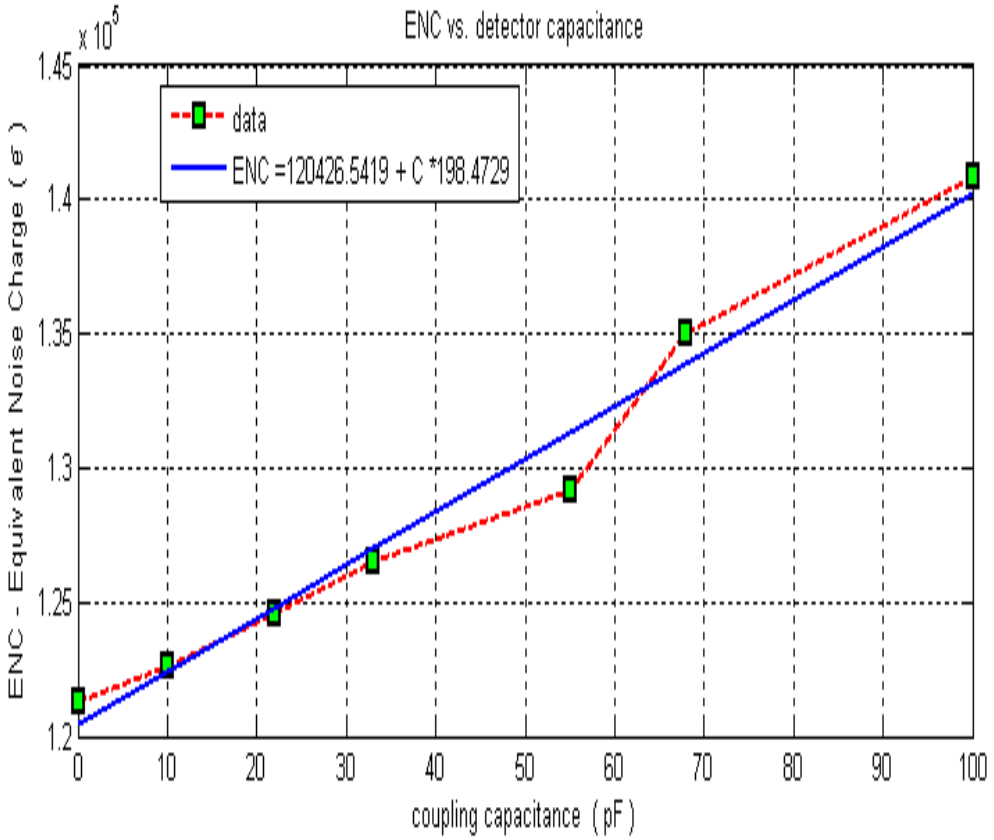
linearity and peaking time







equivalent noise charge vs. detector capacitance

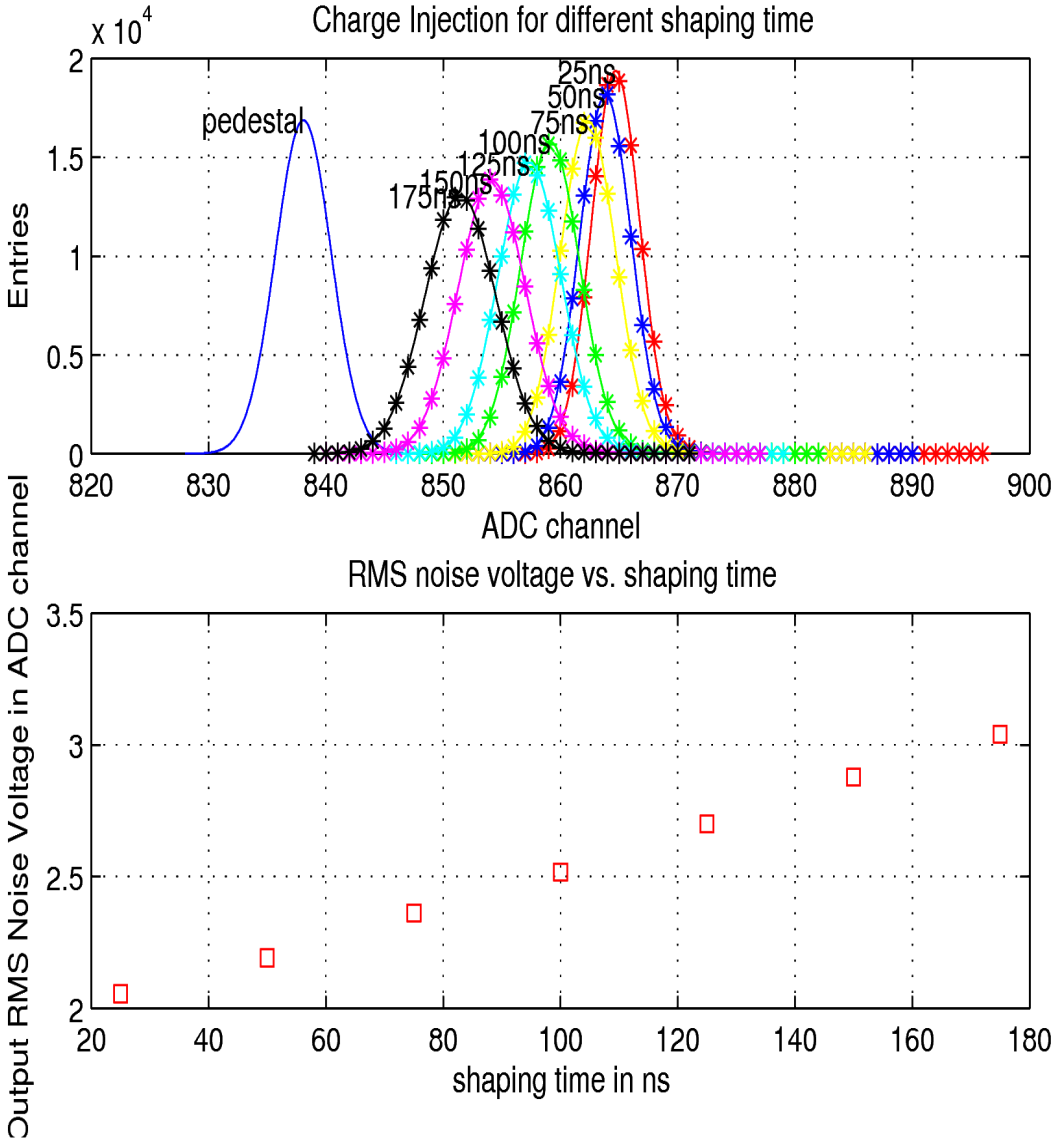


1.3 *10^5 electrons @

SiPM cap. ~ 50pF

Sg/N ~ 3.8 @

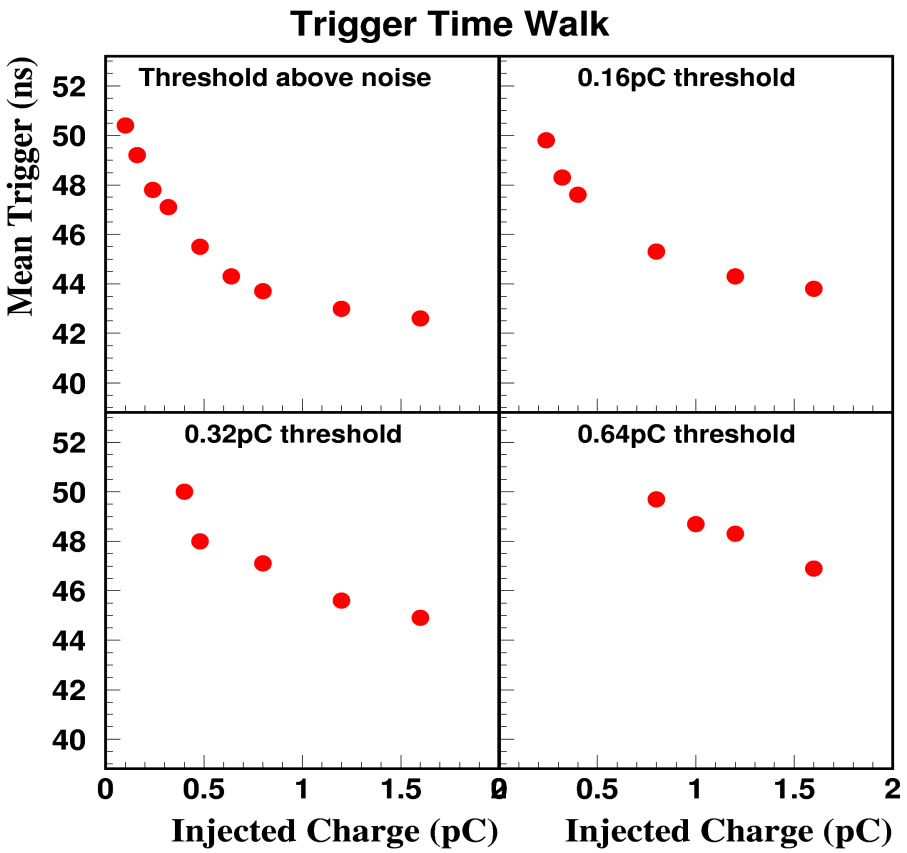
SiPM Gain 0.5*10^6

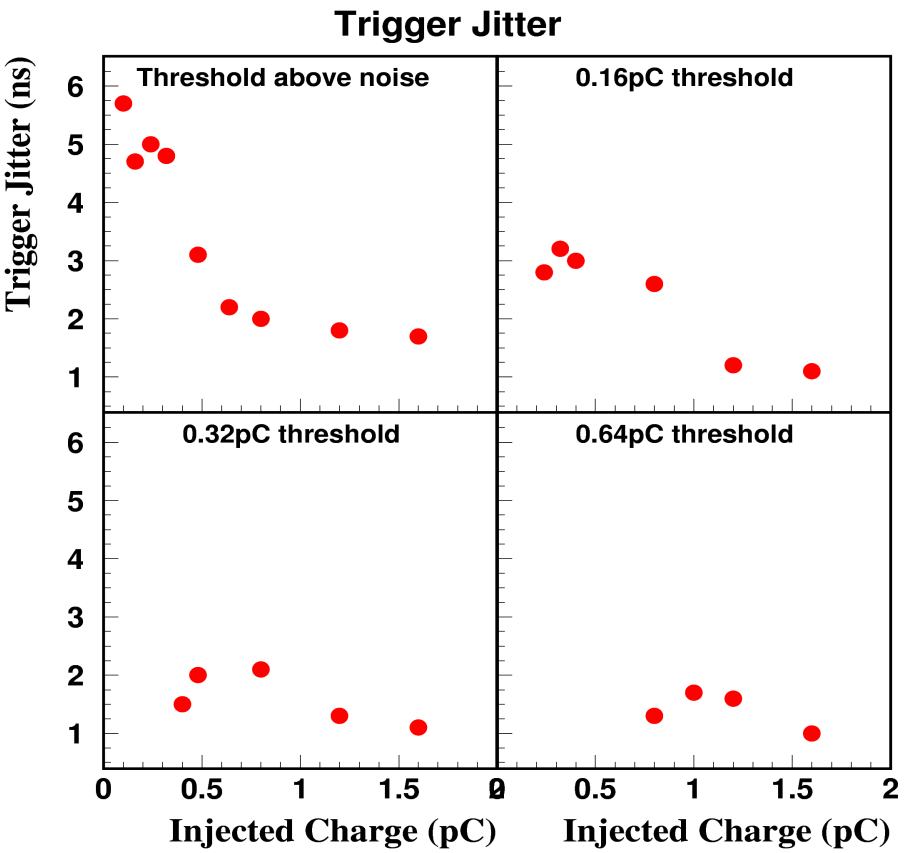


noise increase
with shaping time

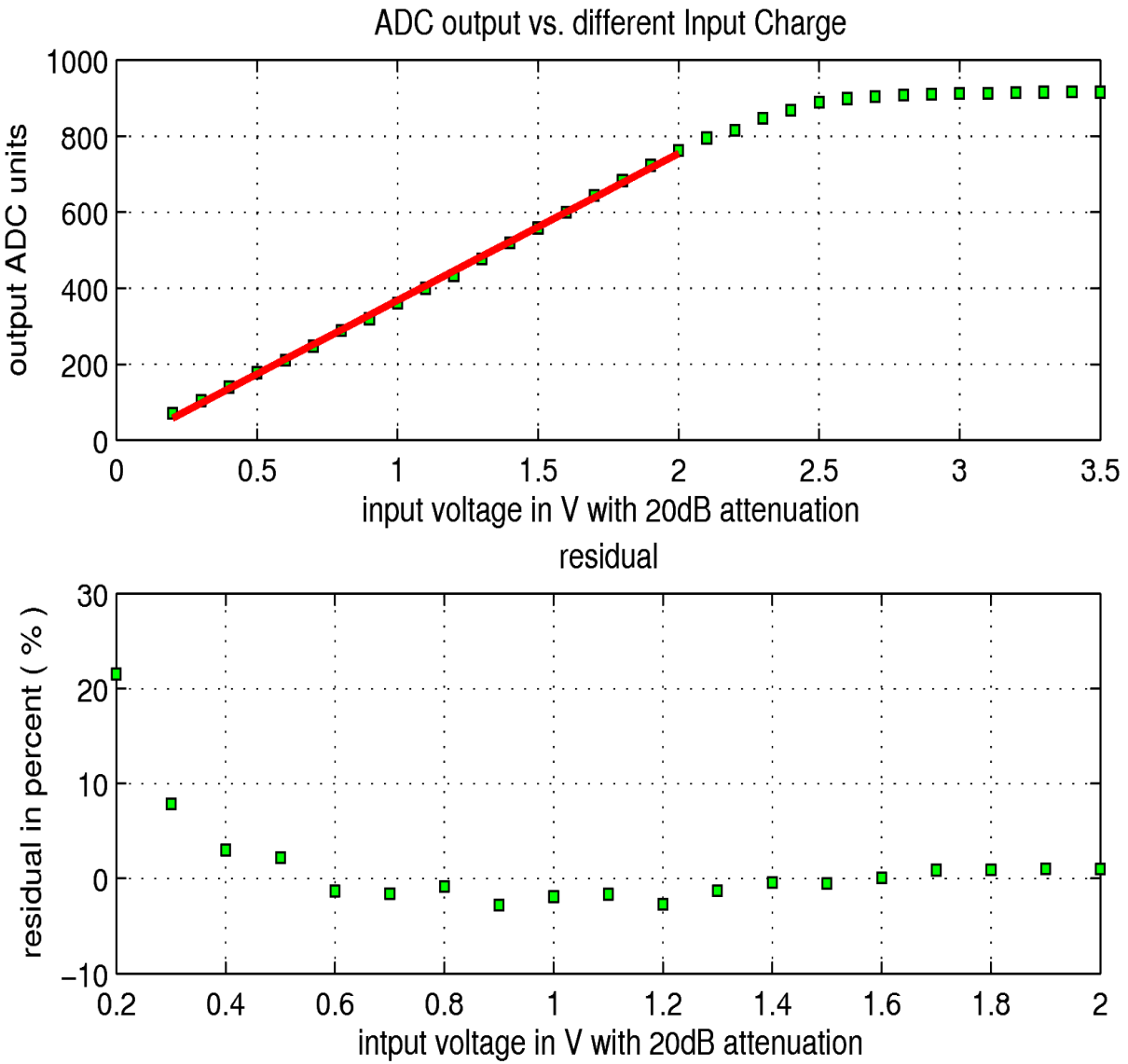
low frequency noise

time walk and jitter

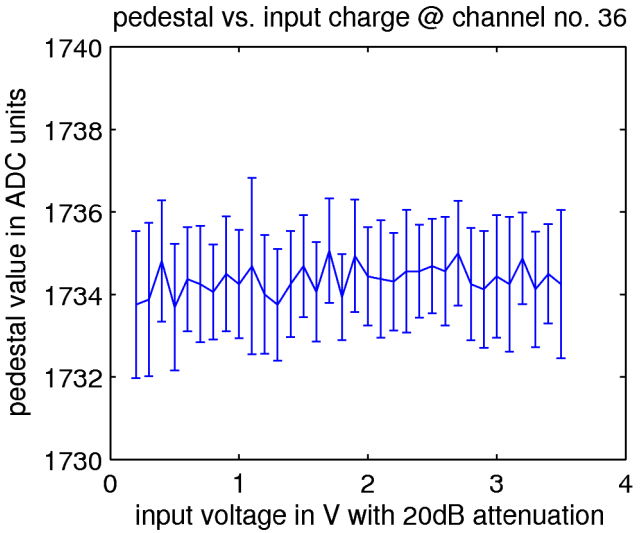


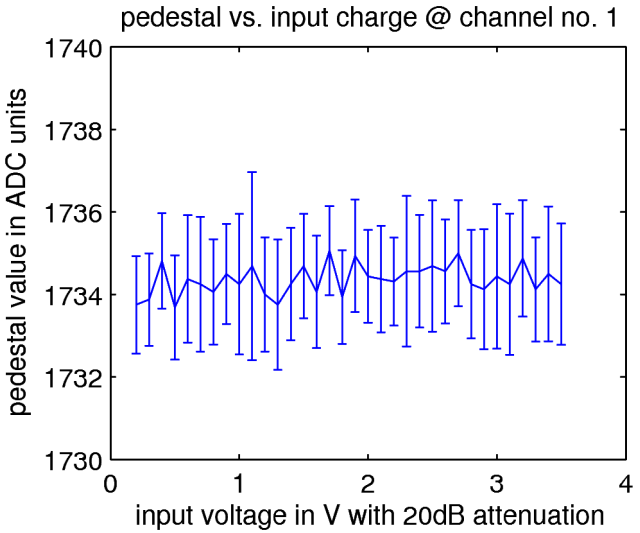


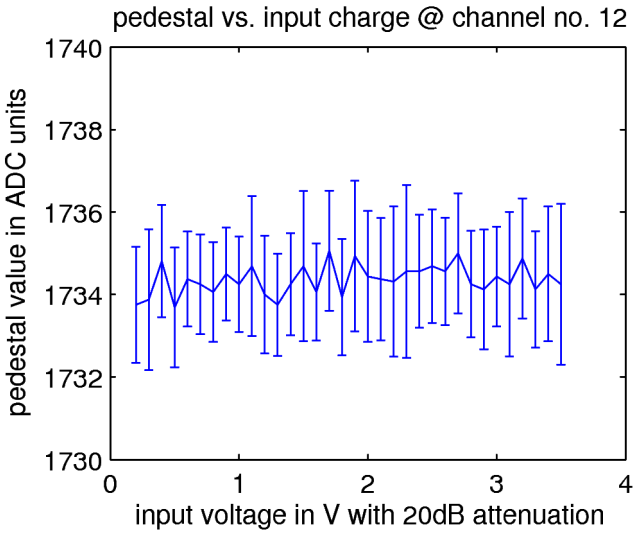
Wilkinson ADC testing

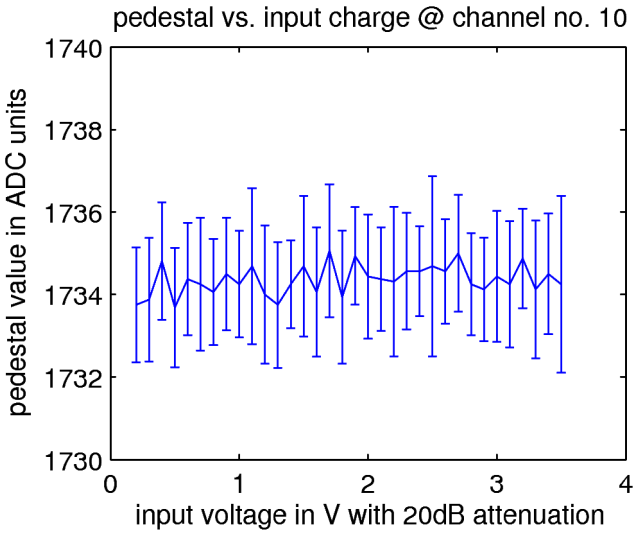


pedestal uniformity

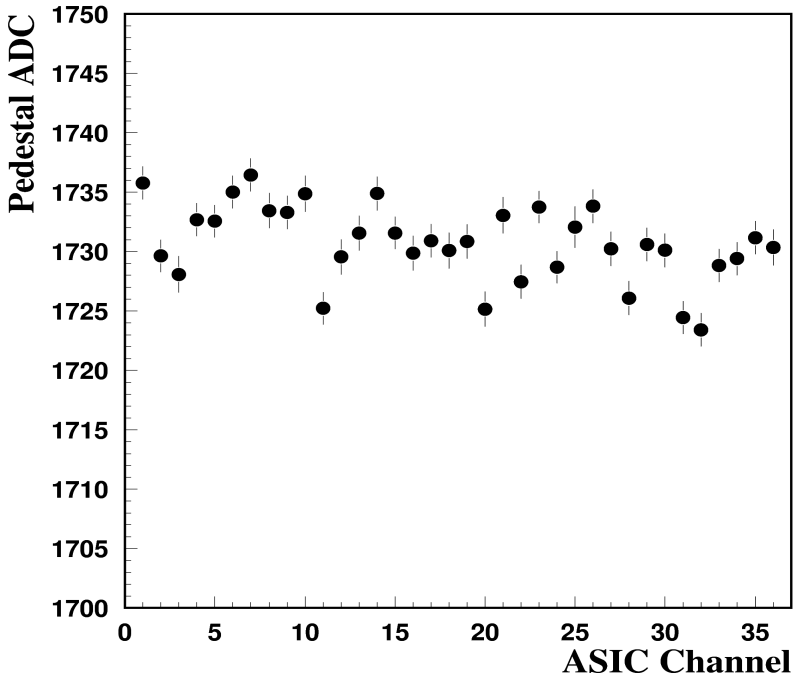


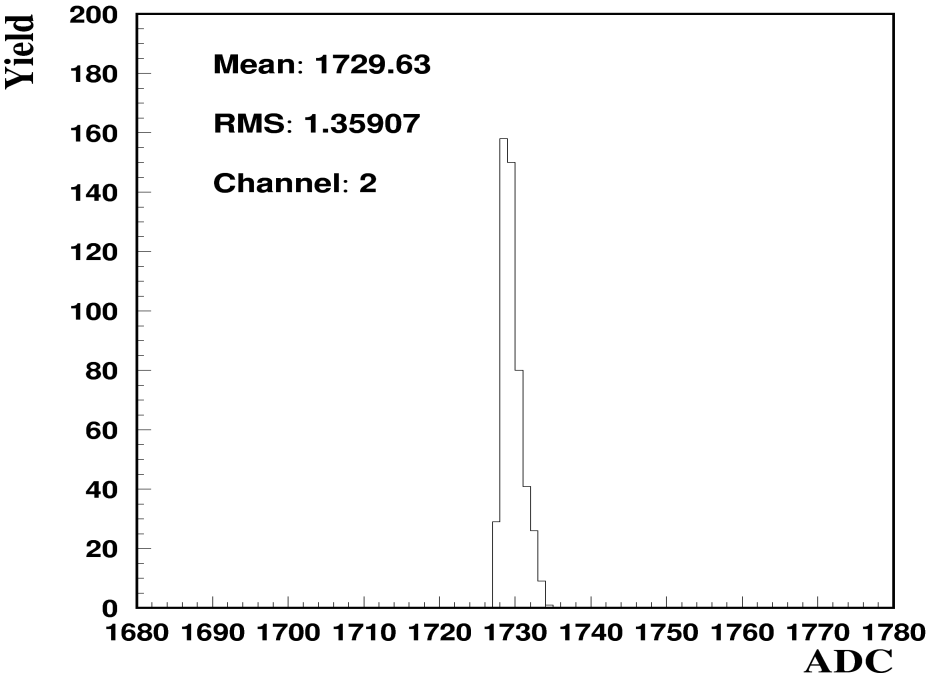




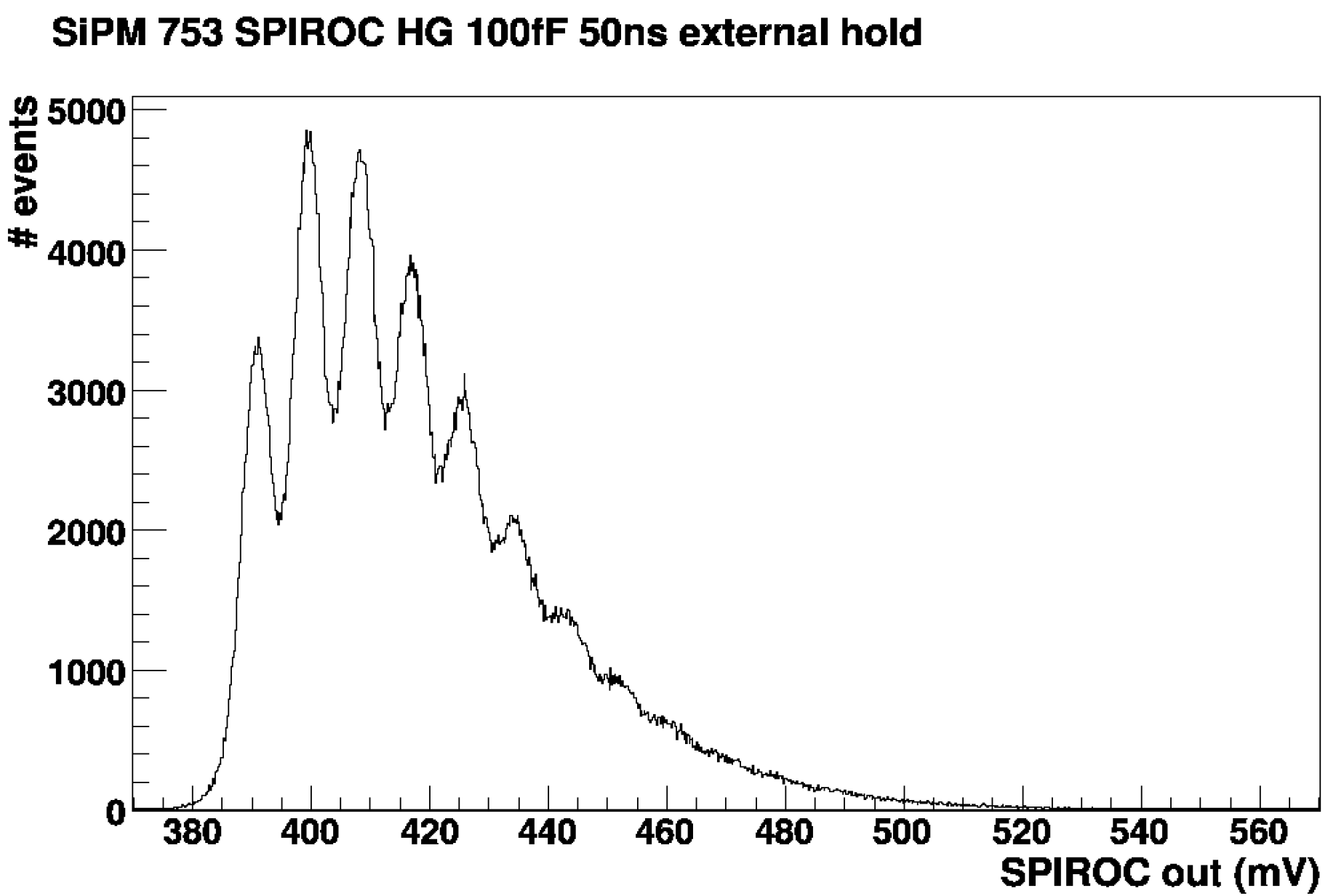


pedestal distributions of all the channels

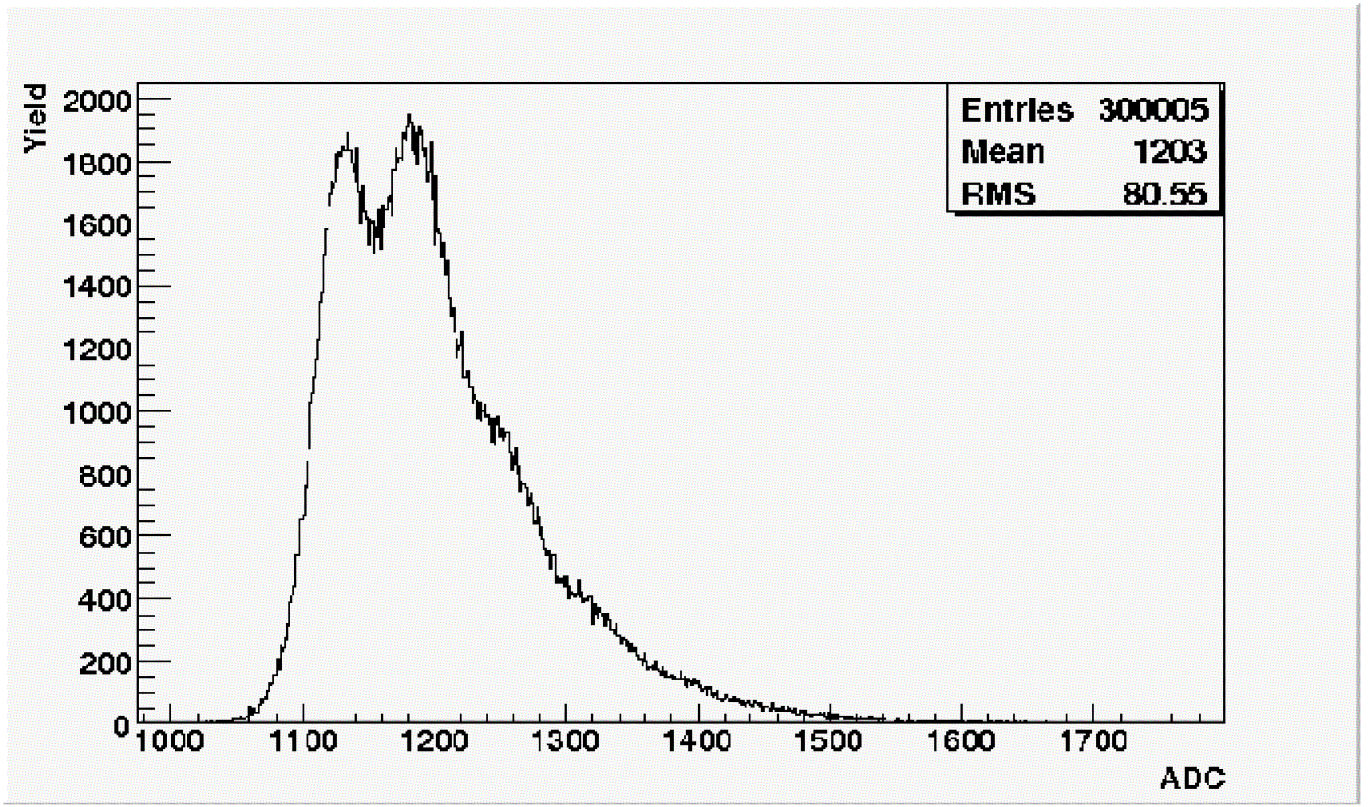




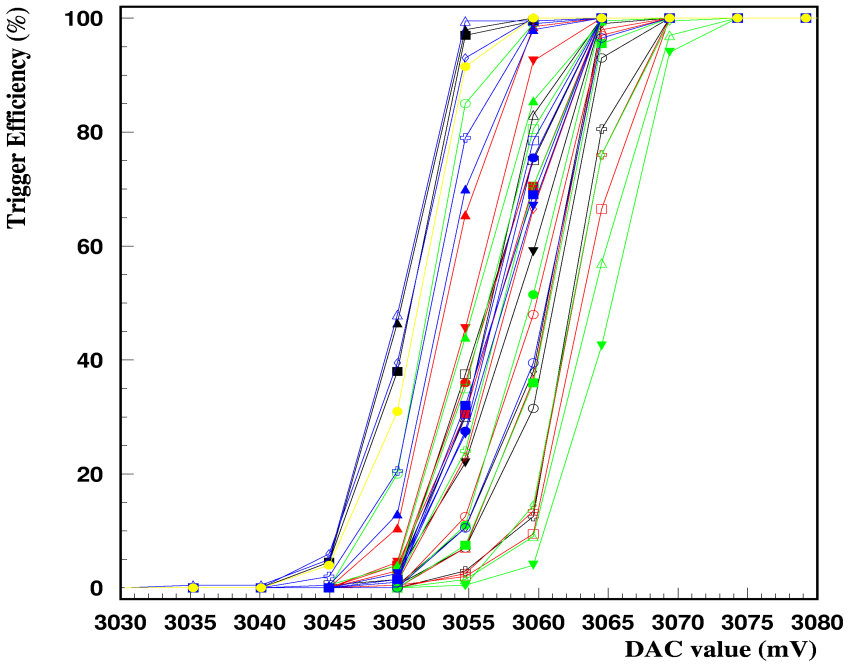
RMS ~ 3.09 ADC

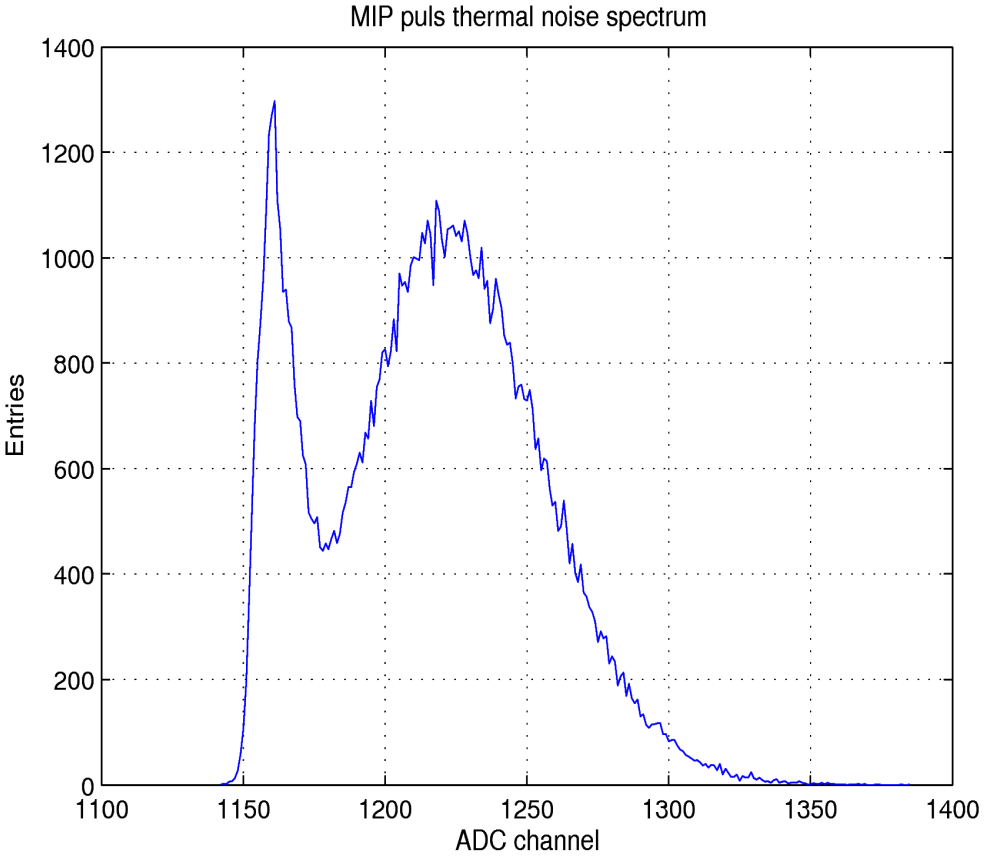

SiPM 753 SPIROC HG 100fF 50ns external hold
events
5000
4000
3000
2000
1000
0
380
400
420
440
460
480
500
520
540
560
SPIROC out (mV)

thermal noise spectrum



S-Curve and thermal noise + MIP signal

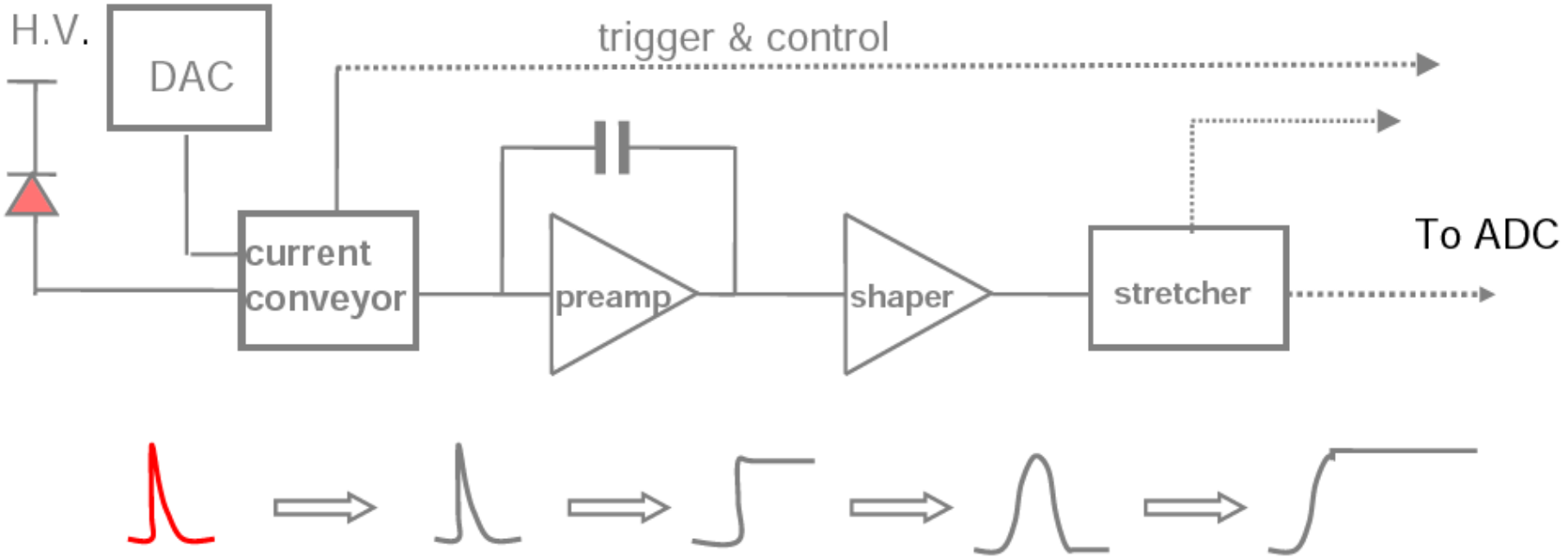




outlook

1. internal delay -> spectrum
2. TAC : resolution , input signal synchronization
3. power pulsing
4. multi-channel test

single channel architecture



input DAC : gain tuning

current conveyor : fast rising edge and large dynamic range

CSA : high signal to noise ratio

different shaping time : avoid pile up

AMS 0.35um CMOS technology

current conveyor

DAC disconnected to signal line

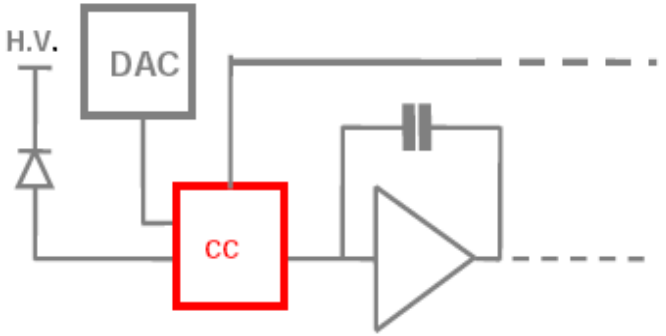
→ avoid disturbance

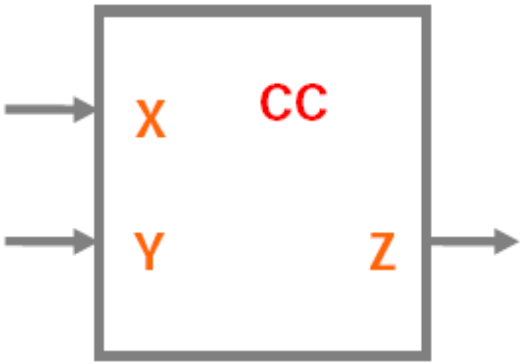
input impedance tunable ~1/gm

→ fast timing

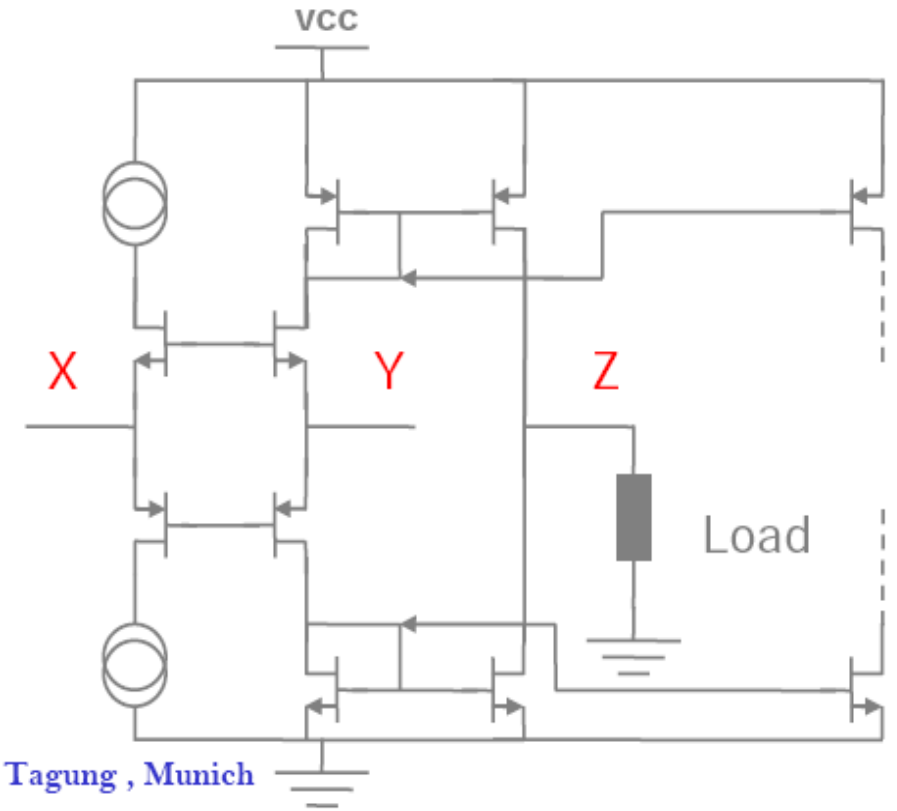
mirror for fast triggering

→ processing capability





$V_Y=V_X$ $I_Z=I_Y$ $I_X=0$

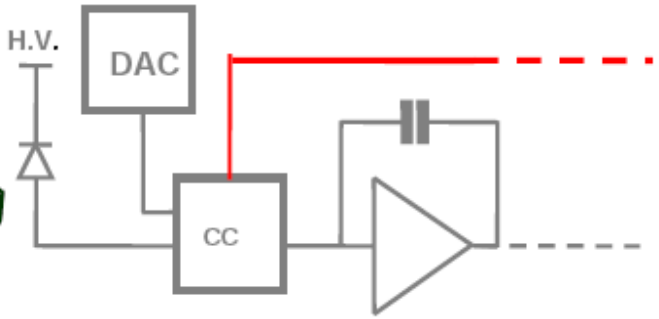


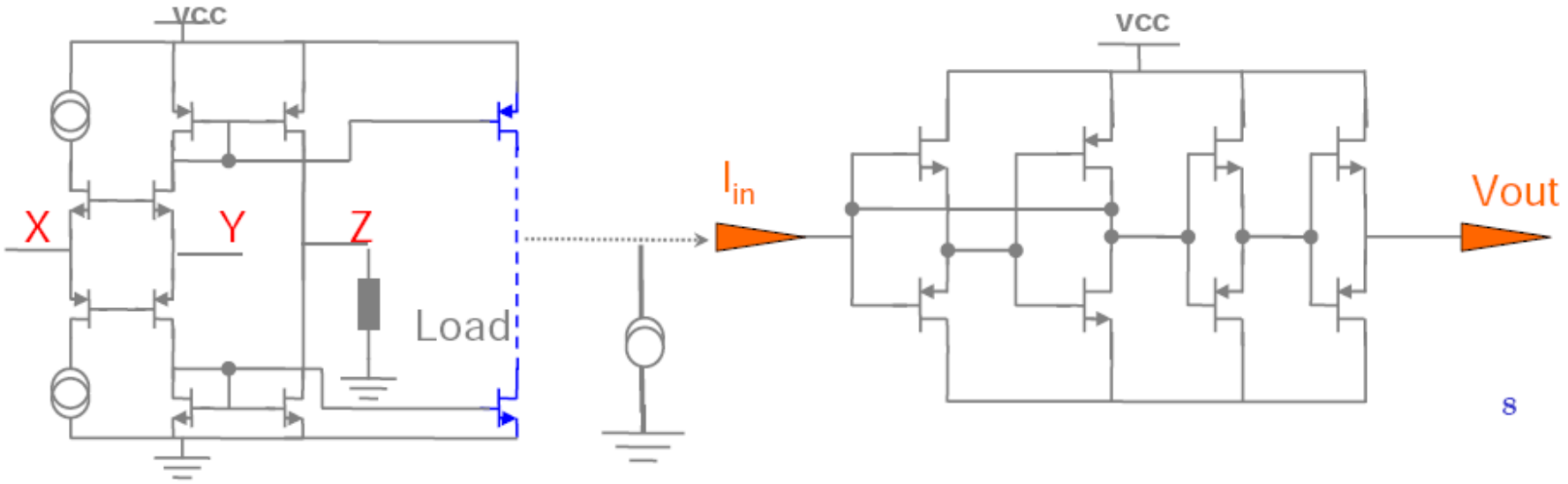
current comparator

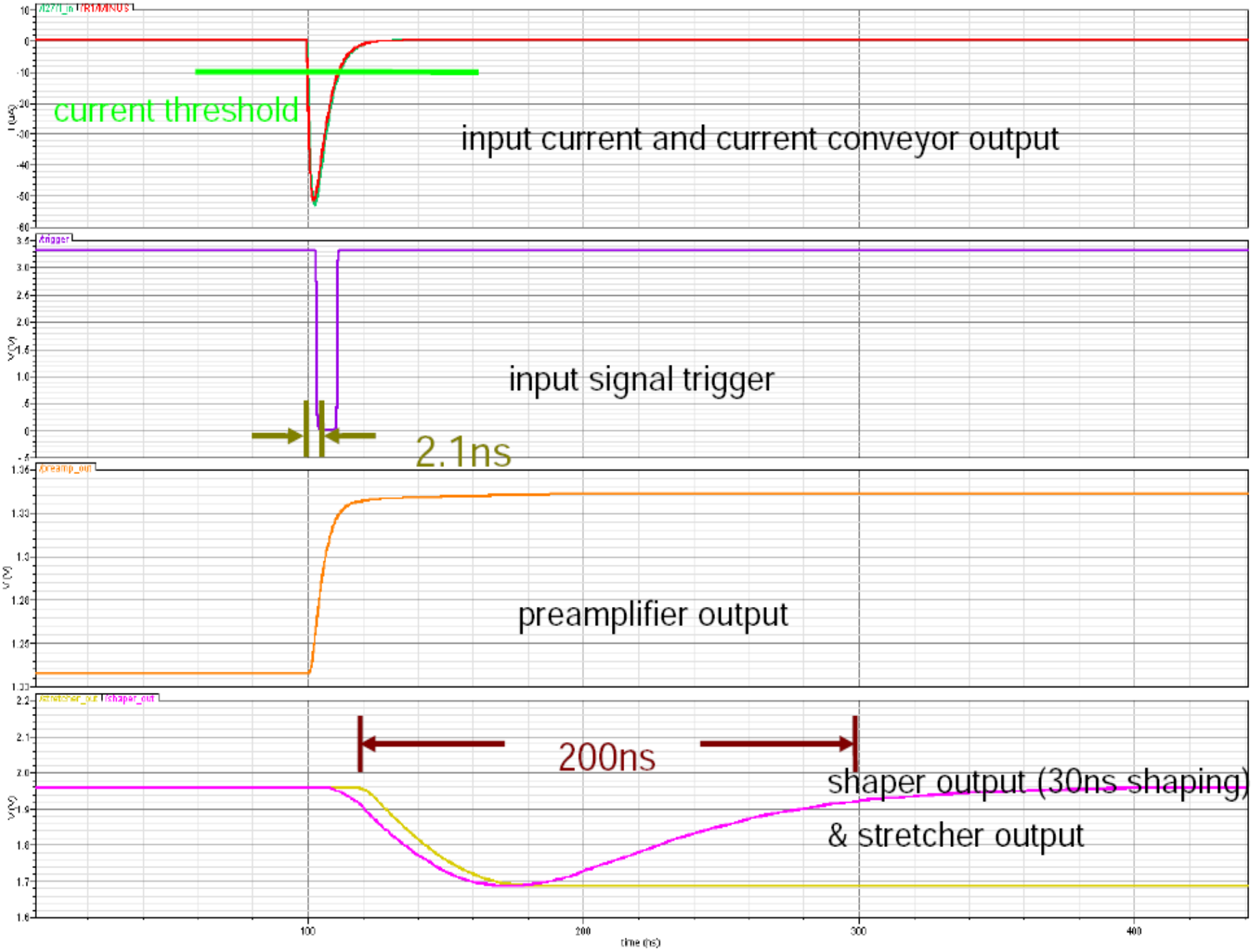
- class B output stage & 3 inverter
  Latched output , low dc offset,
- low power consumption
- ~2 ns delay with leading edge triggering

TTL logic output

•different threshold can be set for triggering (standby current) ~50uA for calorimeter application






current threshold
input current and current conveyor output
input signal trigger
2.1ns
preamplifier output
200ns
shaper output (30ns shaping)
& stretcher output
time (ns)

SUMMARY

- Analog channel designed for silicon photomultiplier
- High S/N ratio (>10 for single pixel w.r.t. 80fC charge)
- Narrow output to avoid pile up (20ns - 200ns)
- Fast trigger information (2ns delay for input current triggering)
- low power consumption : 6 mW
- dynamic range : ~120pC