Status of the DHCAL 1m2 GRPC Acquisition
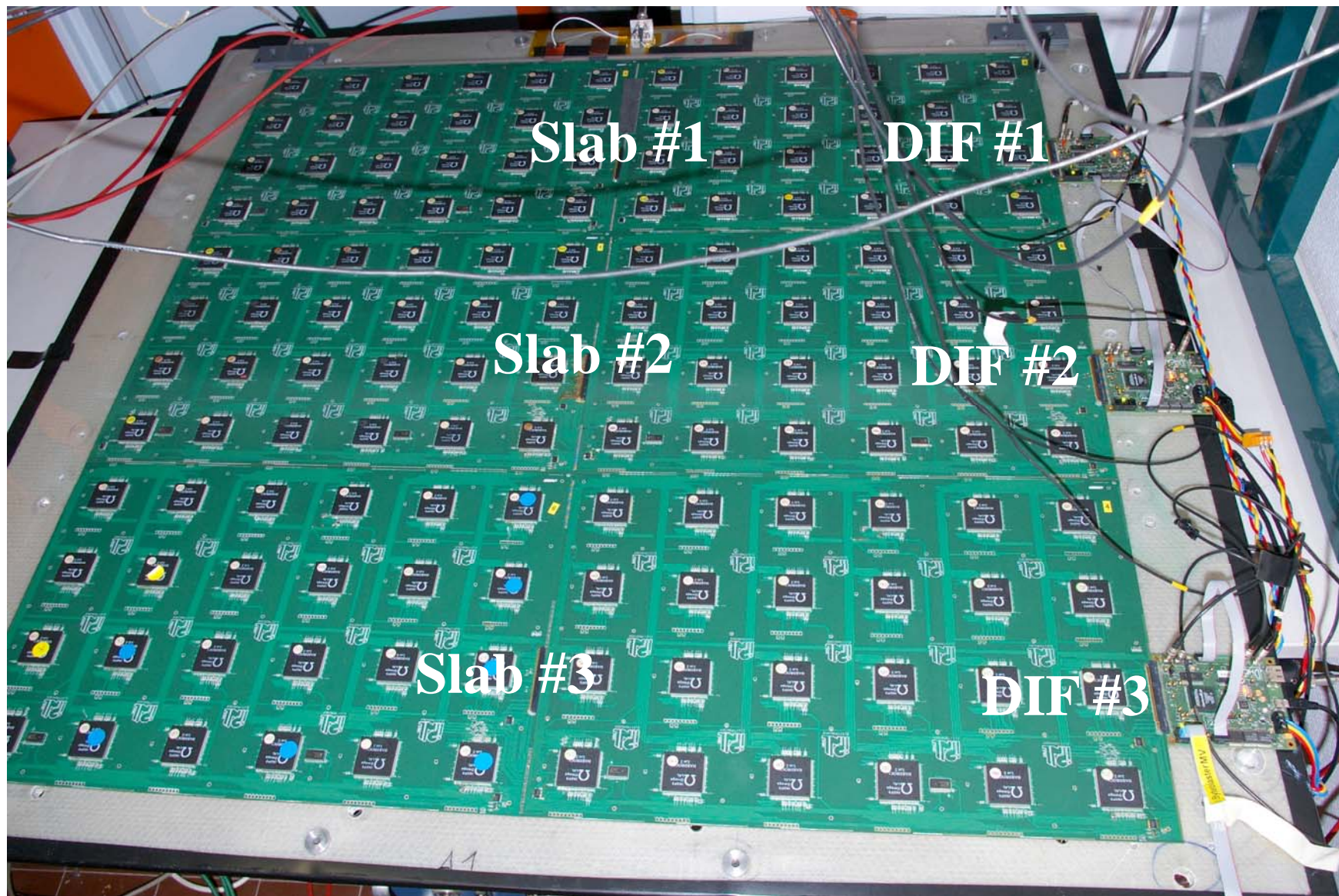
C. Combaret

IPNL

Status on march 31st

- Setup with :

    - Detector : 1m2 GRPC
    - Electronics : 3 IPNL slabs (48 Hardrocs v1), made with 2 single slabs (24 Hardrocs v1 each)
    - 1 DAQ PC (Dell Poweredge 2950) running SL5
    - 1 windows PC for user interface (mostly for convinience and to run Quartus)
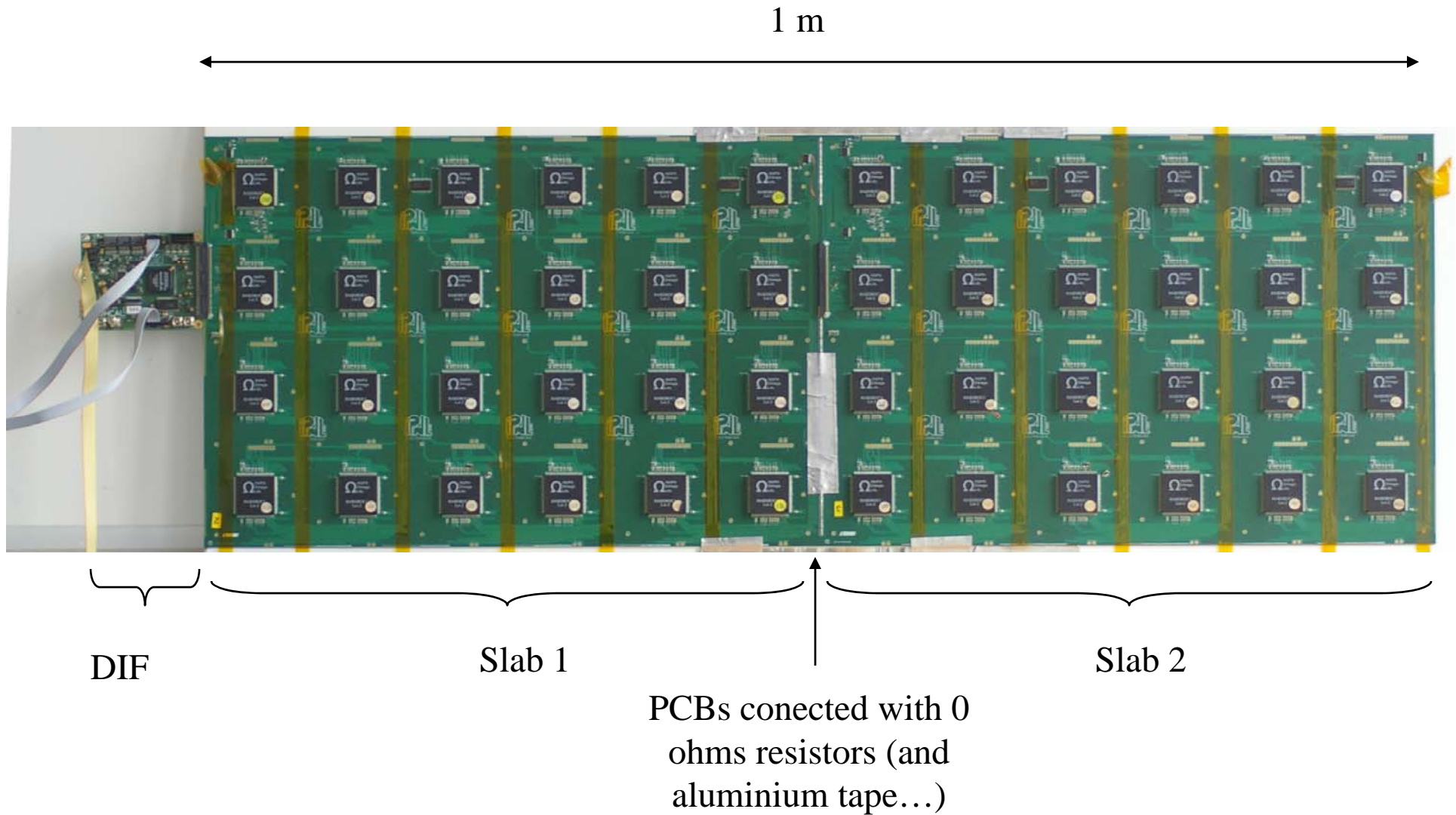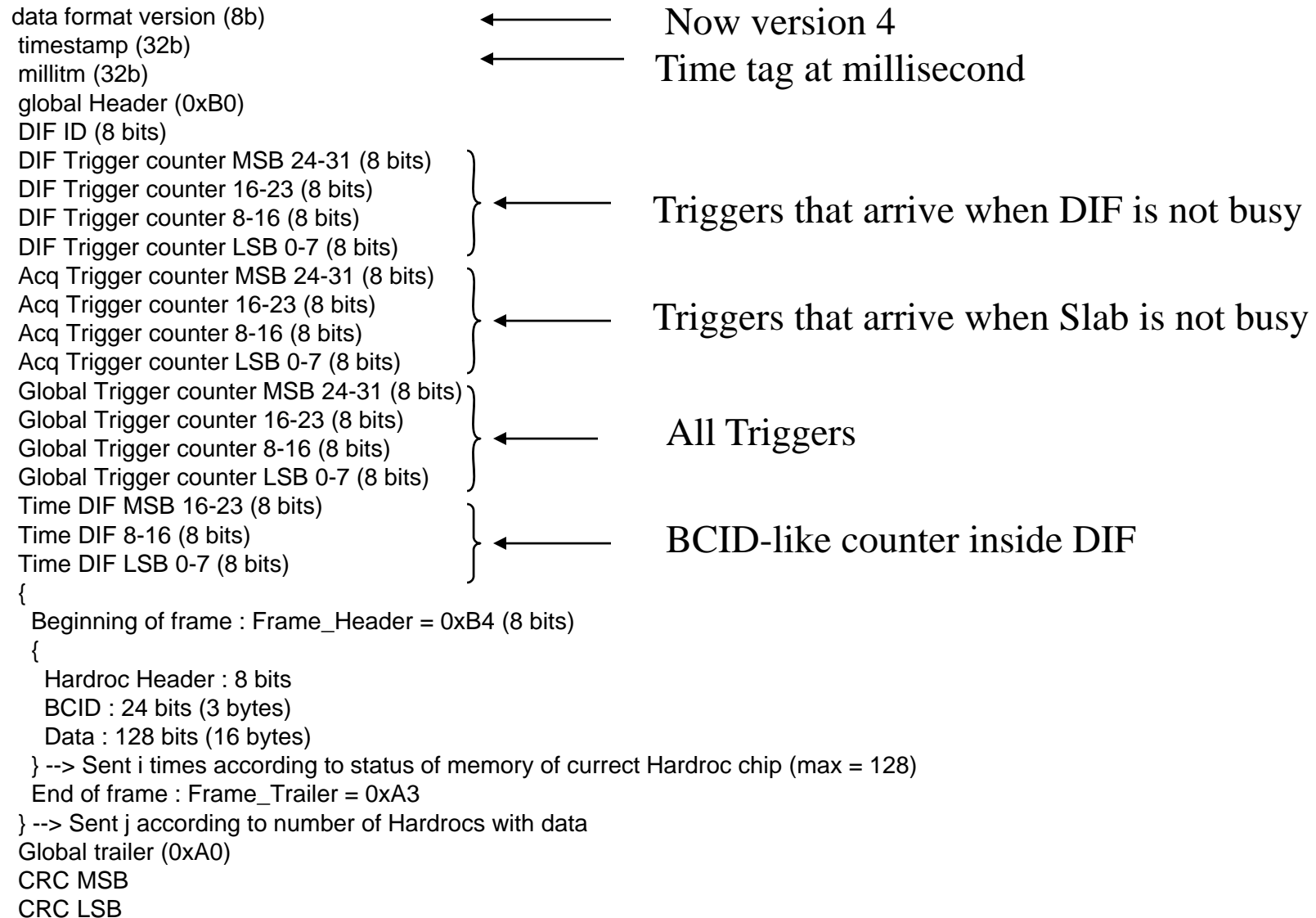   - XDAQ software running on the DAQ PC

Slab #1   DIF #1

Slab #2   DIF #2

Slab #3   DIF #3

1 m

DIF

Slab 1

PCBs conected with 0
ohms resistors (and
aluminium tape…)

Slab 2

data format version (8b) ←———————— Now version 4
timestamp (32b) ——————————→
millitm (32b) ←———————— Time tag at millisecond
global Header (0xB0)
DIF ID (8 bits)
DIF Trigger counter MSB 24-31 (8 bits) ⎫
DIF Trigger counter 16-23 (8 bits) ⎪
DIF Trigger counter 8-16 (8 bits) ⎬ ←———————— Triggers that arrive when DIF is not busy
DIF Trigger counter LSB 0-7 (8 bits) ⎭
Acq Trigger counter MSB 24-31 (8 bits) ⎫
Acq Trigger counter 16-23 (8 bits) ⎪
Acq Trigger counter 8-16 (8 bits) ⎬ ←———————— Triggers that arrive when Slab is not busy
Acq Trigger counter LSB 0-7 (8 bits) ⎭
Global Trigger counter MSB 24-31 (8 bits) ⎫
Global Trigger counter 16-23 (8 bits) ⎪
Global Trigger counter 8-16 (8 bits) ⎬ ←———————— All Triggers
Global Trigger counter LSB 0-7 (8 bits) ⎭
Time DIF MSB 16-23 (8 bits) ⎫
Time DIF 8-16 (8 bits) ⎬ ←———————— BCID-like counter inside DIF
Time DIF LSB 0-7 (8 bits) ⎭
{
  Beginning of frame : Frame_Header = 0xB4 (8 bits)
  {
    Hardroc Header : 8 bits
    BCID : 24 bits (3 bytes)
    Data : 128 bits (16 bytes)
  } --> Sent i times according to status of memory of currect Hardroc chip (max = 128)
  End of frame : Frame_Trailer = 0xA3
} --> Sent j according to number of Hardrocs with data
Global trailer (0xA0)
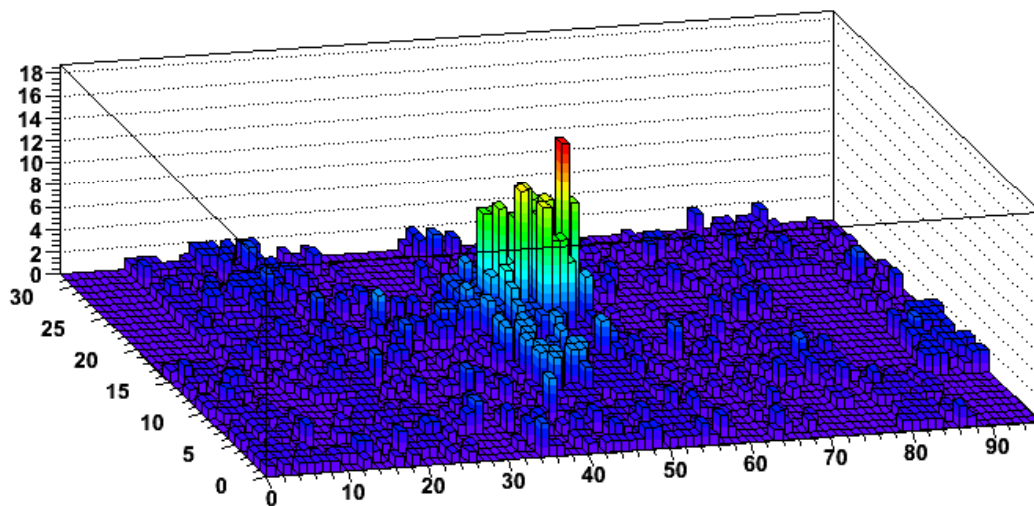CRC MSB
CRC LSB

A run taken one 1slab

Board2D
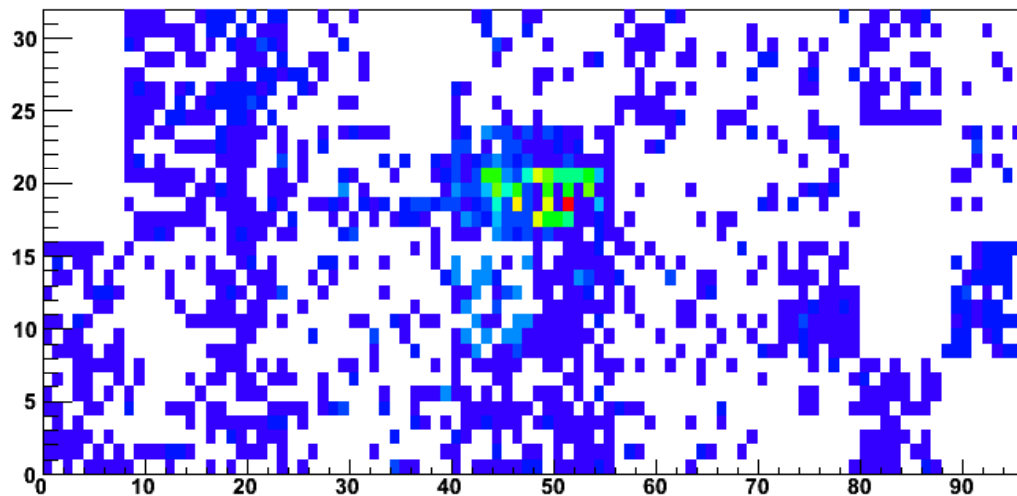
Board2D

Data taken for 1 slab
with a small PM as
cosmic trigger
Limitation on 1 slab is
due to the fact that we
only have small PMs for
cosmic trigger

Status on march 31st : where are we?

Xdaq Software with Hardroc asics is functional :

Stable (tested over few hours)

DIF with one 48 Hardroc PCB is fully functional (Slow control, digital readout)

3 DIFs (for 1 m2) used in parallel with Xdaq

Calibration package (to record S-curves) is (almost) working

Need a few VHDL lines from Guillaume to synchronize Slabs when a ramfull occurs (Thursday?…)

Need to test, test and test before june beam test…