Laboratoire d'Annecy-le-Vieux
de Physique des Particules

Status of DHCAL first level DAQ Electronics

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Electronic/DAQ Calice meeting at DESY

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IN2P3
INSTITUT NATIONAL DE PHYSIQUE NUCLÉAIRE ET DE PHYSIQUE DES PARTICULES

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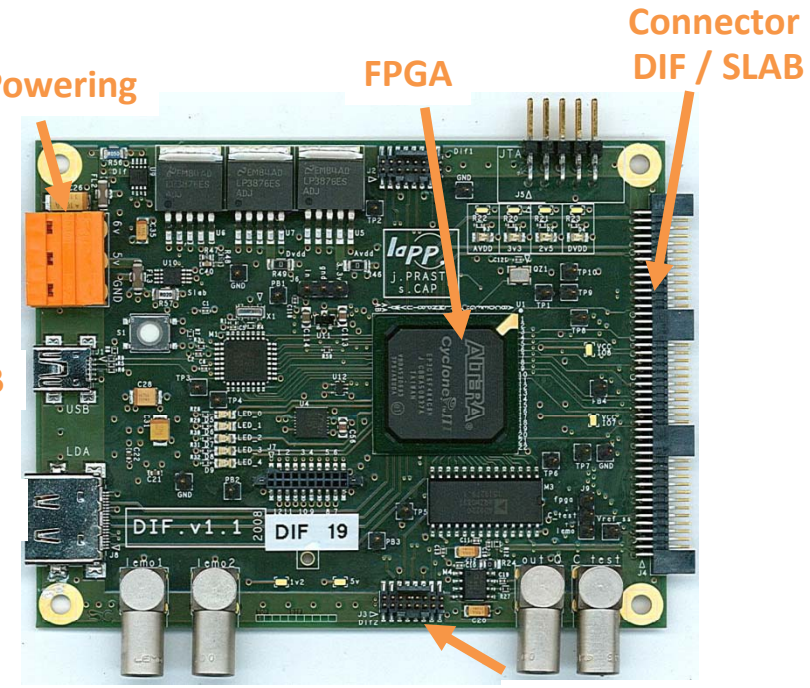
Summary

- **DIF (Detector InterFace)**
  - Cap Sébastien, Prast Julie, Vouters Guillaume.
- **MiICROMEGAS and RPC ASU (Active Sensor Unit) with HARDROC 1/2 or DIRAC**
  - Dalmaz Alexandre, Drancourt Cyril for MICROMEGAS ASU
- **Past Beam Test**
  - LAPP MICROMEGAS beam test
  - IPNL RPC beam test
- **On Going works**
- **Next for MICROMEGAS**

DIF (Digital InterFace)

DIF board :

- Independent board to have more flexibility
- It provides the communication with HARDROCs or DIRACs
- It allows ASICs configuration and performs analog and digital readout
- Also compatible with SPIROC and SKYROC (ECAL and AHCAL)
- Two DAQs :
  - Through USB : Cross DAQ
  - Through HDMI : Calice DAQ
- This DIF (with XDAQ software) is the first level DAQ electronics for RPC and MICROMEGAS test beams.

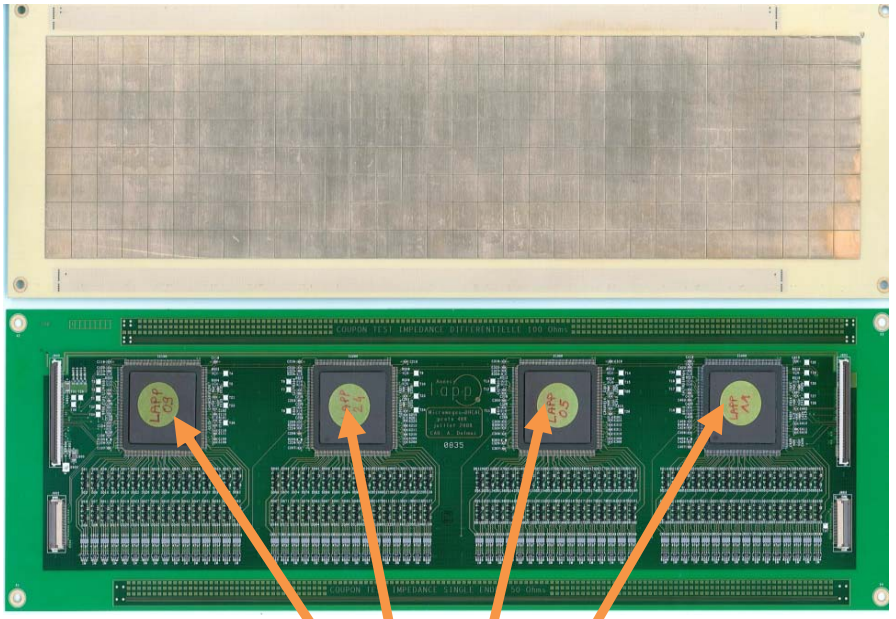


ASU for MicroMEGAS

ASU board with HARDROC 1 (8x32cm², 1cm² pad)

- 8 layers with careful routing to avoid crosstalk
- Sparks protections included

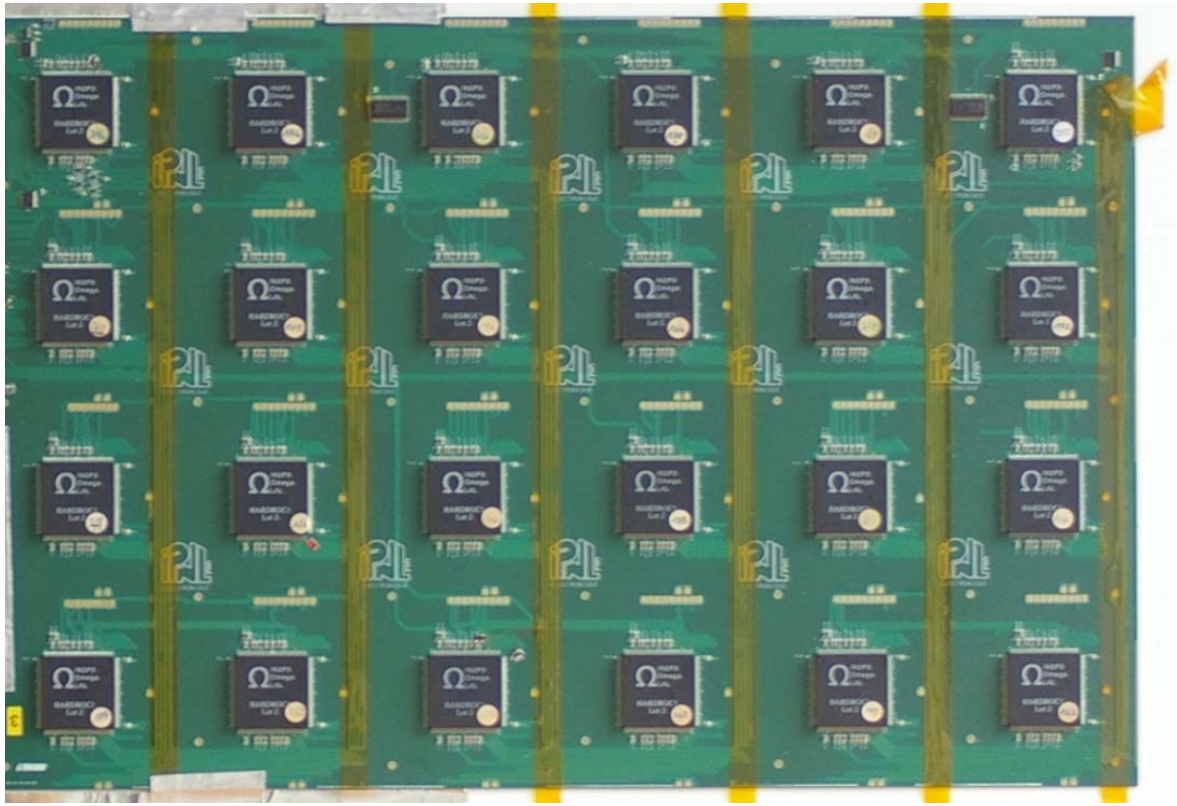
- HARDROC 1 (16 mm²)
  - Analog and digital readout
  - 64 channels
  - 2 thresholds in 10 bit precision
  - Digital memory for 128 events
  - Dynamic Range – 10 fC to 1 pC
  - Low consumption < 10µW/channel



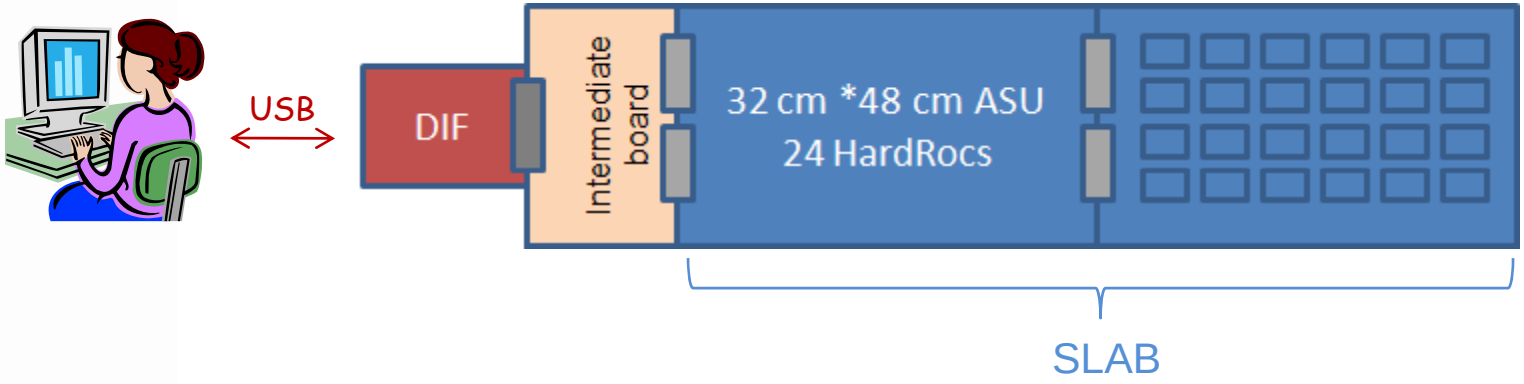
4 HARDROC for 8x32 pads

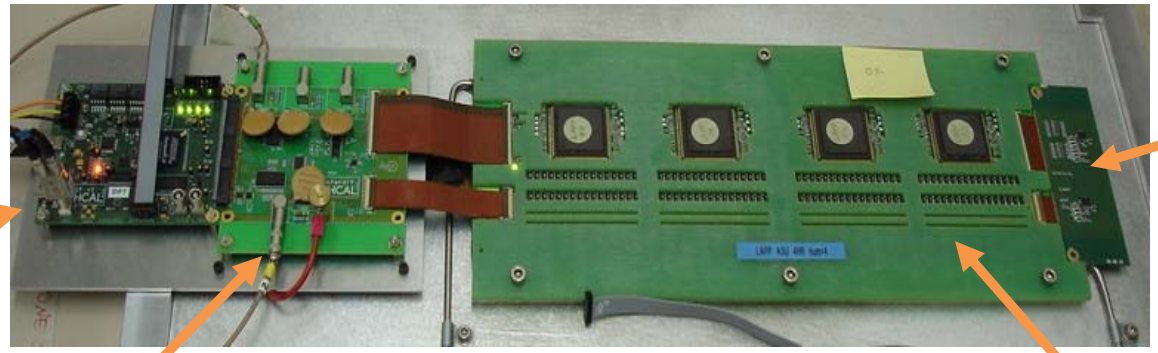
ASU for RPC

ASU board with HARDROC 1 (48x32cm², 1cm² pad)



The DHCAL Architecture





The DHCAL Architecture

DIF

Slab 1

Preliminary Tests at LAPP

First tests with DIF

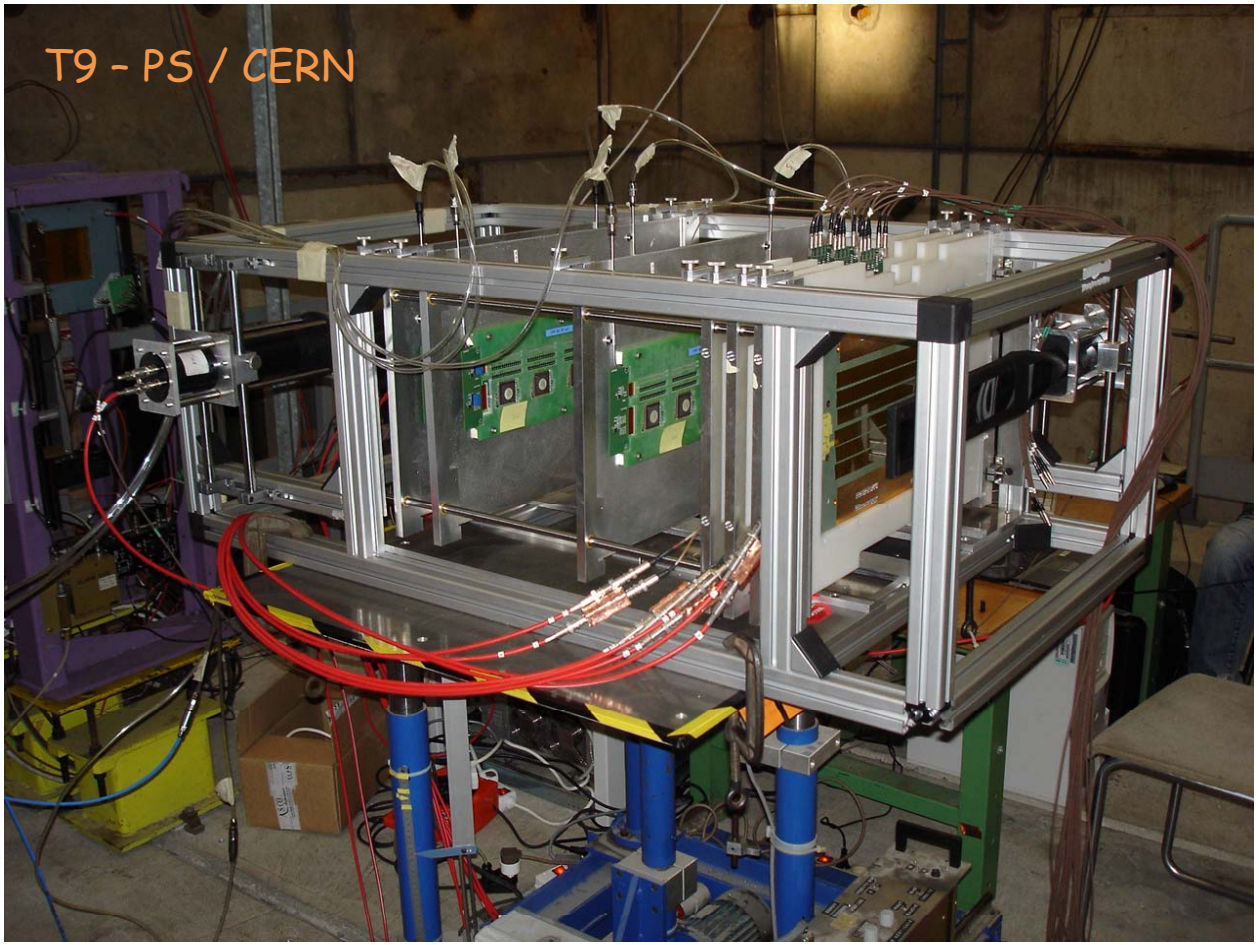
- All DIF are fully operationnal
- Command and register acces : ok
- Monitoring : ok
- Calibration of HARDROCs : on going

First tests with ASU

- 2 ASUs are fully fonctionnal
- 1 ASU : ASIC configuration doesn't work
- 1 ASU had a dysfunctionnal HARDROC
- 3 ASUs brought for the beam test

ASU was ready to test less than one month before the start of the Beam Test. We had less than one month to make electronics ready for the Beam test.

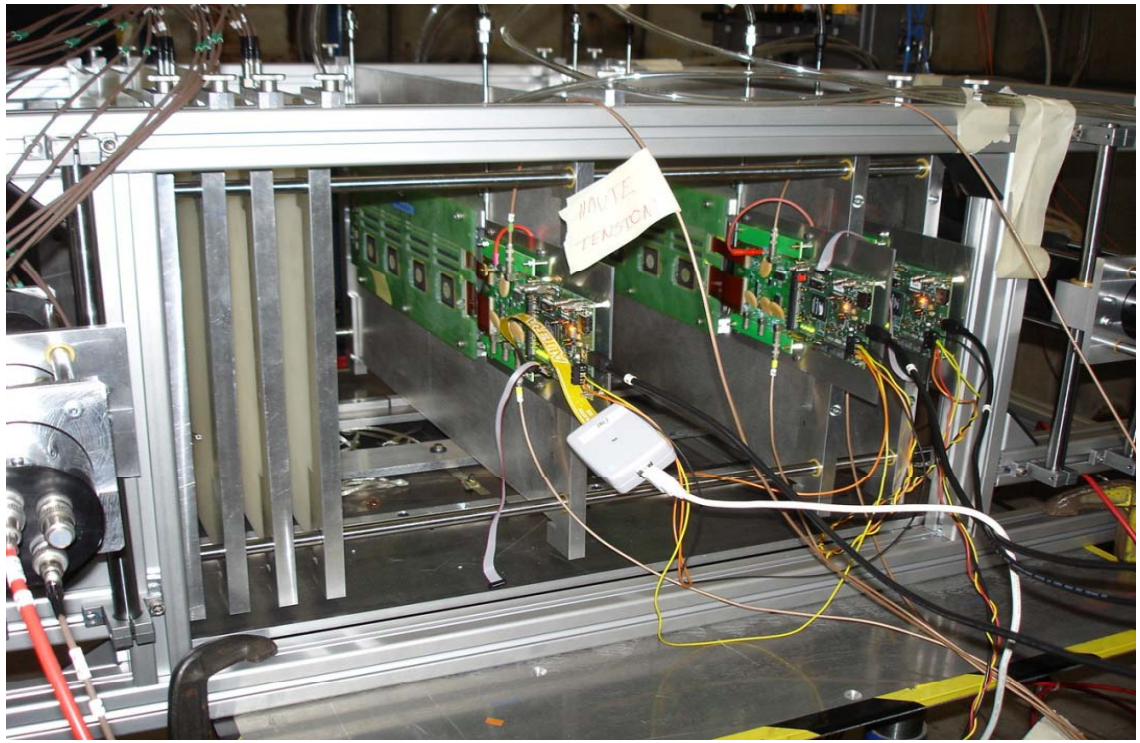
2008 November Beam Test



Installation

Setup with

- 3 (ASU+DIF) connected to the DAQ through a USB hub (MICROMEGAS)
- 1 ASU connected to the DAQ through a USB (RPC)



Results

Configuration of ASICs (Slow Control)

- Tested with all HARDROC
- Checked by controling DAC values and the DIF firmware

→ Stable and reliable

(tested also with 24 HARDROCs from the IPNL ASU)

Synchronisation of the 3 DIFs

- Synchronization of 5MHz clock and reset BCID
- Synchronization of the start of digital readout for several DIF

→ Stable and reliable

→ First time that several (DIF+ASU) were synchronized !!

Results

Digital Readout

- Tested with the manual and trig_ext/trig_int mode
- Tested with the automatic and trig_ext /trig_int mode
- Tested with the Beam Test mode

→ Stable and reliable

(tested also with 24 HARDROCs from the IPNL ASU)

Beam test mode

- Start Acquisition
- HARDROC data memorisation
- Erasing memory if there is a full HARDROC memory
- Read out if there is a particle (trigger)

Analog Readout

- Not tested yet

Data taken

The DIF developed features worked with all ASU but mesh high voltage was only stable on one ASU…

… so beam data were taken only with one ASU.

Data analysis is on going (LAPP/LLR) !

Data format

<Format version = 2>
<Timestamp>
<Header global numérique>
<ID DIF>
<Counter trigger>
<Counter particule>
<Header data HARDROC1> <data HARDROC1> <Trailer data HARDROC1>
<Header data HARDROC2> <data HARDROC2> <Trailer data HARDROC2>
...
<Header data HARDROCn> <data HARDROCn> <Trailer data HARDROCn>
<Trailer global numérique>
<CRC>

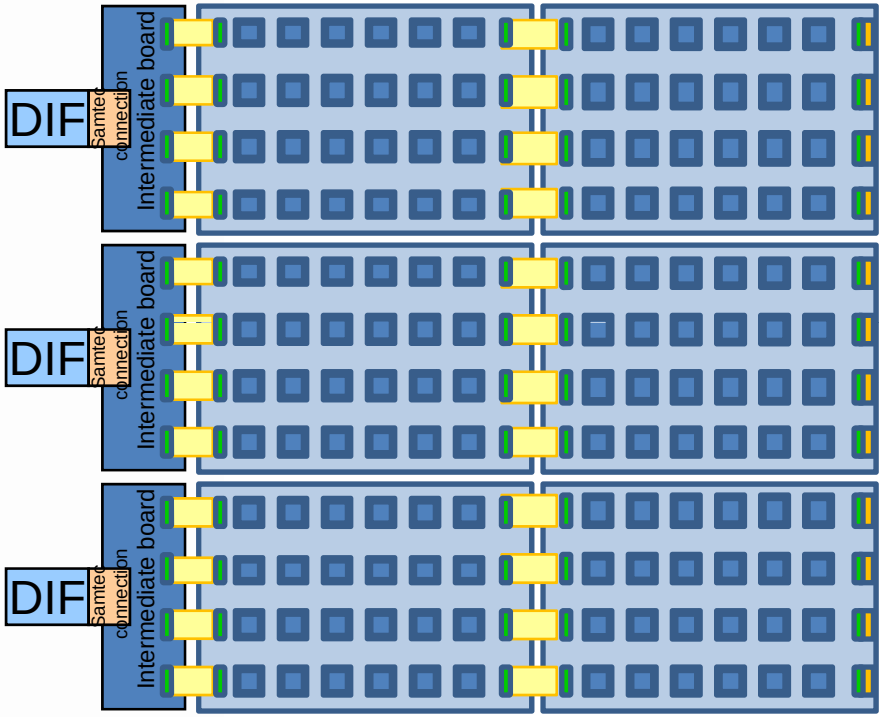
Currently Data format

<Format version = 3>
<Timestamp>
<Header global numérique>
<ID DIF>
<Trigger Counter>
<Particle Counter (only during acquisition)>
<Particle Counter>
<Timedif> (BCID like in the FPGA)
<Header data HARDROC1> <data HARDROC1> <Trailer data HARDROC1>
<Header data HARDROC2> <data HARDROC2> <Trailer data HARDROC2>
...
<Header data HARDROCn> <data HARDROCn> <Trailer data HARDROCn>
<Trailer global numérique>
<CRC>

On going works

- **MicroMEGAS Square meter and DIF VHDL code with Hardroc 2**
  - Cap Sébastien, Dalmaz Alexandre, Drancourt Cyril, Prast Julie, Vouters Guillaume. Christophe Combaret (XDAQ)
- **DIF VHDL code for DIRAC 2**
  - Gaglione Renaud, Prast Julie, Vouters Guillaume, Christophe Combaret (XDAQ)
- **DIF VHDL code for Calice DAQ**
  - Prast Julie, Vouters Guillaume

MicroMEGAS Square meter



m² status:

- 10 new DIFs produced
- New Inter-DIF : design on going
- New ASUs with HARDROC 2 are in production and will be ready on the half of April

DIF status:

- The VHDL code has been updated to HARDROC 2

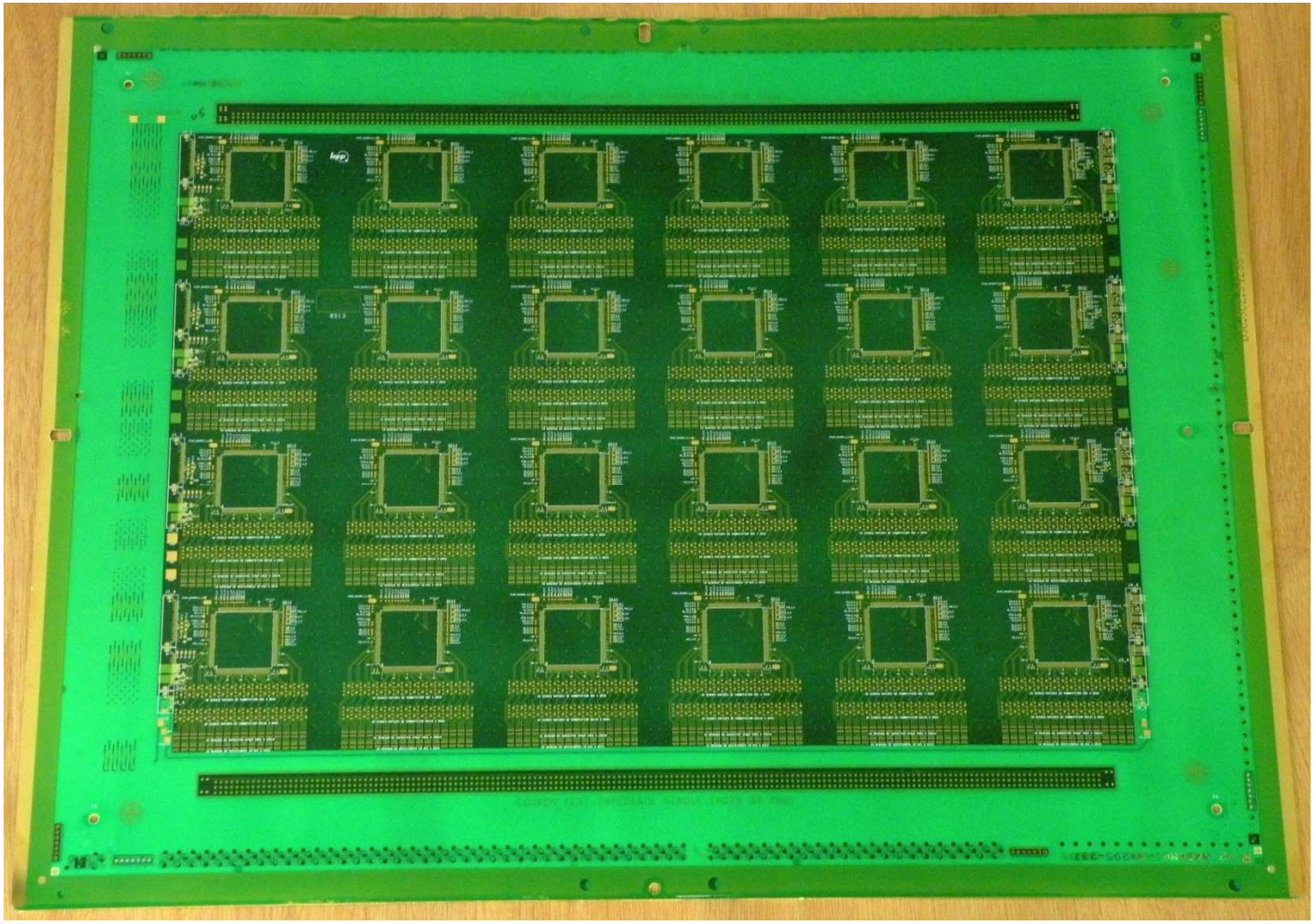
: Flat Printed Circuit

: ASIC chip (64 channels)

: Hirose connector

: Terminaison board

MicroMEGAS Square meter



RPC Square meter

- 8 PCB of 50X33.3 cm^2 were conceived and produced
- 8-layer, class 6 (buried vias)
- 6 were equipped with hardroc1 (plastic packaging)→ 144 ASICs
- PCB are connected 2 by 2 using zero resistor

DIF

Slab 1

Slab 2

DIRAC 2

DIRAC 2 status

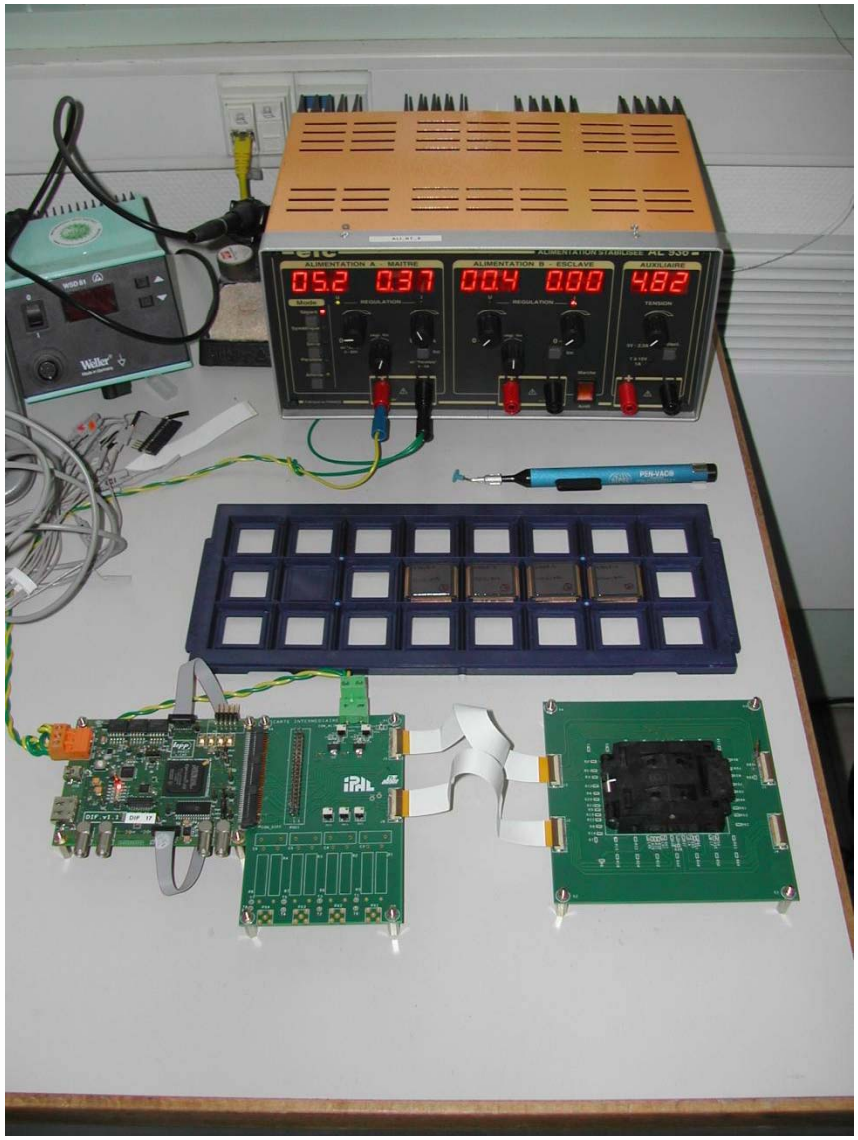
- DIRAC 2 ASICs and IPNL test board have been produced and are now available to be tested.

- Tests
  - → test of Firmware and Software
  - → test of Dirac 2 features
  - → Characterization of ASICs
  - → …

- If everything is ok, next step : 24 Dirac 2 ASU for MicroMEGAS

DIF Status

- The VHDL code is developed and we will test it soon.



DIRAC 2

CALICE DAQ

A protocol between the LDA and the DIF has been done by the DIF Task Force

- The Calice DAQ use the HDMI connector
- The document take into account AHCAL, ECAL and DHCAL project.
- DAQ chain : ODR, LDA, DCC and DIF boards

- Baseline for the DAQ (usb used only for test and debug)

Next for MICROMEGAS

- **Beam Test in May**
  We expect to take lot of data with 8x32 ASUs (HR 1).
  2 News 8x32 ASUs have been produced.

- **Beam Test in August**
  We expect to be ready to test 32x48 ASUs (HR 2)
  We expect to take data with DIRAC 2 ASUs

- **Beam Test in September**
  Test of m^2 MICROMEGAS

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Thank You

For Your Attention !

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