A 12-bit low-power ADC for SKIROC

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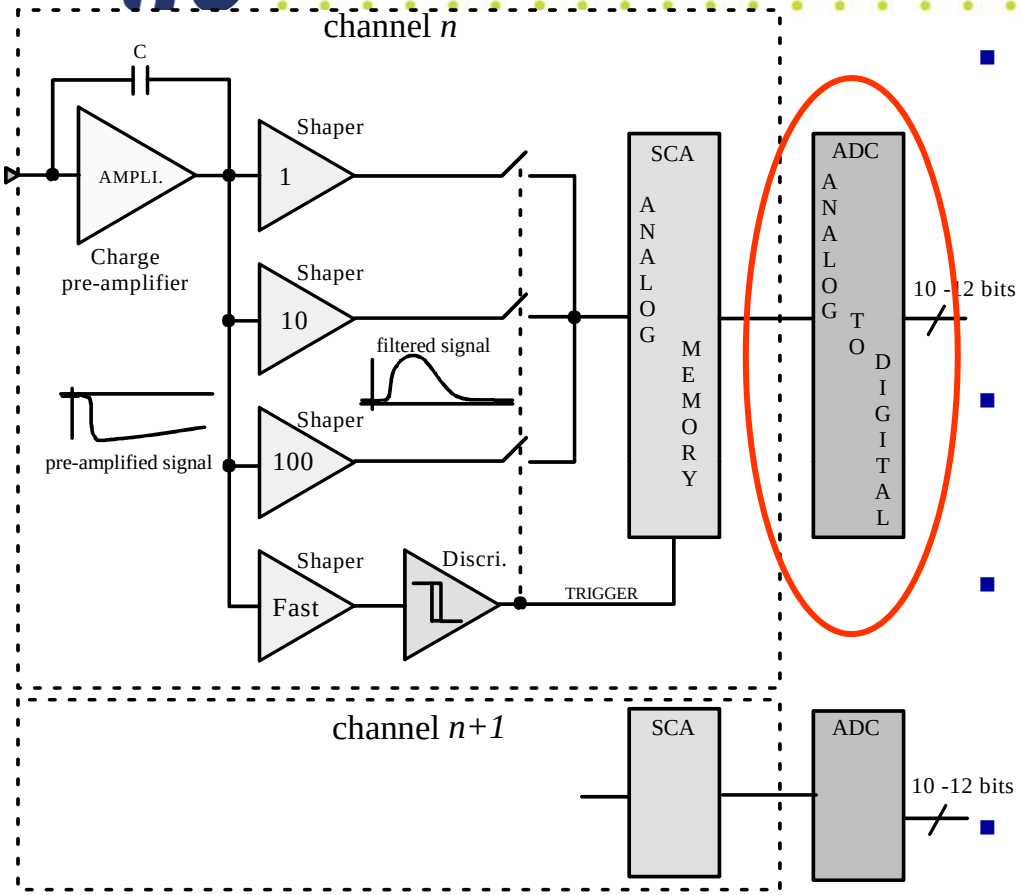
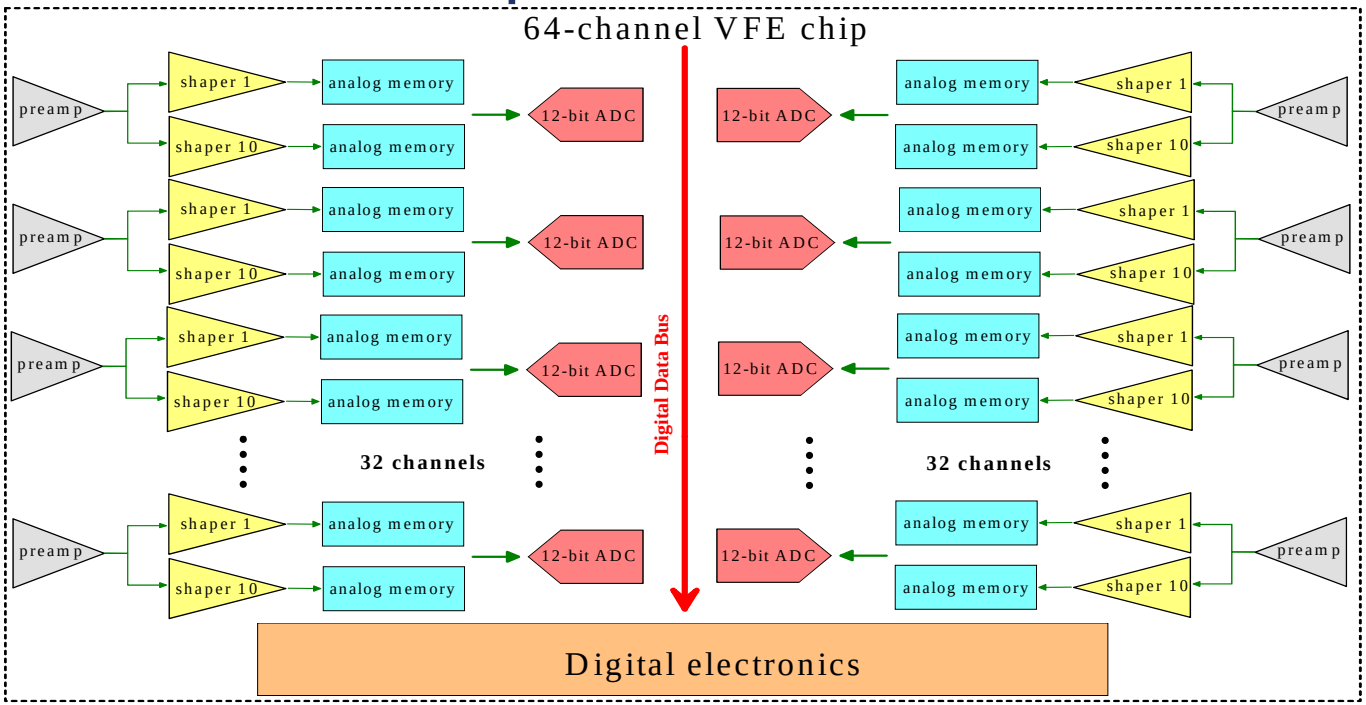
ADC requirements for Si-W Ecal



- **Consumption:**
  - For ADC, arbitrary limited to 10% of the VFE power budget)
    - **2.5 µW/ch max.**
    - **Power pulsing needed**
- **Resolution:**
  - 12 bits (with a 2-gain shaping)
- **Time of conversion:**
  - Time budget of 500 µs to convert all data of all triggered channels
- **Compactness**

Analog electronics busy	A/D conv.	DAQ	IDLE MODE
1ms (.5%)	.5ms (.25%)	.5ms (.25%)	198ms (99%)

Cyclic ADC well-adapted for a one-ADC-per-channel architecture



With <u>one-ADC-per-channel</u> architecture:

☺ **Short analog sensitive wires from memory to ADC**

☺ **A digital Data Bus far from sensitive analog signals**

⇒ **Integrity of analog signals saved**

☺ **Only ADCs of triggered channels powered ON** ⇒ **Power saved**

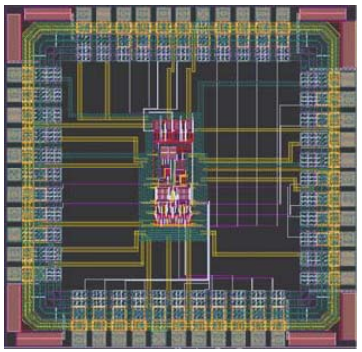
☺ **Conversions of channels done in parallel** ⇒ **No "fast" ADC required**

☹ **Pedestal dispersion of ADC "added" to the dispersion of the analog part …. but calibrated**

The 12-bit cyclic ADC

- Low cost technology: 0.35 µm CMOS Austriamicrosystems
- Clock frequency: 1MHz
- Resolution: 12 bits
- Supply voltage : 3.5V
- Power pulsing system implemented
- Digital process of the bits (1.5 bit/stage algorithm) done with an external FPGA
- 10 chips have been tested

  → Results in the Calice Internal Note CIN-14

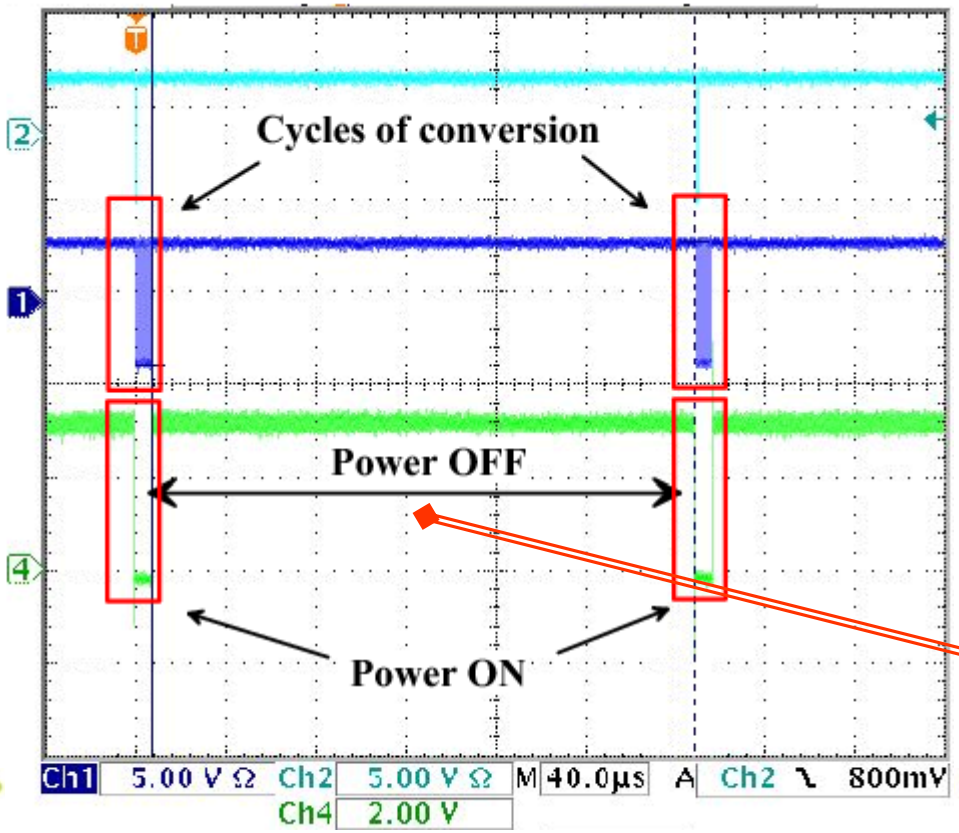


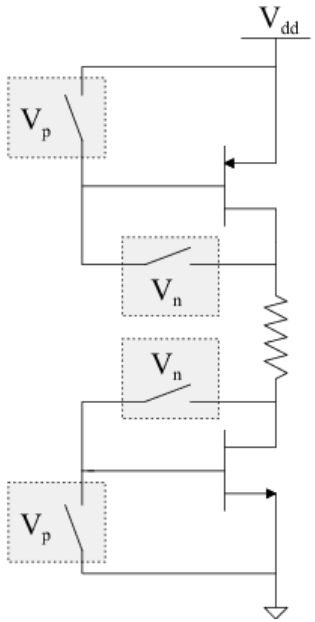
Power pulsing measurement

Table 1: Summarized performance of the 10 chips tested.

Power supply	3.5 V
Consumption	3.5 mW
Time of conversion	7 μs

1 µs for recovery time after swicth ON included

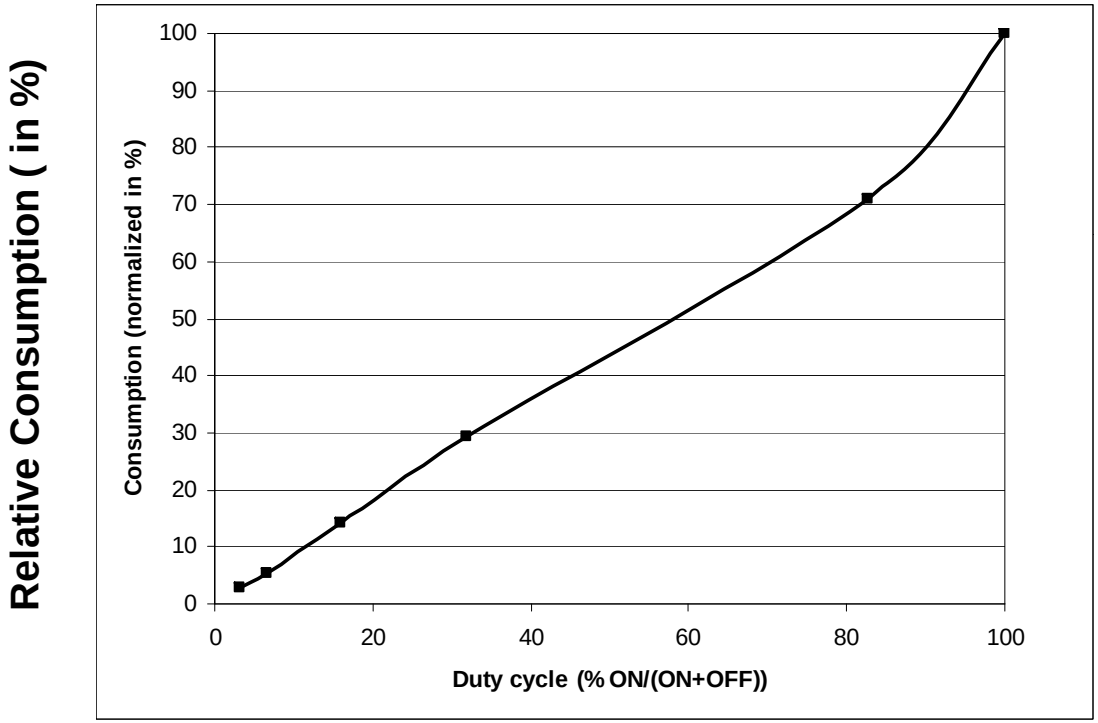




Master current sources switched OFF

Power pulsing measurement

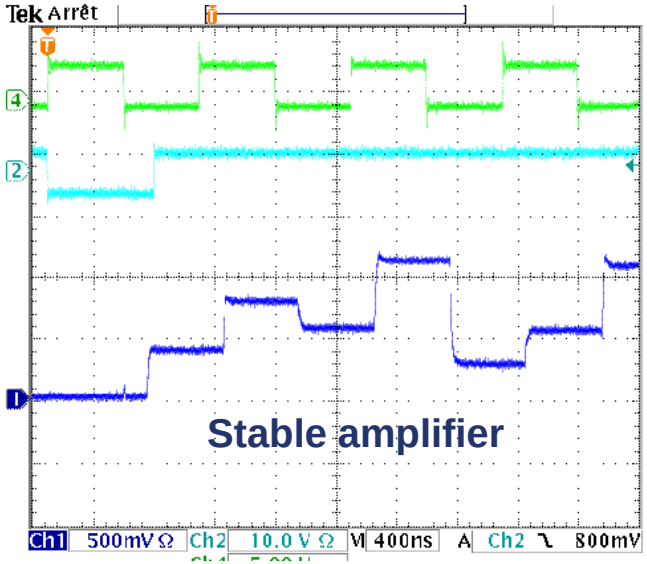
Variation of consumption vs Duty cycle of power pulsing

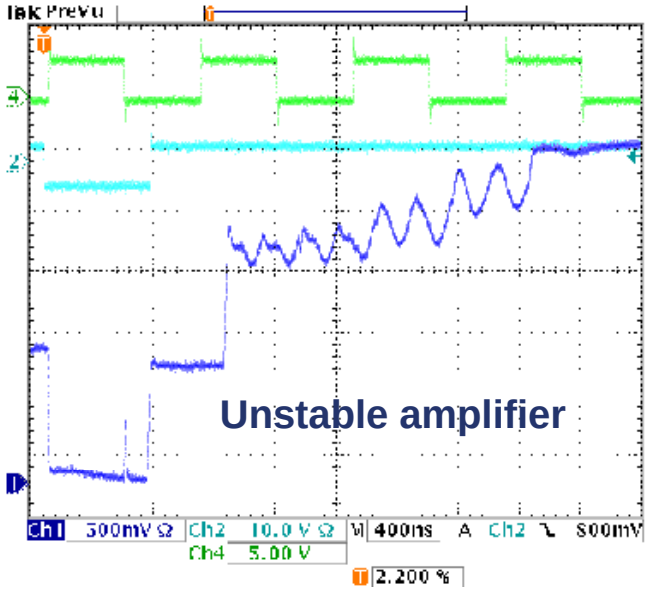


Duty cycle (time ON / total time of one cycle in %)

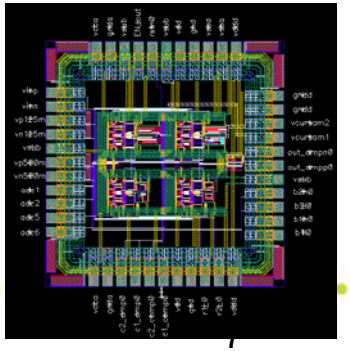
Instability

Chip number	1	2	3	4	5	6	7	8	9	10
Stability	OK	NO	OK	OK	NO	OK	NO	OK	NO	OK



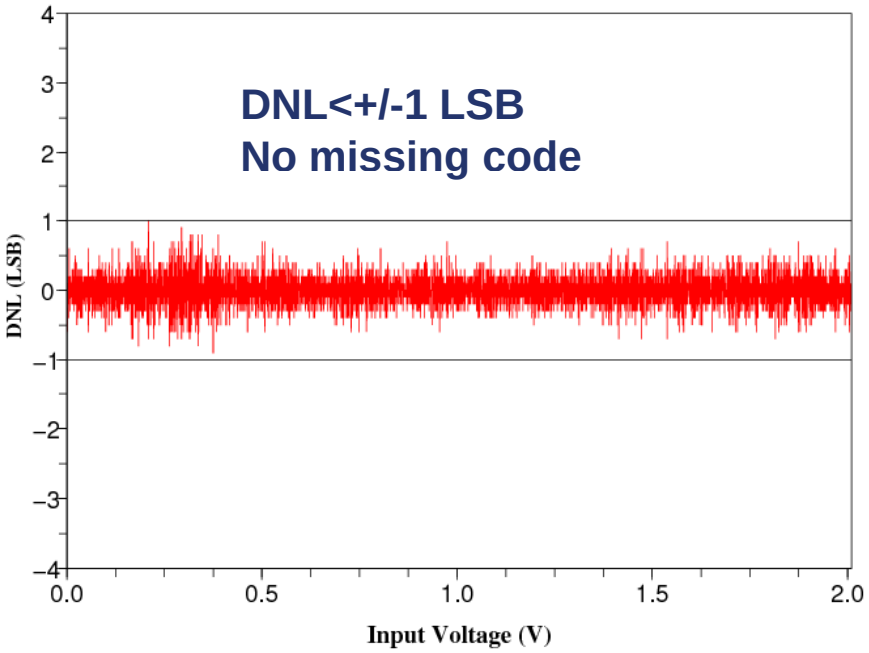


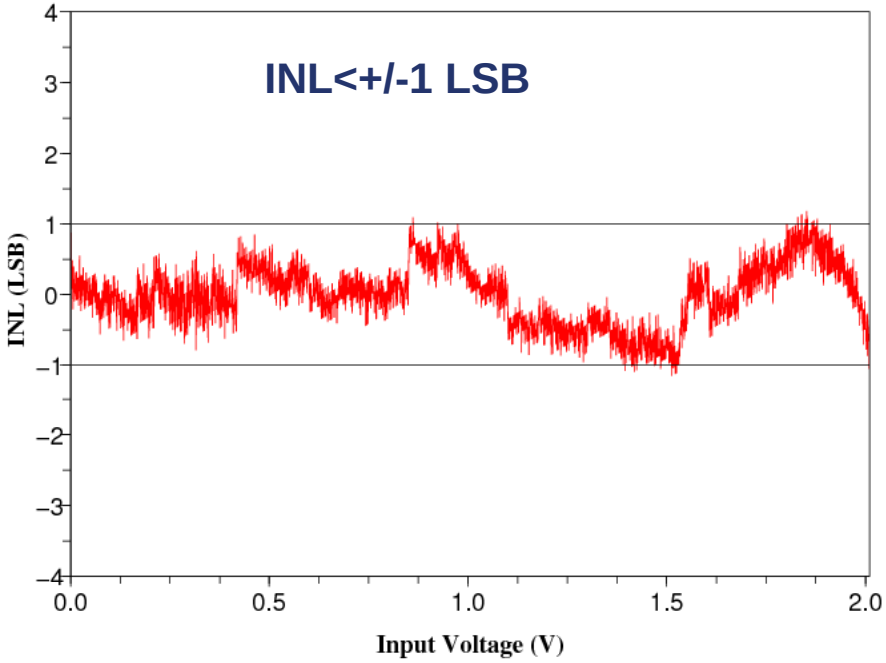
- The problem has been fixed → Common Mode FeedBack instability with process fluctuation
- Chip submitted in March 09 to test the improvement



Measurement of the Linearity

Chip number	1	2	3	4	5	6	7	8	9	10
Stability	OK	NO	OK	OK	NO	OK	NO	OK	NO	OK
INL (min/max)(LSB)	±1.5	–	±2	±1.5	–	-1.5/+2	–	±3	–	±1
DNL (min/max)(LSB)	±1	–	±1	±1.5	–	±1	–	-2/+1	–	±1

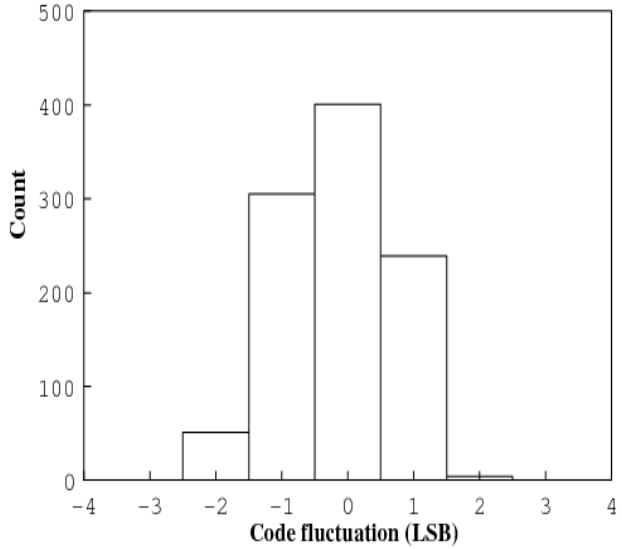




Estimation of the Noise

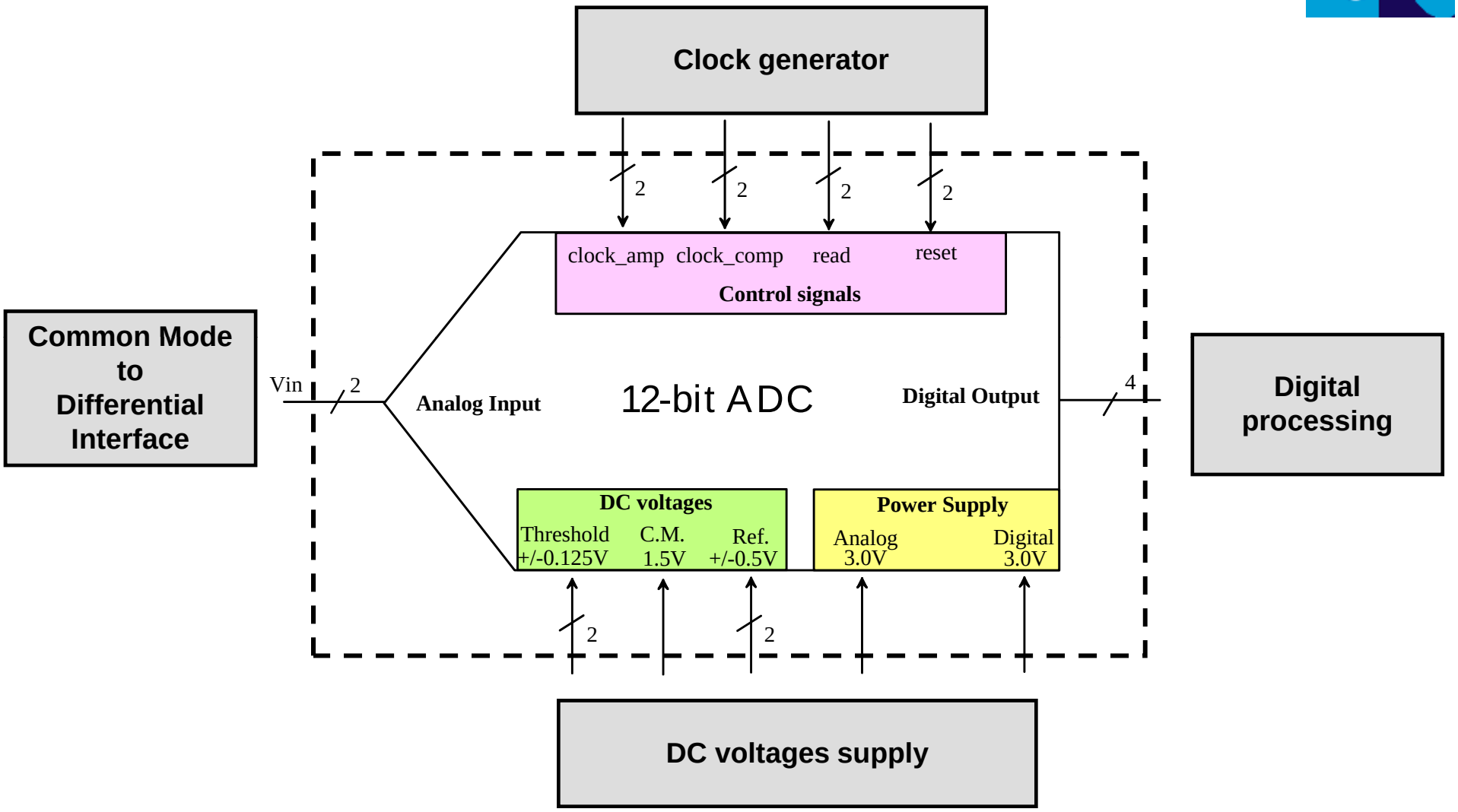
Chip number	1	2	3	4	5	6	7	8	9	10
Stability	OK	NO	OK	OK	NO	OK	NO	OK	NO	OK
INL (min/max)(LSB)	±1.5	–	±2	±1.5	–	−1.5/+2	–	±3	–	±1
DNL (min/max)(LSB)	±1	–	±1	±1.5	–	±1	–	-2/+1	–	±1
Noise @0.1 V (std dev.)	0.72	–	0.72	0.70	–	0.76	–	0.79	–	0.77

Code distribution (input 1V)



Standard deviation = 0.84 LSB (420µV)

A Building Block for the next version Skiroc



Summary

- Measured performance in accordance with Si-W ECAL VFE requirements
  - Time conversion < 7µs
  - Consumption < 0.6µW per channel (power pulsing included)
    - 2.5% of the power budget of one VFE channel
  - Linearity: DNL < +/1 LSB & INL < +/-1 LSB
  - Noise standard deviation < 0.8 LSB
- Yield improved with the new design of the amplifier
- A 12-bit cyclic ADC, dedicated to Si-W ECAL of ILC ready to be implemented in the next Skiroc chip.