MANCHESTER 1824

The University of Manchester

The Status of the LDA

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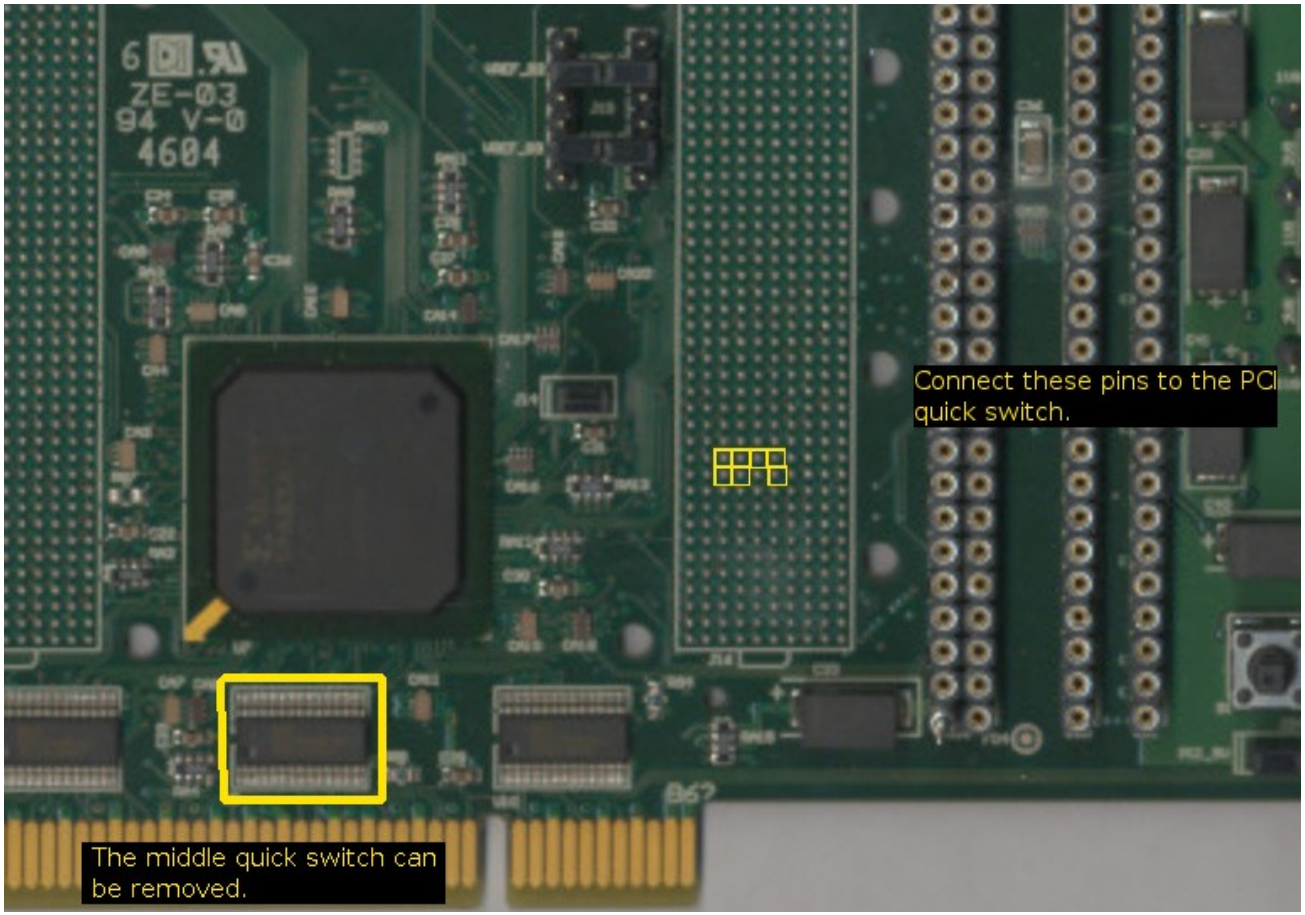
Marc Kelly

(University of Manchester)

A quick History of the LDA

- Commercial Board chosen to be the basis of the LDA. Enterpoint Broaddown2, as it was cheap, available and had good usable IO.
- Enterpoint designed and built a HDMI daughter card as well as a high speed serial IO card, with Ethernet and TLK 2.5Gig chipsets.
- There then followed what can best be described as a small series of technical hiccups.
- Firmware development continued despite this.
- The technical problems were slowly overcome, with the final delay being a manufacturing/commercial one.
- New boards are in hand, and things are undergoing rapid developments.

Some minor modifications required



Technical problem No.1.
The discovery, much to ours and Enterpoint's surprise of a board routing problem.

A large number of pins that existing only on chips larger than S3 1000 had not been routed correctly.

The board lacked the required IO to drive the Ethernet daughter card, 5 RX, 1 TX and a control line were missing.
Minor surgery was needed to get the prototype working.

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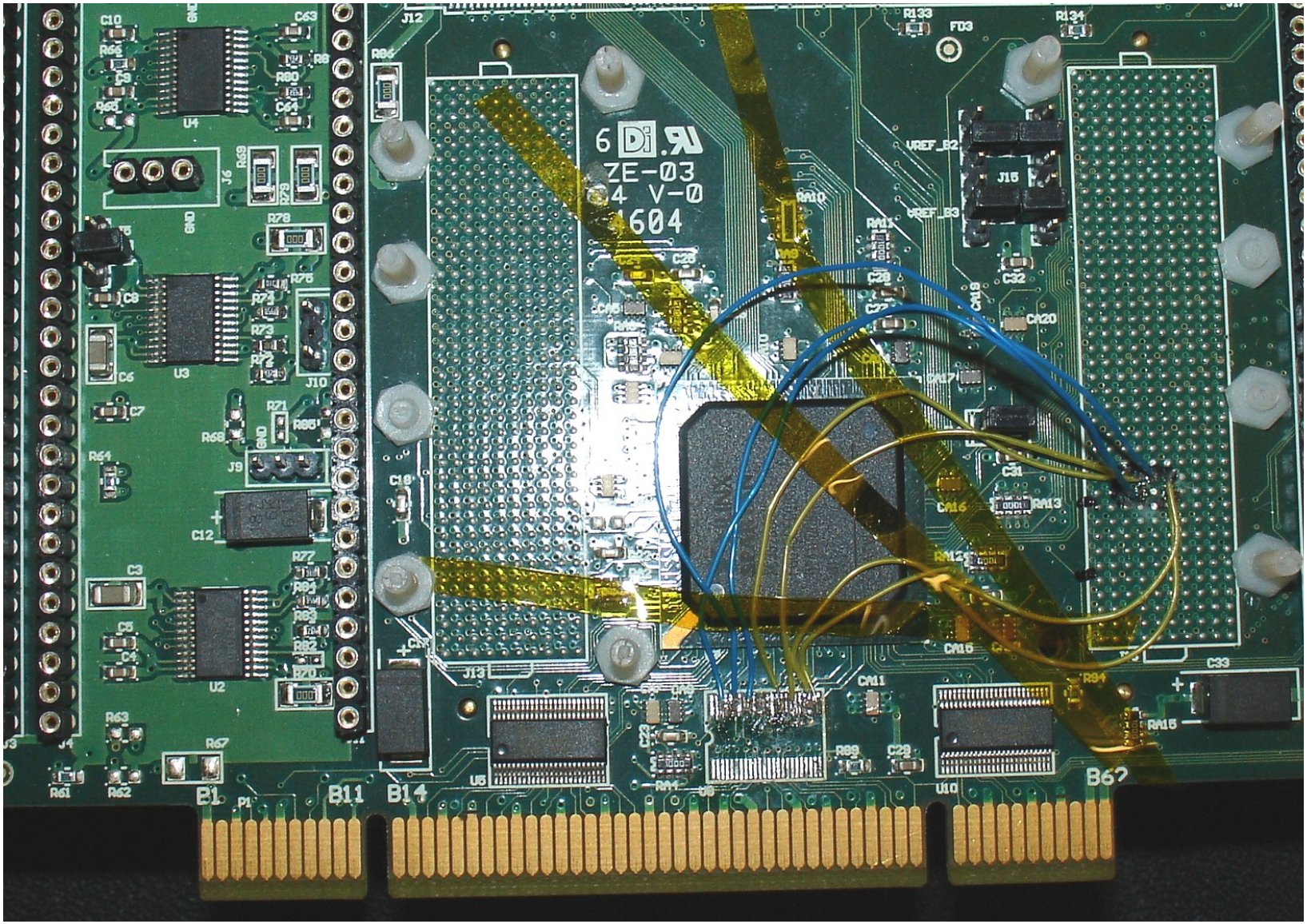
IO fixed. We can now talk to the Ethernet



But the Ethernet cannot talk to the outside World.

- RX data is seen without any problems coming into the FPGA from the Ethernet.
- Yet, Auto negotiation of Links totally fails.
- Using a Virtex4 board, loaded with firmware to perform low level Ethernet diagnostics we see corruption of the TX data.
- Periodic, at ~ us intervals. Bursts of data that cause the remote side to loose bit sync with the data stream.
- We Suspected that the Ethernet board was damaged, so asked them to ship the remaining 4 board to us.
- ...queue second interesting hardware adventure.

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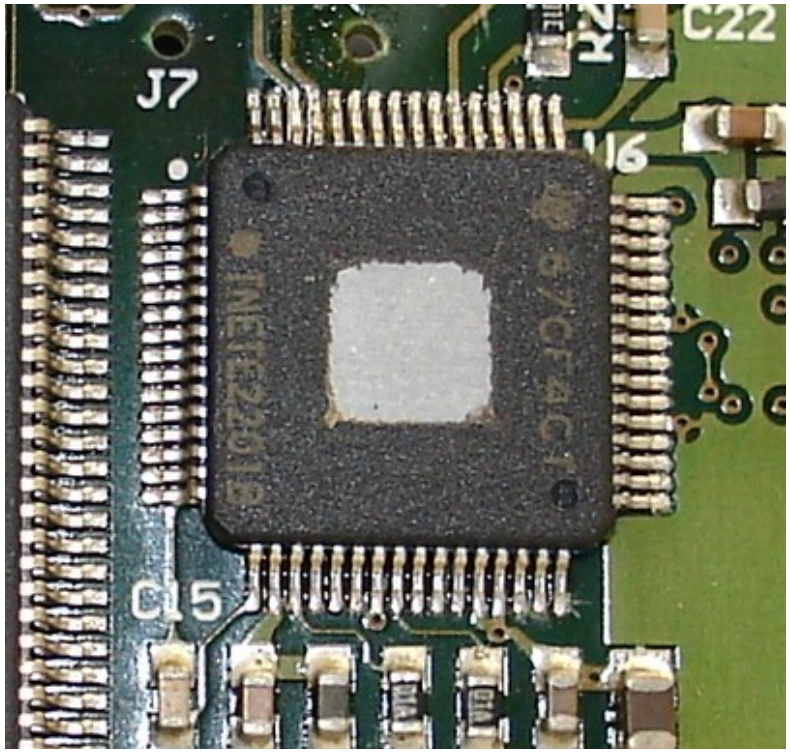
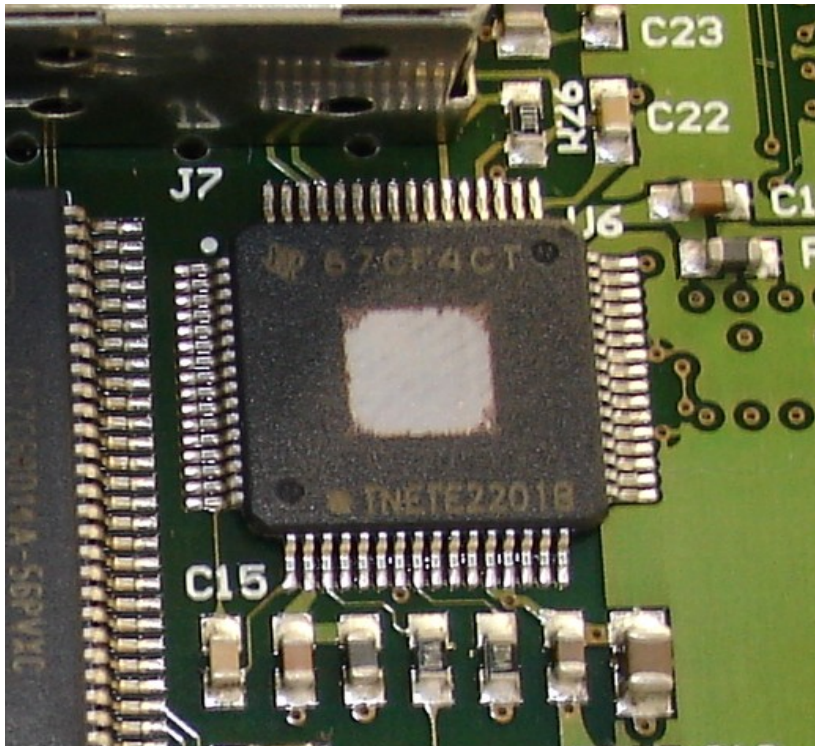
Spot the Difference

Original Ethernet Board



Other Ethernet Board(s)

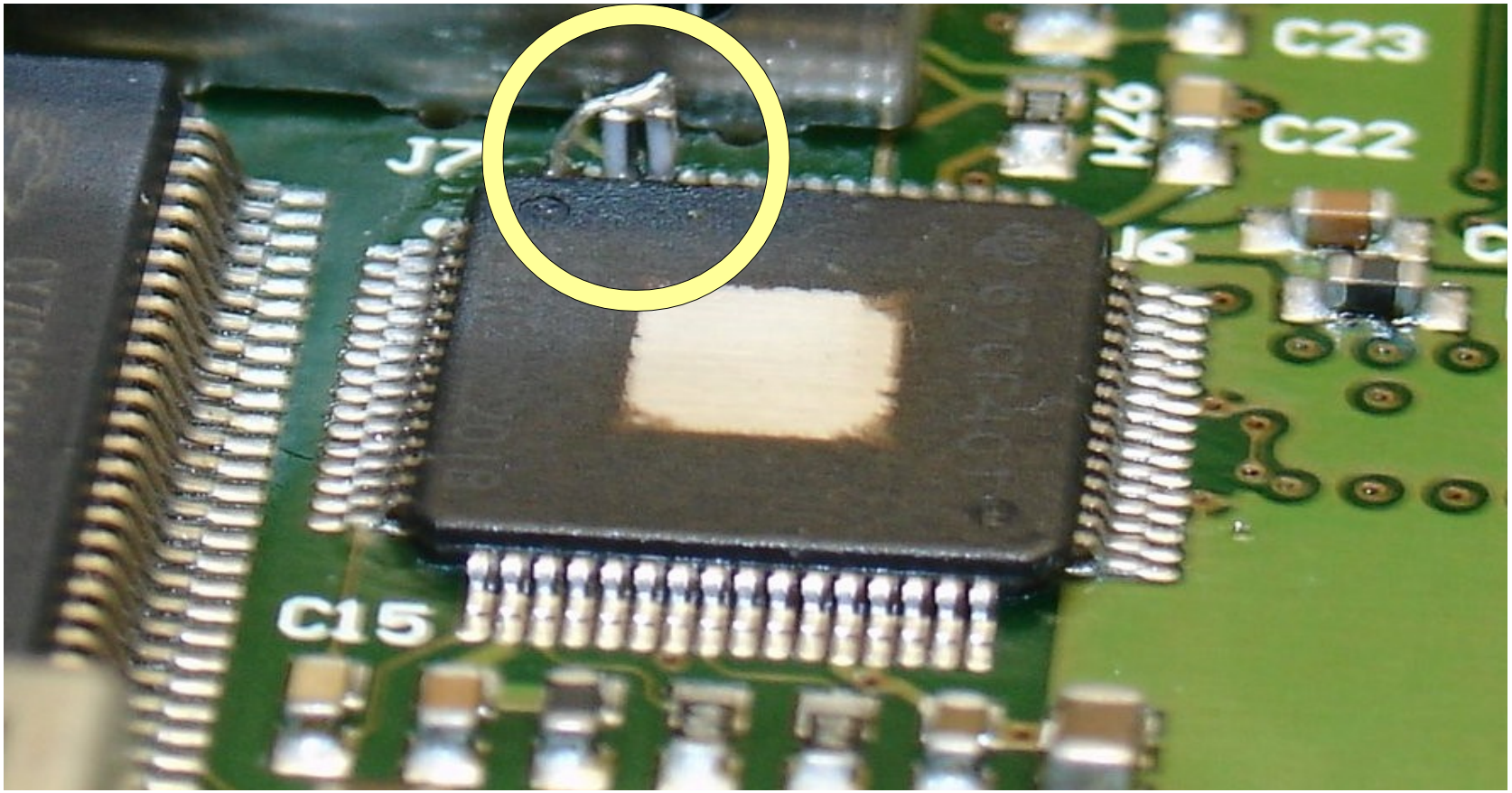


All 4 of the boards were identical...So went back to get fixed... Once returned, they too exhibited the exact same data corruption issue.

Strange effects seen.

- When the chip was put into Loopback diagnostic mode the system would auto negotiate (with itself)
- Using a single fibre to loop it back on itself would result in failed negotiation.
- Hence, FPGA to PHY connection was deemed sane, and working and suspect the PHY to SPF connection.
- Queue another amusing session of problem solving... resulting in the understanding that the PHY to SFP connection is an AC coupled differential PECL and someone had forgotten to put the termination resistors on...

Add the Resistors

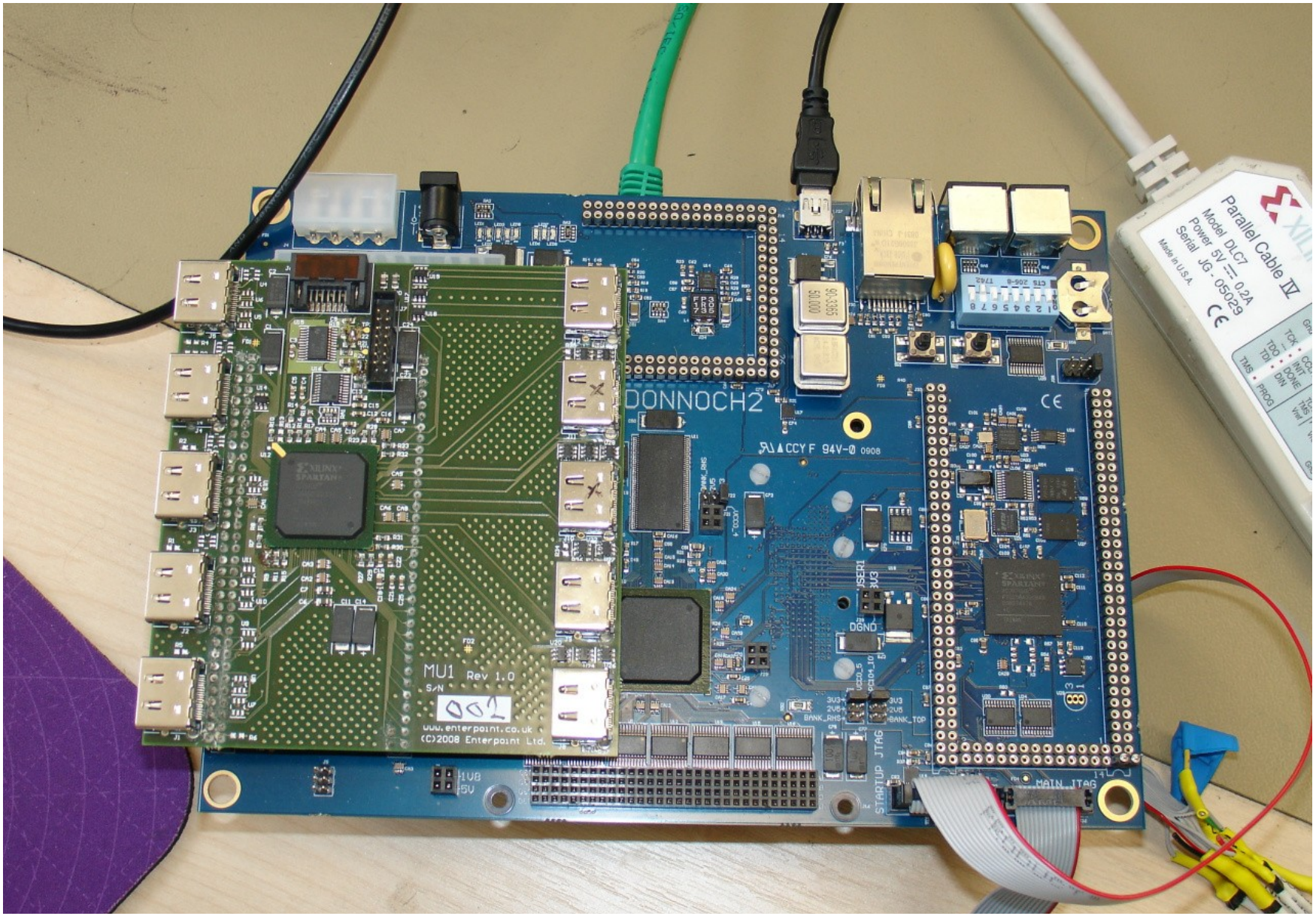


Mike Perry, a Manchester technician, expertly manages to solder on the two required resistors, connecting the TX+ and TX- to GND.
The board the successfully auto negotiates and we see Ethernet data.

Enterpoint announce their BD2 Replacement

- BD2 board is replaces by Mulldonnoch2 board.
- Has same S3_2000 FPGA, plus same rear connector. Can still house the HDMI board on header socket.
- New form factor, ETX PCI104 design.
- Can be powered via USB, DISK or JACK plug.
- On board SDRAM (256Mbit or 512Mbit).
- Second Spartan3A FPGA, designed to be a “Startup FPGA” This controls the Voltage regulators, SPI flash, SPI Ethernet, FTDI USB, Clock generation, RealTime Clock, 1-Wire MAC address.
- 10 bit communication bus between 2 FPGAs.
- Price is about the same as old BD2.
- Board is in production, we have a Prototype at Manchester.

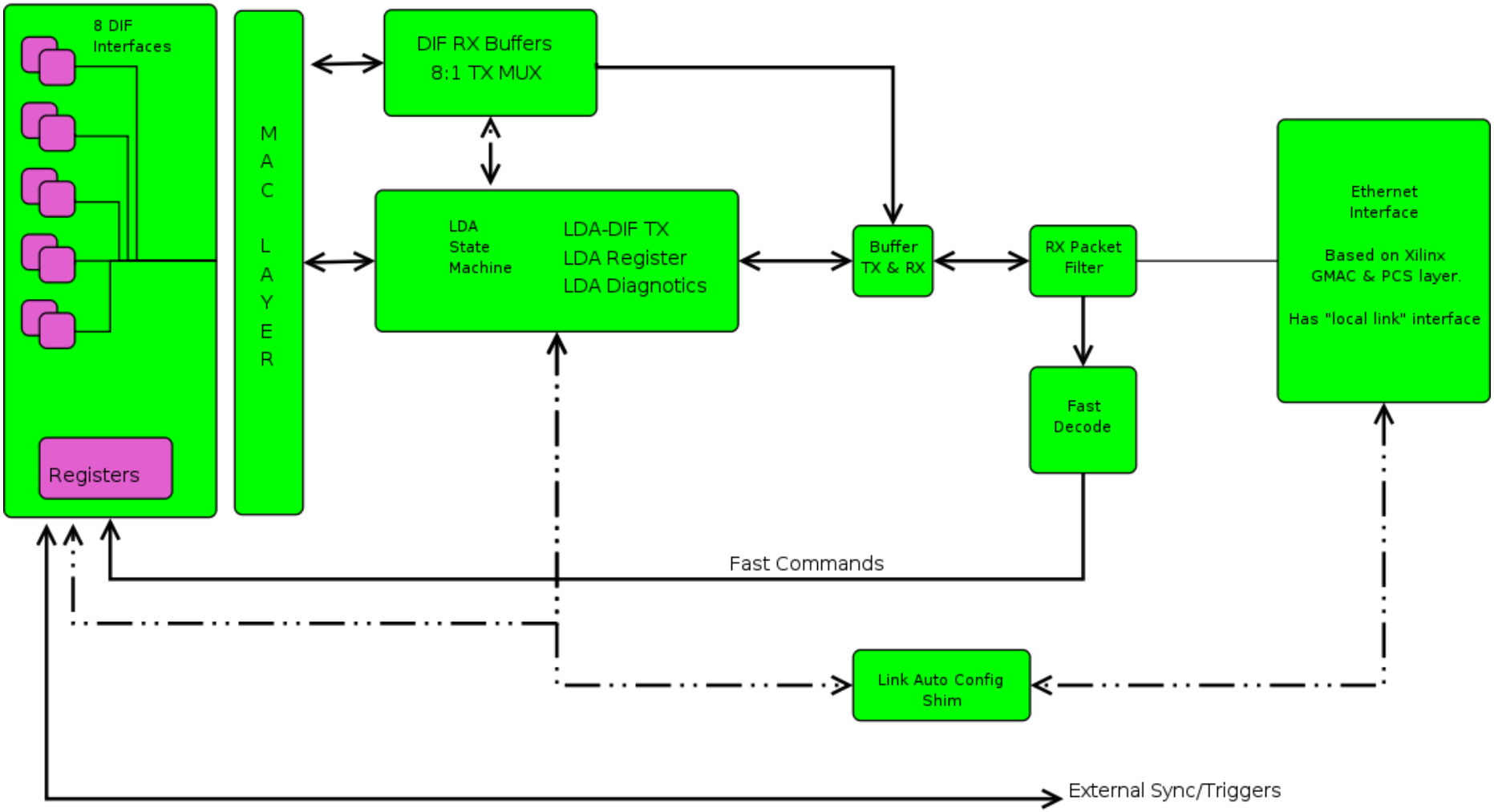
The all new LDA board



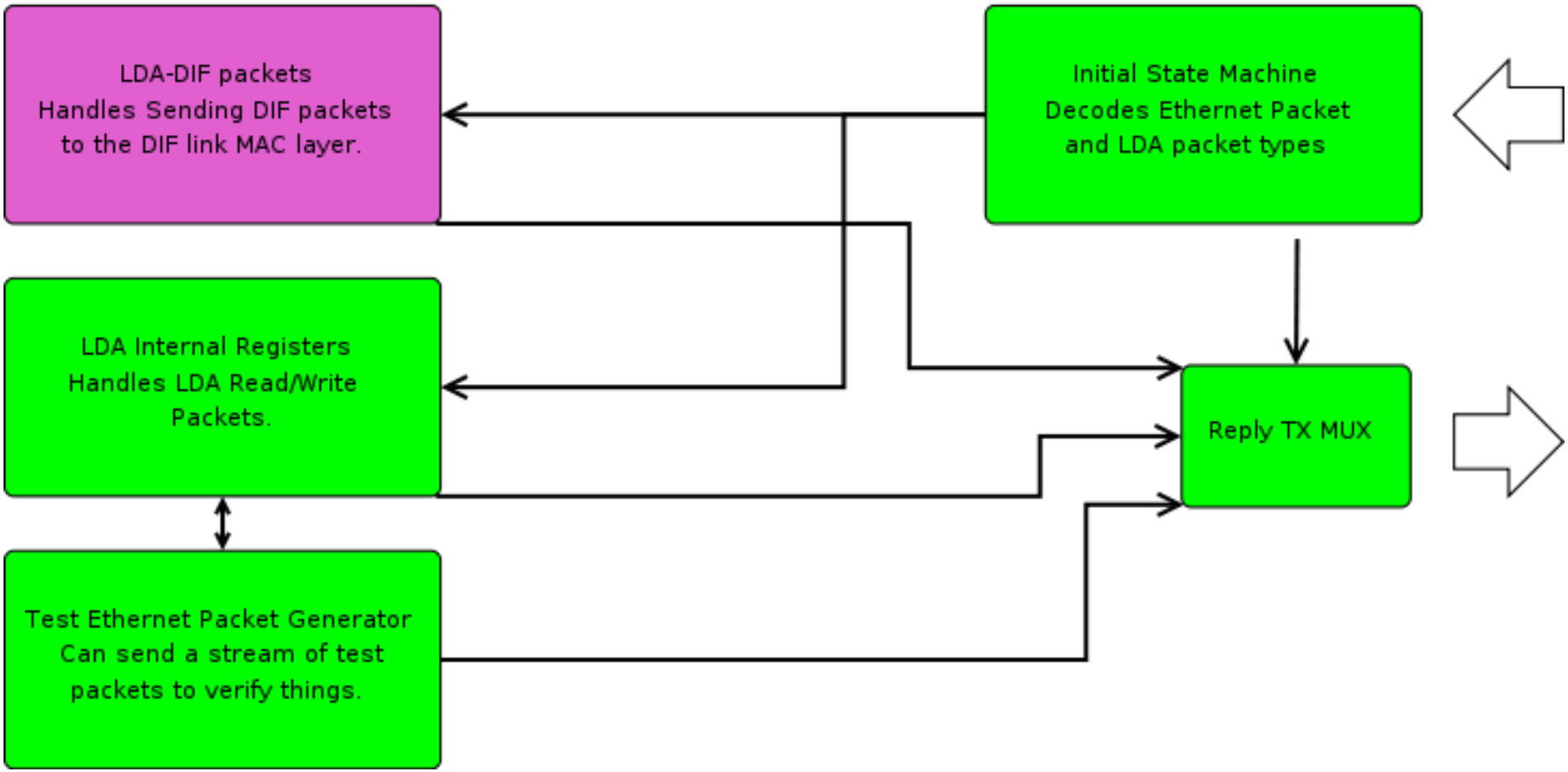
How things stand right now.

- As of Friday the Ethernet seems to be fine, it had connected direct to an Ethernet card, and also works when hooked to a Switch.
- Internally Packets were being received and the state machines where attempting to process the packets.
- Currently there are some bugs.
- The state machines were debugged originally in the LODDAR at UCL/RHUL. However, when moved to the S3 from the V4, they needed to be re-coded to meet the timing.
- 2 more pieces of firmware needed for full chain to work:
  - 1st is State Machine to receive LDA packets via Ethernet and send the encapsulated DIF data onwards.
  - 2nd is the reverse part, an 8:1 MUX that puts all the DIF data into the Ethernet TX buffer.
- Working on these in next few days.

Minimal LDA Internals.



State Machine Internals.



The Next Few Weeks

- Will get the Ethernet fully tested. Some small little tweaks need doing to finish things fully.
- Hardware for “n” LDA system will be ordered, with stripped down Ethernet boards to save cost, we will remove the TLK and USB from the next batch.
- Finish Firmware and get the data path from ODR-LDA-DIF tested in Manchester.
- Finalise any other firmware issues with functionality of the MD2.
- Fast Command Path currently Exists, untested as yet.
- External Sync/trigger path inputs into MD2 board need finalizing.
- System integration testing in London with ODR and DIF.
- Also will add more technical info to the Calice twiki page.