

AHCAL Electronics.

Status and Outlook

Mathias Reinecke

for the AHCAL developers

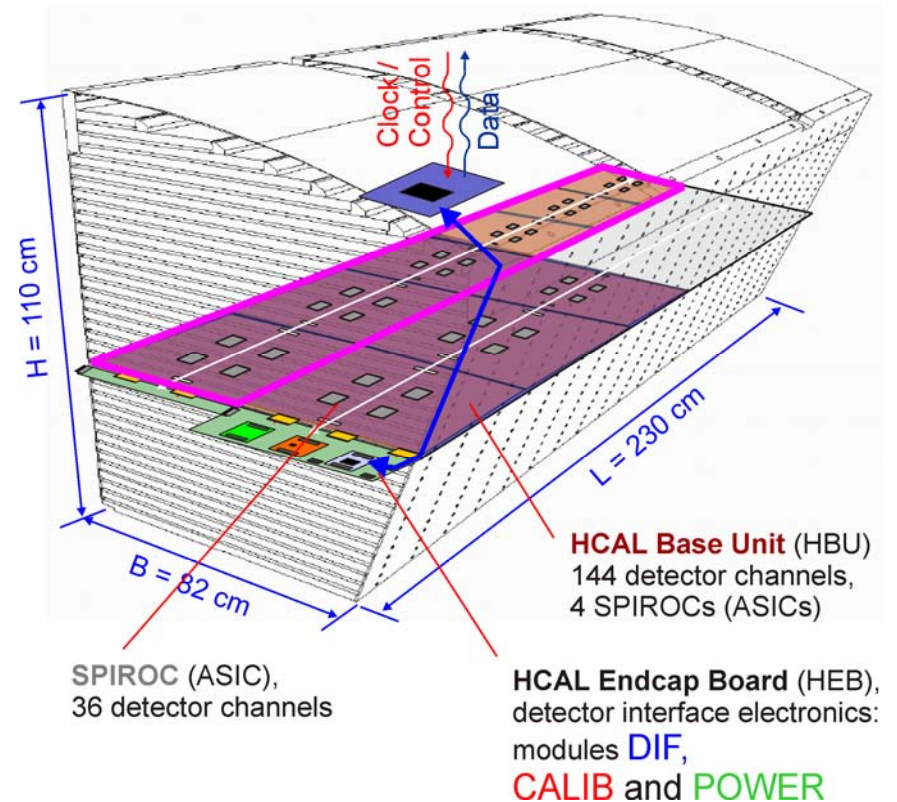
CALICE Days

DESY Hamburg, March 31st, 2009



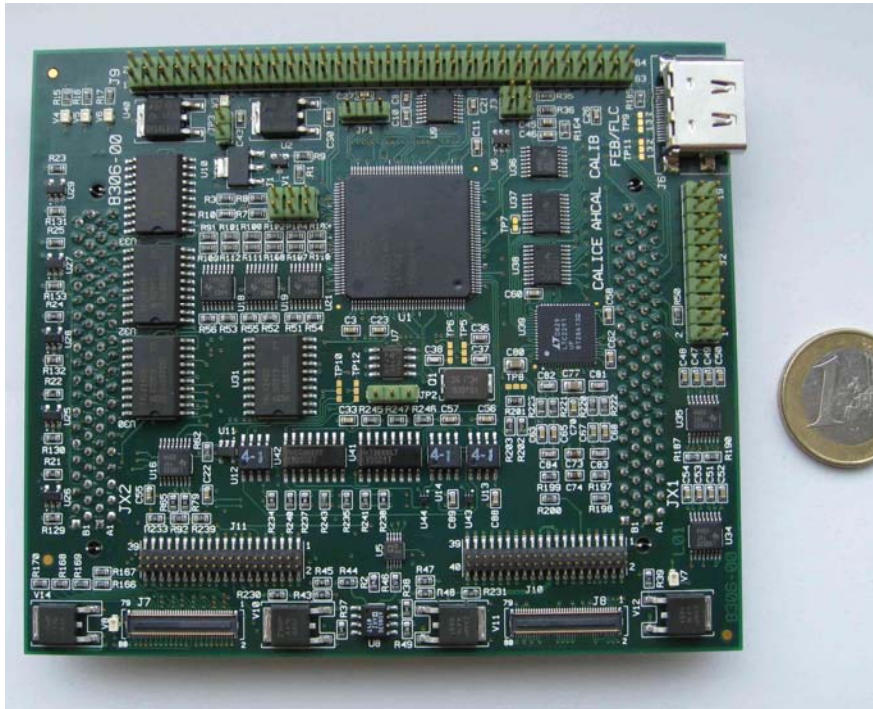
Outline

- > Status of (open) Developments
 - CALIB, POWER, Flexleads
 - Scintillating-Tiles and HBU0
 - DIF + mechanical setup + Labview
- > Commissioning Plans / Redesigns
 - HBU and DIF redesigns
 - Labview (USB) / 'final' DAQ
- > Conclusions and Outlook



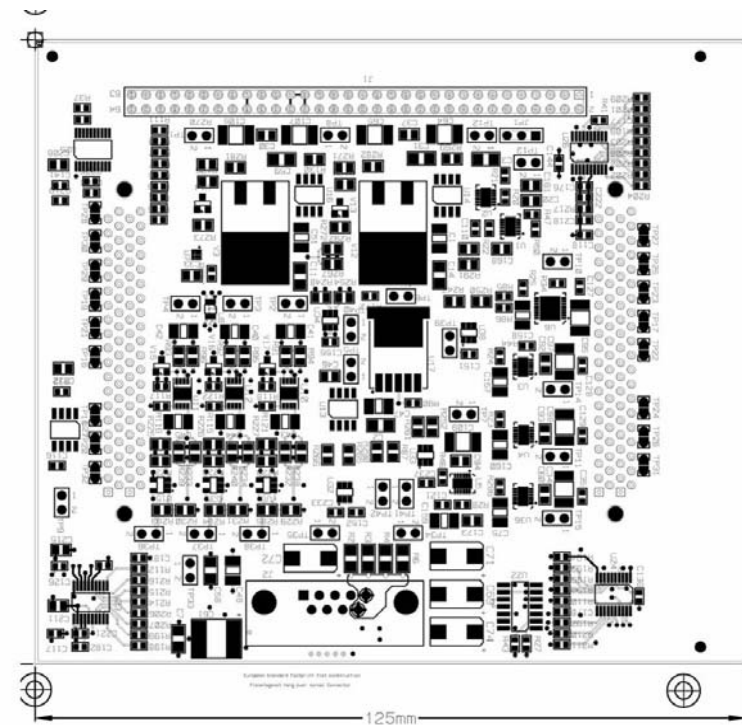
CALIB and POWER modules

CALIB module: 11 x 10 cm²



- > 4 Modules finished.
- > First tests successful.

POWER module: 12.5 x 11 cm²



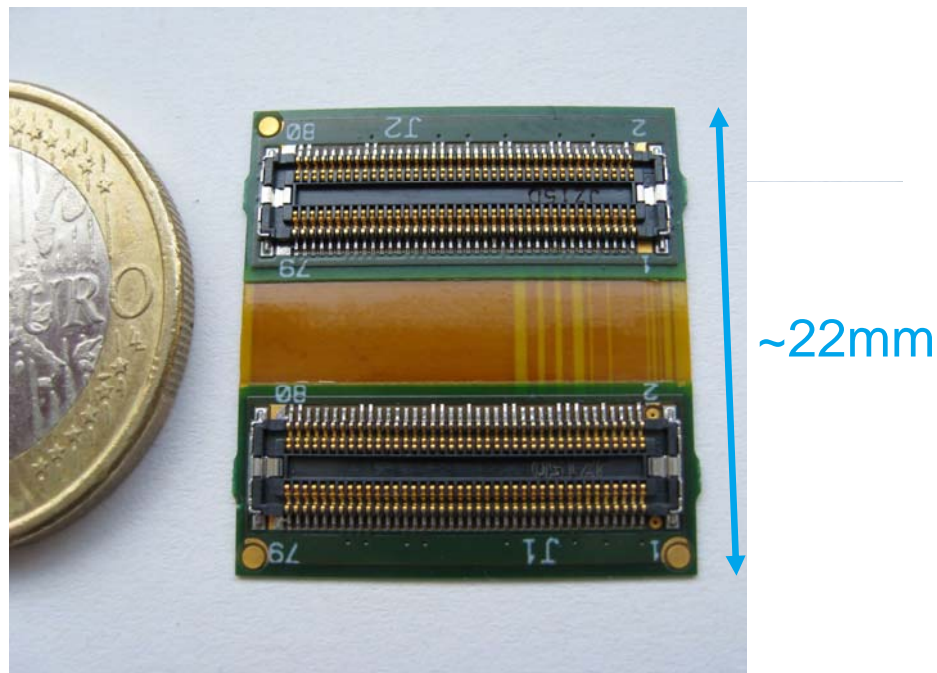
- > Layout ongoing.
- > Expected end April.

CALIB: M. Zeribi,
POWER: H. Wentzlaff



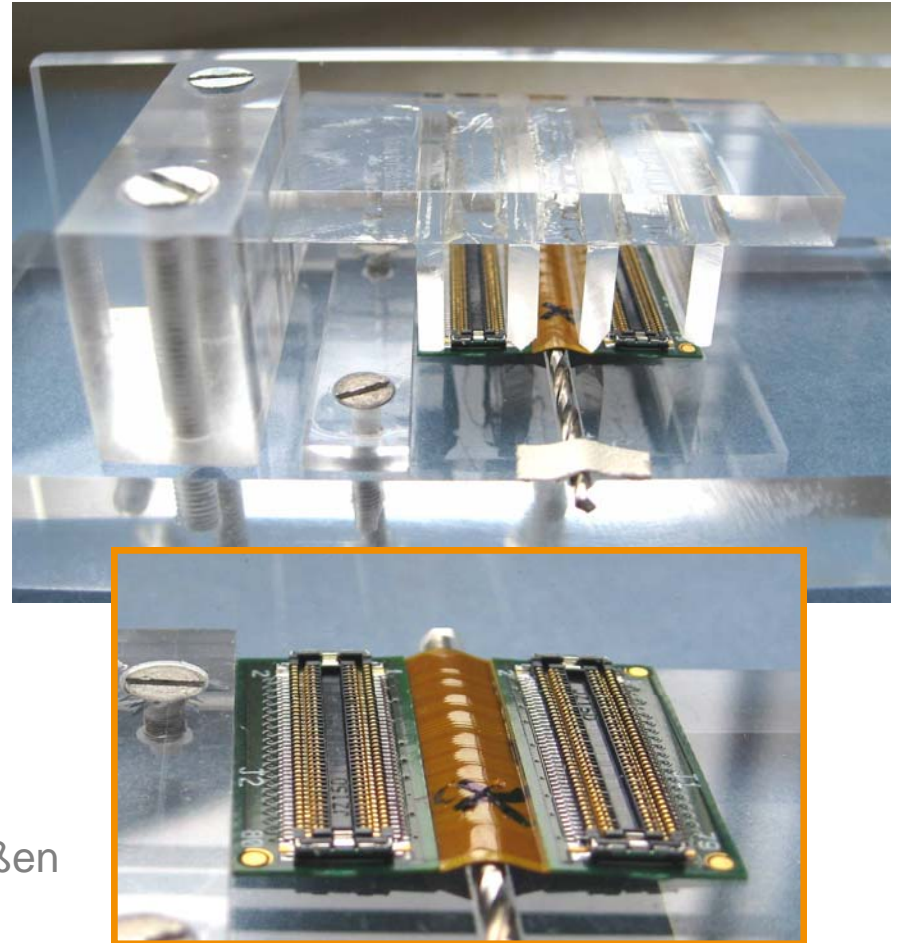
Flexleads (SIGNAL and POWER)

Flexleads finished:
20 pieces of each type.

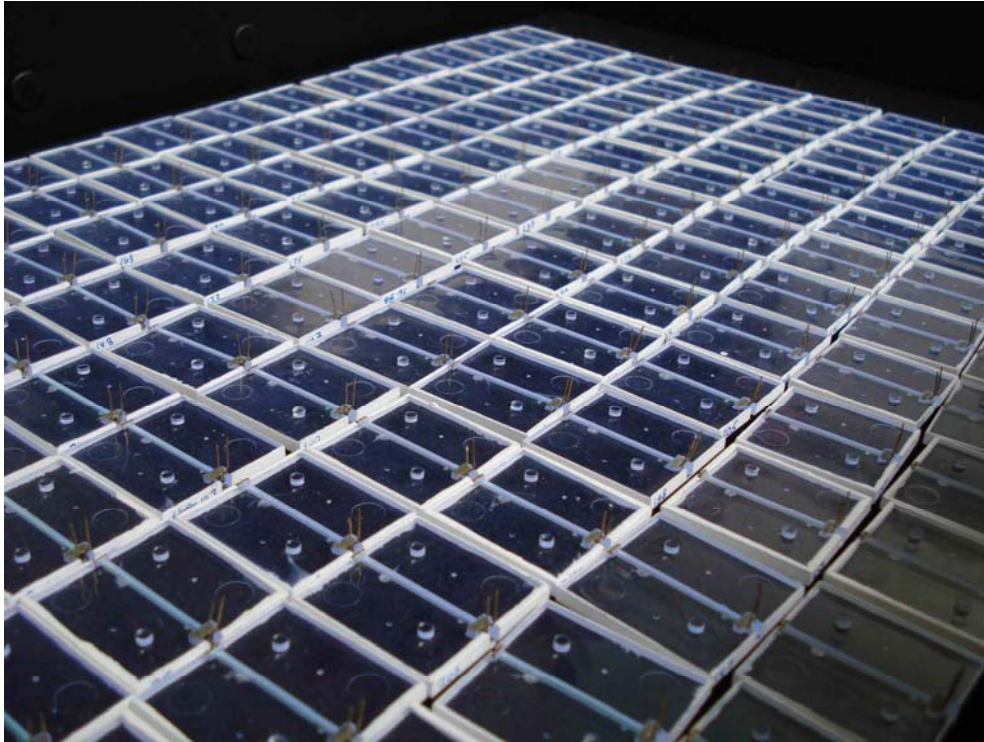


Bending Adapter: K.-H. Gooßen

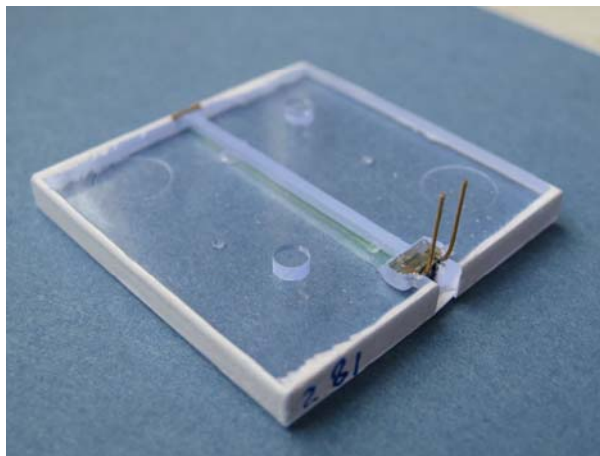
Flexlead Pre-Bending:



Tiles

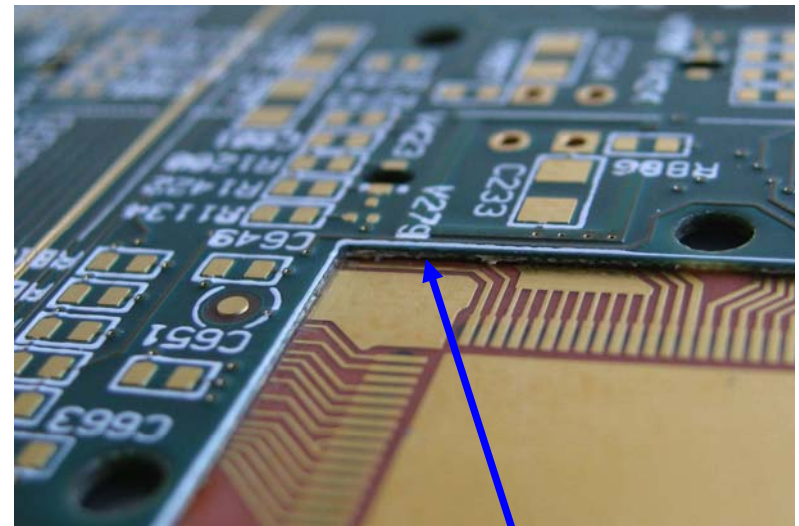
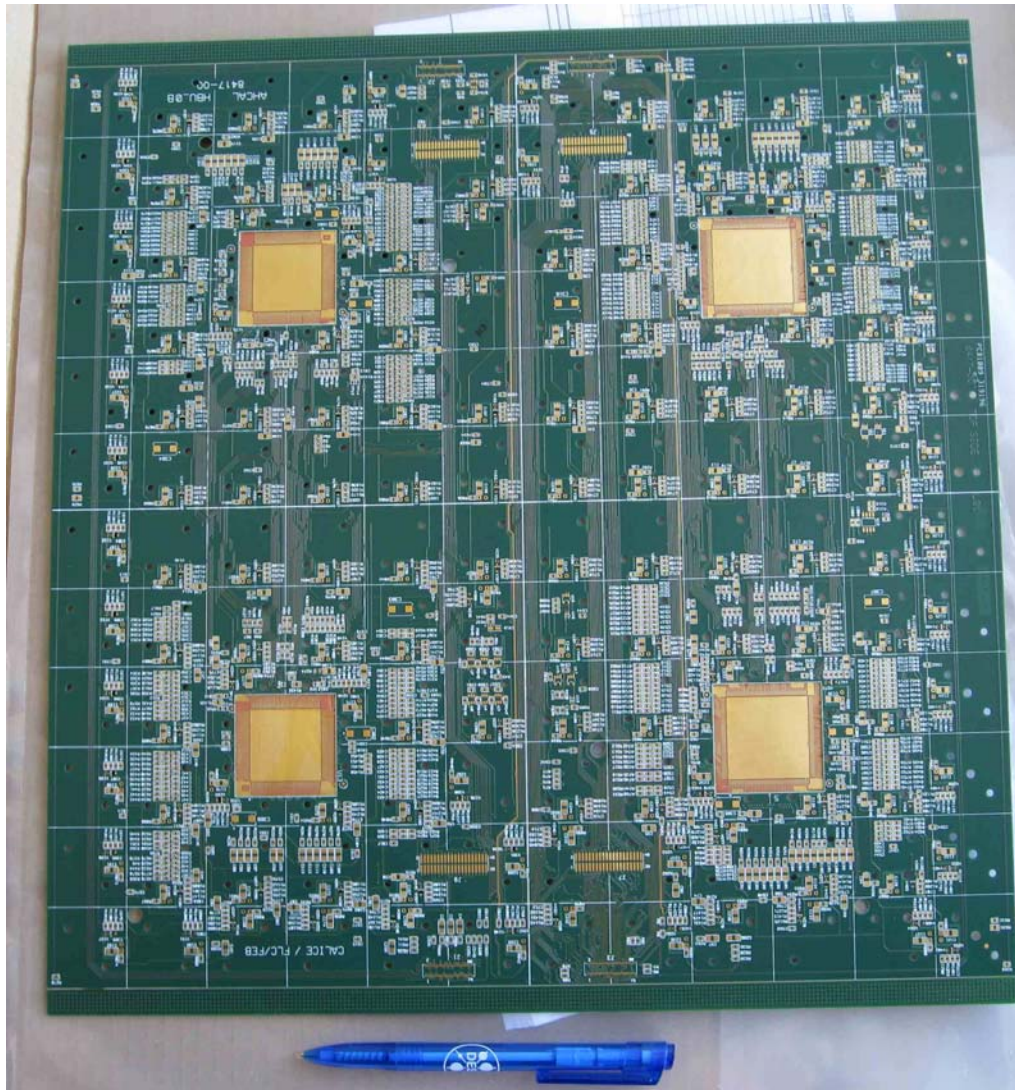


- > 153 prototype tiles arrived at DESY (144 needed for a HBU0).
- > Assembly procedure Tiles-HBU (alignment pins) works at least for one tile.
- > 20% of the SiPMs show 'long tail' response (under investigation).



Tiles: ITEP, SiPMs: CPTA

HBU0

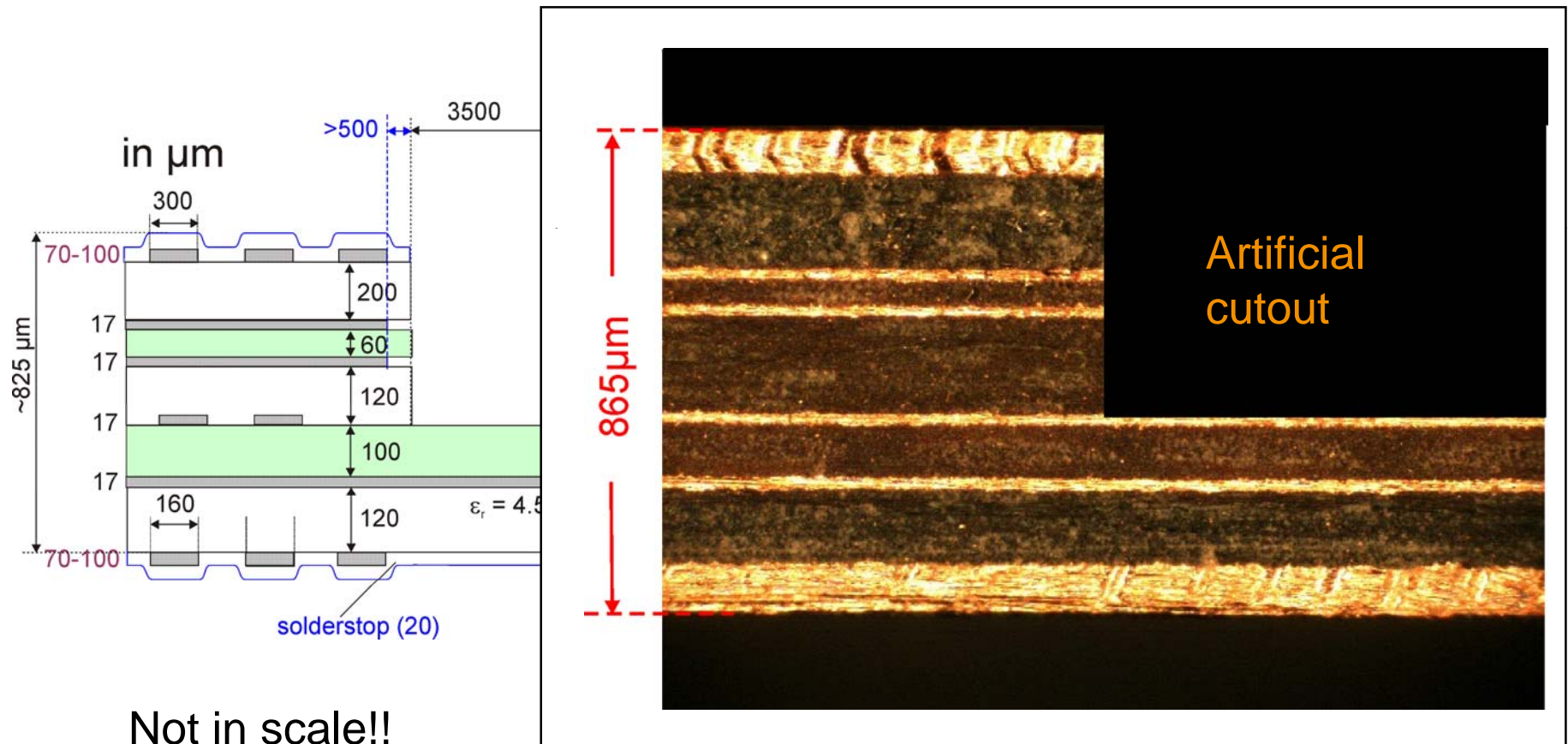


Cutout in PCB (~300 μ m)

- > 3 Boards from 2 suppliers arrived at DESY.
- > In assembly right now!

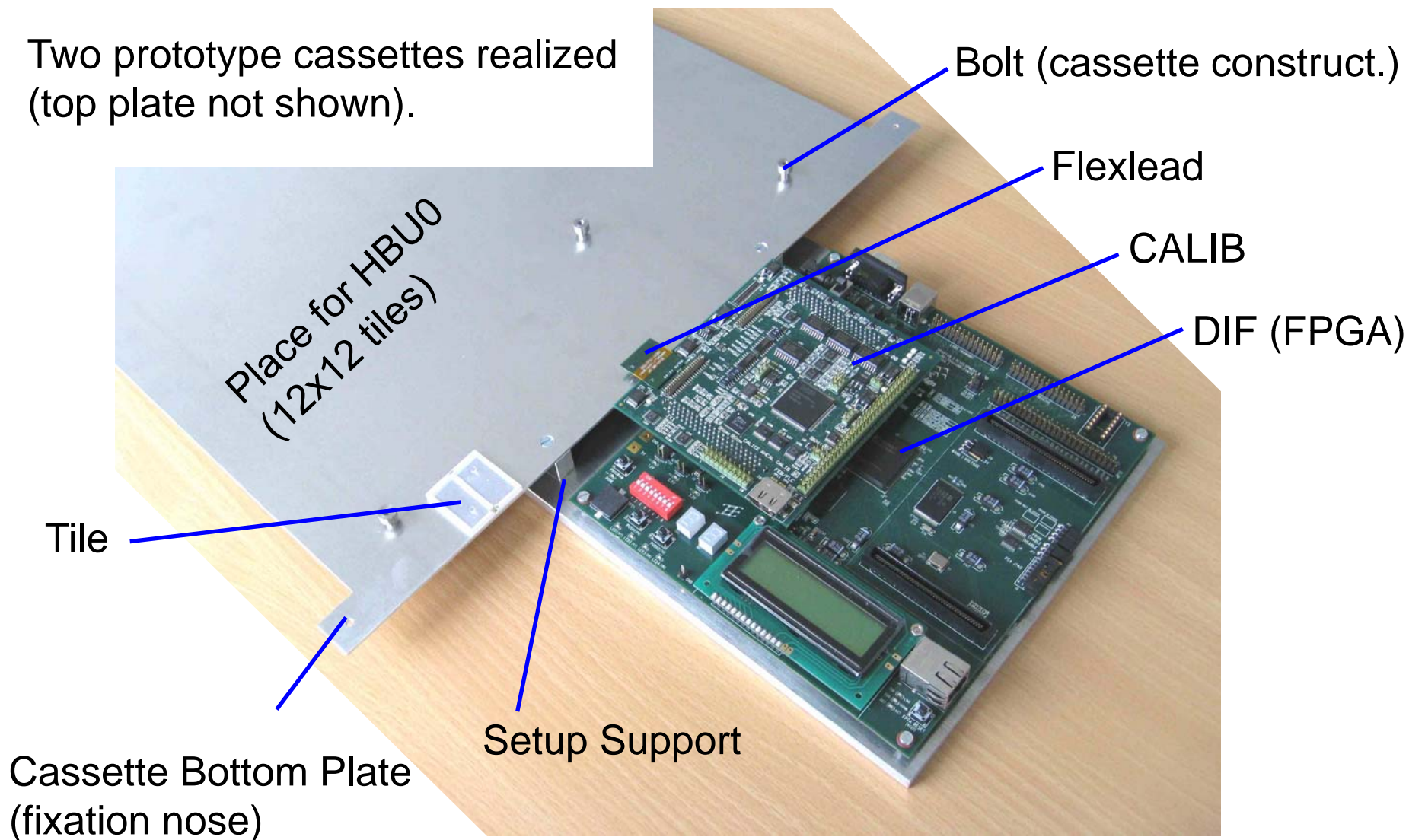
HBU0

HBU0 Cross Section: Concept and Reality:



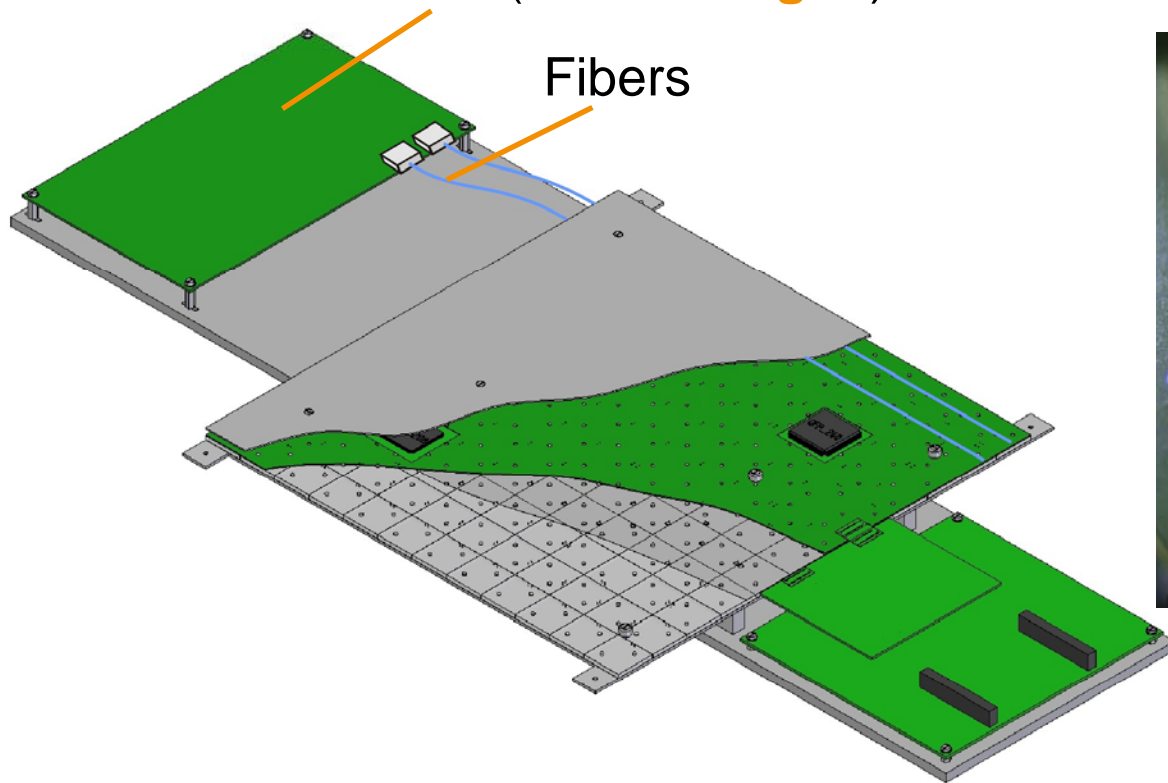
Mechanical setup (Prototype)

Two prototype cassettes realized (top plate not shown).

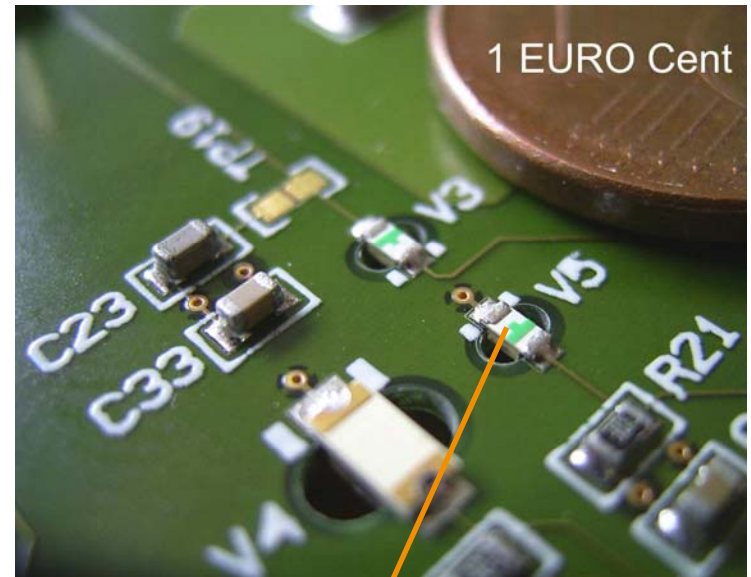


LED Light Calibration Systems (2 concepts)

'Notched' Fiber-Based:
QRLD6x board (**ASCR Prague**):



'Integrated' LED Based
(**Uni Wuppertal**)



UV LED '0603'

Uniformity, Dynamic Range, Crosstalk

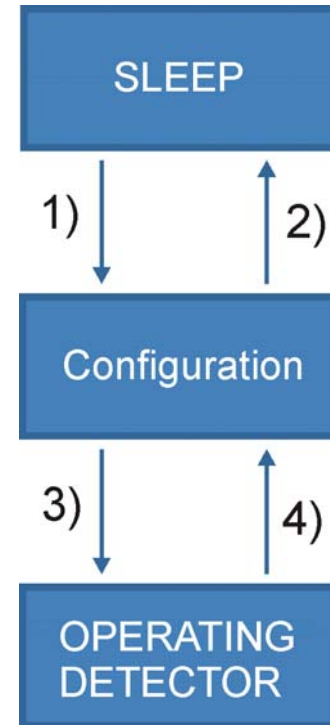
DIF

DIF Firmware (preliminary):

- > Top Level FSM done.
- > Interface to Labview done.
- > First sequences to ASICs done.

Missing (next steps):

- > Interface to Calibration System
- > Automatic Sequencing (e.g. for measurements)
- > **Tests with the actual HBU!**



Development in close coordination within the DIF task force (quite a lot communication / discussion).



Labview Control of the Prototype System

Operation of AHCAL Calibration System (CALIB)

Set Delay Lines

Delay Line Value (8-bit): 01000010 LSB

Select Delay Line: Delay Line 1

DelayLine: Set, Set 2, Ack 2

DAC1 (LED Bias, 16bit): 0100000101000010 LSB

Select DAC: DAC2

On/Off?: ON, OFF

DAC1, DAC2

DAC2 (Charge Bias, 16bit): 0100000101000010 LSB

Set_DAC: Write, Set, Ack

ReadDAC: Read, Read Ack, DACRead hex

Enable Section

LVDS1, LVDS2, LVDS3, LVDS4, LVDS5, LVDS6, LVDS all

PWR_LED, Slab_Pow, C_Power

PWR_Charge, SiPM_Bias, Pre_Bias

Define settings and press 'Set' afterwards

Read Info

Si Serial no. (hex)

Calib_Info: Read, Set 3

SW Date: 0 0 0000

SW Version: 0 0

Board Version: 0

ADC operation

ADC_Cal: Calibrate, Set, Ack

No. Avgs: 1..255, 1

ADC_AVG: Set, Set, Ack

No. Avgs (hex)

R_ADC1	R_ADC2	R_ADC3	R_ADC4
Read, Set	Read, Set	Read, Set	Read, Set
Temp1: 0	VCALIB1: 0	VDAC: 0	HV1: 0
Temp2: 0	VCALIB2: 0	IDAC: 0	HI1: 0
Temp3: 0	VDDD: 0	VREF: 0	HV2: 0
Temp4: 0	IDDD: 0	IREF: 0	HI2: 0
Temp5: 0	VDDA: 0	VADCREf: 0	HV3: 0
Temp6: 0	IDDA: 0	reserved: 0	HI3: 0
reserved: 0	reserved: 0	reserved: 0	reserved: 0
VADCREf: 0	VADCREf: 0	VADCREf: 0	VADCREf: 0

voltages in V
currents in mA
temperatures in degrees C

Tab Control

4 of 6 tabs filled

AHCAL: Focus on:

- > USB Interface
- > Slow-Control
- > Take Data
- > Readout

- > First CALIB commands



Labview: Slow Control Data Generation / Status

- > Slow control data (703 bits):
 - generated by Labview
 - stored ASIC-wise in ASCII file (8-bits per line). Readback from file possible.
- > Labview Control software:
 - takes data from file (+transfer to ASICs).
- > Solution for CALICE DAQ:
 - Files for ASICs / Slabs / Layers? But: Files!

Status Labview Control software:

Connection Labview => USB => DIF (in- and output) established.

Basic operations ready, following DIF task force command list, vers. 1.11.

Main work: complex DIF firmware (Frantisek Krivan).



Commissioning of the Prototype System

Status: Huge Stack of 'untested' hard- and soft-, and firmware.

- > Timeline is challenging. First steps (SPIROC1):
 - Connect everything together and look for smoke.
 - Try basic accesses to the ASICs (SPIROCs) and look with scope.
- > Highest priority is the operation of the ASICs:
 - Write slow-control data
 - Measure / Readout
 - Signal degradation on the long lines.
- > Operate Calibration System / Power module



Commissioning of the Prototype System

How to explain our Status?
Well, ...

XFEL construction
site at DESY



Redesigns for the EUDET module

Minimum redesign effort: HBU, (DIF), ((POWER))

- > Redesign Preconditions :
 - SPIROC Pinout and Tile Dimensions (needed beginning June 09)
 - Experiences from prototype (needed mid May 2009)
 - Only digital-part tests foreseen up to now.
- > Prototype tests must go on in parallel to redesigns:
 - DESY FE needs support for the tests (manpower for redesigns needed).
 - First real system tests with CALICE DAQ, LCS tests, **SPIROC2!**
 - What are the most necessary tests?
- > Mechanical Cassette (EUDET module) => concept pending!



Conclusions and Outlook

- > Timeline is challenging.
- > No further delays in module production have to be expected.
 - HBU0 Development
 - HBU delays for DIF and CALIB commissioning
- > Tests have already started, we proceed in step-by-step mode.

A lot of work ahead, but

**as soon as our prototype system is running, we have
a really impressive system !!**

