Si-W ECAL DIF firmware for EUDET

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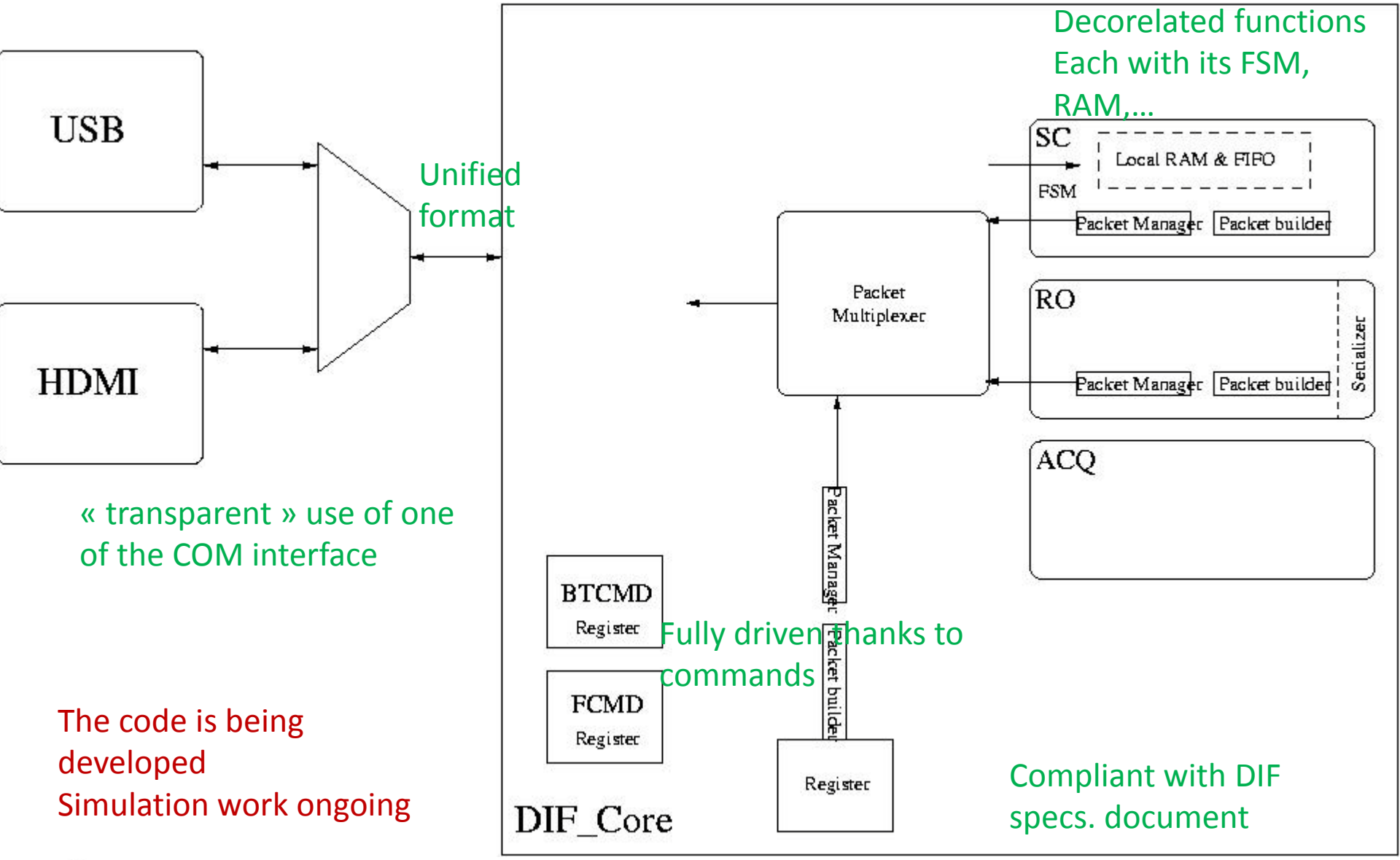
DIF

- At LLR :
  - Basic version from student's work in order to start testing FEV7_CIP, ready by the end of June
  - Will be upgraded to a mature version by the end of the year
- Hope to work together with Bart and Mathias
- Designed for Xilinx
- 100 MHz
- SPIROC 2 & SKIROC2

Who? Faeez + Rémi

DIF : basic version



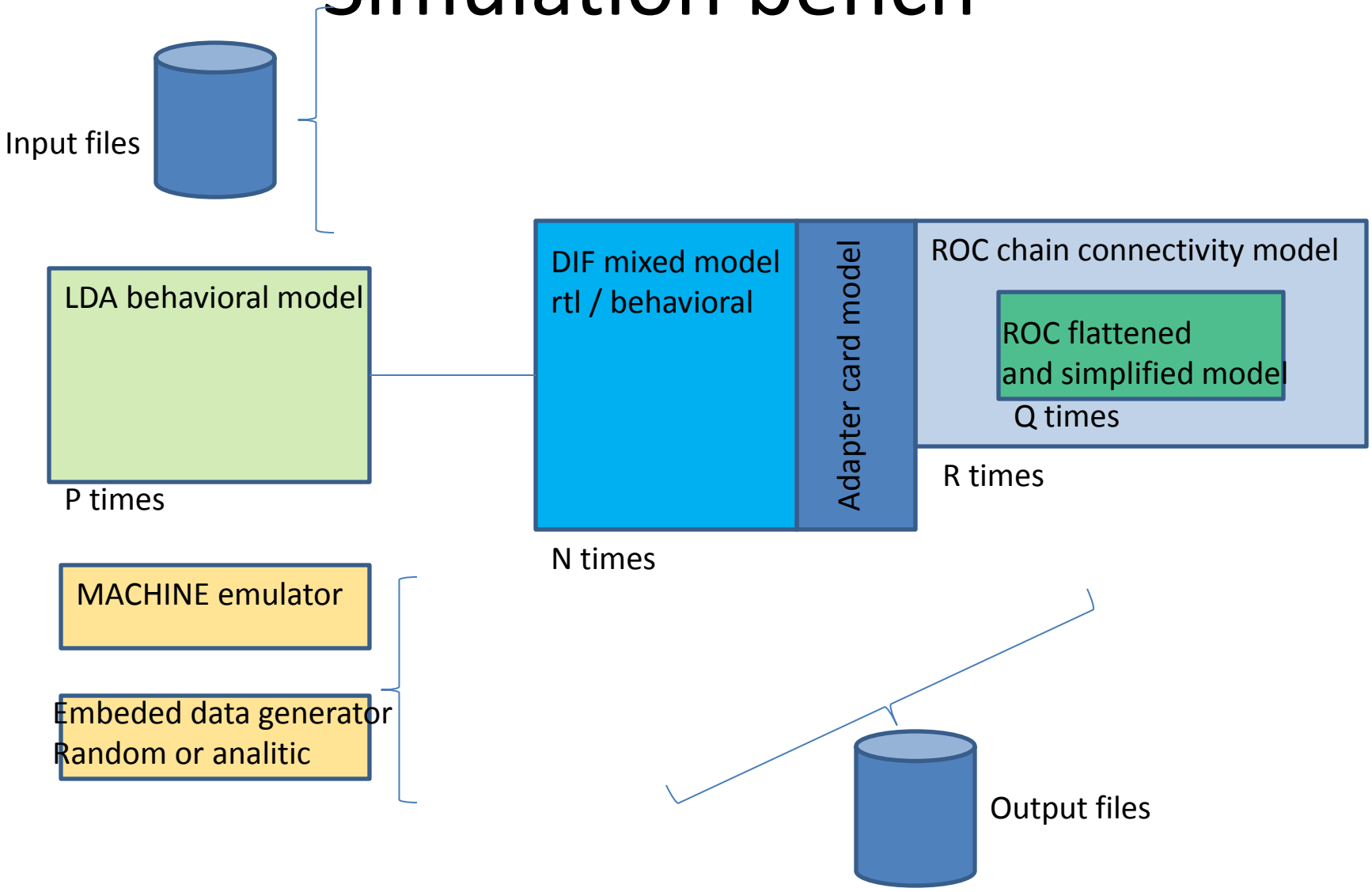
« transparent » use of one of the COM interface

Fully driven thanks to commands

The code is being developed
Simulation work ongoing

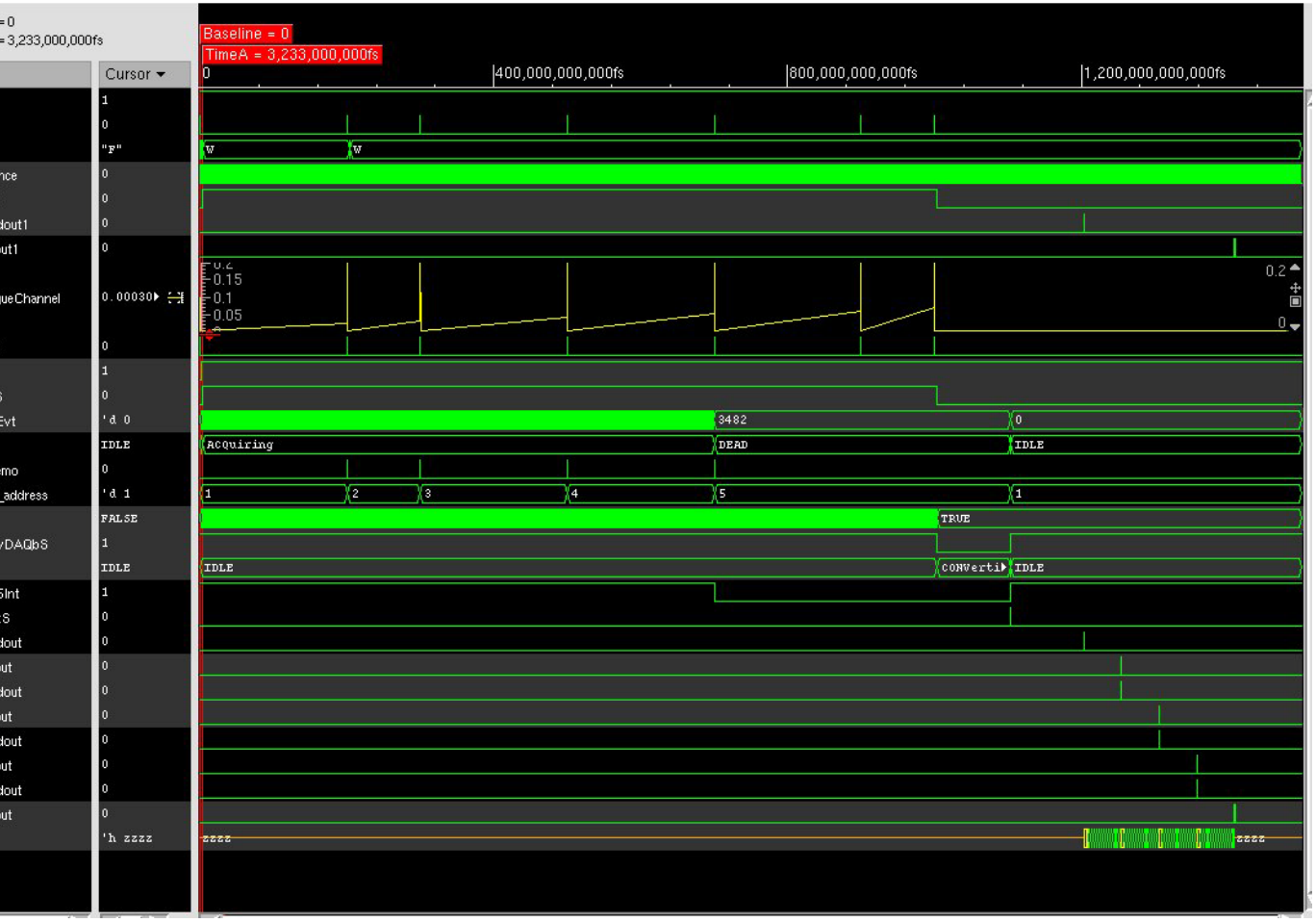
Compliant with DIF specs. document

Simulation bench



Example of DEMO 0.5 version

COSMIC mode : acquisition, conversion and read-out



Random trigger pulses
Machine CLK

Optional analogue data generator

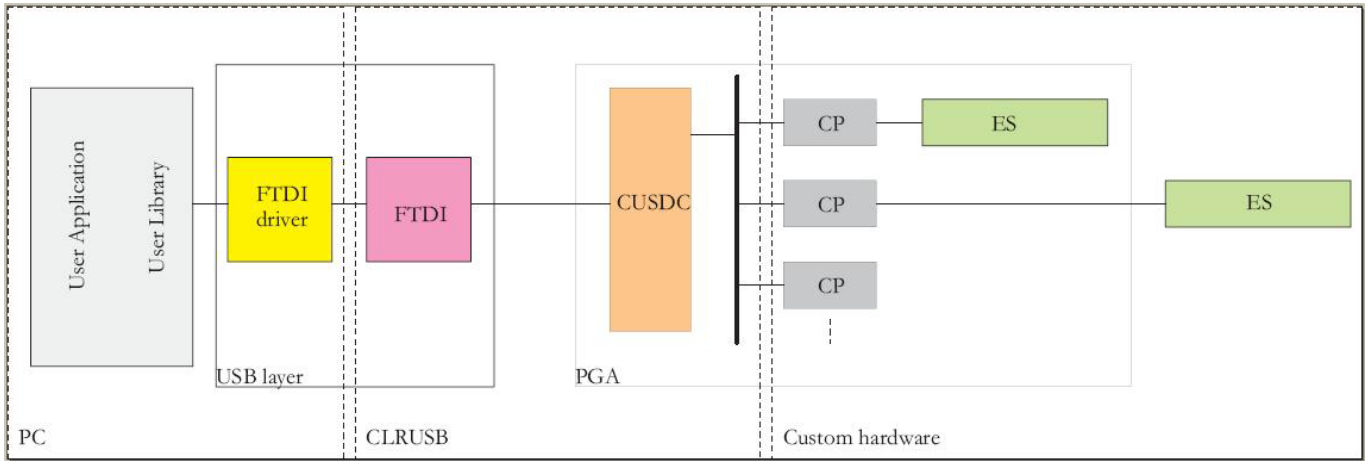
ROC model : amplifier, gain selection, internal trigger, analogue memory, digital part, etc..

DIF signals (start/stop read-out)

Data flow (simplified interface, allow to check buffer occupancies, etc…

USB

- The transfer is **always** initiated by the software
- Standard frame format
- Internal bus with double handshake
- Modular « CP » blocks
- Was designed for 40 MHz



USB

Input packet format

USB data (8b)	Comment
START	START word
Header	2 b config, 5 b CP address, 1b r/w*
SIZE	Size of data bloc MSB
SIZE	Size of data bloc lsb
DATA	Raw Data bloc transferred to CP
…	
DATA	
	STOP : end of transfer

Internal bus

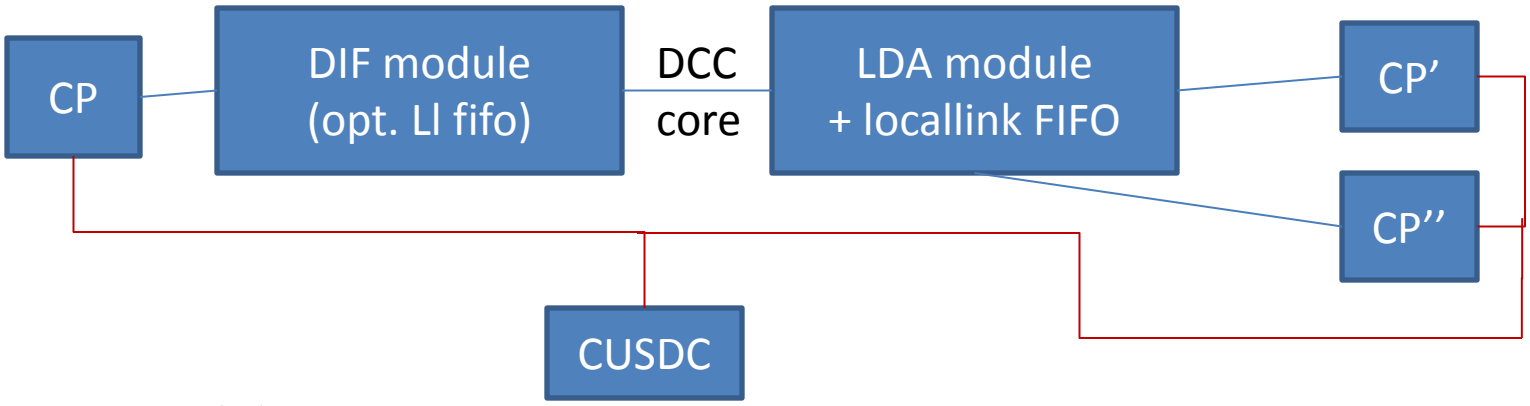
Name	Function	Format
cp_enable	Enables the CP (decoded from header word) Resets CP when inactive	Active high
cp_direction	CP/ES Data flow direction	Low for CP to ES flow High for ES to CP flow
cp_select	Select a CP according to the port address in the header	
cp_ready	CP ready to accept new CUSDC data	Active low
dc_dvalid	Current CUSDC redirected byte is valid	Active high
dc_data	CUSDC redirected byte	8 data bits
dc_dready	CUSDC ready to accept new CP byte	Active low
cp_dvalid	CP byte is valid	Active high
cp_data	CP byte output to CUSDC	8 data bits
cp_enddata	Last data word sent	Active low

USB : CP library

- Generation of a fast command
- Configuration of the registers to enable 8b/10b link (LDA side)
- R/W interface to DIF module (fifo included)
- R/W interface to LDA module
- Register bank
- I2C master
- …

HDMI link tests

- First step in DAQ use
- See DCC talk (Franck)
- Simulation + synthesis + P&R (DIF & DCC)
- LDA side and DIF side
  - In same fpga
  - On two separate boards
- Some minor bugs found
  - Forgot to update code from Marc
  - Being fixed
- Have some difficulties to enable DIF->LDA
- Test bench using USB pattern generator, HW tests soon (post P&R sim OK)



firmware @ LLR

- https://svn.in2p3.fr/calice/hardware/trunc
  - Ask for a login

Unfortunately, copies of hdmi link code
No automatic update from Marc's repository

Index of /hardware/trunk

Files shown: 0
Directory revision: 377 (of 381)
Sticky Revision: Set

DIF firmware (DEV)

DCC firmware (DEV)

USB firmware (snapshot)

File	Rev.	Age	Author	Last log entry
Parent Directory				
DIF_FEV7/	338	5 days	faeez	
behavioral_sim/	342	5 days	hsieh	
dhcal_dcc/	377	43 hours	gastaldi	premier test avec usb (comportement) test effectué avec cp "host write"
usb_cp/	350	5 days	gastaldi	generic removed
usb_dcc/	53	3 months	gastaldi	
usb_proposal/	199	8 weeks	rcornat	