# Status of the Data Concentrator Card (DCC)

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UCL

# Goal of DCC

- Main specification :

Reduce the number of LDA and ODR for the DHCAL & optimize the data flux

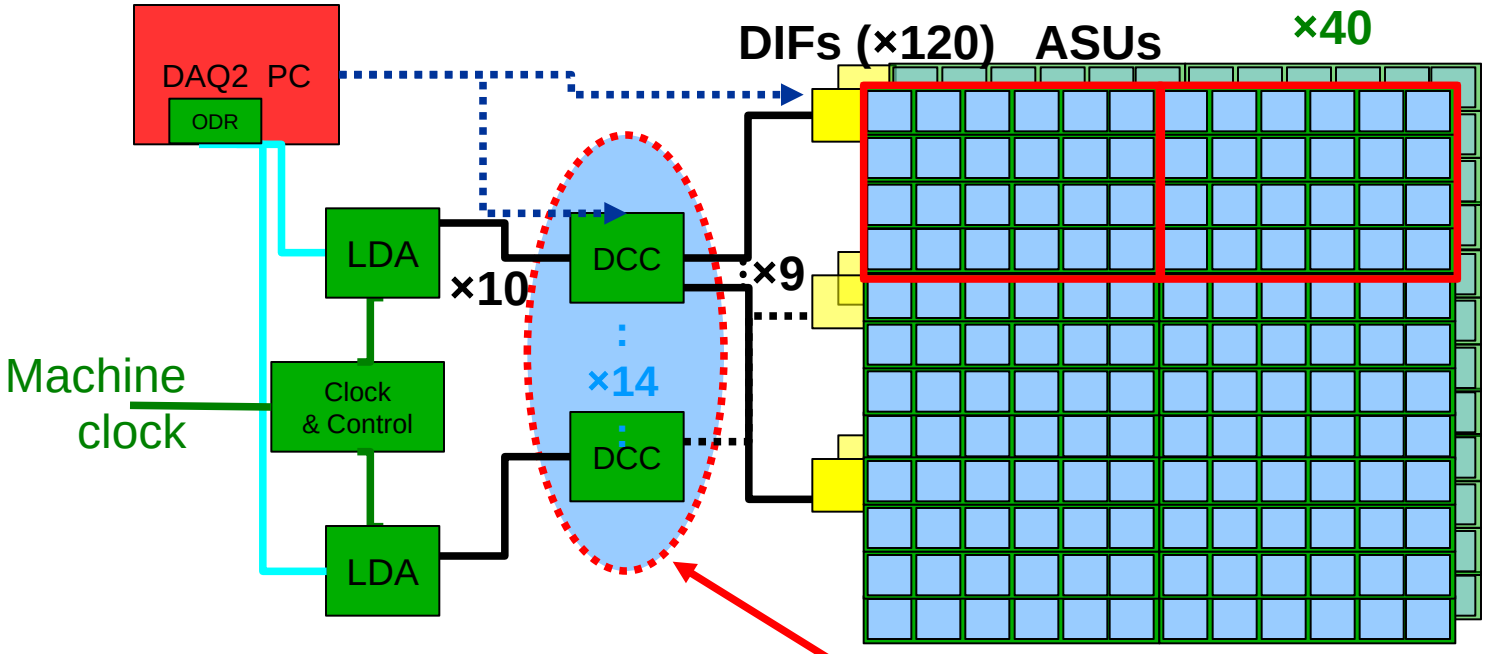
- Without DCC :

  3 Difs/layer (40 Layers)

  10 Difs/LDA => 12 LDA and 3 ODR

- With DCC, we need :
- 9 DIFs/DCC => 14 DCC => 2 LDA and 1 ODR
- Characteristics :
  - To be transparent between DIF and LDA
  - Broadcast all fast commands from LDA to all DIFs
  - Send the packet R/O one after the other
  - Read 9 DIFs (objective)
  - Availability of USB access
- Firmware : Re-use as far as possible existing VHDL blocks (Marc, Clement, Guillaume)
- Homemade card
  - Cheaper: objective (max 1000 € /card) for the production

# DAQ overview



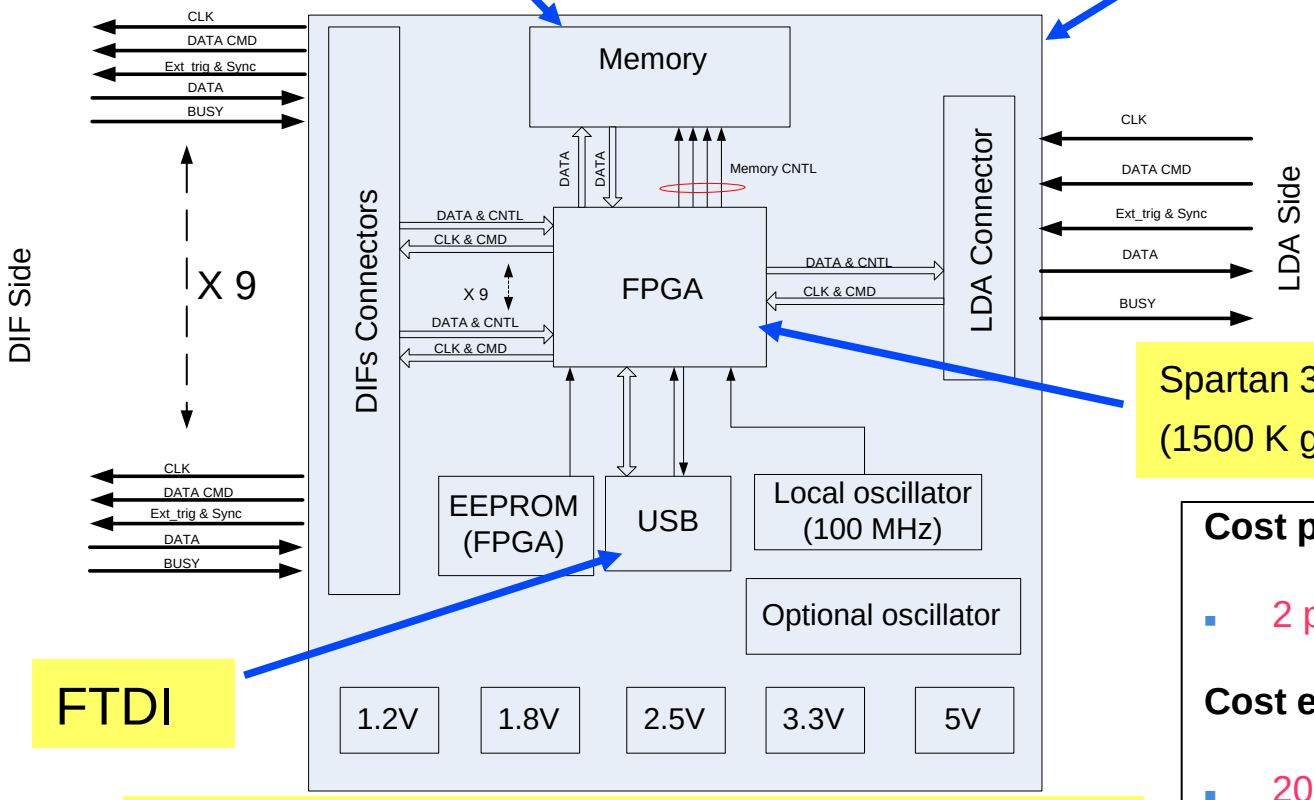

**Gain for DCC ≤ 1600€**

# Card overview

16×1M ZBT
(no latency BUS RAM)

DCC

Card size: VME 6U




Spartan 3
(1500 K gate)

FTDI

**Est:** 1.2A 10mA 400mA 2.25A 30mA

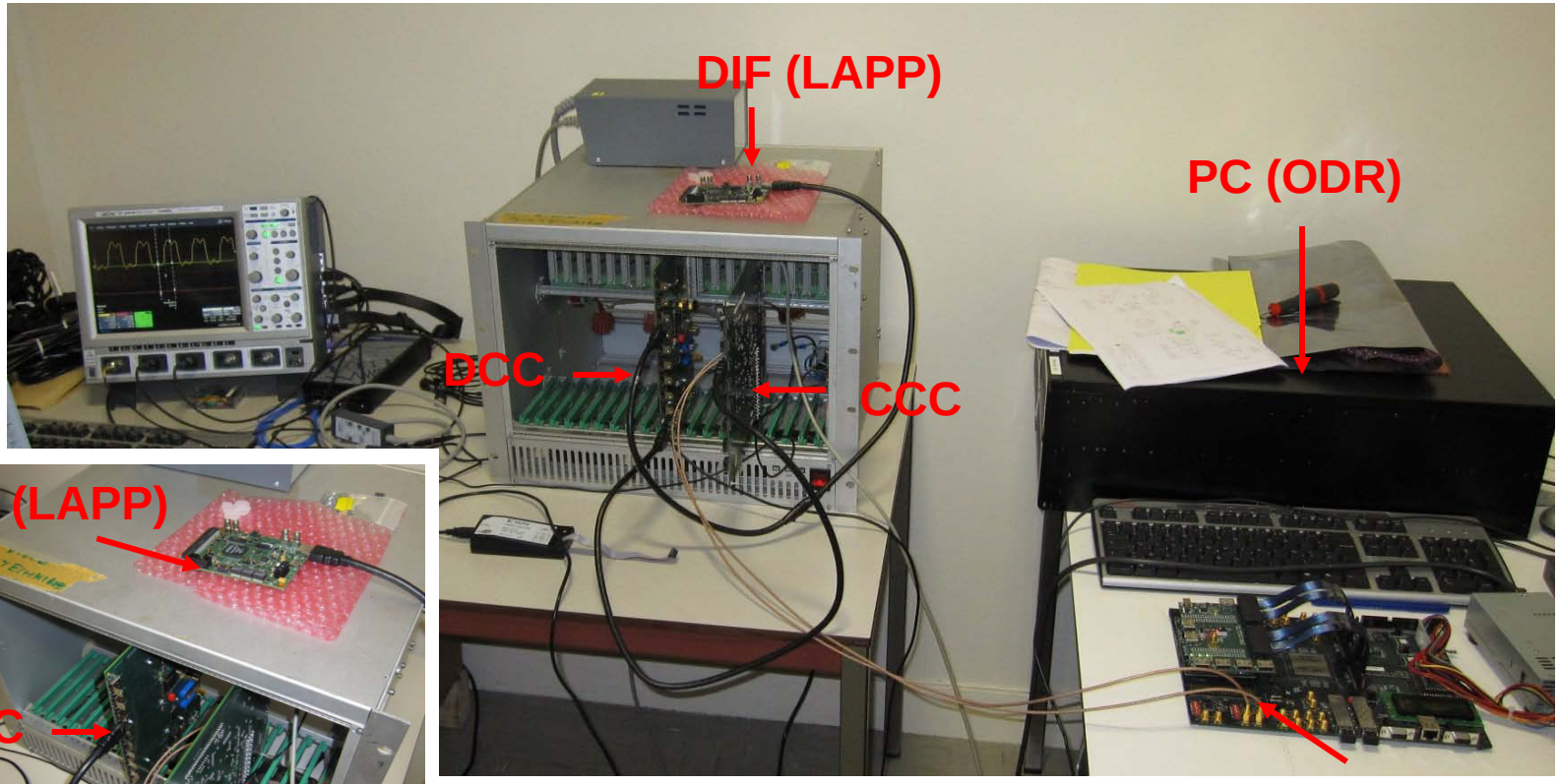
**Cost proto I:**

- 2 protos: ~ 19**00**€/card

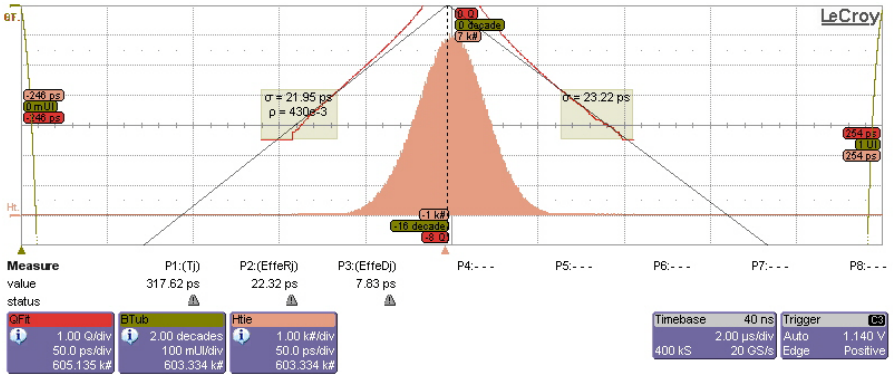
**Cost est.:**

- 20 prods: ~**600**€/card

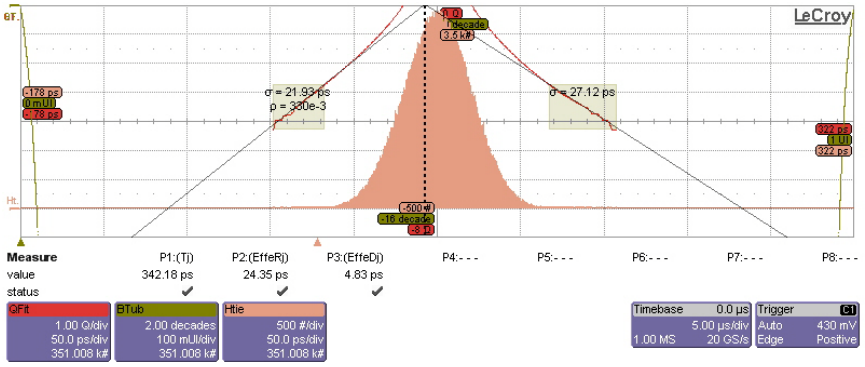
# Test Bench



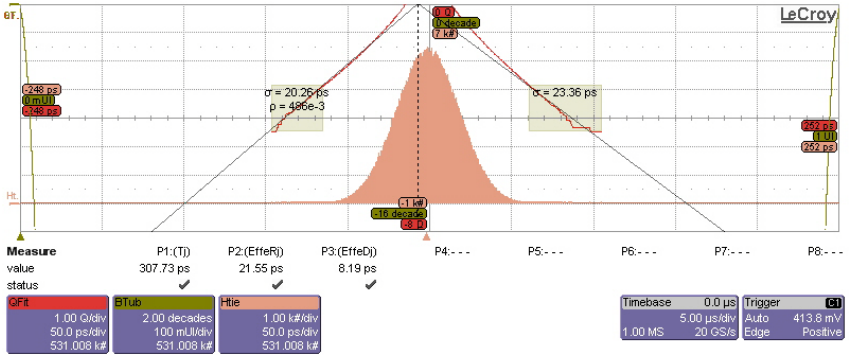
# First test (clock)
# ccc => dcc => dif




Jitter at the input of CCC

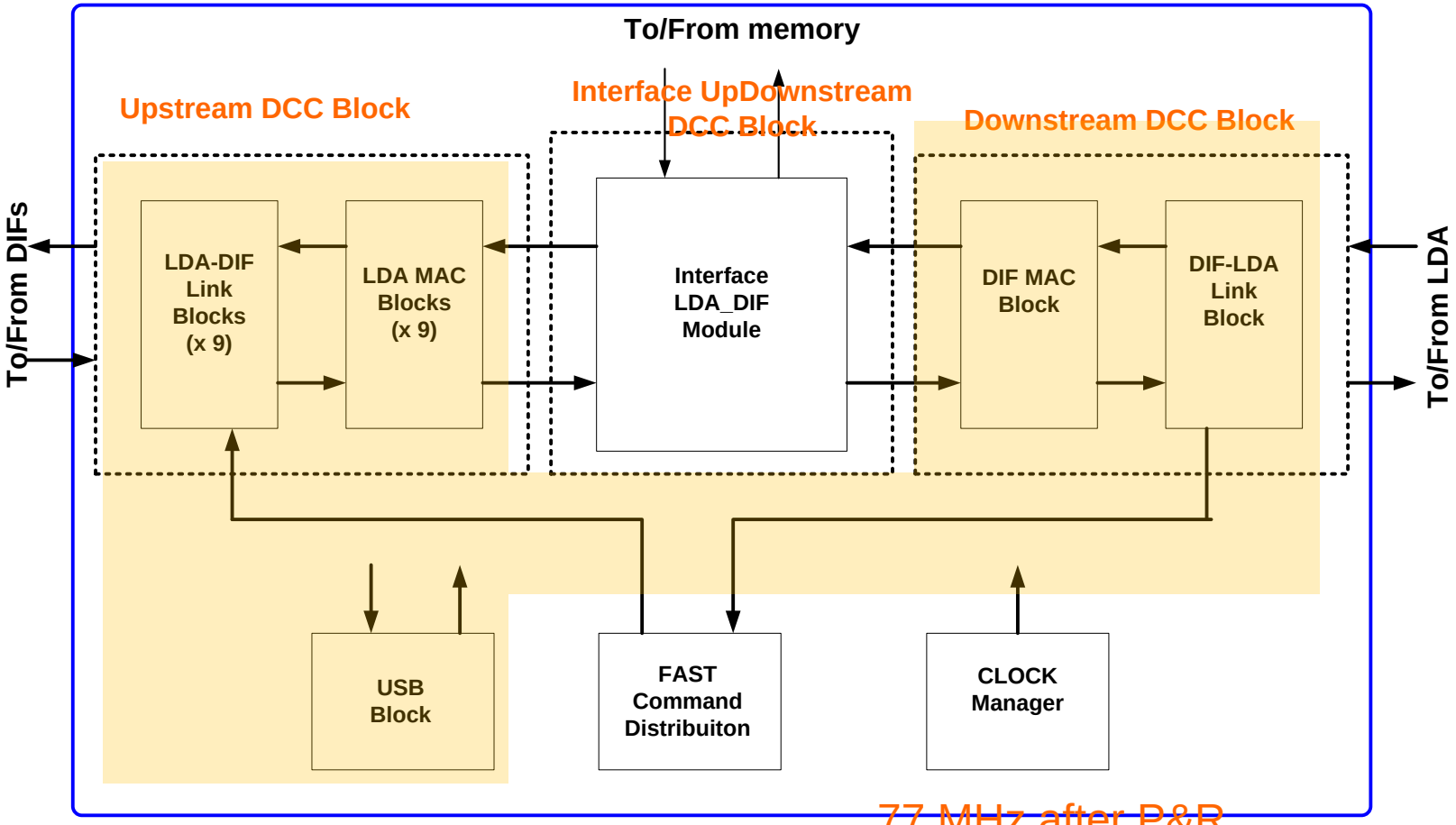



Jitter at the input of DCC




Jitter at the input of DIF

# FPGA architecture by functionalities




**TOP DCC**

77 MHz after P&R
Critical path is 8b/10b encoder
But we have a Spartan3 1500

# Design under test and planning estimation

We have the most of VHDL blocks and our To Do List is:

1 - Test the "LDA module" alone via USB

2 - Test the "DIF module" alone via USB

- June/July 2009: Simulation and implementation on DCC

3 - Test one channel DCC via USB

( LDA module – interface – DIF module)

4 – Test a true DAQ channel:

(DIF ⇔ DCC ⇔ LDA ⇔ ODR)

- Objective of first tests before September 2009

5 - Add one DIF and make the tests

6 - And so on…

# Few questions

Hardware :

Do we foresee a shunt resistor for the voltages connected on HDMI ? And who send this voltage ?

On the LAPP DIF, the voltage comes from the DIF side !?

On LVDS line, do we foresee an AC coupling ? (we then need a resistor bridge for the LVDS common mode)

Firmware:

The last modification made by Marc have improved the functionalities on LDA module used on DCC, however we have seen other problems and we shared it with Marc.

# Conclusion

- We are working on the first DCC
- Firmware is under implementation on DCC
- During summer:
  - Tests & validation of VHDL code implemented on DCC
- DCC Production
  - 2 months are required for the production and a cheap price
  - Due to some delays on the tests, production could be scheduled by the end of autumn 2009.

*Thanks to Remi for having represented me today for this talk*

# Back up

# DCC Firmware

**Our goals** :
Try to stay on standard with DHCAL/AHCAL/ECAL
Ensure the transparency between LDA and DIFs
Re-using as far as possible existing codes : For this, Thanks to Marc ,Guillaume and Clement for sharing their codes

- DCC functionalities:
  - Upstream block :
    - LDA-DIF link is the same than Marc (it's the LDA module)
    - LDA Mac block is on the same idea and uses a reference design from XILINX (Local Link FIFO)
  - Downstream block :
    - DIF-LDA link is the slightly modified DIF module (DIF packet is transferred in DIF Mac block)
    - DIF Mac block with the "DIF packet" is based on the same idea than LDA Mac block (XILINX reference Local Link FIFO)
  - **Interface Up Downstream block**:
    - Allows the selection of the channels to read and send the packet to the LDA. These packets must be clearly identified for a proper data organization by the software
  - USB block :
    - Used for debug or for a local test or to emulate a DIF or LDA.
  - Fast Command Block:
    - Received by the LDA and broadcasted on each DIFs.
  - Clock Manager :
    - We use the clock machine for the LDA-DIF link (LDA module) and DIF-LDA link (DIF module)
    - We use the local clock for the interface module.