

## FEV7/DIF testbench at LLR

Rémi Cornat

Marc Louzir

Antoine Mathieu

Michel Bercher

Chi-Chung Hsieh (student)

#### DIF

- Proto1
  - In use at cambridge
  - FW under dev. at LLR: try to sync. with Cambridge

- Eudet
  - Being tested at Cambridge

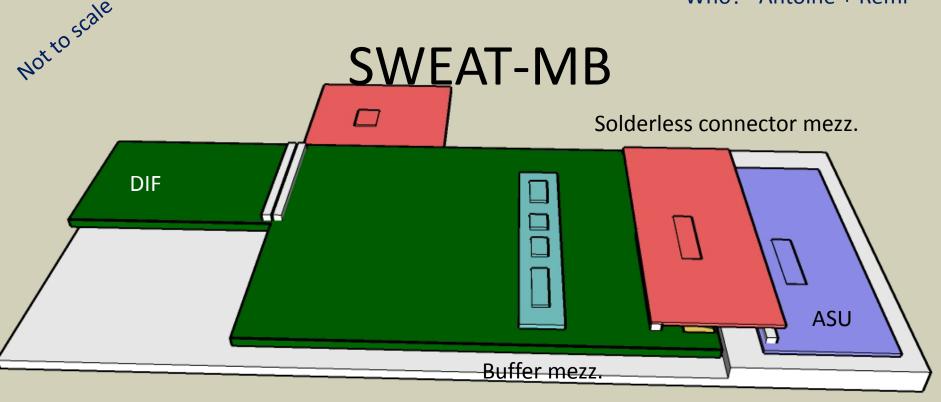
- DIFp for DCC tests
- DIFp DIFe

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june 1 1 nov 3 5-6 -----2010 feb 3 7 May 3 15 oct 3 30
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# adapter

- SWEAT-MB (Si-W Ecal AdapTer-MainBoard)
  - Main board
  - Mezzanine for Power, tx/rx buffers, connector development
  - Expected end of June (no mezzanines)
  - Also for Cosmic test bench
- SWEAT-Eudet
  - Version for eudet
  - Extended size (perpendicular tower)
  - Spring'10







### Y

- CCC (clk+trig) + DCC/LDA (data) to a single DIF HDMI connector
- Allows to work without LDA or with a DCC (no clk/trigger)
- Use of external generator
- Will have few of them



### Plans?

 We expect the FEV7\_CIP (Chip In Package) by mid june. We will enable a test bench for this board together with a prototype for the adapter board (doc sent to Bart&Maurice yesterday). It would be better if we could have a eudet DIF (DIFe).

Then we expect the FEV7\_COB (Chip On Board, bonded) by October. Most probably the test bench would be duplicated at LAL, so a 2nd DIFe could be useful.

Intermediate fake short slab based on FEV7 could be built with available thinks (no additional DIF required: same test bench).

The first FEV8 with 16 SKIROC2 could be available by the end of the year (time to test the chips, solve bonding issues, etc...). It means that the first short slab is not expected by spring'10. From spring'10 to winter'10 our need of DIFe will increase ie 10 in may, 20 in July, 30 in october following the production of slabs).



