



Ecal Front End Electronics Status

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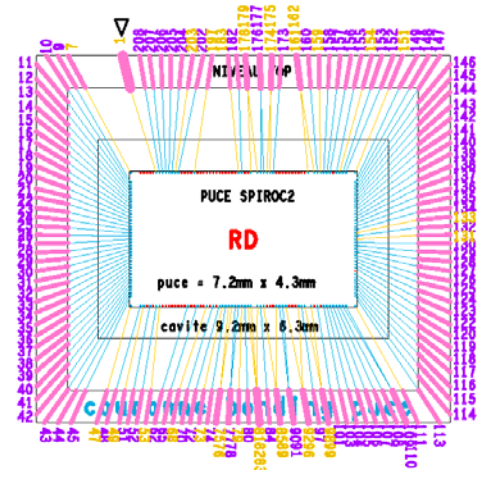
Chip Embedding



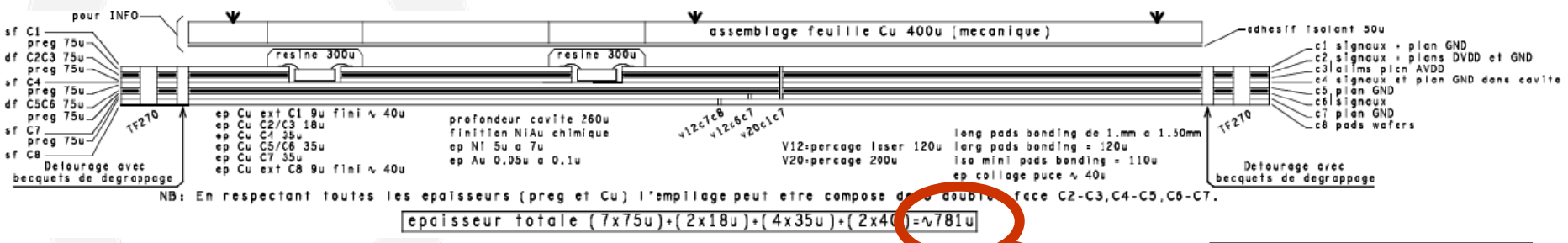
Pile-up

TOP	GND + Input chip signal
C2	horizontal routing + DVDD + GND
C3	AVDD
C4	GND + vertical routing
C5	GND (pads signal shielding)
C6	pads routing
C7	GND (pads shielding)
BOT	PADS

FEV 7
COB



- 4 drilling sequences :
- Laser C7-C8 120μ filled
 - Laser C6-C7 120μ
 - Mechanical C1-C7 200μ
 - Mechanical C1-C8 (for PCB fastening)

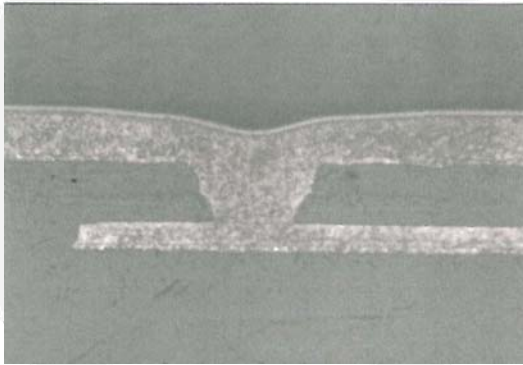


PCB Thickness
~781μm

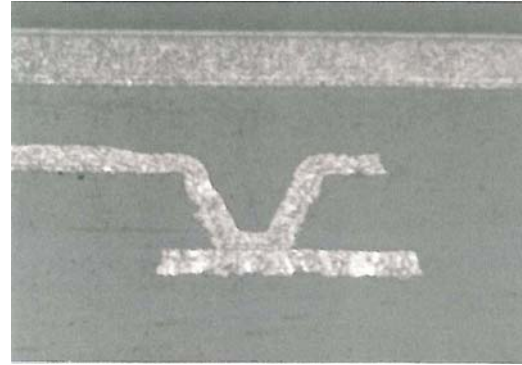
- Front End Board using Chip-On-Board
- Nearly Identical to Chip-In-Package
 - Schematics identical
 - Same number of channels
 - Same pinout on Adapter Board/Slab Connector
- Except :
 - Pads connections to chip pins
 - Position of Wafer on the bottom side
 - Packaging of the Chip (!)
 - Thickness thinner to comply with H alveolar structure
- Layout finished
 - Send to Manufacturing next Thursday
 - Need to buy new chip to foundry

FEV7_COB 0901	XXXXXX	QTE 10	QTE 50	QTE 100	OUTILLAGE	QTE 10 TOTAL HT
APPARATUS						
ELVIA	03--06	2774	10140	19890	850	3621
PROTECNO	27--05	4400	13400	25100	521	4921
ELCO	19--05	5230	15050	21800	1130	6360
PHOTOCHEMIE	02--06	10290	30800	61600	614	10904
EXCEPTION	X	X	X	X	X	X
ATLANTEC	X	X	X	X	X	X
CERN	22--04	4700	X	X	660	5370
le 03/06/09 D.CUISY CAO/LAL/ORSAY						

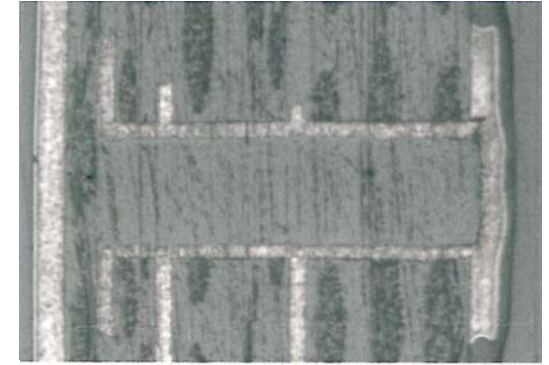
- 2 Manufacturers :
 - Elvia : 10 PCB received last week
 - Protechno : 8 PCB expected next Thursday
- Manufacturers report :
 - Thickness Measured : 0.90mm to 1.00mm (0.96 desired)
 - Metal minimum thickness on vias : 25 μ m
- Plated Through Hole Cross Section :



Blind via (C7-C8)



Buried via (C6-C7)



Mechanical (C1-C7)

- 11 SPIROC2 chip in TQFP available
 - 1 board will be equipped with 1 device
 - 1 PCB will be assembled with 4 chips
 - No way to test the devices before !!
- On the board, we have access to :
 - Analogue Output
 - DAC and Bandgap Output
- Immediately after cabling, close work with LLR :
 - Need of SWEAT-MB and DIF Boards (-> see Remi's talk)
 - And also software/firmware (!)

- First Step : Electrical tests (continuity / shorts)
- Second Step : Slow Control Loading
- If OK, we can start real tests ! 😊
 - Check all Analogue Channel Outputs
 - Ensure Discriminators, Masks, Calibration Tests Input work accurately
 - ADC Tests
 - Analogue and Digital Measurements
- Then, tests with 2 PCBs
(-> need interconnection techniques)
- Finally, tests with Wafers ?
(-> need of wafer/pcb assembly)

- We should have 1 or 2 PCB ready for the 30th June
 - (Eudet deliverable : 30th June 2009)
 - Lot of debug to do...
 - FEV7_CIP is a small step but a giant leap for FEV7_COB!
- > Look forward to FEV7_COB for a complete working SLAB

Backup Slide : FEV7 Board(s)



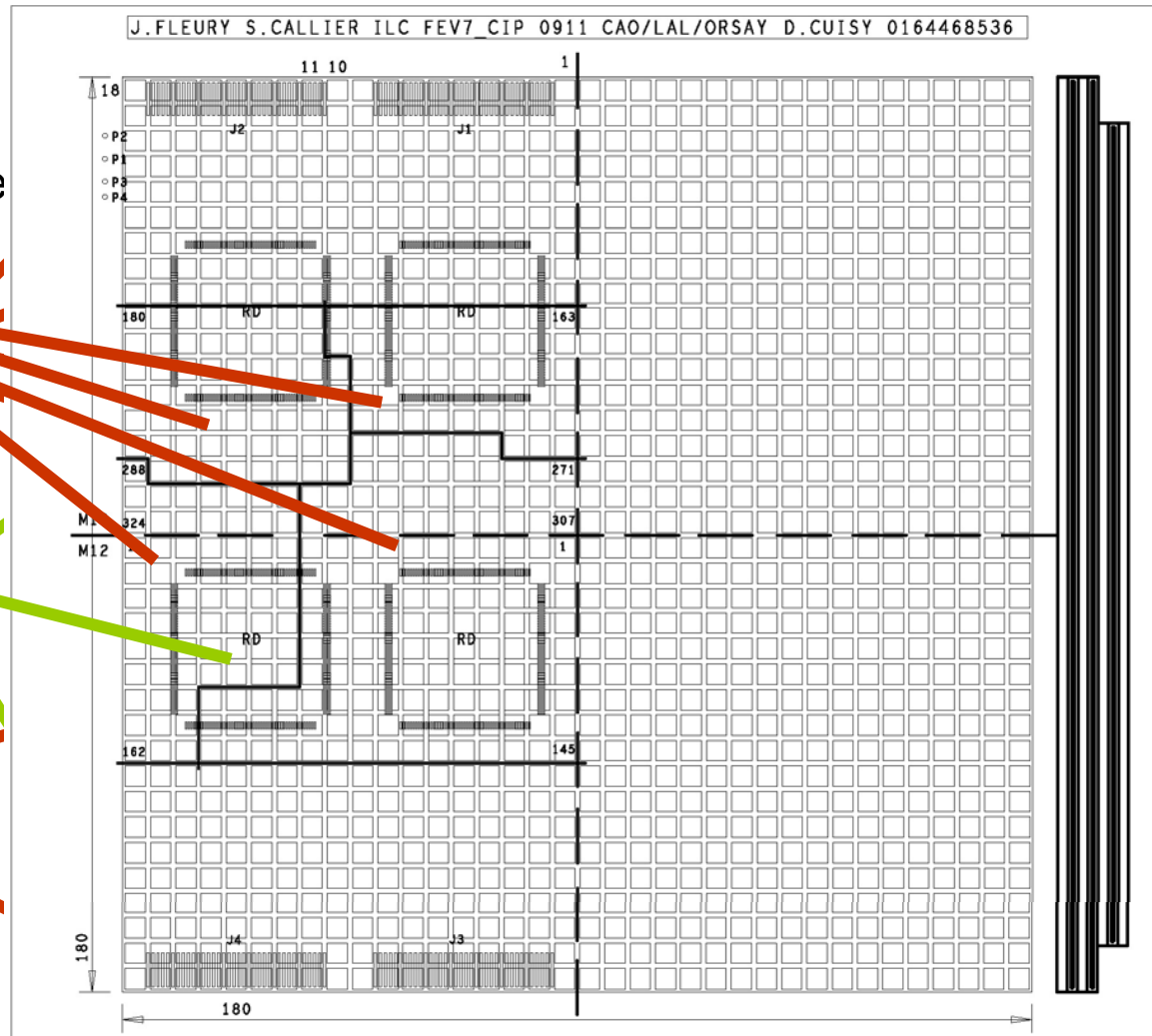
FEV7 board
 5 mm x 5 mm pads size
 180 mm x 180 mm Wafer size
 -> 324 pads on a 1/4 board
 2nd board!

36 channel areas
 use of SKIROCZ (36 ch)
 in SKIROC mode
 -> 144 Channels (4 x 36)
 will be used for Wafer
 Characterization

Chip on Board

Why such a board?
4 PADS merged
 - Due to the troubles with
 FEV5 manufacturing
9 PADS merged

Purpose :
Wafer footprint
 - EUDET deliverable
 - Allow SLAB + DIF debug
 - Allow mechanical integration



Epaisseur max CI 12/10 CI 8 couches

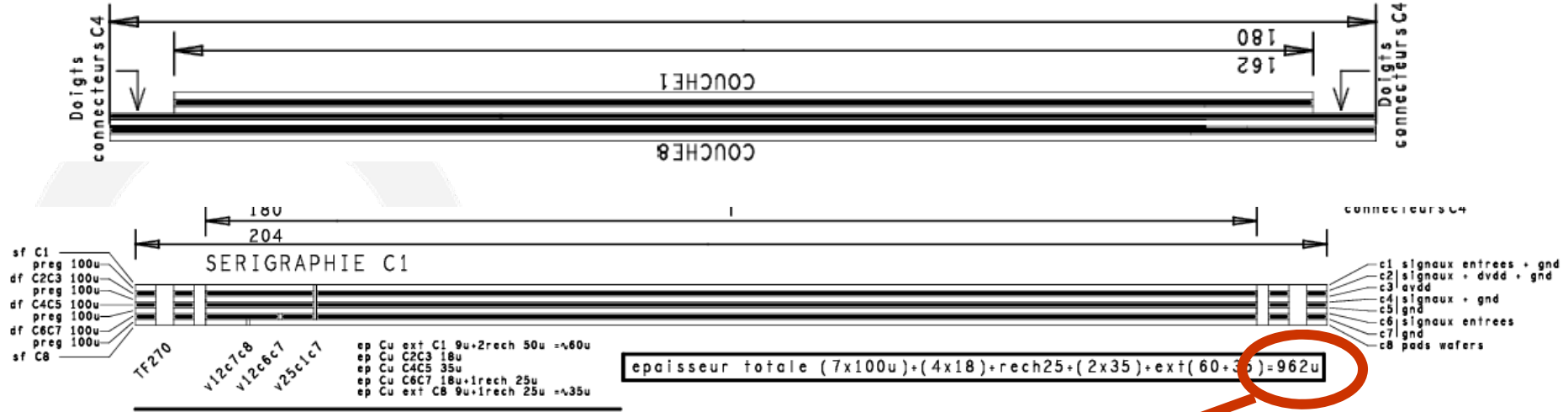
Chip Embedding + Final PCB Pile-up



Pile-up	
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**FEV 7
CIP**



PCB Thickness : 962μm

- Board Stack Up



		Unit of measurement	µm	
LAYER	TYPE	THICKNESS requirement	TOLERANCE requirement	THICKNESS MEASUREMENT
1	Clad copper	9+50		6+35
	Dielectric	100		98
2	Clad copper	18		15
	Dielectric	100		100
3	Clad copper	18		15
	Dielectric	100		90
4	Clad copper	35		8+22
	Dielectric	100		105
5	Clad copper	35		30
	Dielectric	100		100
6	Clad copper	18		30
	Dielectric	100		95
7	Clad copper	18+25		6+20
	Dielectric	100		65
8	Clad copper	9+25		6+35