Status of DIF, DAQ for SiW Ecal

Brief overview of:

DIF status

LDA status

DAQ (ODR & software) status

For extensive and more detailed information: look elsewhere in UCL

ECAL DIF status: hardware

DIF prototype II: smaller than a credit card (in at least 2 dimensions)

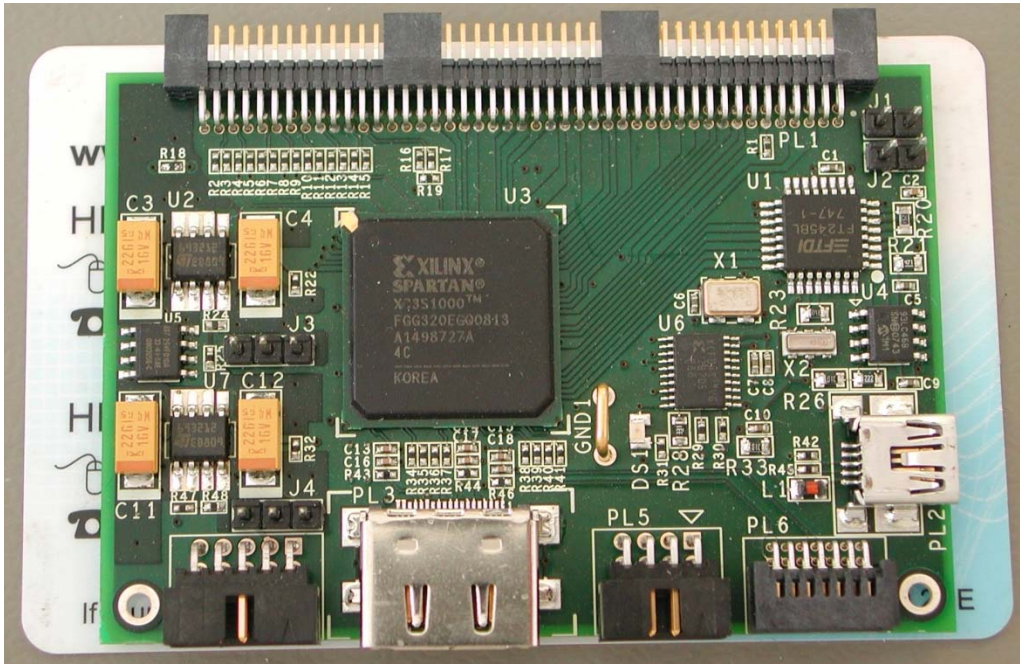
Going from v.1 to v.2: few components went. Main FPGA is the same: Xilinx X3S1000

Power envelope identical to V.1

2 DIFs fully populated:

- Powered up OK
- Test firmware being ported

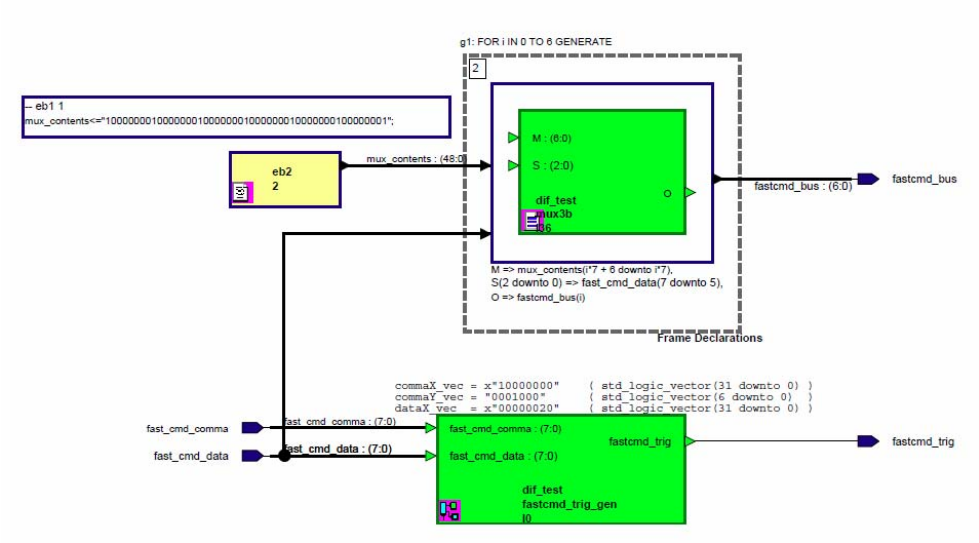
Components & PCBs in house for full production of 40x

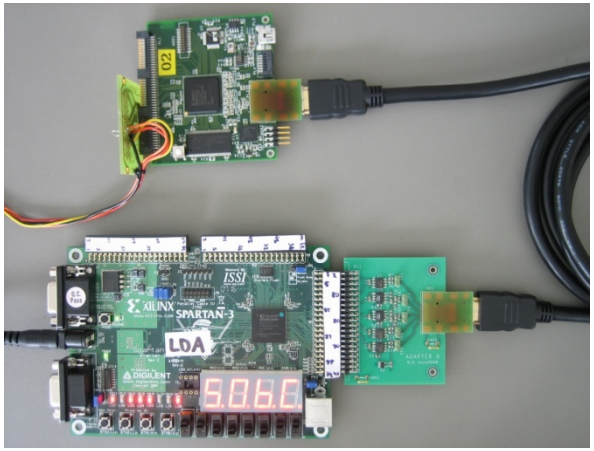


Main changes wrt V1 proto:

- DIF powered from rear edge, has regulators on-board. (not unlike HCAL DIF)
- Analog channels have test points (top right)
- No SRAM but serial Flash-RAM
- 10MHz Xtal for local clock generation
- side-mounted USB for testing and stand-alone operation

ECAL DIF status: firmware

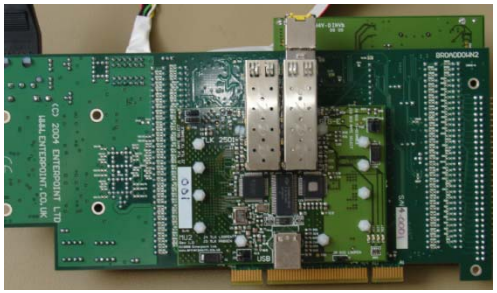




Stable version for DAQ test

- Provides pseudorandom fake data
- Reacts on fast commands from LDA
- Data format being updated to proposed DIF data format
- Fast commands:
  - Reset Spill counter
  - Increment spill counter
  - Send single packet
  - Send (random) multiple packets
  - Continuous sending of packets
- Verified & tested in hardware –using fake LDA

LDA Status: hardware



Many hardware issues now resolved: 3 LDAs being tortured here & now(!)

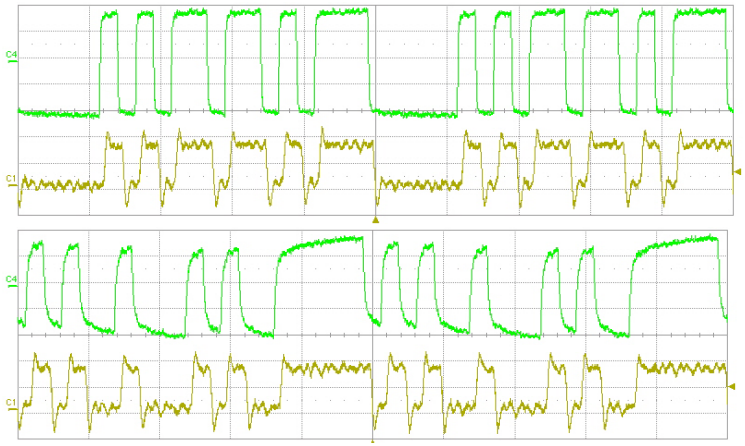
Production lot:

- Baseboard rev.II now at Manchester
- Ethernet add-on boards now in production
- HDMI boards now ordered (20 off)

HDMI board: implementing full AC-coupling would have required a re-design (time, £££)

- Alternative AC coupling with reduced component count studied, seems to be OK
- Link requires to be 'always-on': send comma characters when idle, otherwise first bits will be missed

2m cable, full AC coupling

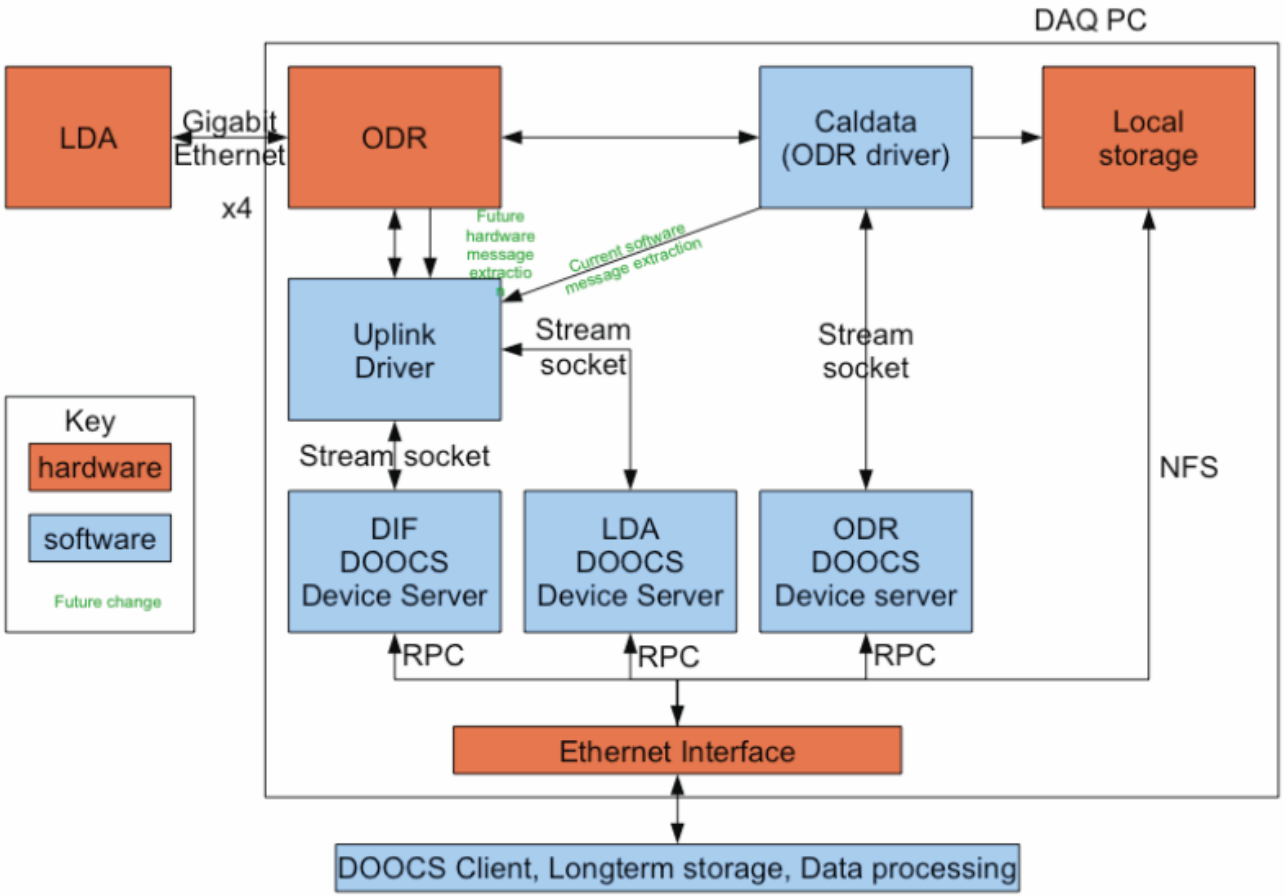


15m cable, reduced AC coupling

LDA status: firmware

- Whilst waiting for hardware: LODDAR test vehicle used for firmware & software development
- ODR-LDA path well established in both directions
- LDA can now talk to DIF as well
- Core functionality seems OK
- Under test at the moment – using real LDA hardware!
- Ask Marc/Matt/Barry if you want to have a look
- More news tomorrow?

DAQ-PC & Off-Detector Receiver



- ODR-DOOCS a well integrated tandem: stable firmware & software
- End-user Software development ongoing

ODR & Software status

Off-detector receiver - DAQ PC resources

- ODR programming manual
  https://www.pp.rhul.ac.uk/twiki/bin/view/CALICE/OffDetectorReceiver4Guide
- ODR firmware description
  https://www.pp.rhul.ac.uk/twiki/bin/view/CALICE/OffDetectorReceiverFPGAFirmware
- Caldata user guide
  https://www.pp.rhul.ac.uk/twiki/bin/view/CALICE/CaldataUserGuide
- DAQ PC experts
  b.green@rhul.ac.uk
  warren@hep.ucl.ac.uk
  misiejuk@pp.rhul.ac.uk
- Software & Firmware CVS
  http://isscvs.cern.ch/cgi-bin/cvsweb.cgi/Stage1/?cvsroot=caldaqwp2.5
  http://isscvs.cern.ch/cgi-bin/cvsweb.cgi/ODR/software/?cvsroot=caldaqwp2.5

  CVS web access is only available to web browsers running within CERN subnet.