AHCAL Electronics.

Status EUDET Prototype

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for the DESY AHCAL developers
EUDET Electronics/DAQ meeting
London, June 9th, 2009

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

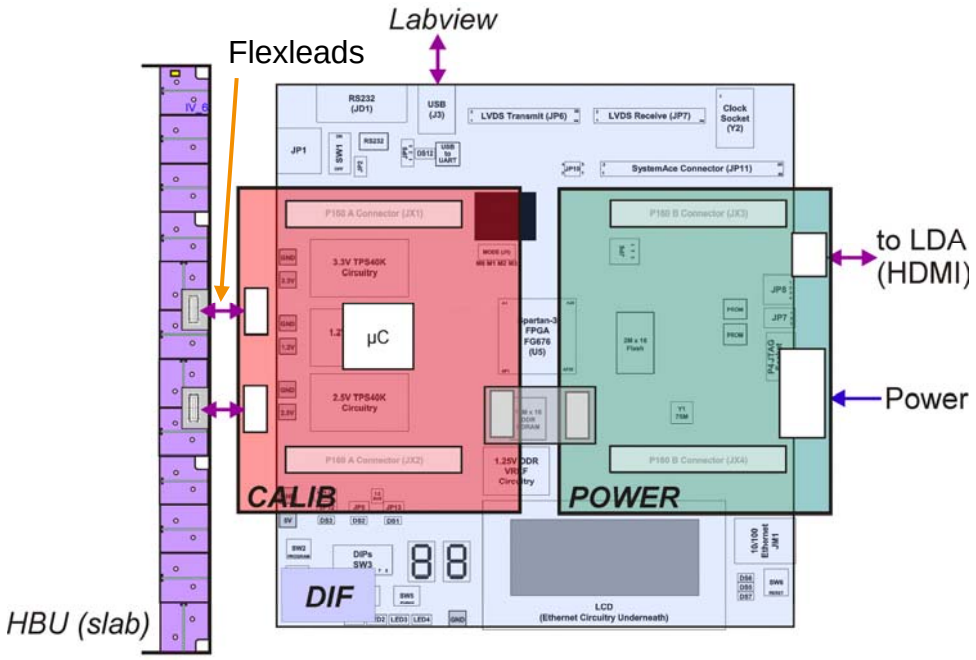
EUDET

DESY

Outline

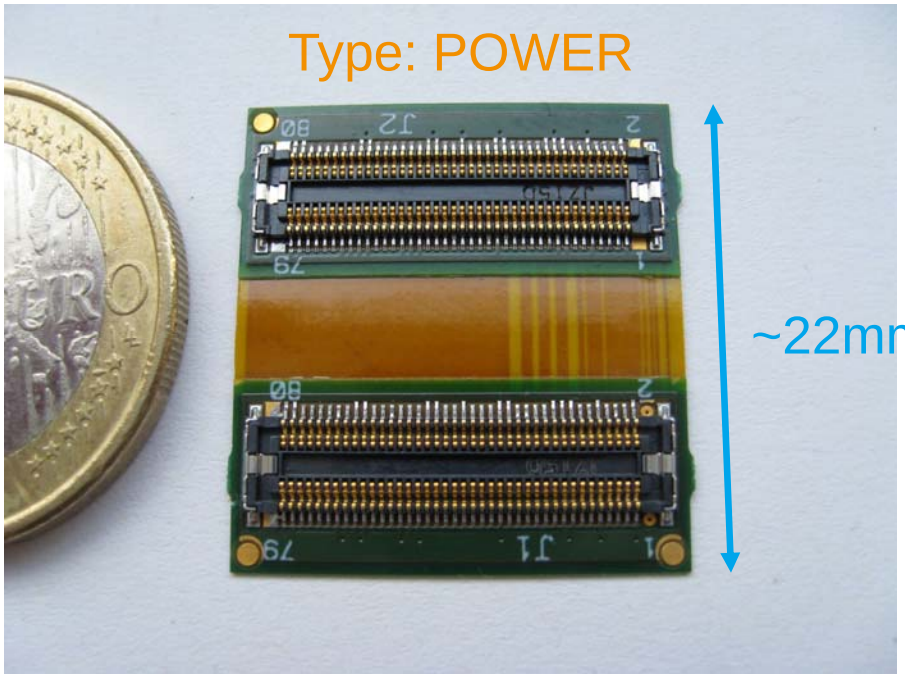
- Hardware Developments at DESY
  - CALIB, POWER, Flexleads
  - HBU0
  - DIF0 and DAQ interface (USB)
  - Tiles integration
- System Commissioning
- Conclusions and Outlook

‘old-fashioned overview’

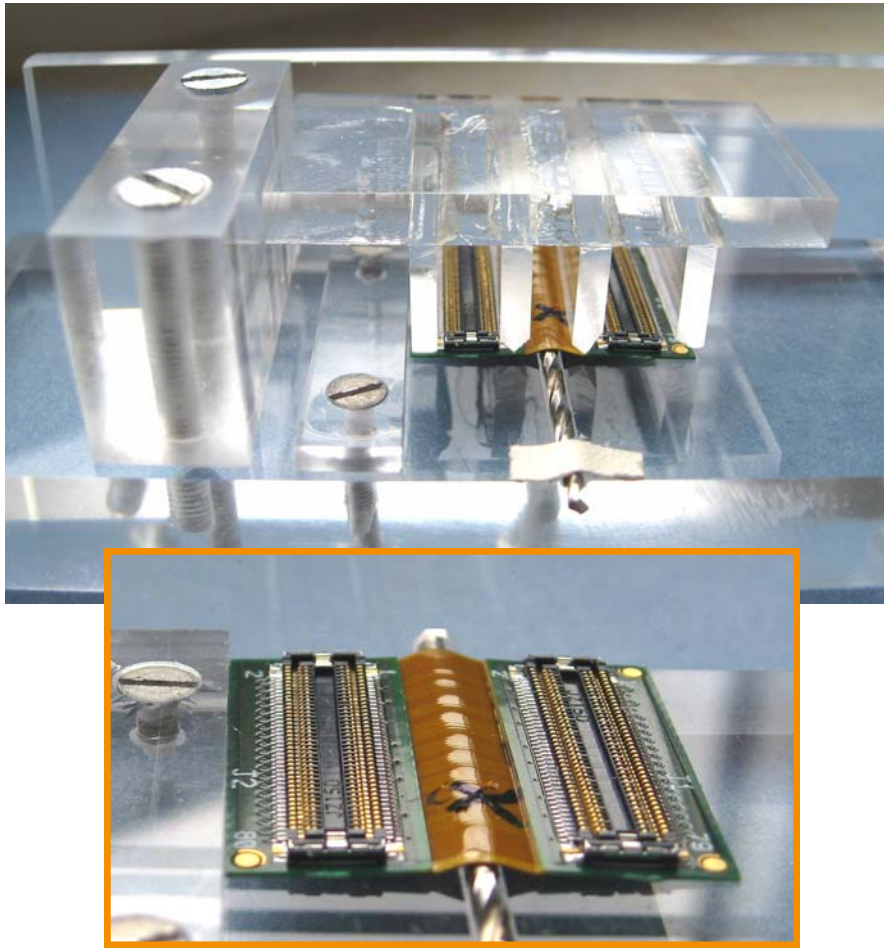


Flexleads (SIGNAL and POWER)

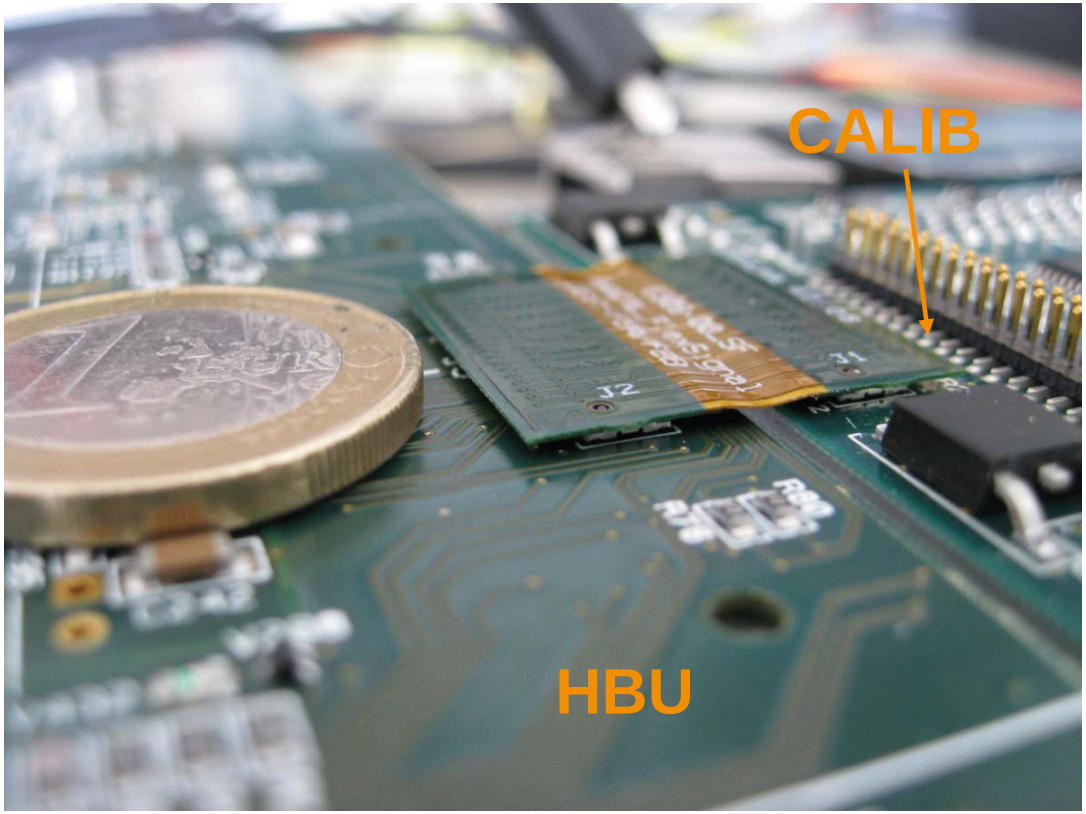
- 20 pieces of each type finished.
- Pre-bending procedure ok.



Flexlead Pre-Bending:



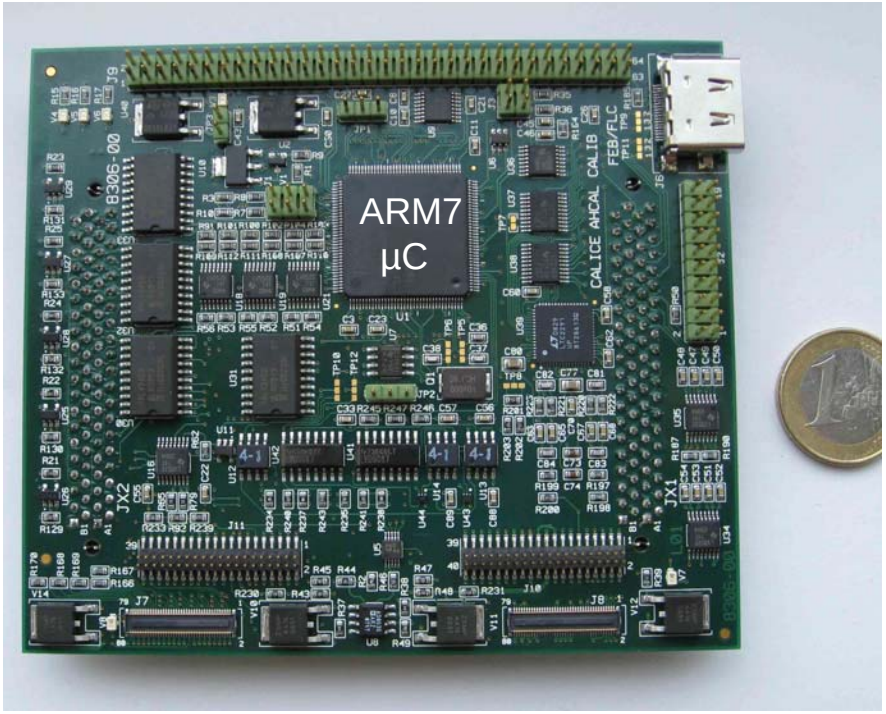
Flexleads (SIGNAL and POWER)



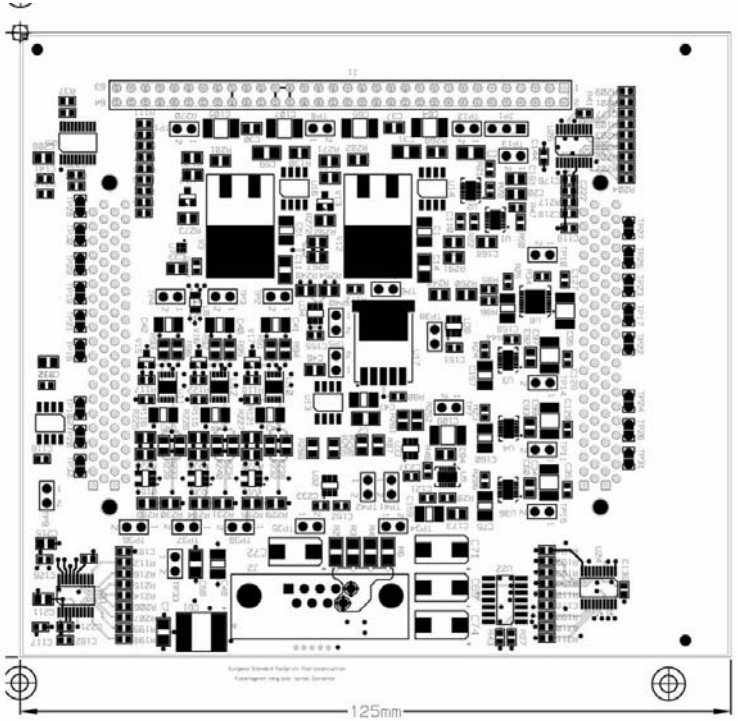
- About 40 connection cycles up to now - still ok.
- Compensate HBU misalignments in distance.
- Fulfill AHCAL height requirements.
- Tests ok concerning:
  - Signal allocation
  - Signal quality
  - Resistance for power

CALIB and POWER modules

CALIB module: 11 x 10 cm²



POWER module: 12.5 x 11 cm²



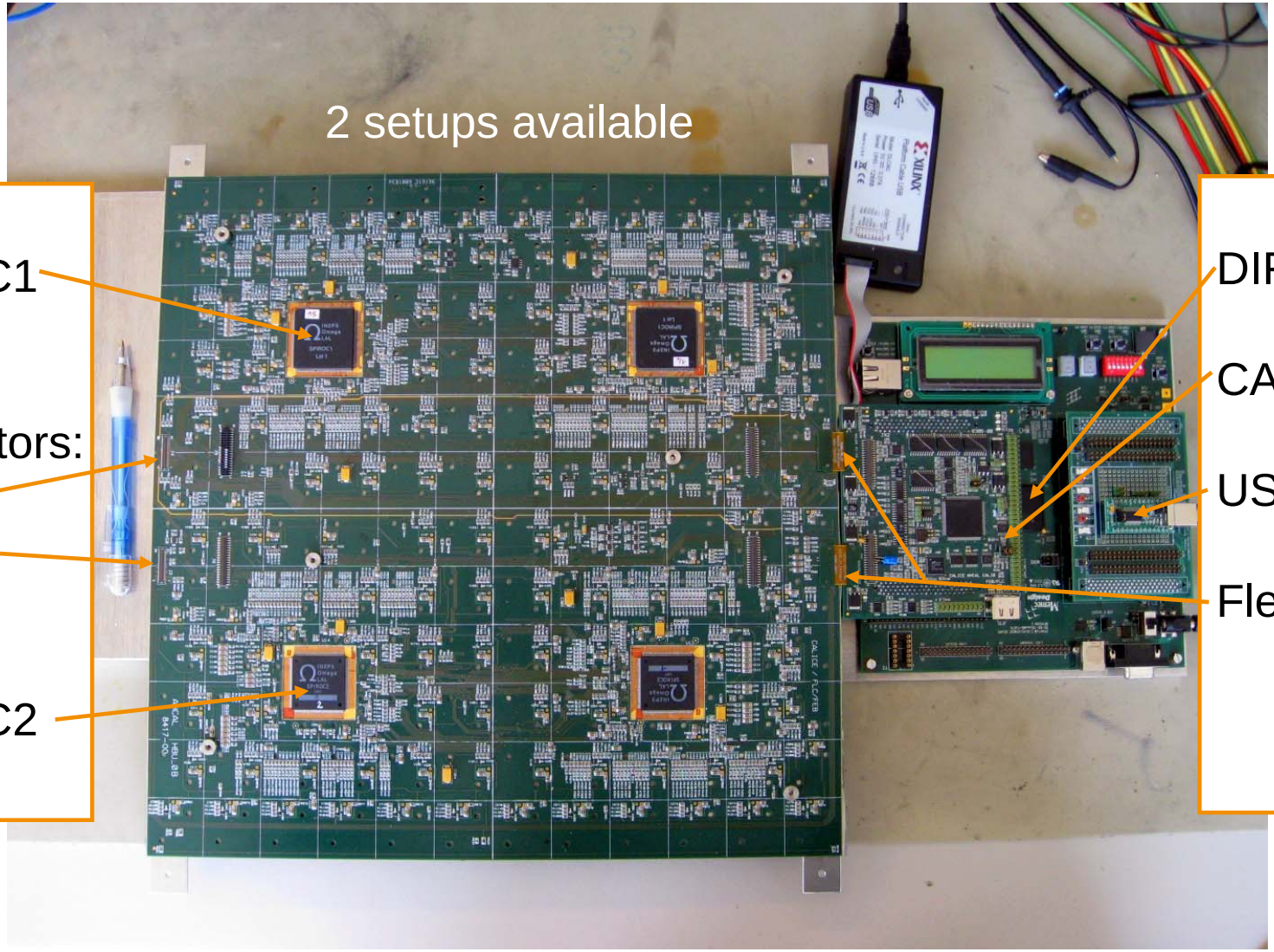
> 4 Modules finished, in operation.
> First tests successful.

> In production.
> Expected end June.

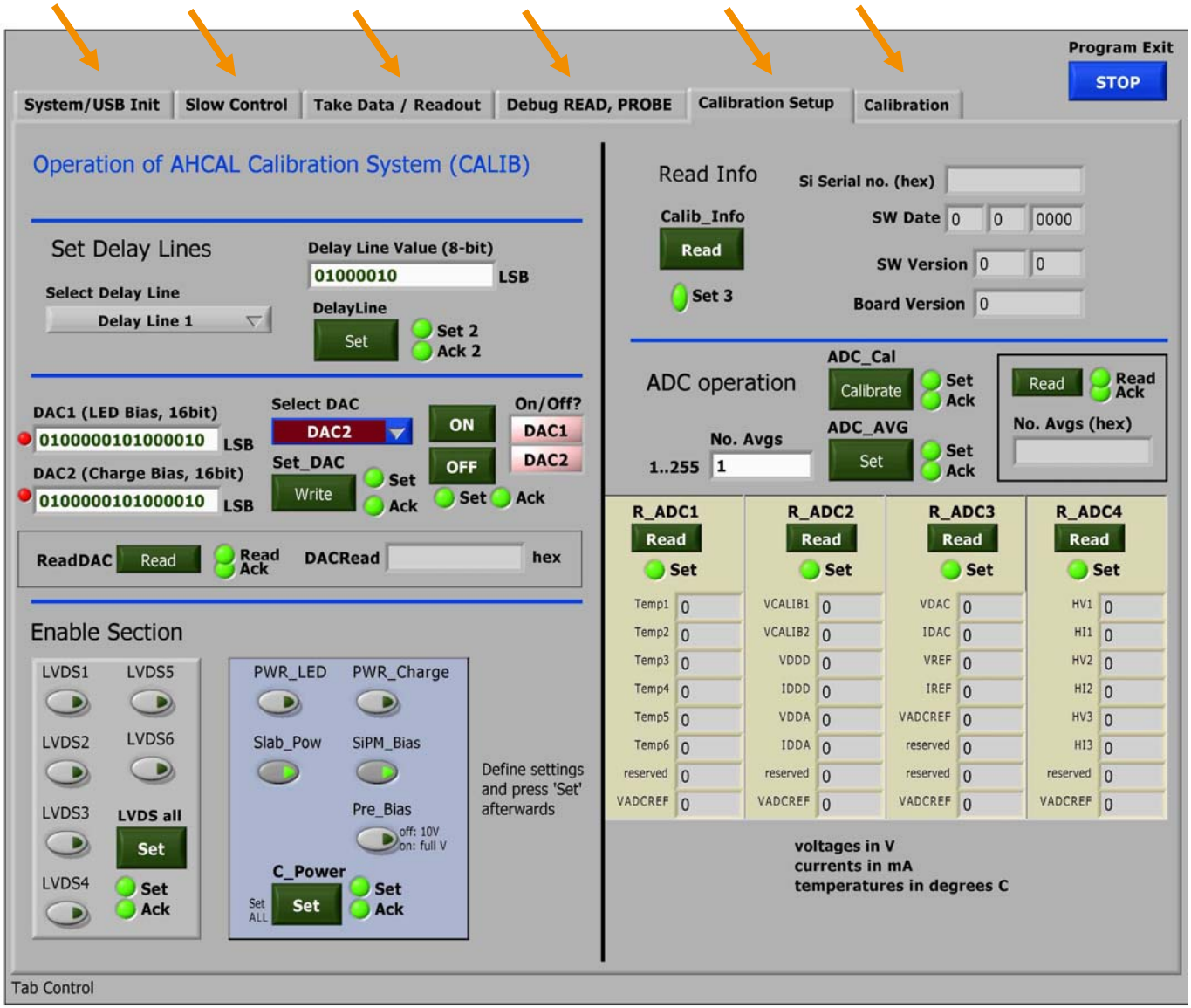
Sizes and heights: To be adapted to ILC mechanics later.

CALIB: M. Zeribi,
POWER: H. Wentzlaff

HBU0 status


2 setups available
SPIROC1
Connectors:
Signal
Power
SPIROC2
DIF FPGA
CALIB
USB / DAQ
Flexleads

Labview Control of the Prototype System

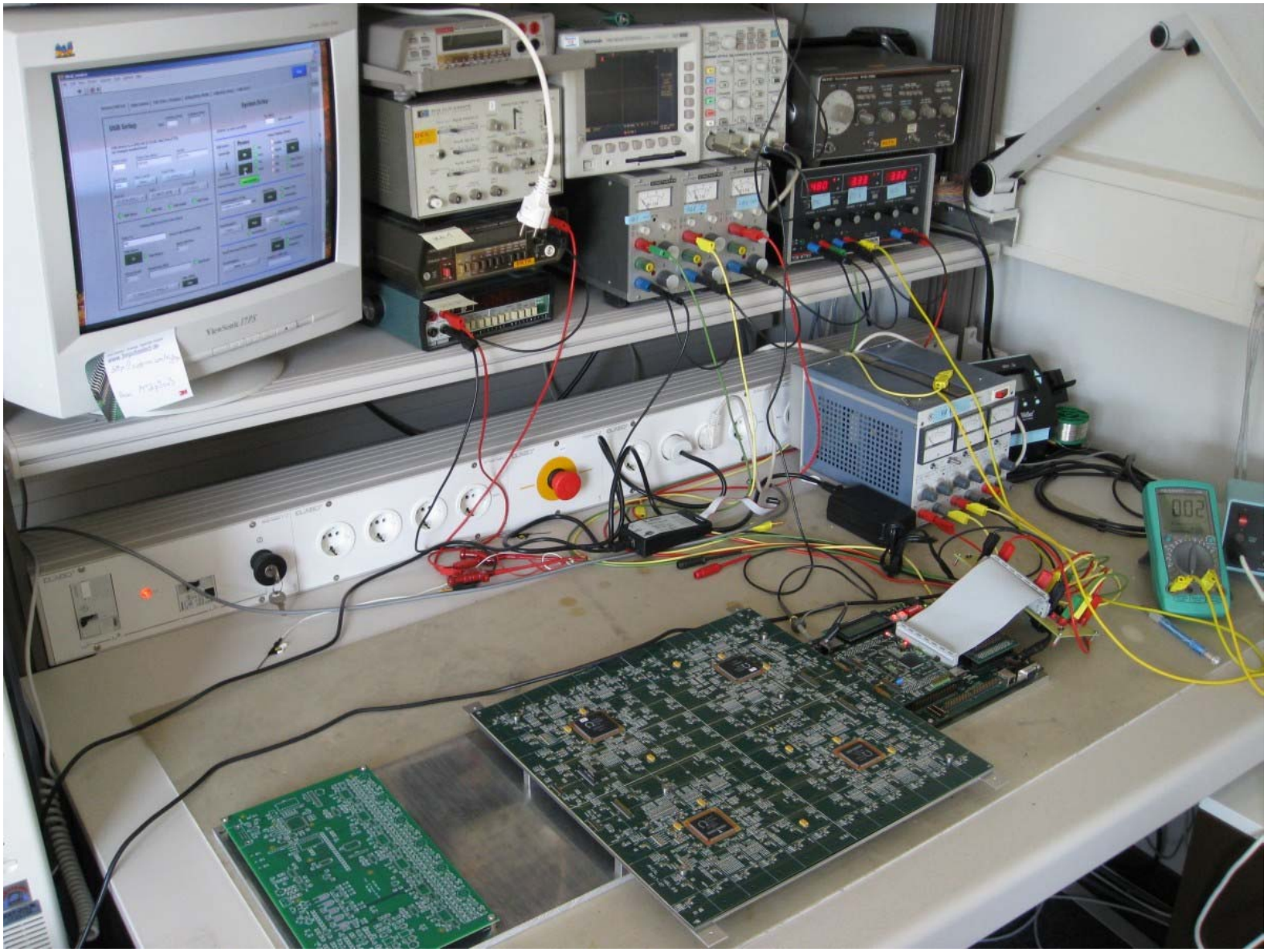


AHCAL: Focus on:

> USB Interface
> Slow-Control
> Take Data
> Readout

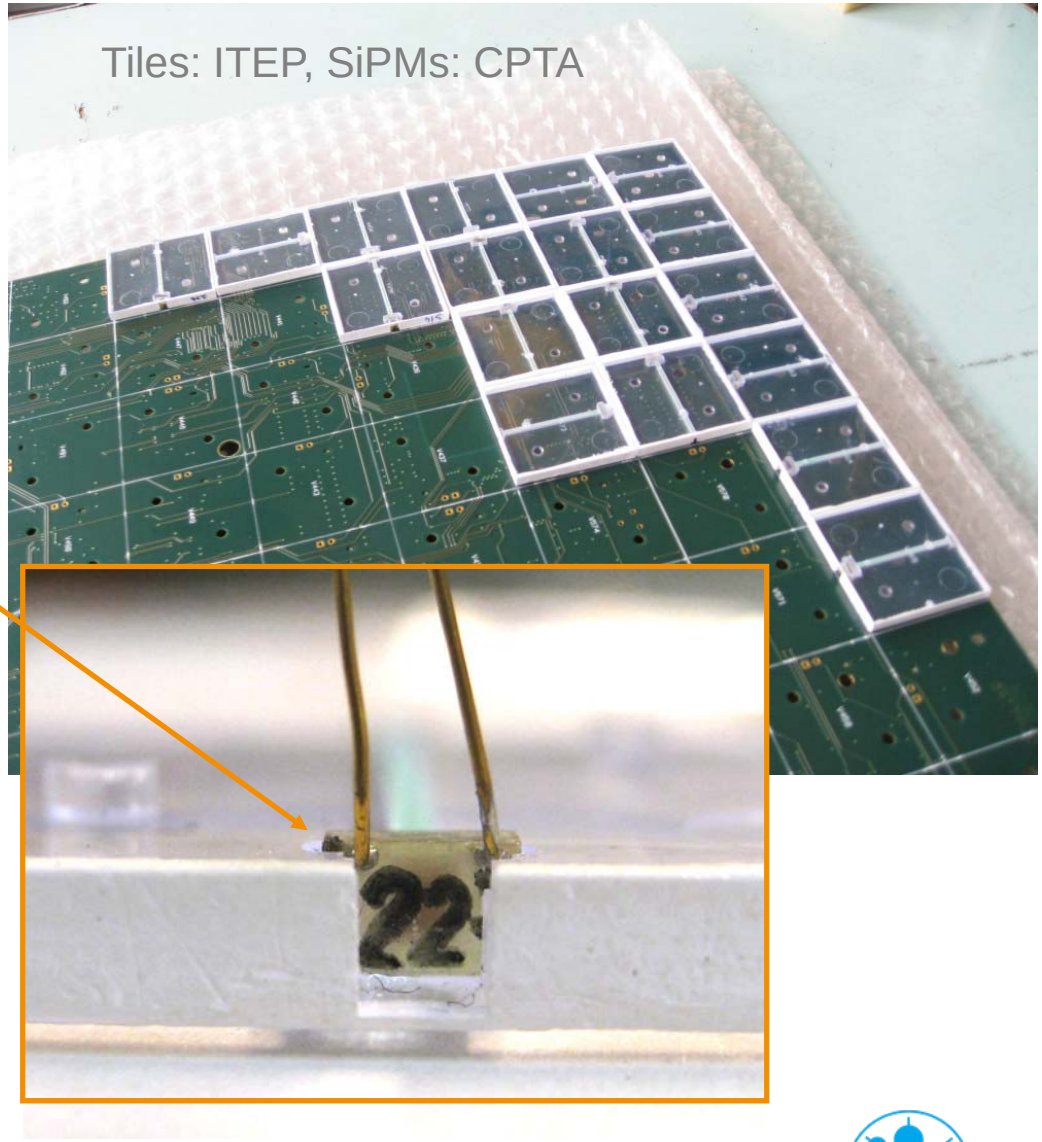
>Current Version: 20

Prototype System Commissioning



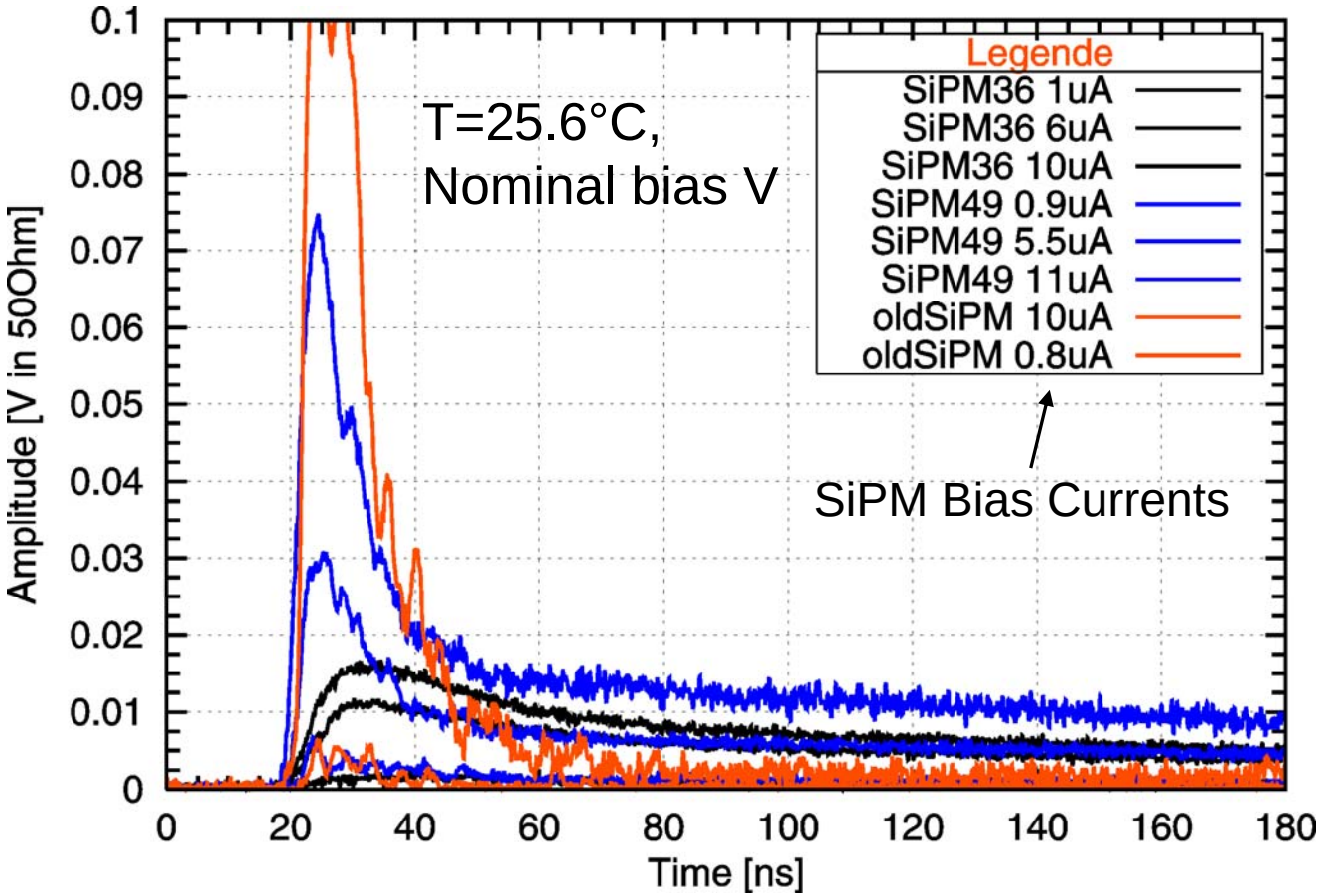
Tiles Interconnection Test

- Tiles not connected yet (HBU electrical test first).
- Test assembly shows:
  - Strong force to SiPM pins during assembly.
  - A few SiPMs cases are too large (only a few!).
  - Mirrors are too large, but can be cut.
  - Alignment concept (-pins) works!!



SiPM long tails - LED Test (3 light intensities)

19% of SiPMs show pulse responses wider than 50ns.



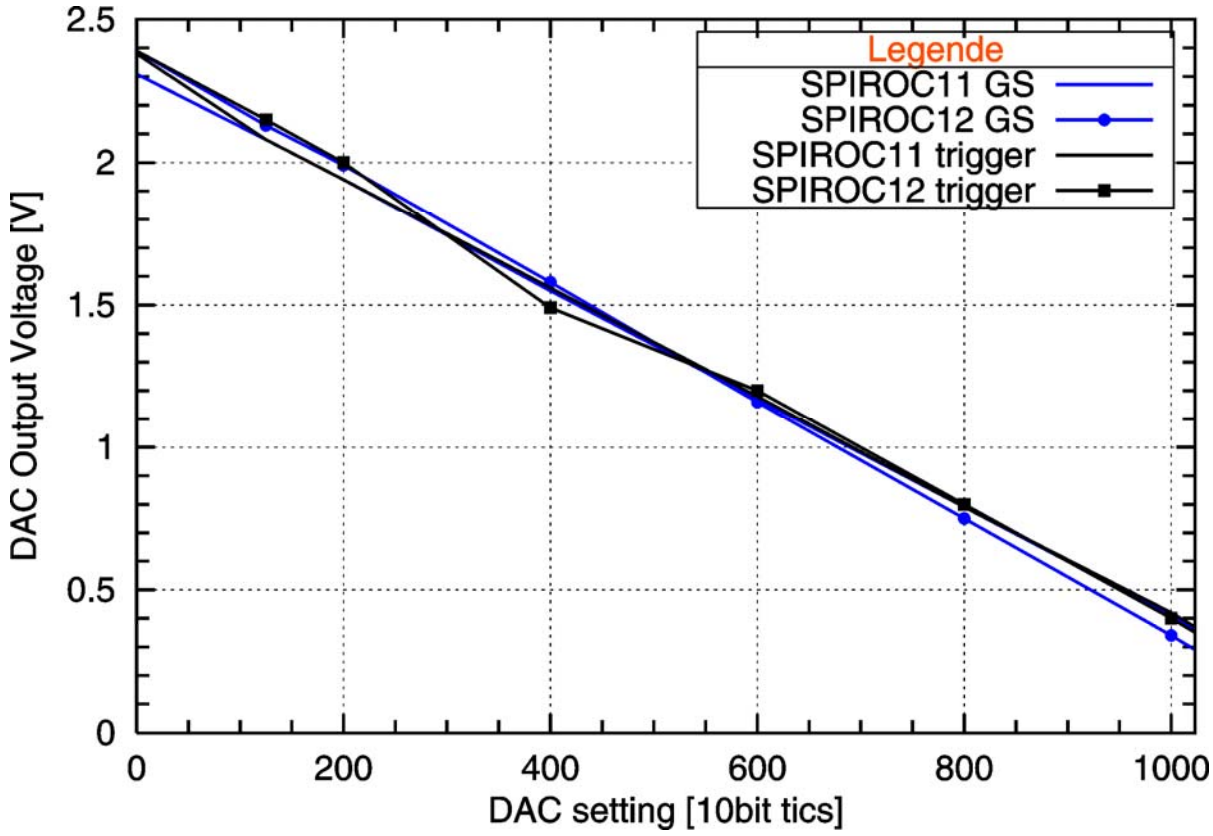
SiPM36: long tail
SiPM49: good

oldSiPM: 6x6 tile with SiPM 538

System Commissioning – Slow Control (SC)

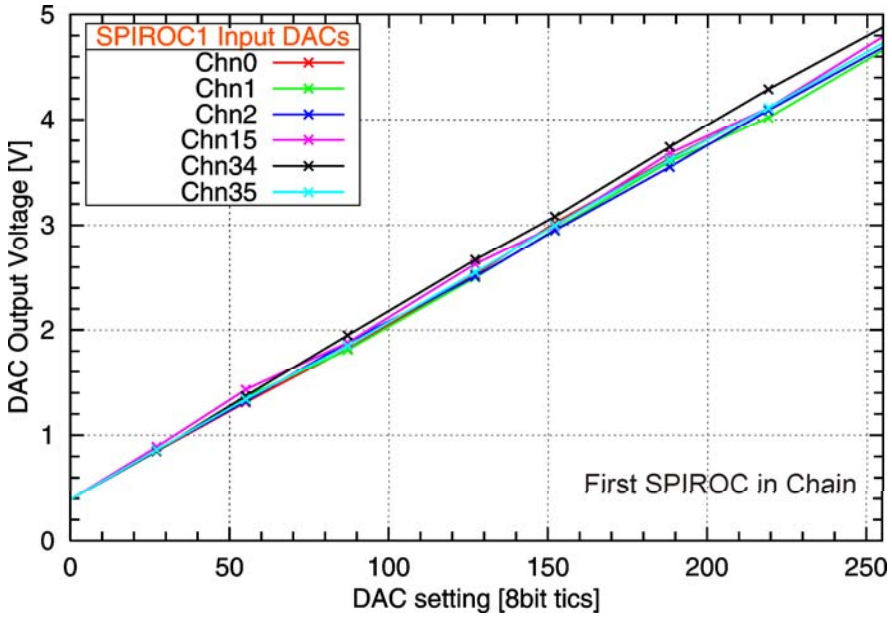
Discriminator DAC Outputs (10-bit)

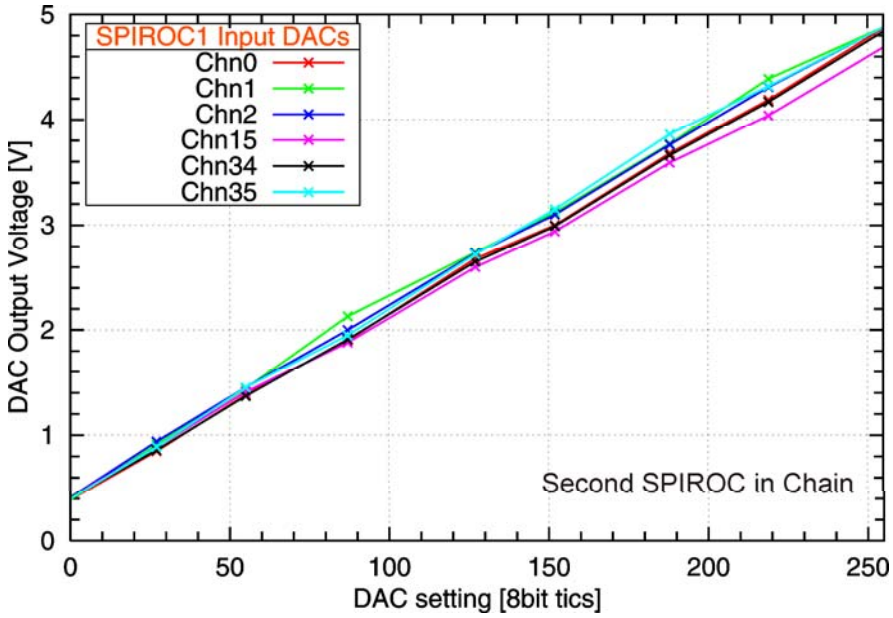
- Two SPIROC1s in SC-chain.
- GS: Pin 83, trigger: Pin 82 (SPIROC1)
- Both SPIROCs show the same behaviour.



System Commissioning – Slow Control (SC)

Input DAC Outputs (8-bit, 5 of 36 channels):





Both SPIROC1s show the same results.
Output voltage measured against +5V.

System Commissioning – Slow Control (SC)

SC programming conclusions

- SC works stable for both SPIROC1s.
- SC Register Length is 701 bits in our case (not 703).
- Rise Time of SC Clock (clk_sc) has to be <12ns.
  How to realize for 2.20m long slabs?? Should be addressed in next ROC generation.
- Power Supply voltages : adjustable <3.25V (except for one pin).
- **Does not work for SPIROC2 up to now** (@VDD = 1.5V), under investigation. Maybe faster clock driver needed (in assembly right now).

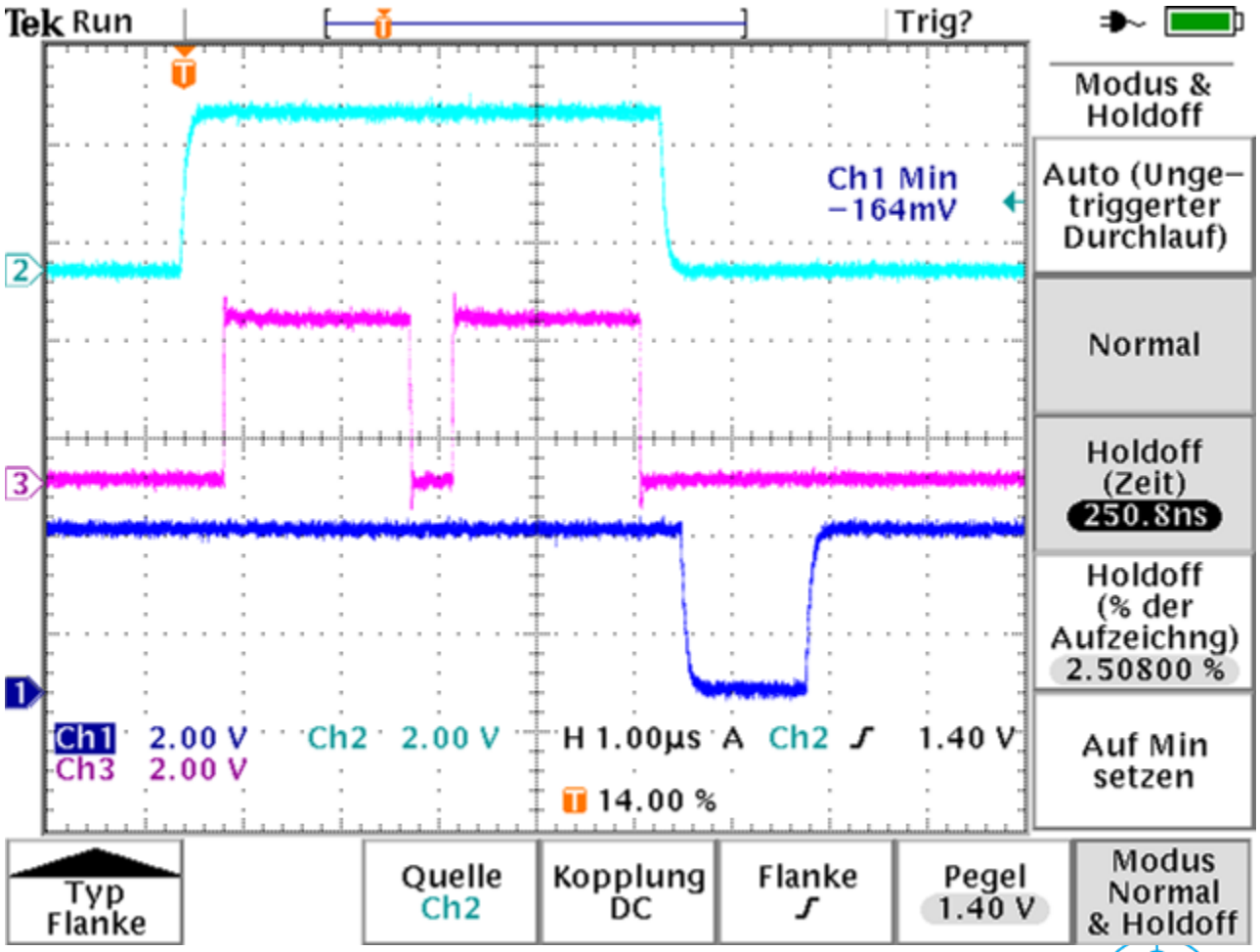
System Commissioning – Data Taking

Signals on HBU, controlled by AHCAL DAQ

start_acqt

ext_trig

start_convDAQb



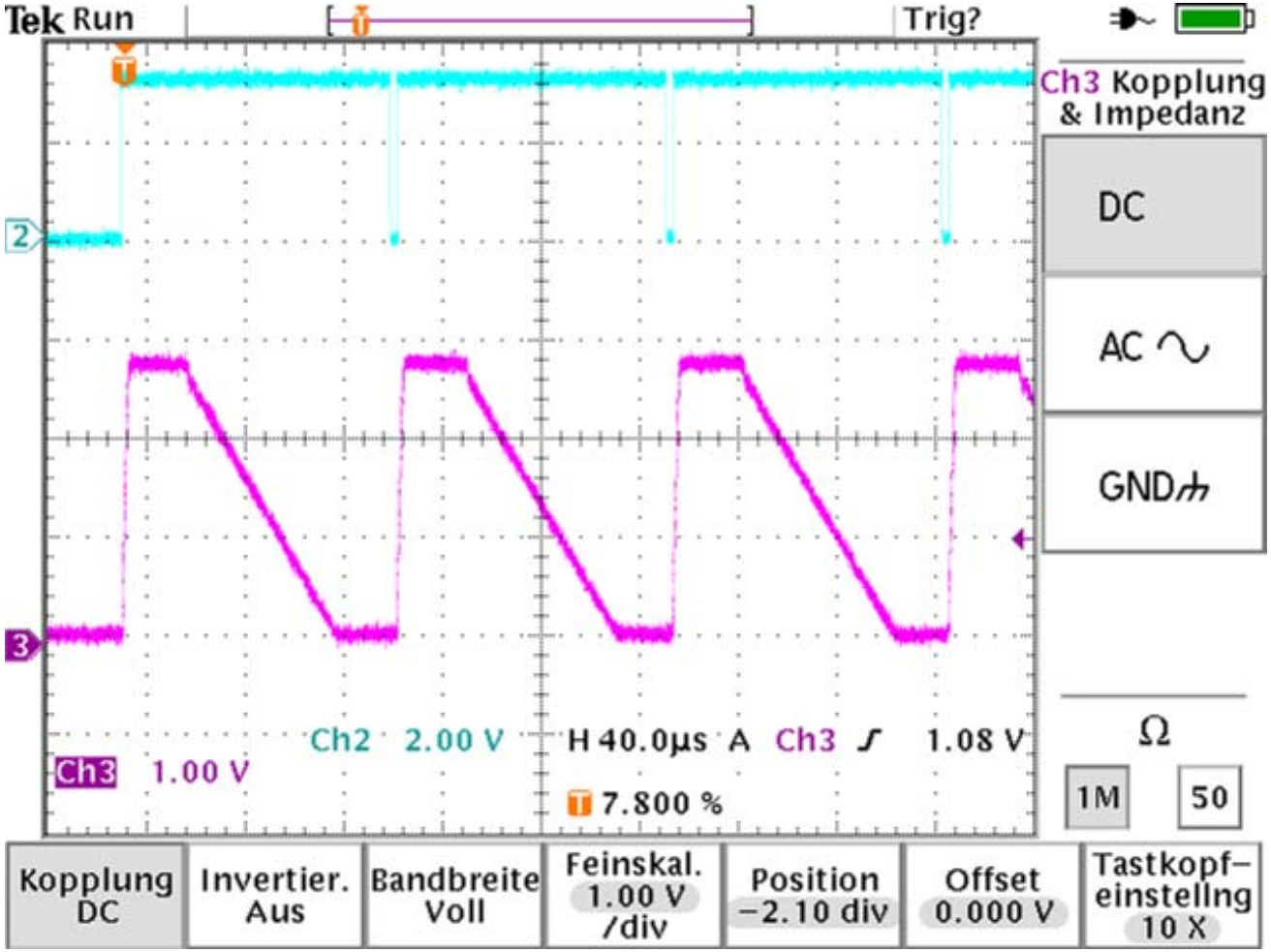
System Commissioning – AD Conversion

External Ramp for SPIROC1 (not final):

start_ramp

External ramp
(2.75V to GND)

Ramp_reset not shown
(start_ramp inverted)

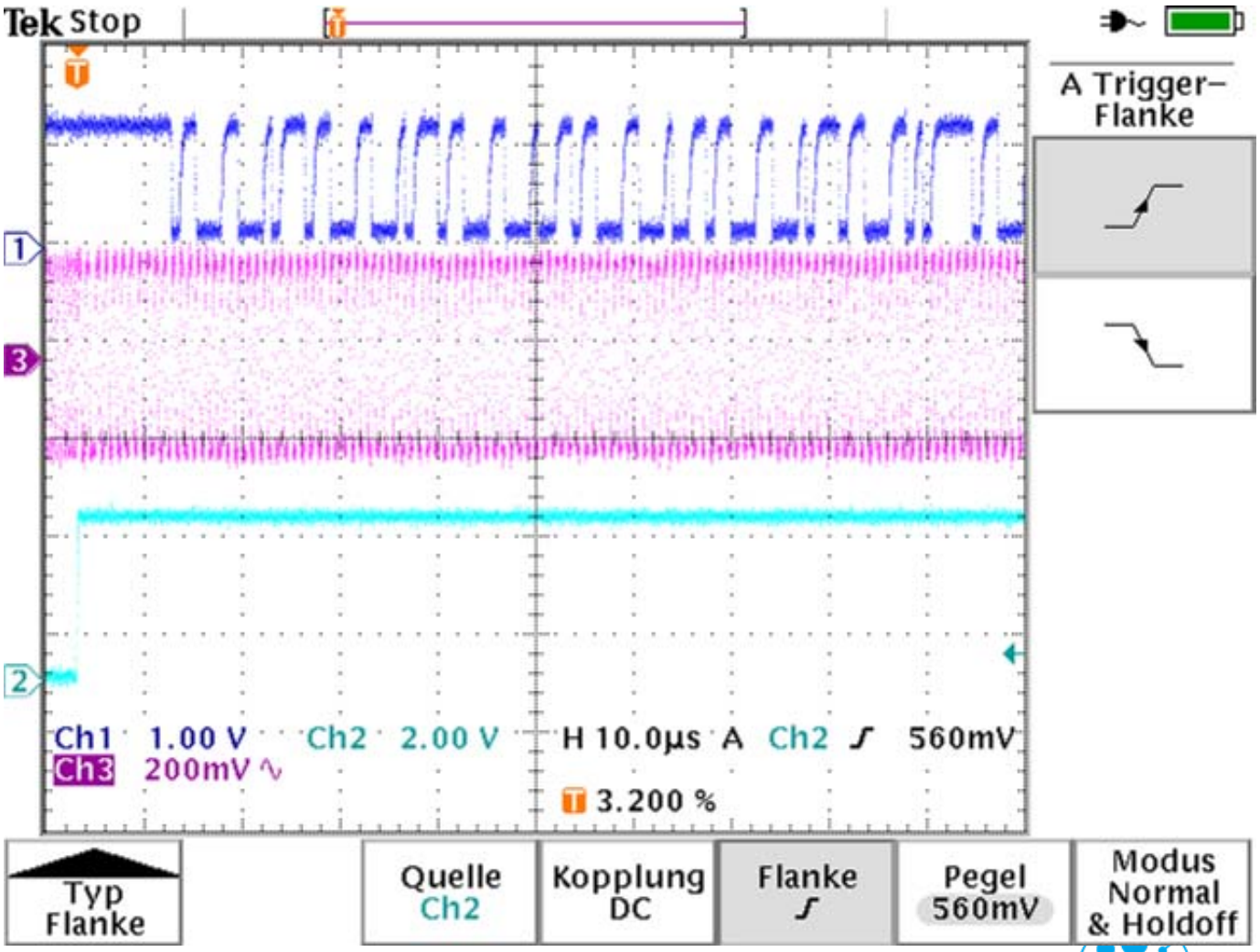


System Commissioning – Readout

Dout
(open collector)

Clock 1.7MHz
(CK_5M+, LVDS)

Start_readout



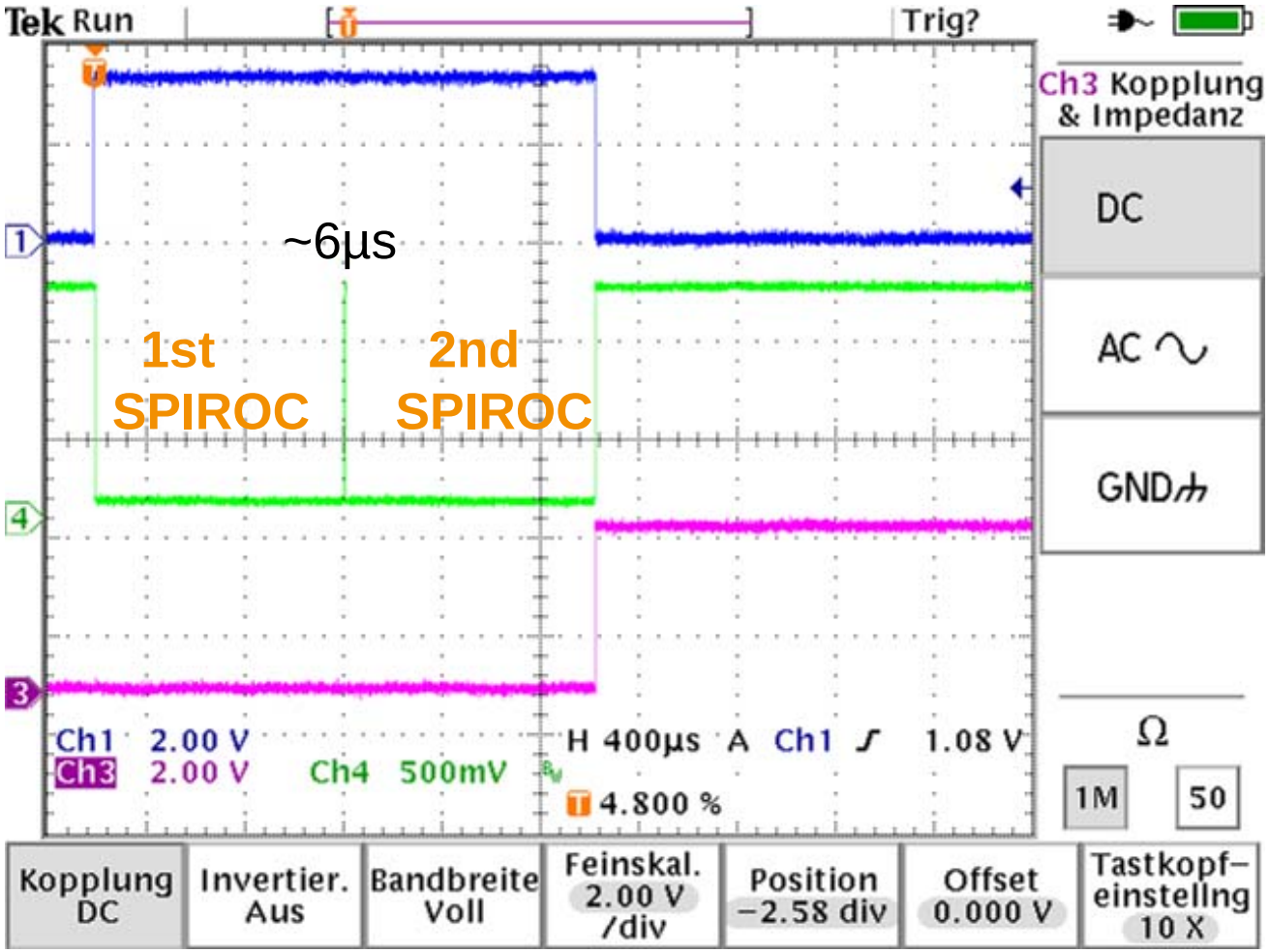
System Commissioning – Readout

First time READOUT of two SPIROC1s in a chain!!

start_readout

TransmitOn
(open collector)

end_readout
(2nd SPIROC outp.)



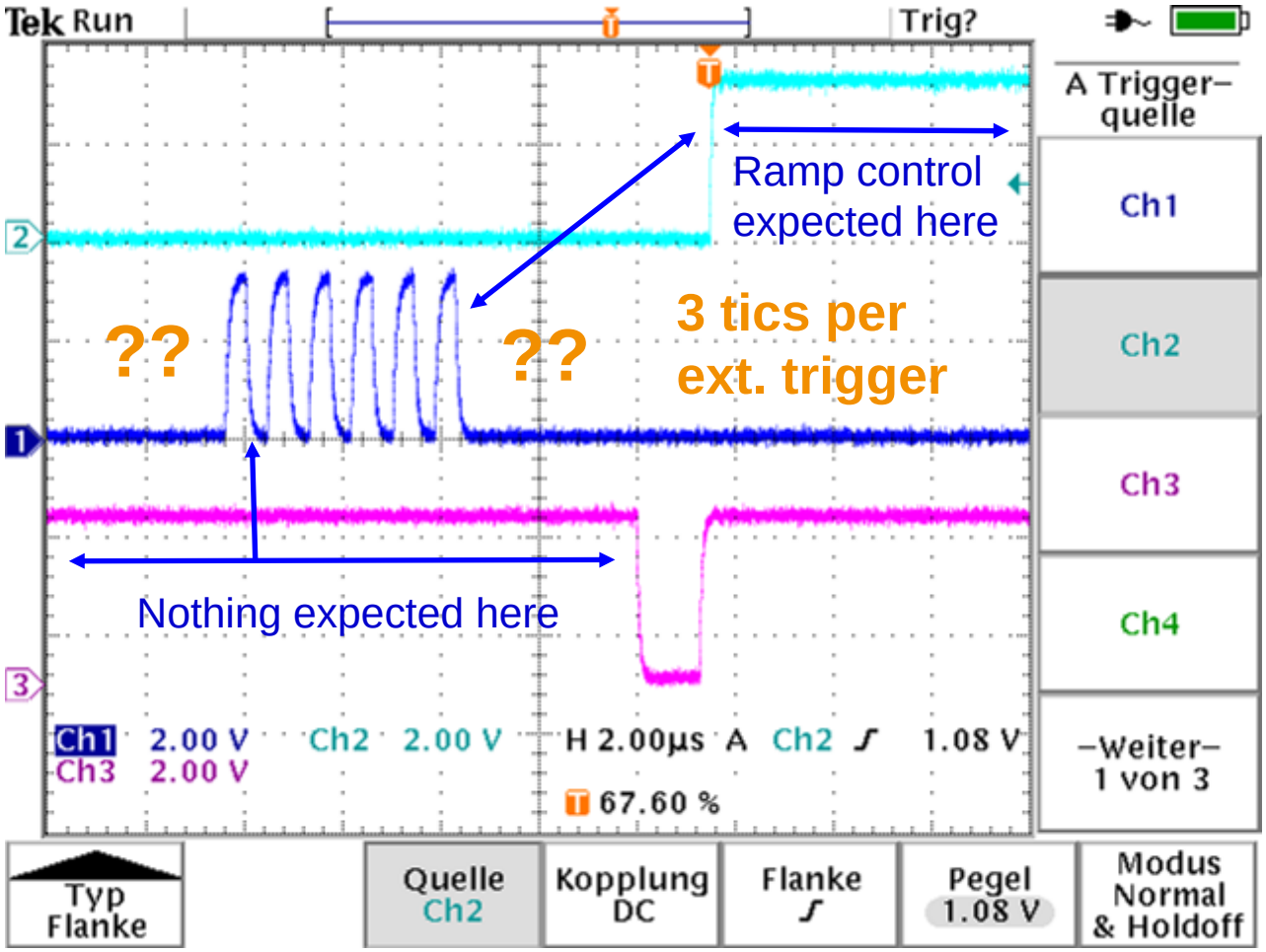
System Commissioning – Probe Register

Probe Register can be written at 1.8V (937/938 bits, not 939)

start_ramp

digital_probe2
(probe bit 7:
Start_Ramp_ADC)

start_convDAQb



Conclusions and Outlook

- CALIB module works fine (communication with DIF, set VCALIB, …).
- No severe errors on HBU up to now (no smoke …)
- Readout (probably DIF to Labview) does not work up to now.
- Probe register works for open collector signals. But not for ramp_control of SPIROC1. Problem unknown.
- Next steps:
  - Commissioning of Calibration Systems as last basic HBU test (start with integrated LEDs)
  - Connection of reflector foils and tiles (in June)
  - **Set SPIROC2 to life (!!!) – foreseen for EUDET module!!**
  - DESY testbeam
  - Switch to CALICE DAQ (early autumn) and use POWER module
  - Redesign HBU (one type of SPIROCs) and DIF (replacement of commercial module)