

AHCAL Electronics.

Status EUDET Prototype

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for the DESY AHCAL developers

EUDET Electronics/DAQ meeting

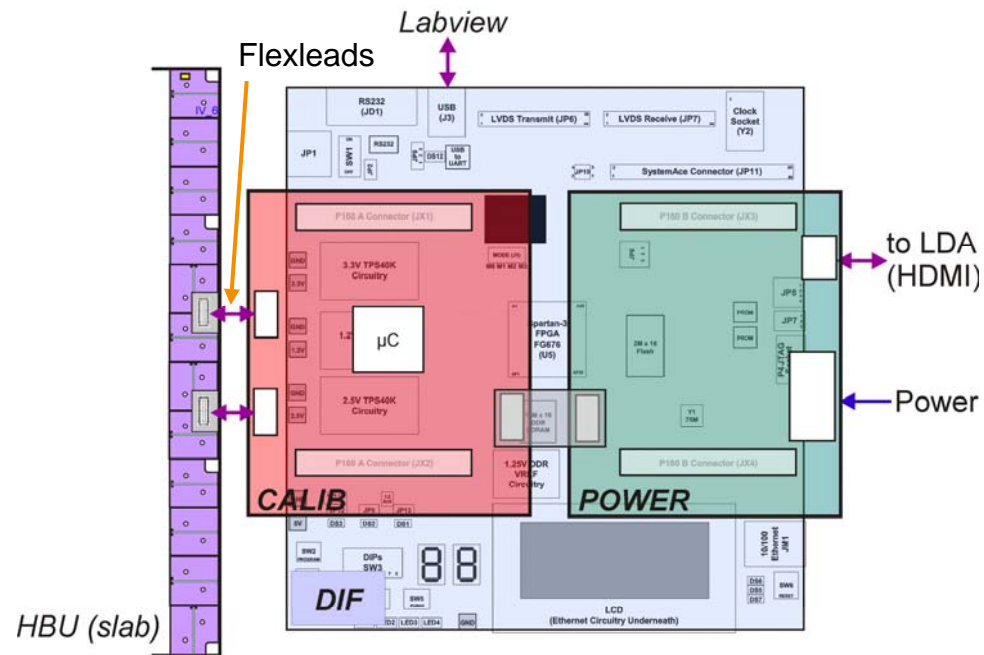
London, June 9th, 2009



Outline

- > Hardware Developments at DESY
 - CALIB, POWER, Flexleads
 - HBU0
 - DIF0 and DAQ interface (USB)
 - Tiles integration
- > System Commissioning
- > Conclusions and Outlook

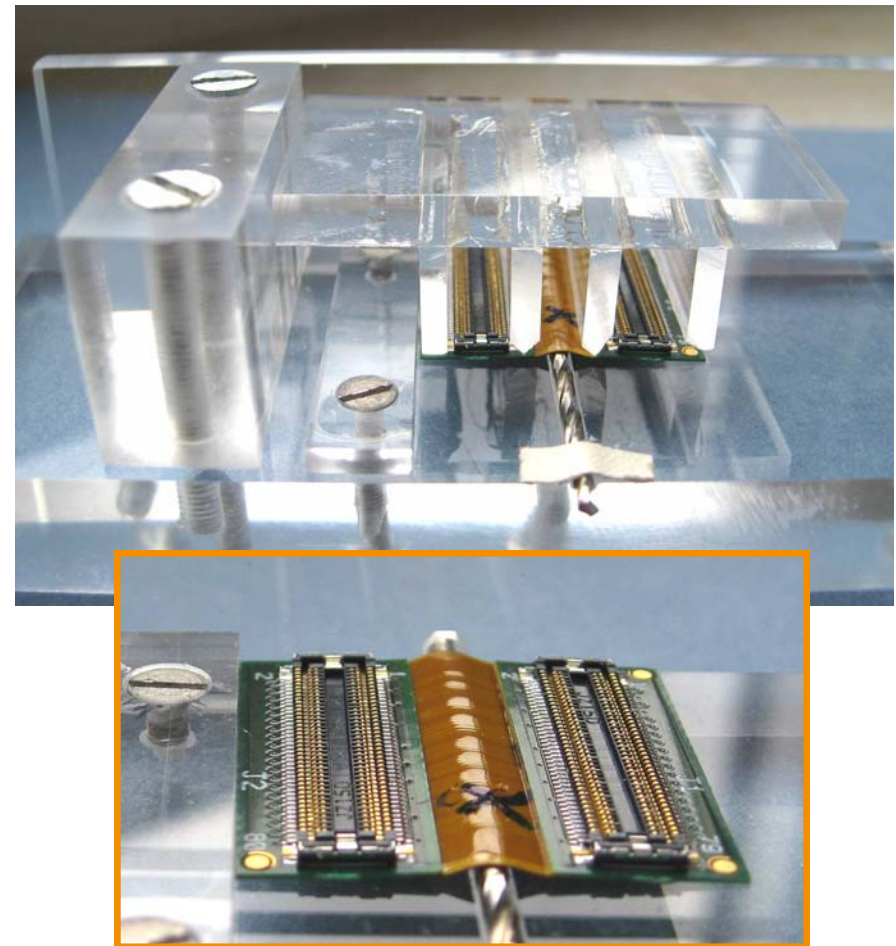
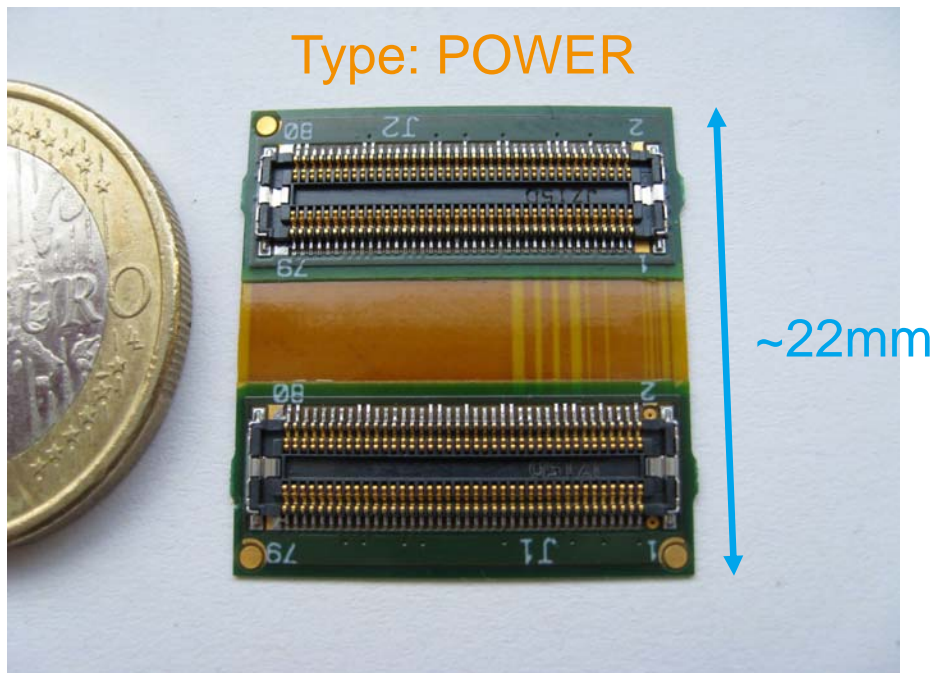
‘old-fashioned overview’



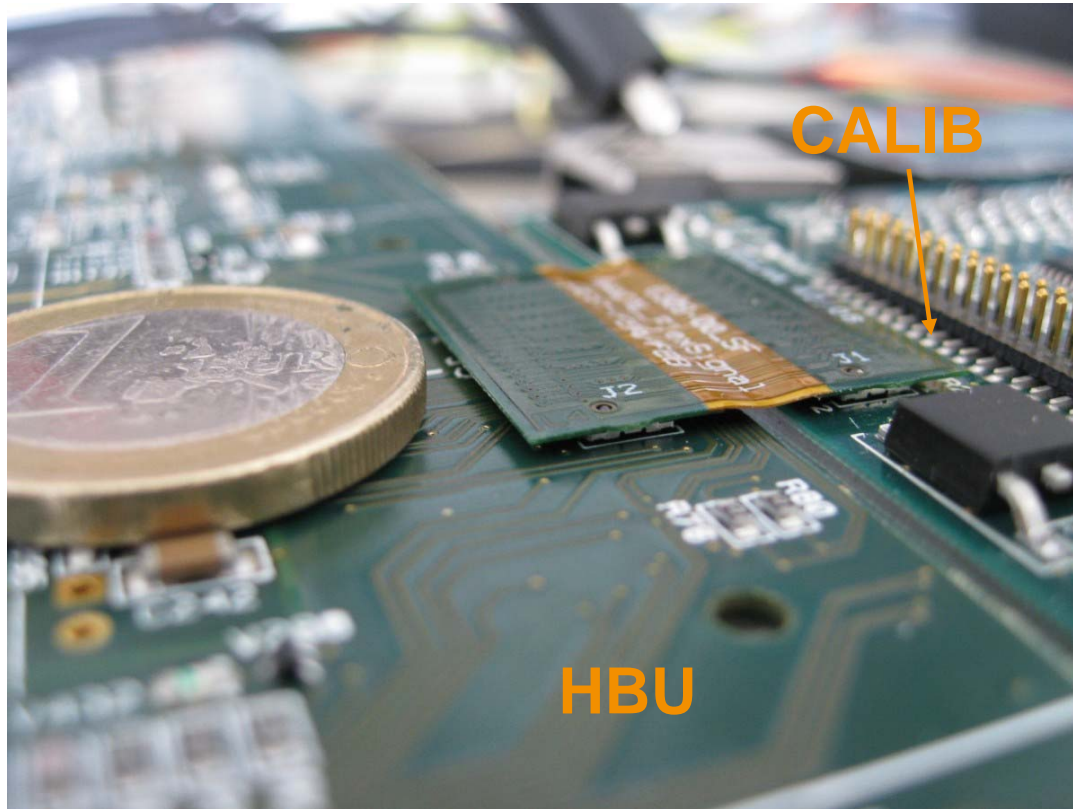
Flexleads (SIGNAL and POWER)

- > 20 pieces of each type finished.
- > Pre-bending procedure ok.

Flexlead Pre-Bending:



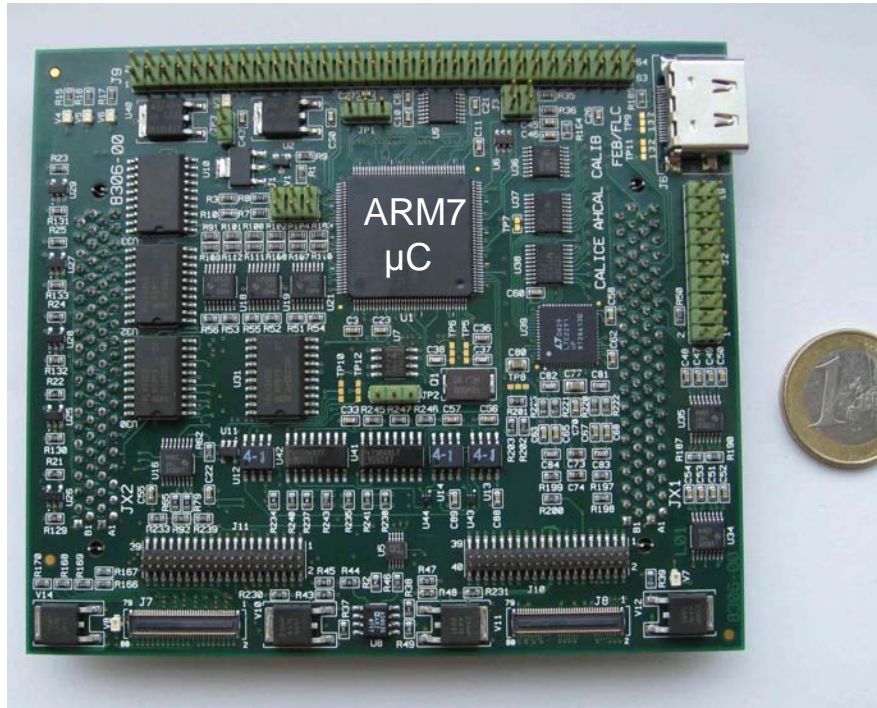
Flexleads (SIGNAL and POWER)



- > About 40 connection cycles up to now - still ok.
- > Compensate HBU misalignments in distance.
- > Fulfill AHCAL height requirements.
- > Tests ok concerning:
 - Signal allocation
 - Signal quality
 - Resistance for power

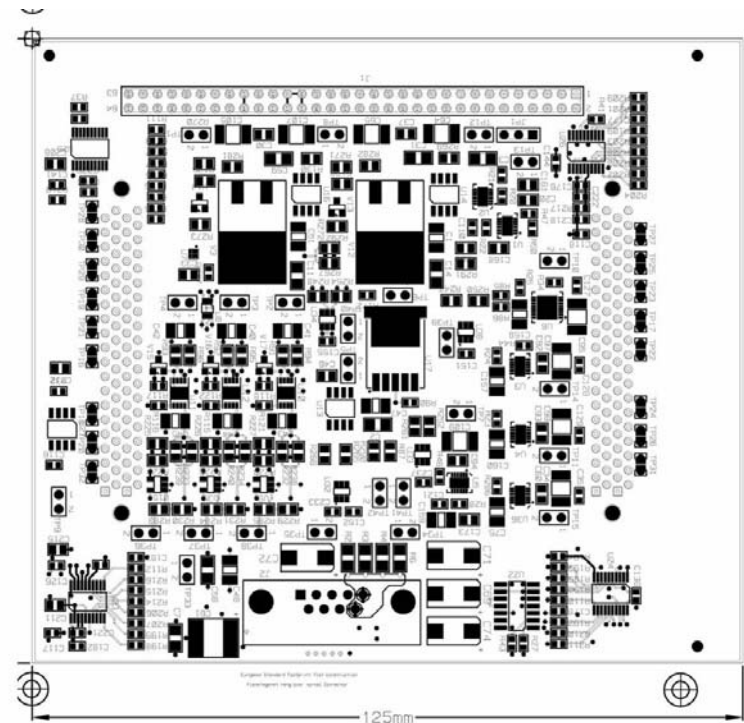
CALIB and POWER modules

CALIB module: 11 x 10 cm²



- > 4 Modules finished, in operation.
- > First tests successful.

POWER module: 12.5 x 11 cm²



- > In production.
- > Expected end June.

Sizes and heights: To be adapted to ILC mechanics later.

CALIB: M. Zeribi,
POWER: H. Wentzlaff



HBU0 status

2 setups available

SPIROC1

Connectors:
Signal

Power

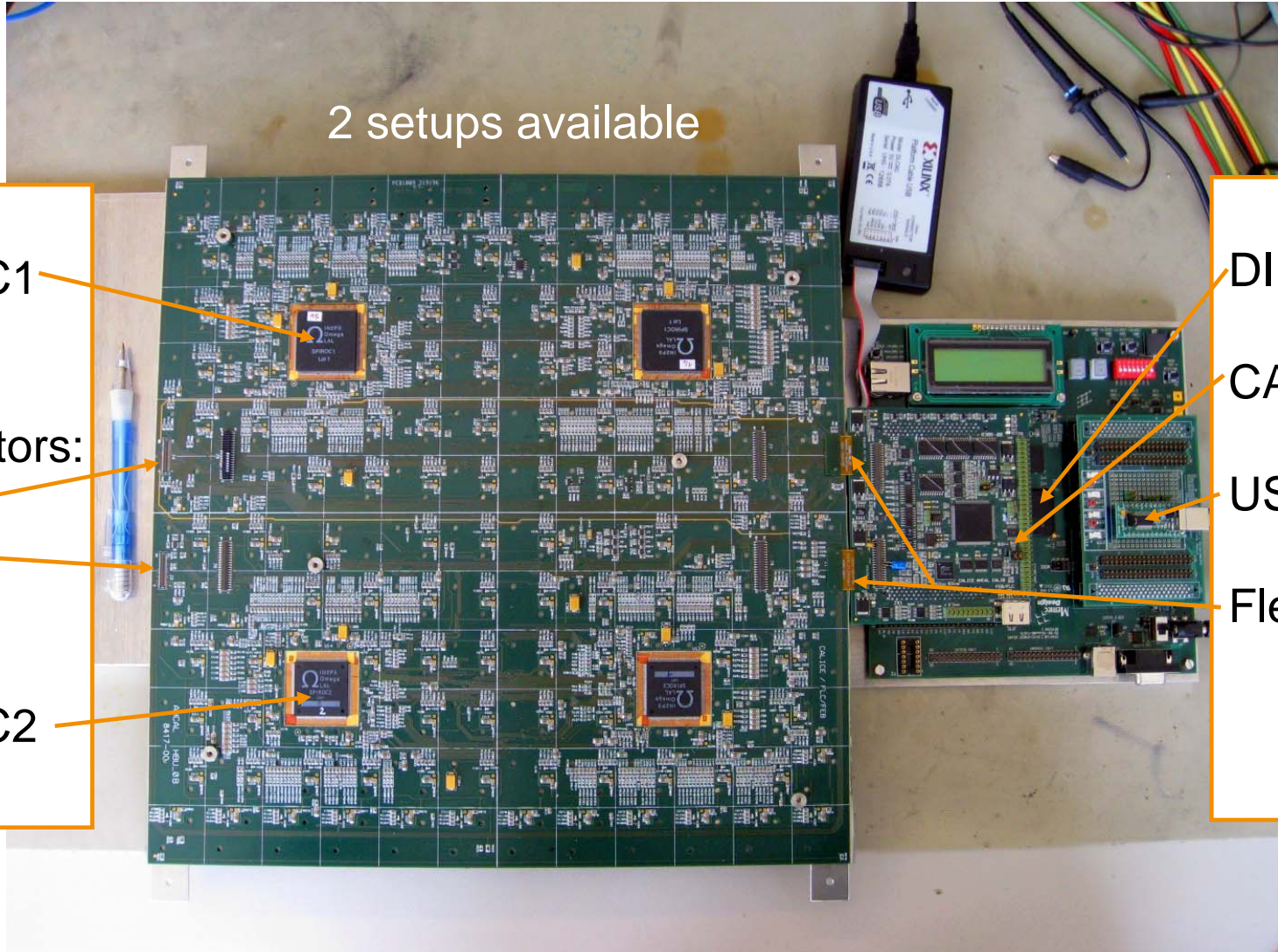
SPIROC2

DIF FPGA

CALIB

USB / DAQ

Flexleads



Labview Control of the Prototype System

System/USB Init | Slow Control | Take Data / Readout | Debug READ, PROBE | Calibration Setup | Calibration | Program Exit STOP

Operation of AHCAL Calibration System (CALIB)

Set Delay Lines
 Delay Line Value (8-bit): 01000010 LSB
 Select Delay Line: Delay Line 1
 DelayLine: Set Set 2 Ack 2

DAC1 (LED Bias, 16bit): 0100000101000010 LSB
 Select DAC: DAC2 ON DAC1
 DAC2 (Charge Bias, 16bit): 0100000101000010 LSB
 Set_DAC: Write Set Ack Set Ack

ReadDAC Read Read Ack DACRead hex

Enable Section
 LVDS1-6, LVDS all Set Ack
 PWR_LED, PWR_Charge, Slab_Pow, SiPM_Bias, Pre_Bias (off: 10V, on: full V)
 C_Power Set ALL Set Ack

Read Info
 Si Serial no. (hex)
 Calib_Info Read SW Date 0 0 0000 SW Version 0 0 Board Version 0
 Set 3

ADC operation
 ADC_Cal Calibrate Set Ack Read Read Ack
 No. Avgs 1..255 1 ADC_AVG Set Set Ack
 No. Avgs (hex)

R_ADC1	R_ADC2	R_ADC3	R_ADC4
Temp1 0	VCALIB1 0	VDAC 0	HV1 0
Temp2 0	VCALIB2 0	IDAC 0	HI1 0
Temp3 0	VDDD 0	VREF 0	HV2 0
Temp4 0	IDDD 0	IREF 0	HI2 0
Temp5 0	VDDA 0	VADCREf 0	HV3 0
Temp6 0	IDDA 0	reserved 0	HI3 0
reserved 0	reserved 0	reserved 0	reserved 0
VADCREf 0	VADCREf 0	VADCREf 0	VADCREf 0

voltages in V
 currents in mA
 temperatures in degrees C

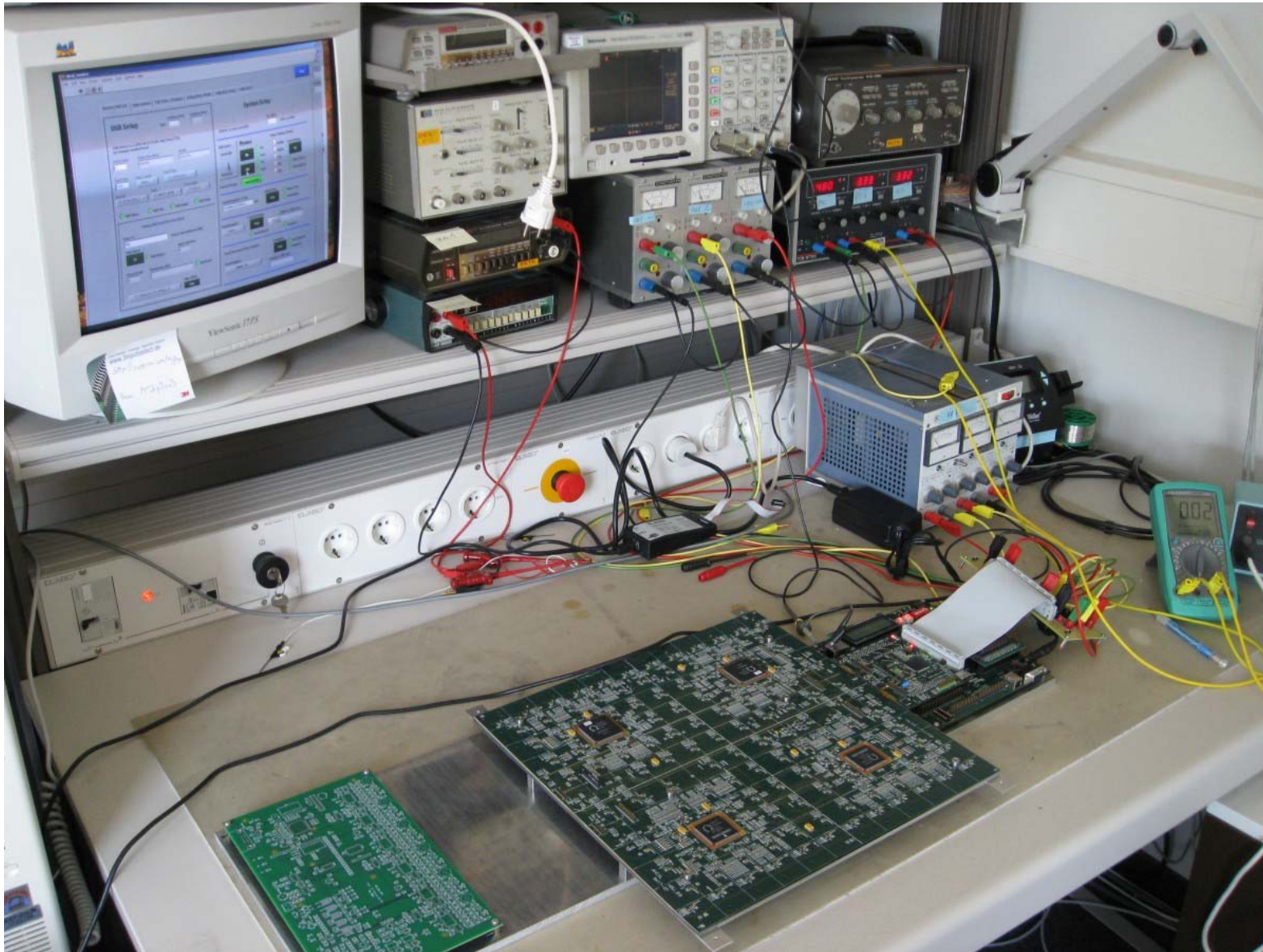
Tab Control

AHCAL: Focus on:

- > USB Interface
- > Slow-Control
- > Take Data
- > Readout
- > Current Version: 20

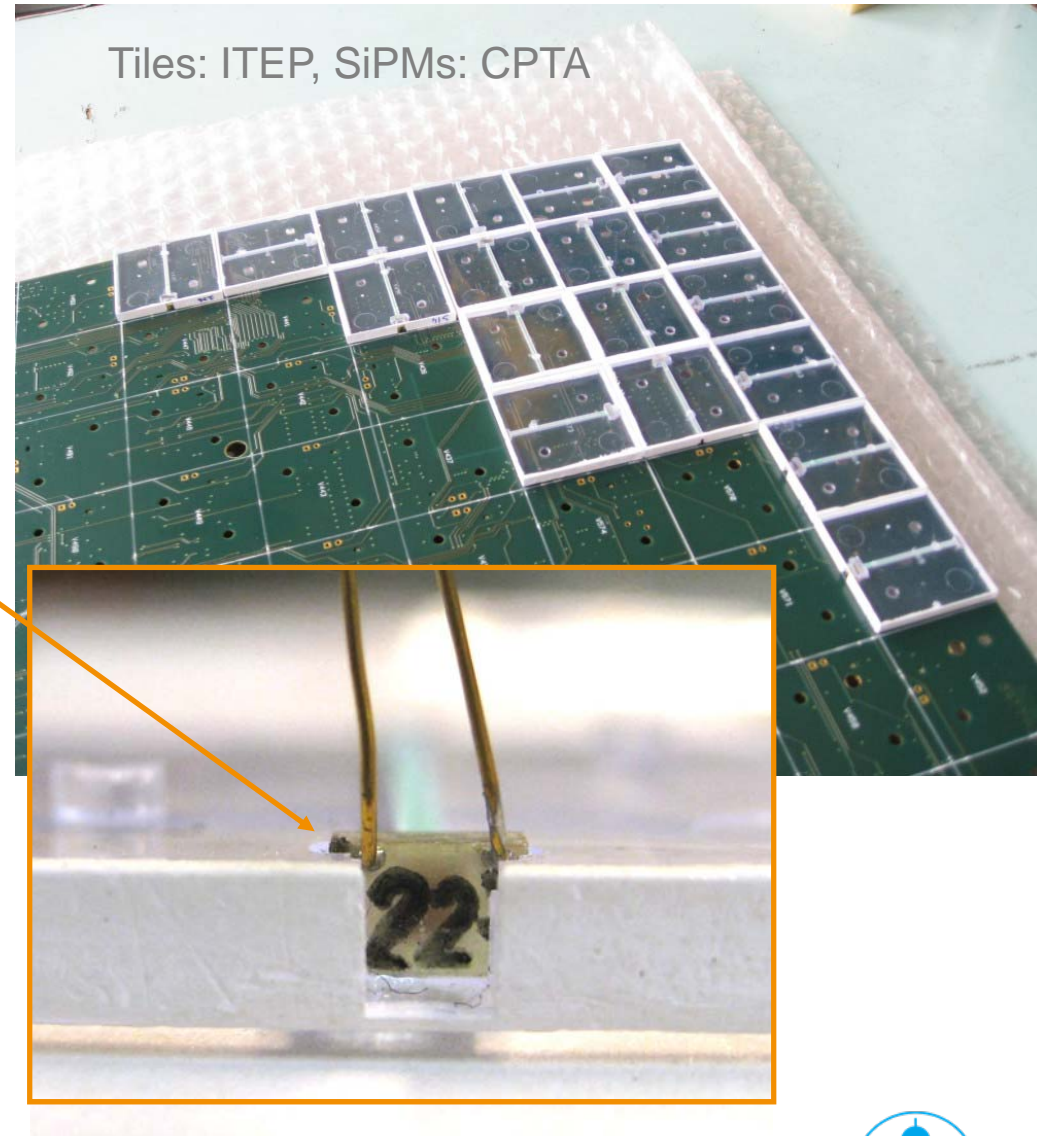


Prototype System Commissioning



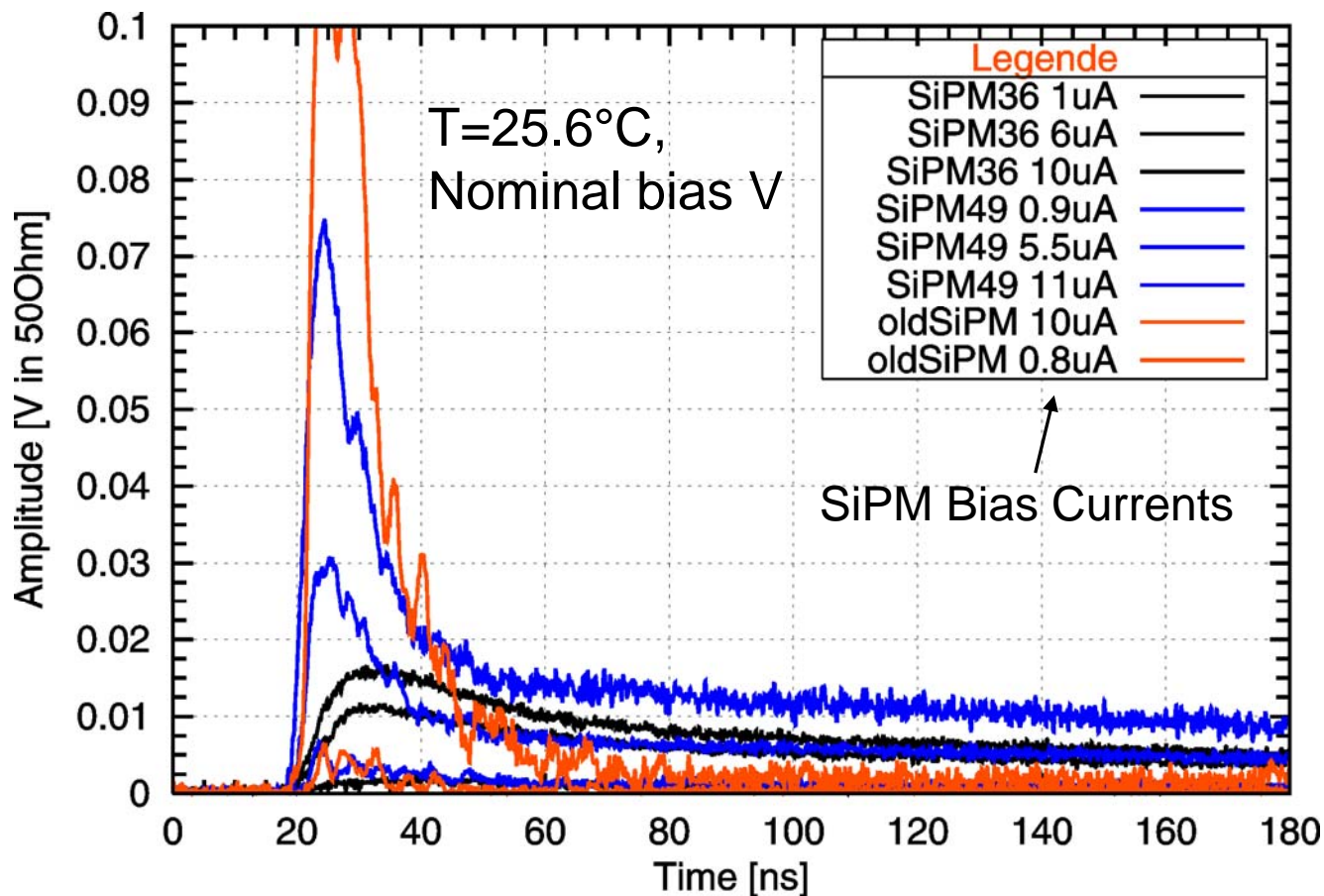
Tiles Interconnection Test

- > Tiles not connected yet (HBU electrical test first).
- > Test assembly shows:
 - Strong force to SiPM pins during assembly.
 - A few SiPMs cases are too large (only a few!).
 - Mirrors are too large, but can be cut.
 - Alignment concept (-pins) works!!



SiPM long tails - LED Test (3 light intensities)

19% of SiPMs show pulse responses wider than 50ns.



SiPM36: long tail

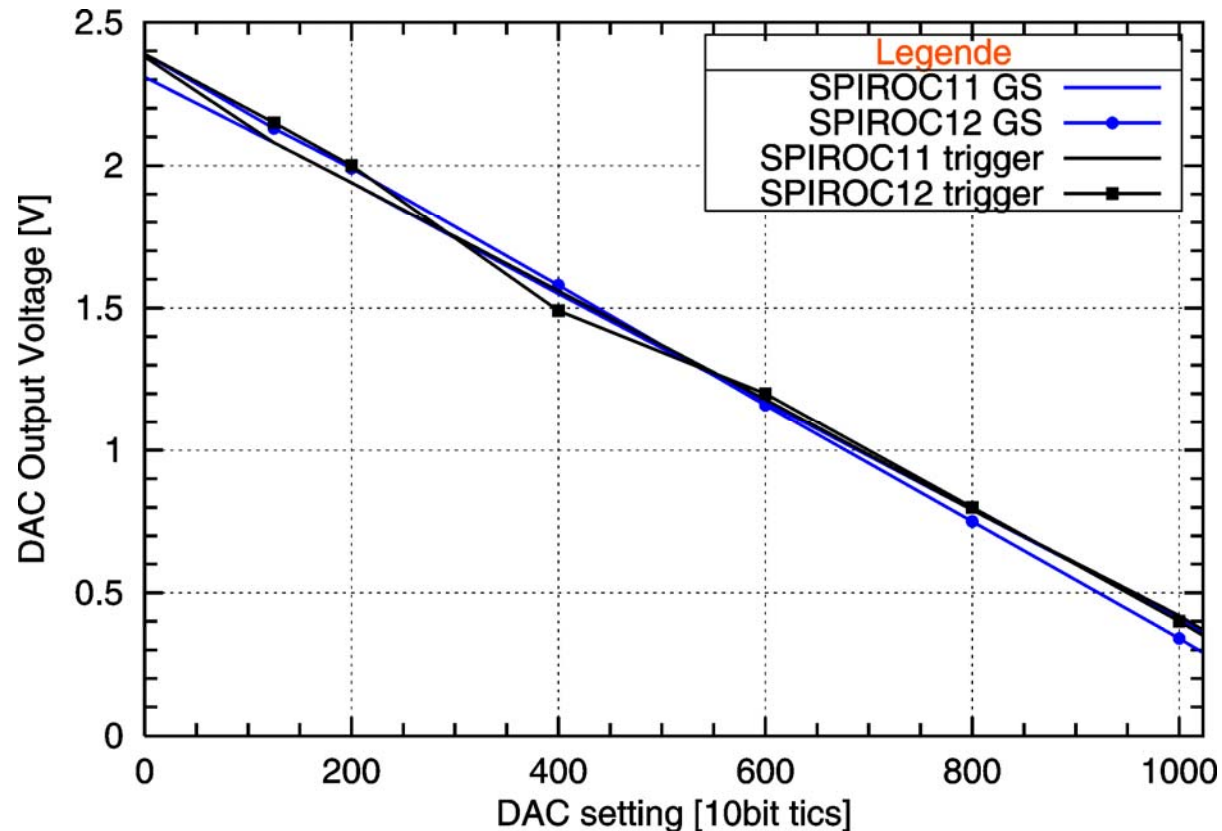
SiPM49: good

oldSiPM: 6x6 tile
with SiPM 538

System Commissioning – Slow Control (SC)

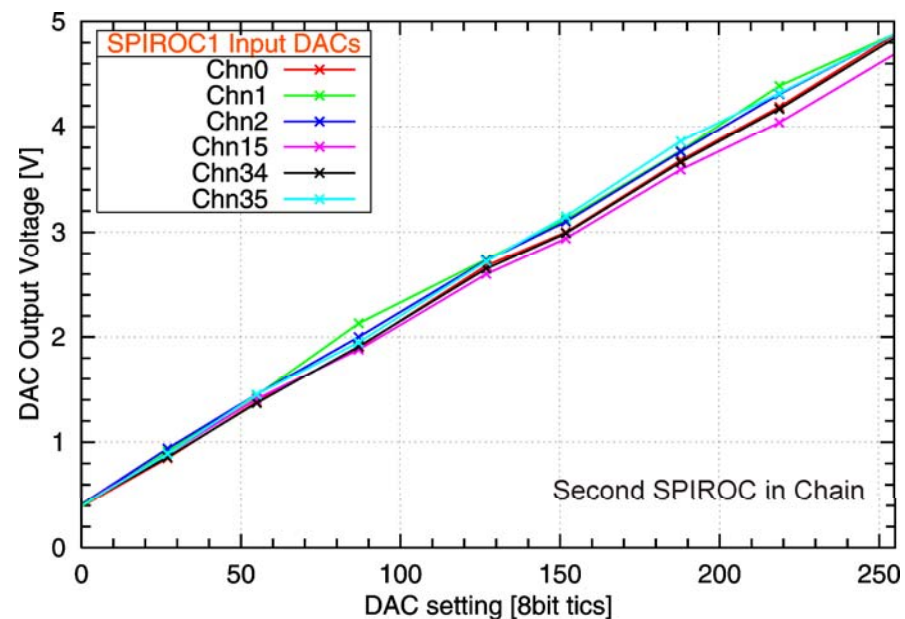
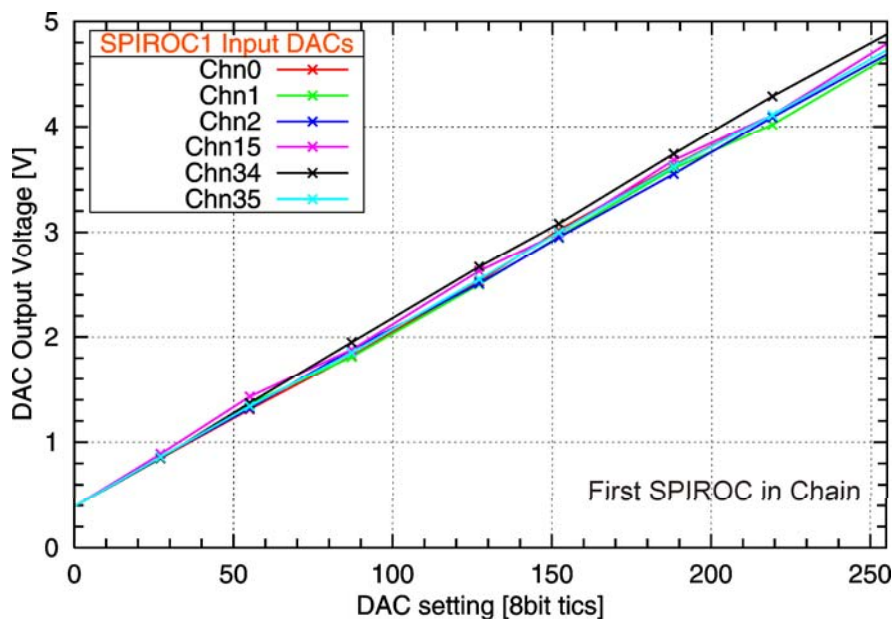
Discriminator DAC Outputs (10-bit)

- > Two SPIROC1s in SC-chain.
- > GS: Pin 83, trigger: Pin 82 (SPIROC1)
- > Both SPIROCs show the same behaviour.



System Commissioning – Slow Control (SC)

Input DAC Outputs (8-bit, 5 of 36 channels):



Both SPIROC1s show the same results.
Output voltage measured against +5V.



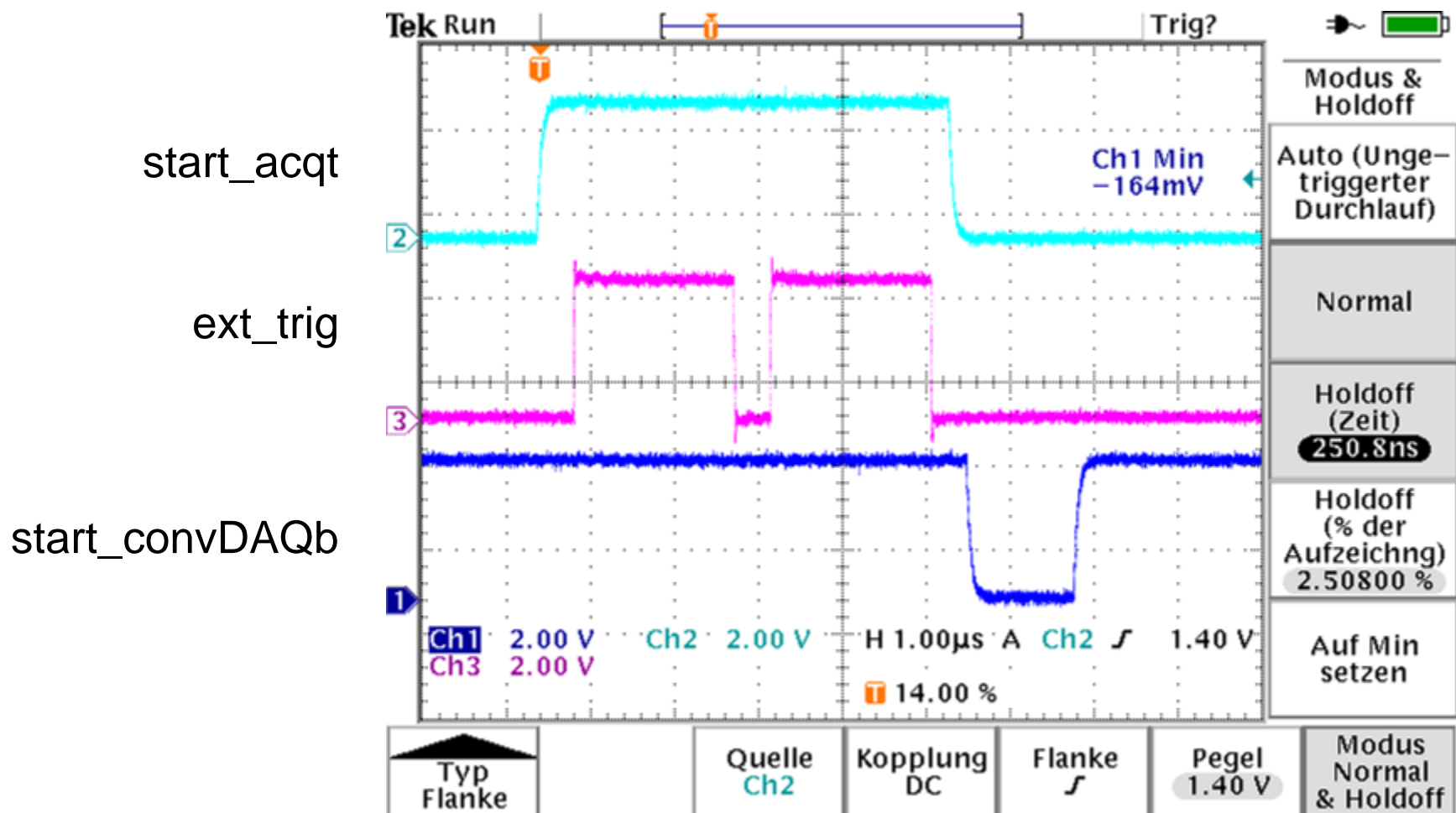
SC programming conclusions

- > SC works stable for both SPIROC1s.
- > SC Register Length is 701 bits in our case (not 703).
- > Rise Time of SC Clock (clk_sc) has to be <12ns.
How to realize for 2.20m long slabs?? Should be addressed in next ROC generation.
- > Power Supply voltages : adjustable <3.25V (except for one pin).
- > **Does not work for SPIROC2 up to now** (@VDD = 1.5V), under investigation. Maybe faster clock driver needed (in assembly right now).



System Commissioning – Data Taking

Signals on HBU, controlled by AHCAL DAQ

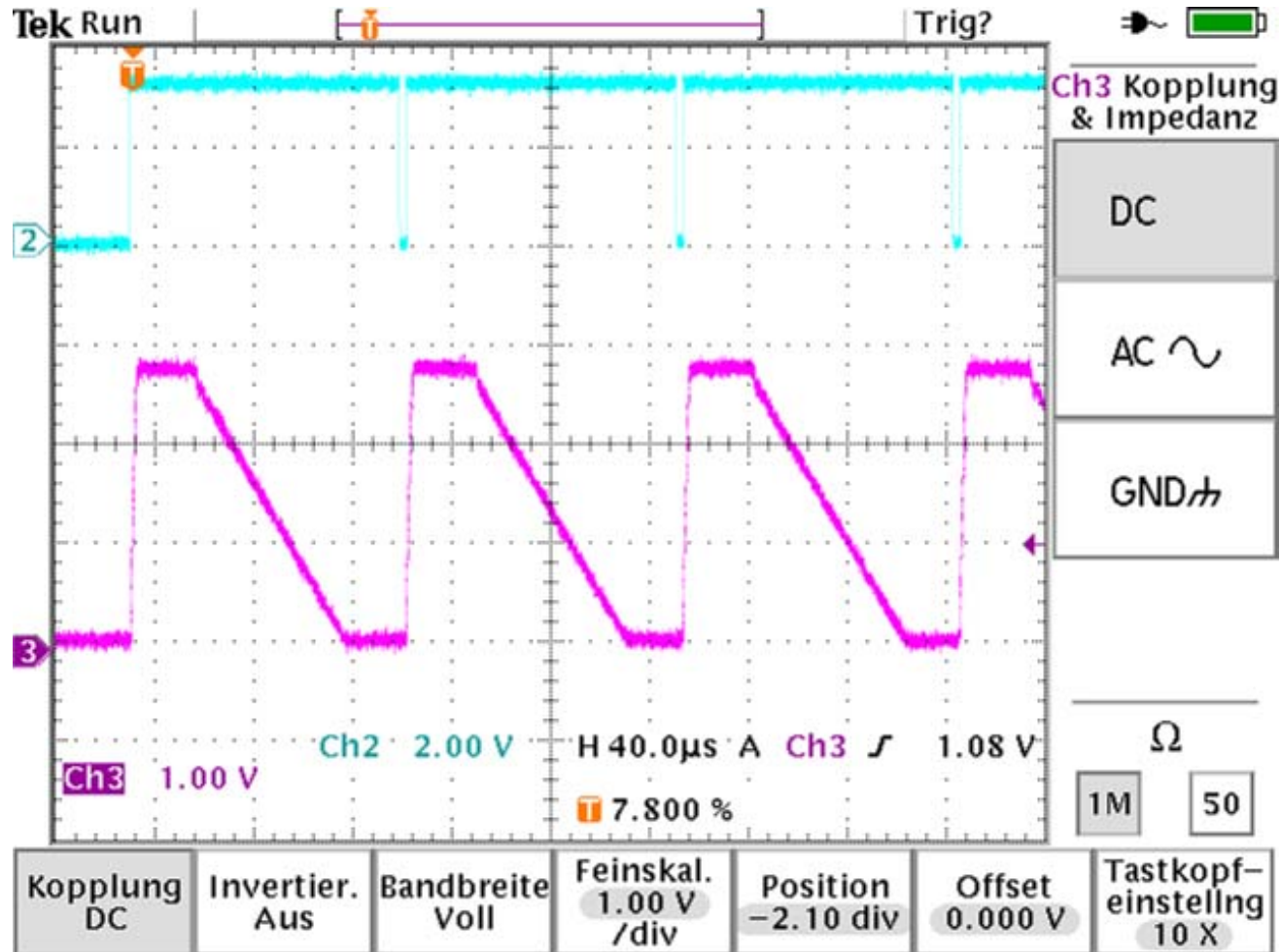


System Commissioning – AD Conversion

External Ramp for SPIROC1 (not final):

start_ramp

External ramp
(2.75V to GND)



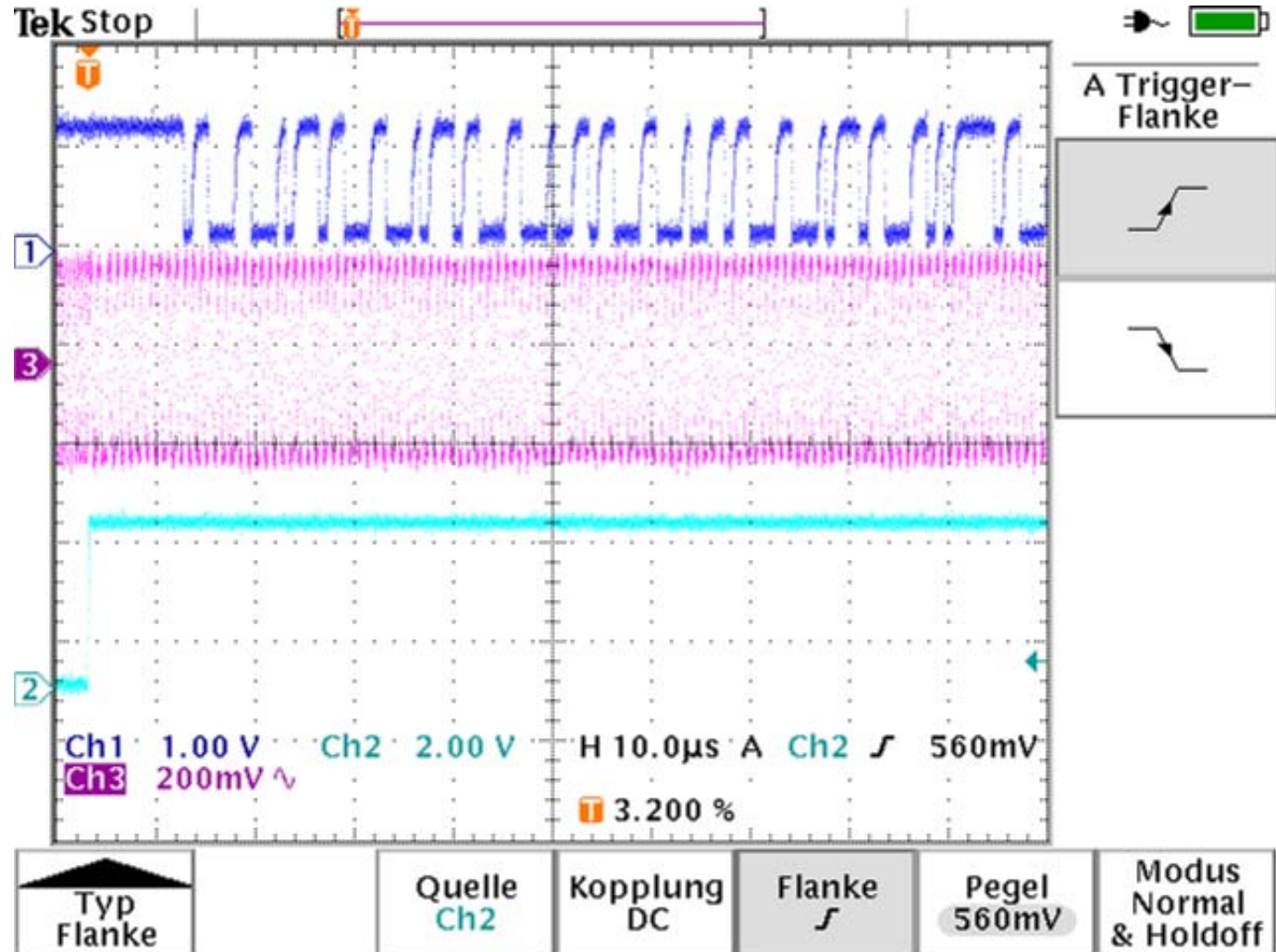
Ramp_reset not shown
(start_ramp inverted)

System Commissioning – Readout

Dout
(open collector)

Clock 1.7MHz
(CK_5M+, LVDS)

Start_readout



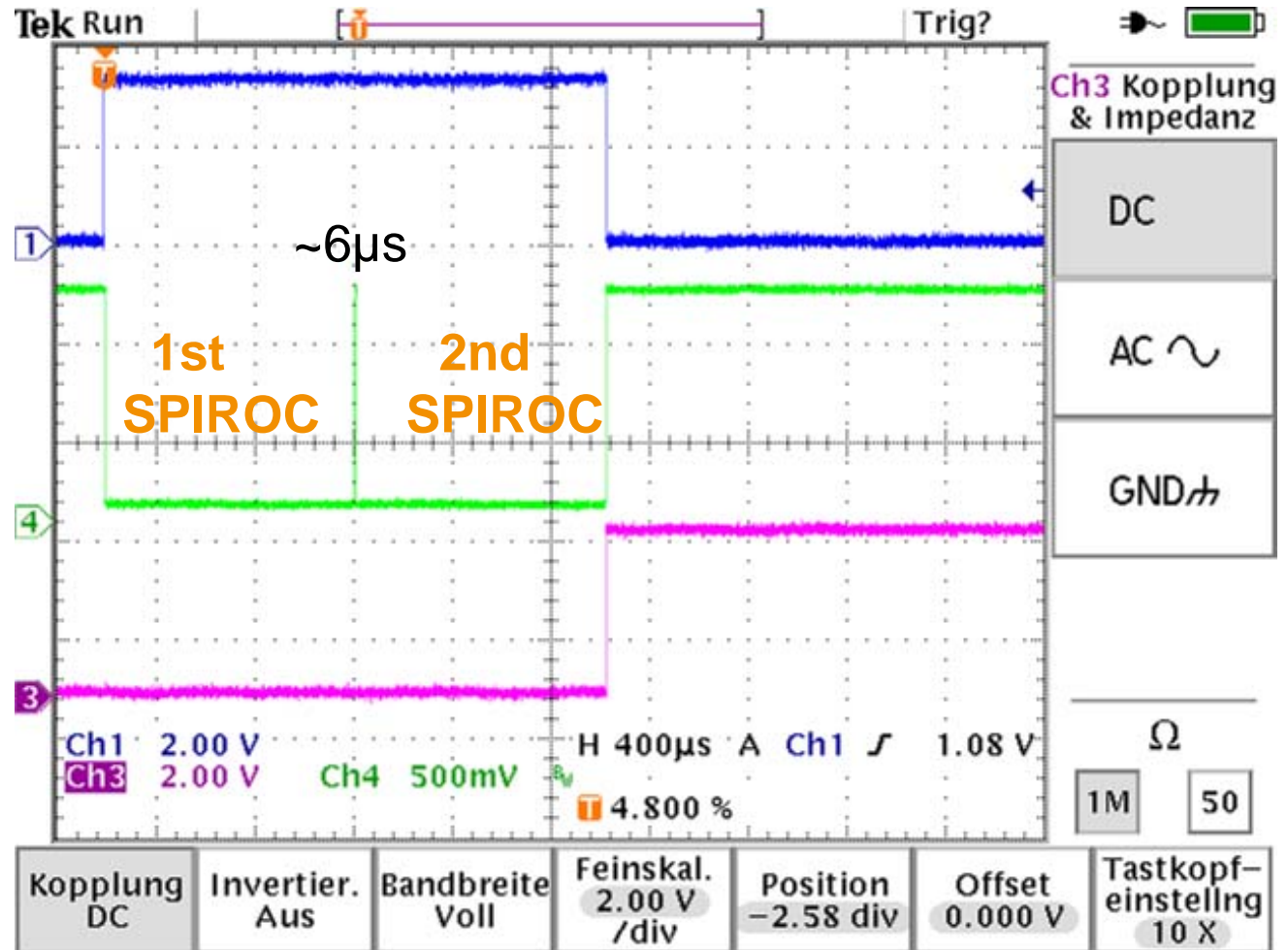
System Commissioning – Readout

First time READOUT of two SPIROC1s in a chain!!

start_readout

TransmitOn
(open collector)

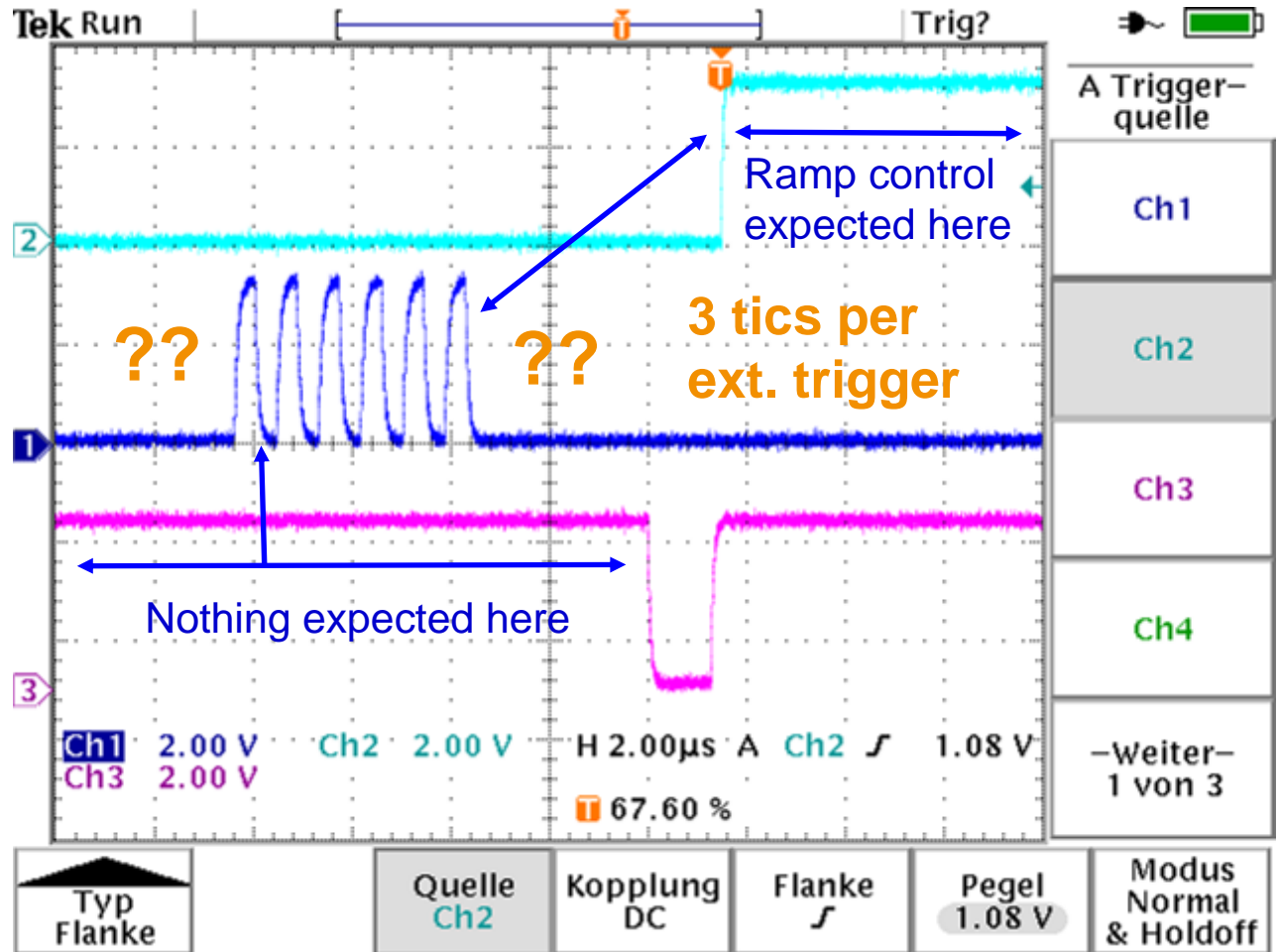
end_readout
(2nd SPIROC outp.)



System Commissioning – Probe Register

Probe Register can be written at 1.8V (937/938 bits, not 939)

start_ramp
digital_probe2
(probe bit 7:
Start_Ramp_ADC)
start_convDAQb



Conclusions and Outlook

- > CALIB module works fine (communication with DIF, set VCALIB, ...).
- > No severe errors on HBU up to now (no smoke ...)
- > Readout (probably DIF to Labview) does not work up to now.
- > Probe register works for open collector signals. But not for ramp_control of SPIROC1. Problem unknown.
- > Next steps:
 - Commissioning of Calibration Systems as last basic HBU test (start with integrated LEDs)
 - Connection of reflector foils and tiles (in June)
 - **Set SPIROC2 to life (!!!) – foreseen for EUDET module!!**
 - DESY testbeam
 - Switch to CALICE DAQ (early autumn) and use POWER module
 - Redesign HBU (one type of SPIROCs) and DIF (replacement of commercial module)

