IN2P3 CSNSM LAL LPN IPN Orsay

Omega

ASIC Skiroc 2

Digital part

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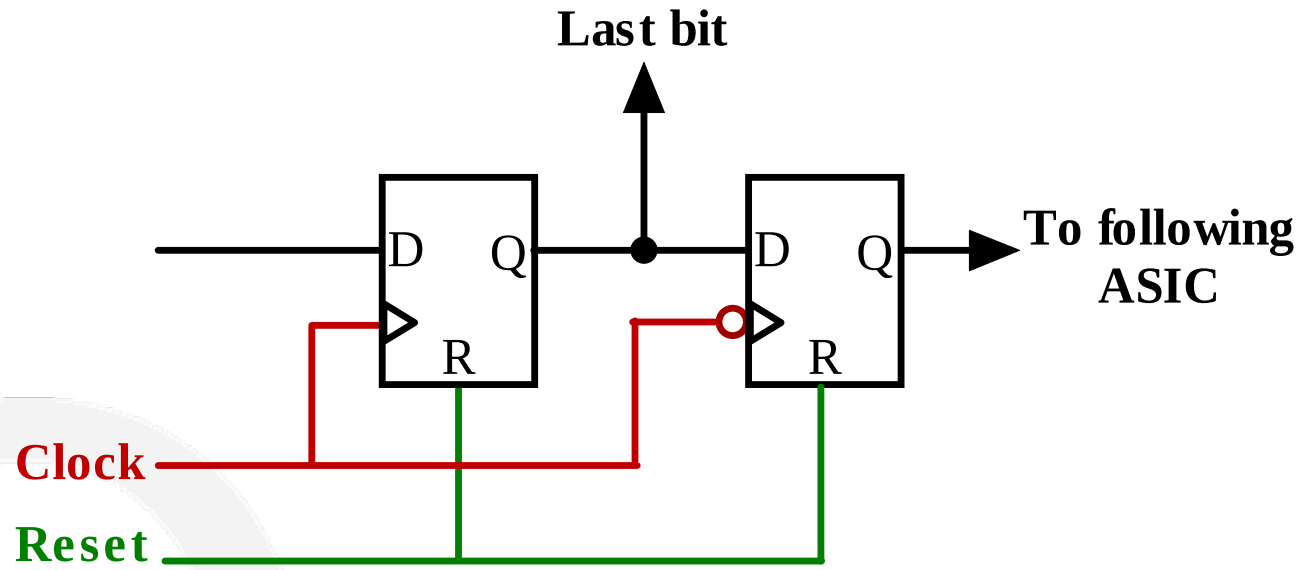
08-09/06/2009

What's new for the digital part ?

- Improved SCA management (Spiroc like)
  - SCA depth of 15: limited by memory size (5 in Skiroc1)
  - 64 channels (36 in Skiroc1)
- New SlowControl registers
- Start/EndReadOut daisy chain improved. EndRO is calibrated (2-3 clock ticks) and synchronized on falling edge
- Compatible with SPIROC1&2 acquisition management
  - Possibility to use a Notrig signal (erase current SCA depth)
- Many other improvements (some from other chips):
  - Hit channel data now stored in analog part (near SCA)
  - Glitchfree signals added
  - Default configuration
  - Internal ADC management (registers)

Slow Control (1/2): Extra FF

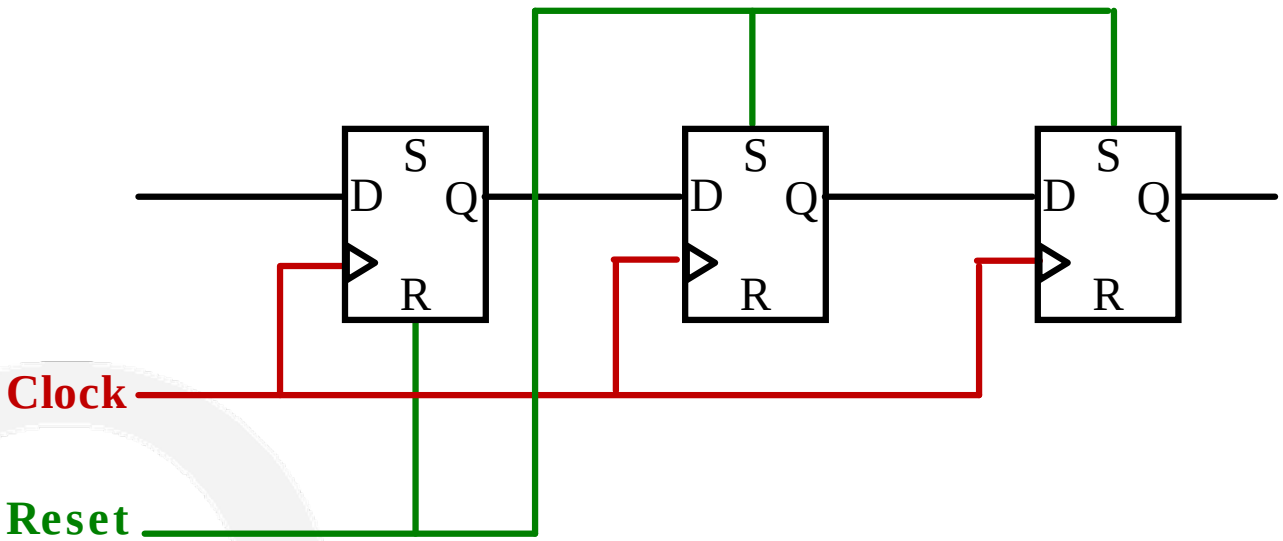
- Improve shift registers daisy chain between / inside ASICs:
  - Add opposite edge FF on each SC bits



- Consequences:
  - Chip “N” sends data at falling edge and chip “N+1” captures at rising edge (time margin = half period clock)
  - Area of SC doubled (N SC bits ➔ 2N SC Flip Flops)
  - No change for the DIF software (N SC bits ➔ N clock tick to load SC)

Slow Control (2/2): default configuration

- Use Set / Reset of Flip-Flops for default configuration of SC

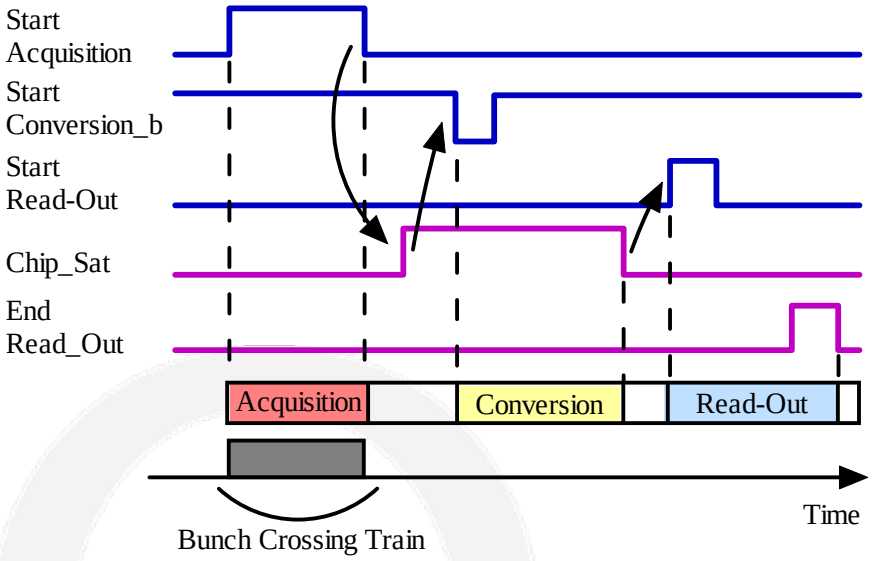


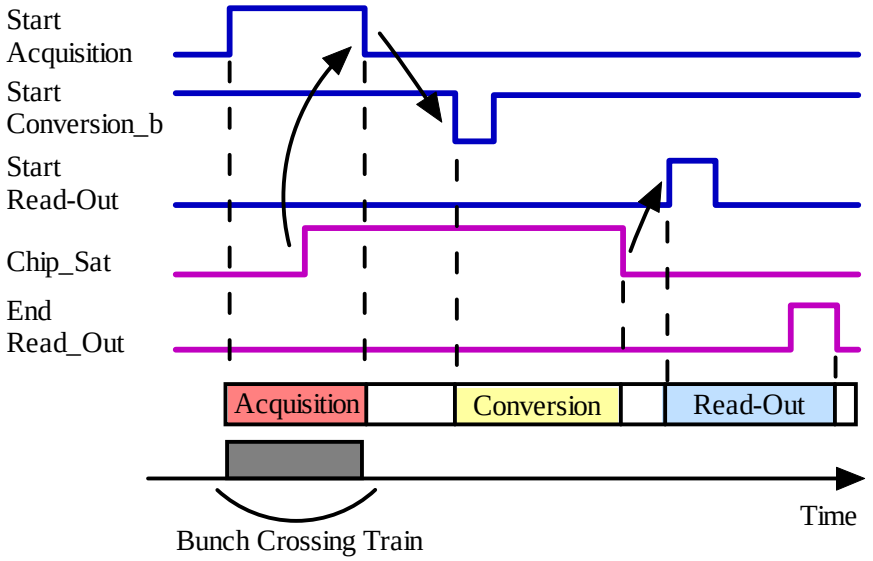
Example default configuration : “011”

- Implemented for digital interfaces (HARDROC2) ➔ Now Skiroc2

DIF Management like all ROC Chips

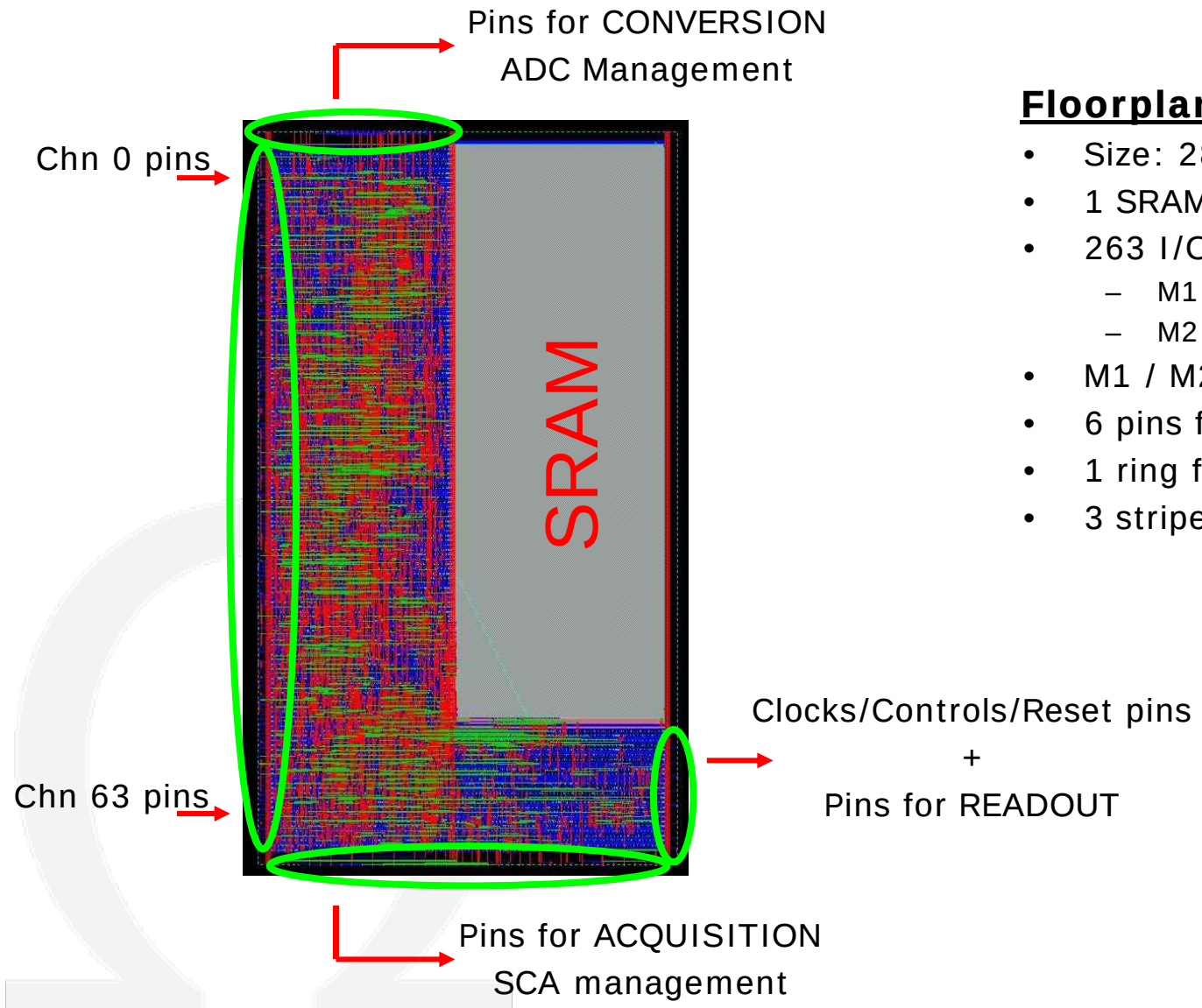
- Same driving sequence for all ROC chips (Hardroc2, Spiroc and Skiroc)
  ➔ “StartAcquisition” active on level.





- ChipSat allows the DIF to know:
  - When to start the conversion after the falling edge of the StartAcq: ChipSat @ ‘1’
  - When the conversion is finished: ChipSat going from ‘1’ to ‘0’
- If one chip stuck the ChipSat, DIF always has the possibility to use a timeout (should be around 4ms for Skiroc2)

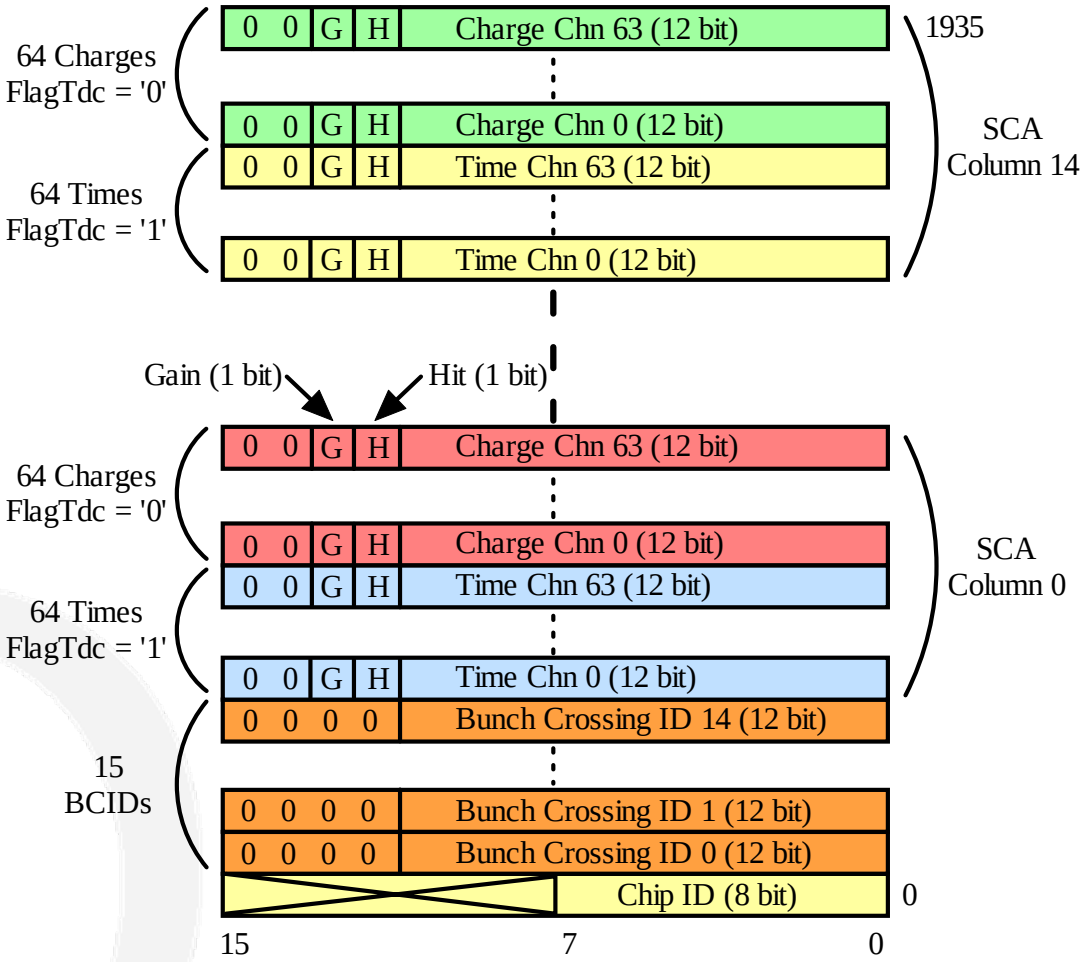
Floorplan & Digital I/O pins



Floorplan features:

- Size: 2800x1600 um
- 1 SRAM 2048x16: 2188x791 um
- 263 I/Os
  - M1 for Left / Right
  - M2 for Top / Bottom
- M1 / M2 / M3 used for layout
- 6 pins for VDD and 6 for GND
- 1 ring for SRAM
- 3 stripes of power

Memory mapping



- Amount of bits in memory:
  - For 0 trigger => Ndata = 0
  - For 0 < n < 16 => Ndata = (1 + n + 64n + 64n) x 16
    (ID & BCID & Charge & Time)