SiW ECAL status and plans

Daniel Jeans - LLR, Ecole Polytechnique
On behalf of the SiW ECAL group

- Mechanics

- Silicon sensors

- Electronics

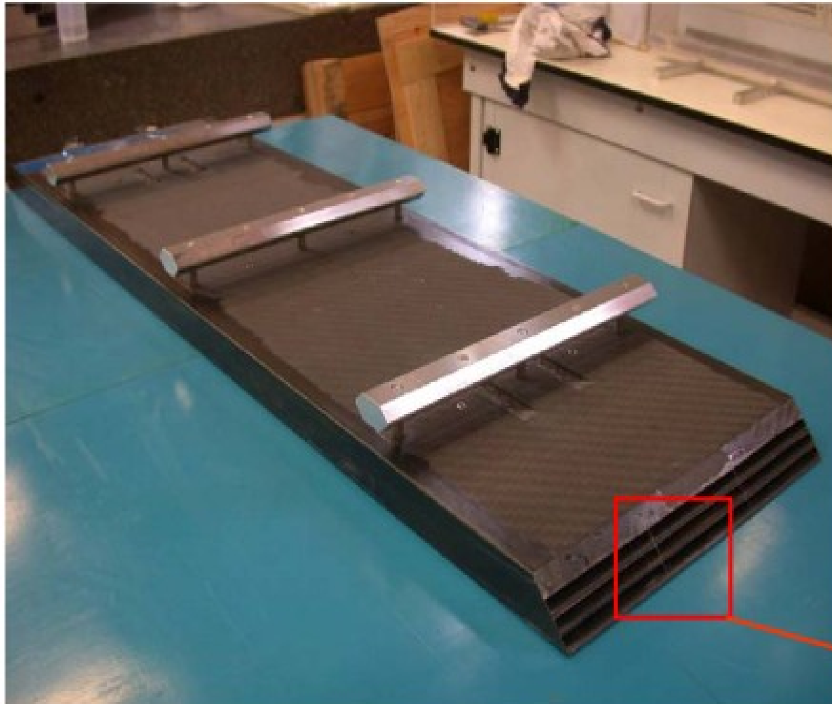
- plans for 2009-2011

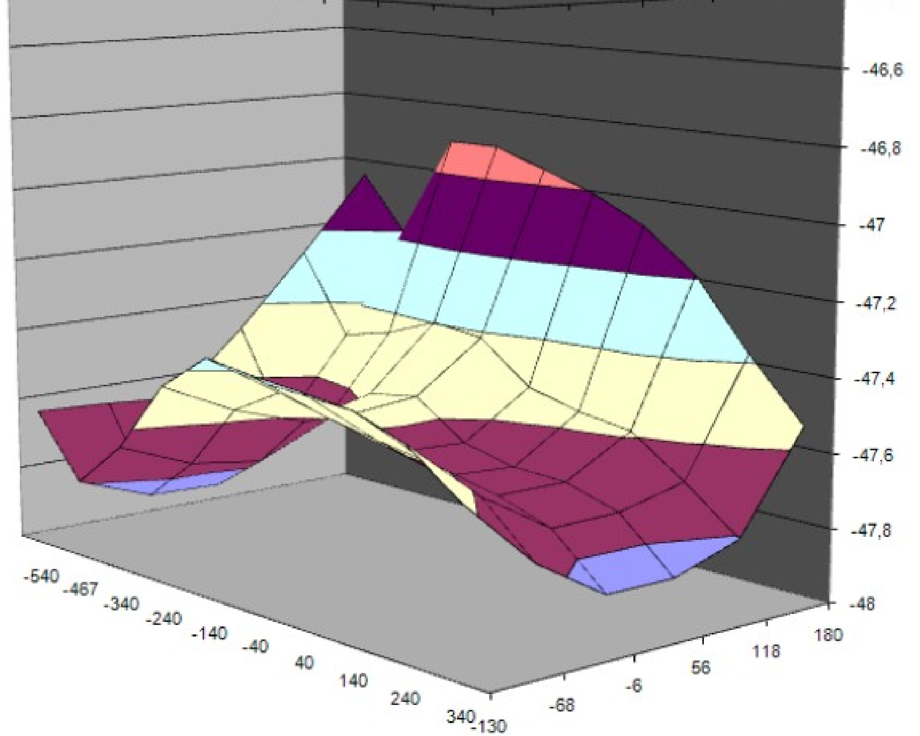
Mechanics

Technological demonstrator constructed

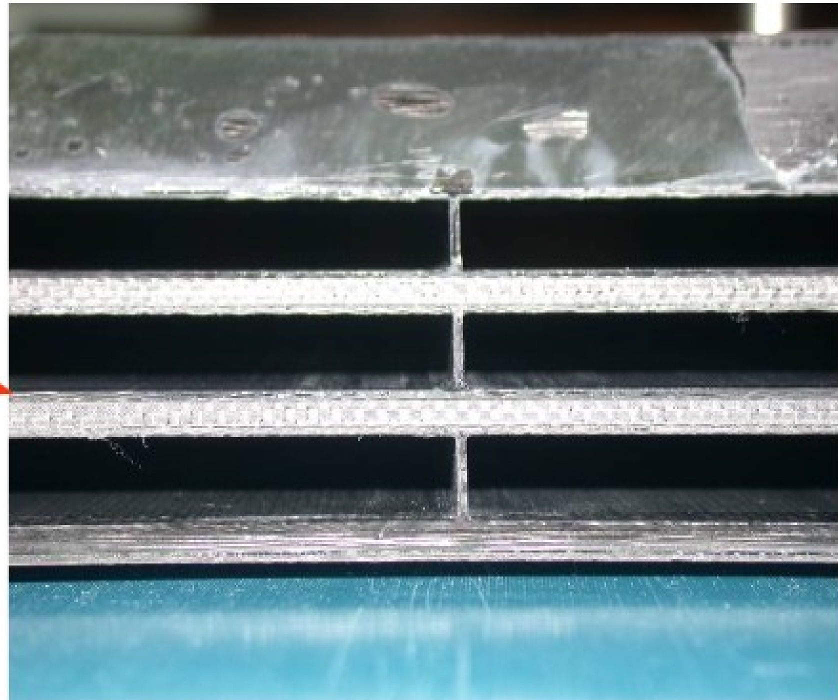
- Alveolar tungsten + CF structure: 3 layers
- No problems in manufacturing process
- Measured to meet required tolerances

Feasibility of alveolar design proven



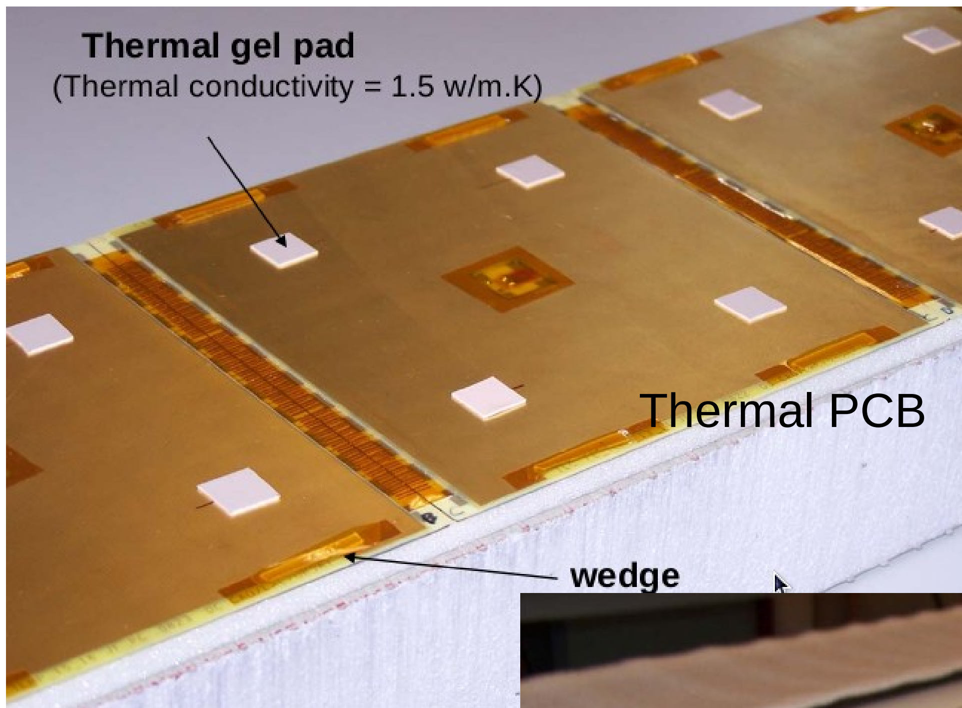


Flatness of top plate within 0.65 mm

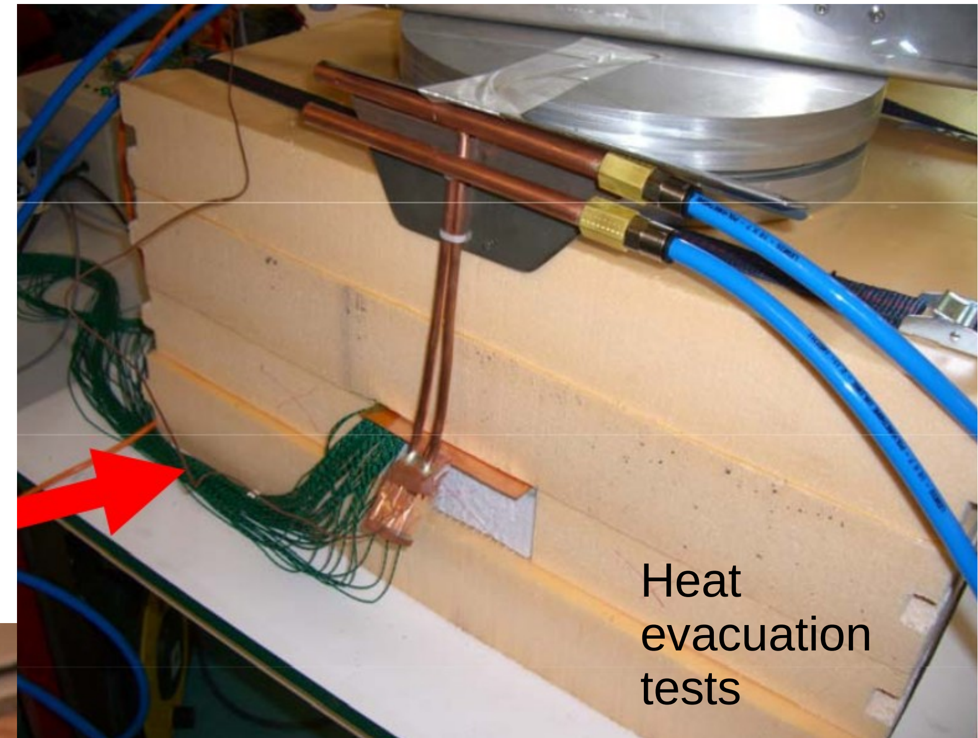


Two thermal slabs constructed

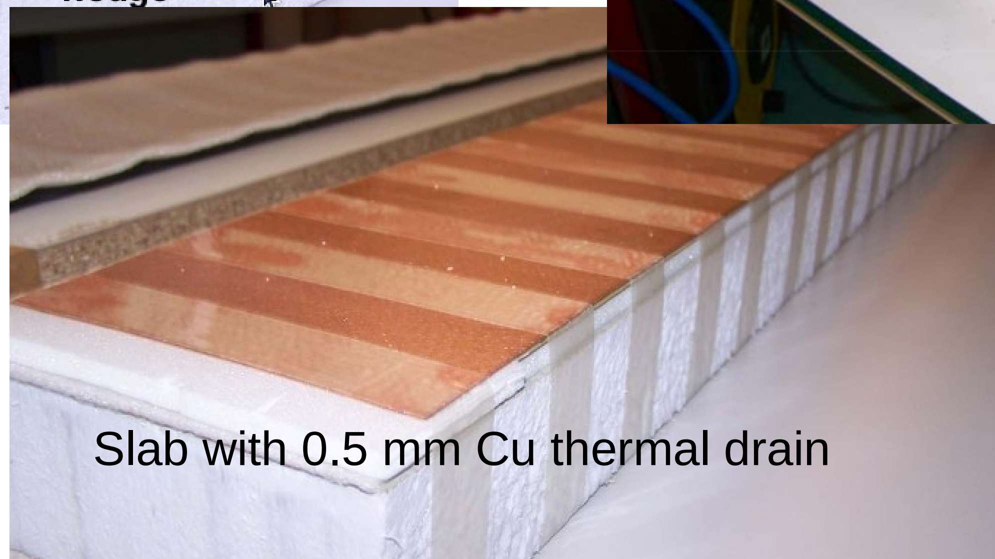
- Thermal PCBs (heating element & thermal sensors)
- PCBs from LAL, bonded and glued in the UK
- Prototype cooling system from Grenoble
- Thermal tests presently underway at LAL & Grenoble
- Understanding of heat extraction & its simulation



Thermal PCB



Heat evacuation tests



Slab with 0.5 mm Cu thermal drain

Silicon sensors

Hammamatsu produced 40 wafers

9X9cm2, 5x5mm2 pixels

A few test samples at LLR for testing

- look OK, will probably be able to accept all 40

Proven wafer technology

- but price is high (~1kEuro/wafer)

Ongoing R&D with OnSemi/Prague

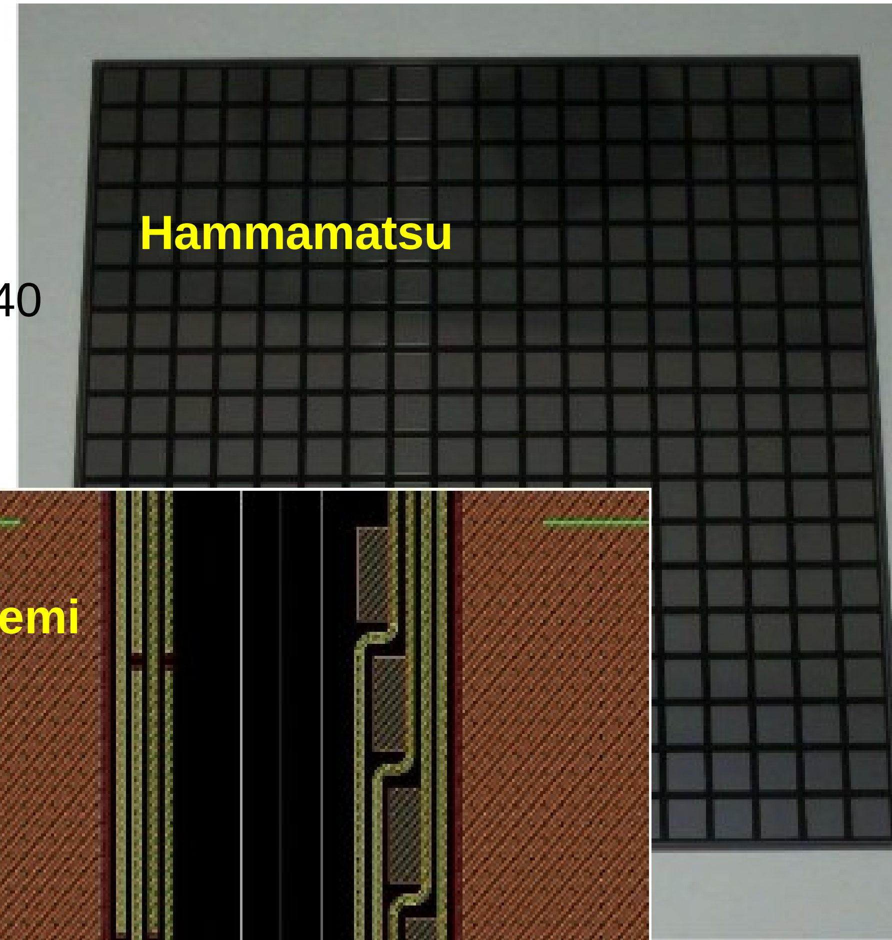
test sensors w/ different guard ring designs

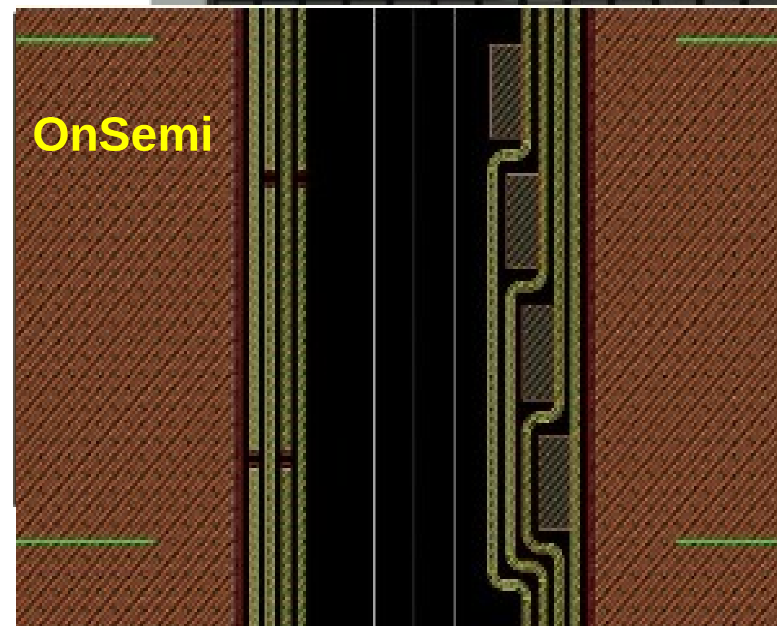
(segmented guard rings)

- signal propagation along guard ring can be controlled

More tests to decide optimal segmentation

Recent contact with BhaBha A.R.C. (India)





Electronics & PCBs

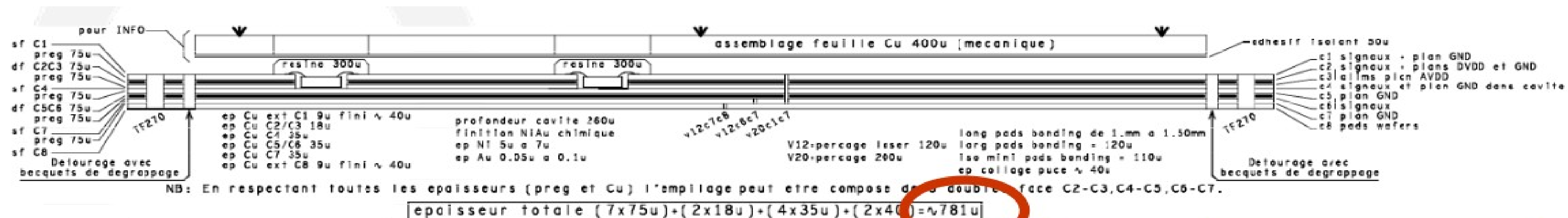
PCBs:

- "FEV7_ChipInPackage"
  - Surface mounted, packaged SPIROC2 chip (running in SKIROC mode)
  - Board has been received from manufacturer
  - Chip being mounted

- "FEV7_ChipOnBoard"
  - Embedded SPIROC2 chip
  - Designed, orders placed

SKIROC2 chip under development
- First version available for tests ~early 2010

LAL/Omega ; More details in Christoph's talk



FEV7_COB design

PCB Thickness ~781µm

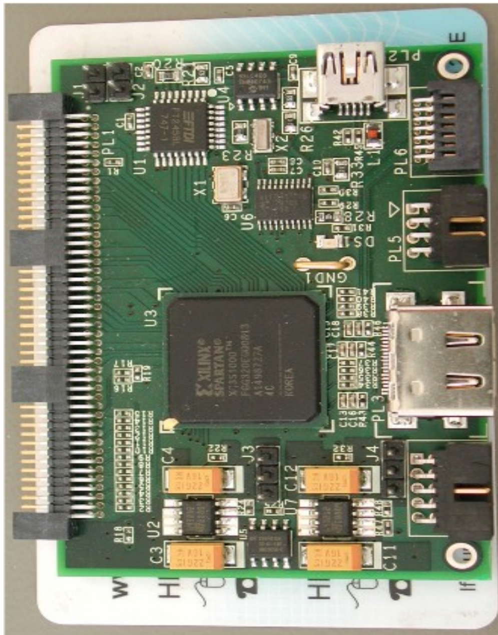
DAQ

(almost) all hardware for DAQ available (UK groups)
Last piece (LDA) should be available in ~1 week

Basic firmware & software architecture is in place
Further developments in progress

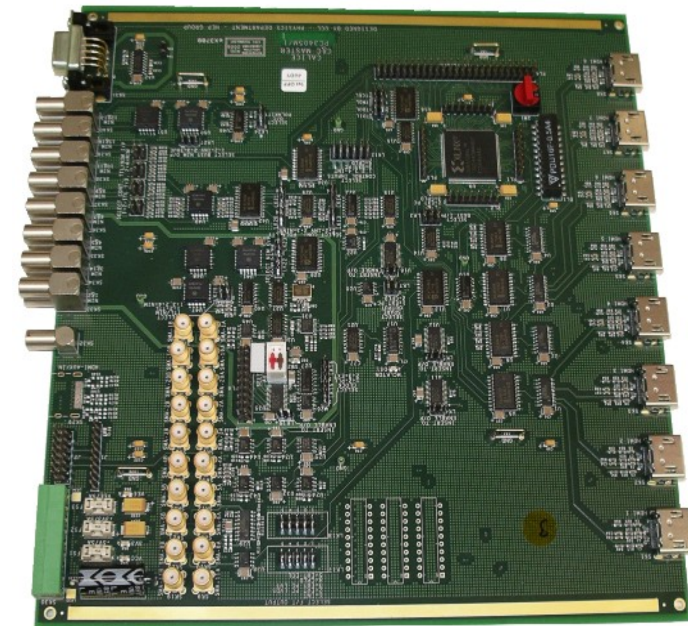
Integration into cosmic testbench underway (LLR)

ECAL DIF



LDA

C.C.C.



Future Plans

Electronics – critical path:
- test of PCB with packages & embedded chips
- Continue development of SKIROC2 chip

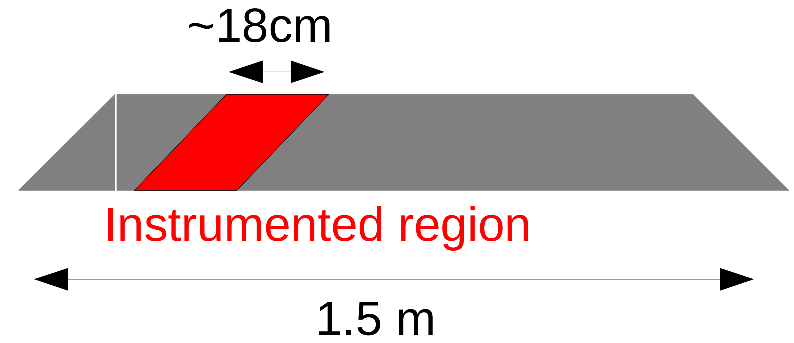
Mechanics:
- Continue thermal tests in demonstrator module
- Clean-ish room for slab construction
- Construct alveolar structure in Q1-2 2010
- Construct H structures

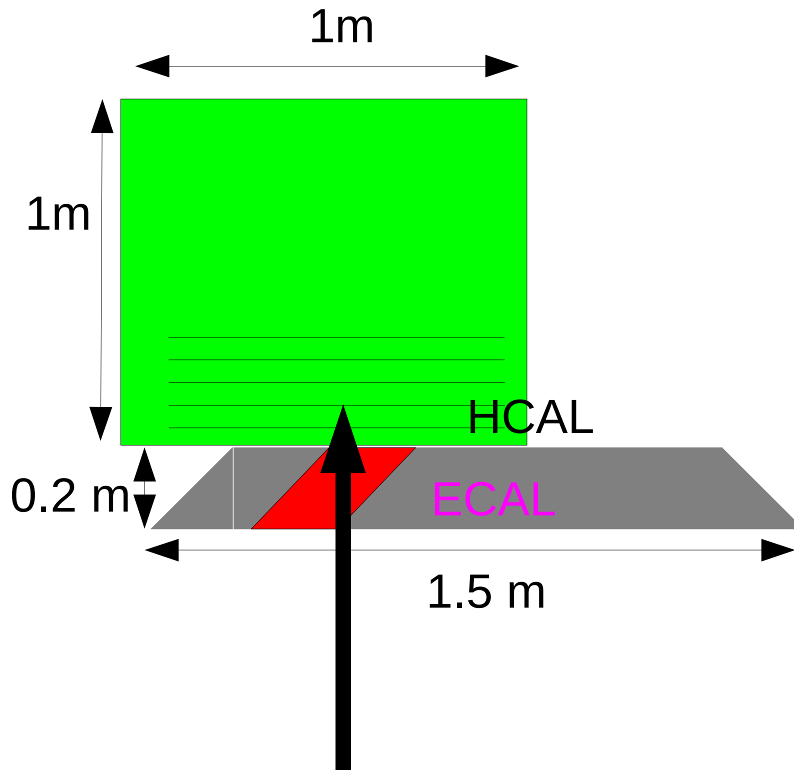
Wafers:
- Develop links with other manufacturers than Hammamatsu
  - Test samples
- Large scale purchasing in late 2010/2011

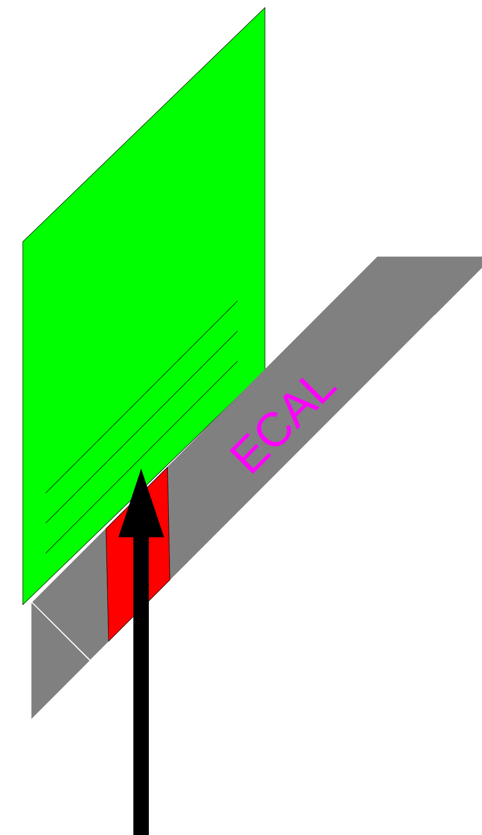
Integration:
- Cosmic testbench with CALICE DAQ
- Test various various PCB/FE chip combinations as available
  - ~1 wafer per PCB
- Start with short slab
- Then 1 long slab ~1.5m long, (partially) equipped

- Equip ECAL as funding allows
  - <~ 10k Euro per layer (wafers + PCBs + ...)

Instrumented region & combined TB integration







Time line

	Mechanics	Electronics	Wafers	Integration
Q3-4 '09	Thermal tests	Tests of surface bonded SPIROC2	Test 40xHammamatsu	DAQ firmware
	Prepare assembly room		Guard ring test samples	Prepare cosmic bench
Q1-2 '10	Make alveolar structure	Tests of embedded SPIROC2	Test samples	Cosmic tests w/ SPIROC2
	Make 'H' structures	SKIROC2	from other	
Q3-4 '10		PCB w/ embedded SKIROC2	companies	
				Cosmic tests w/ SKIROC2
Q1-2 '11	Slab assembly		Order wafers	Start to instrument structure
Q3-4 '11				Partially instrumented
Q1 '12				Fully instrumented