Future DAQ system status

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CALICE Technical Board Review Meeting, FNAL, 16–17 June 2009

Outline

- System overview and recent progress
- Individual (hardware) component status and functionality
- DAQ software status
- Numbers of each component and availability
- Schedule to completion of DAQ system

DAQ system overview

(**Detector Unit**: ASICs)

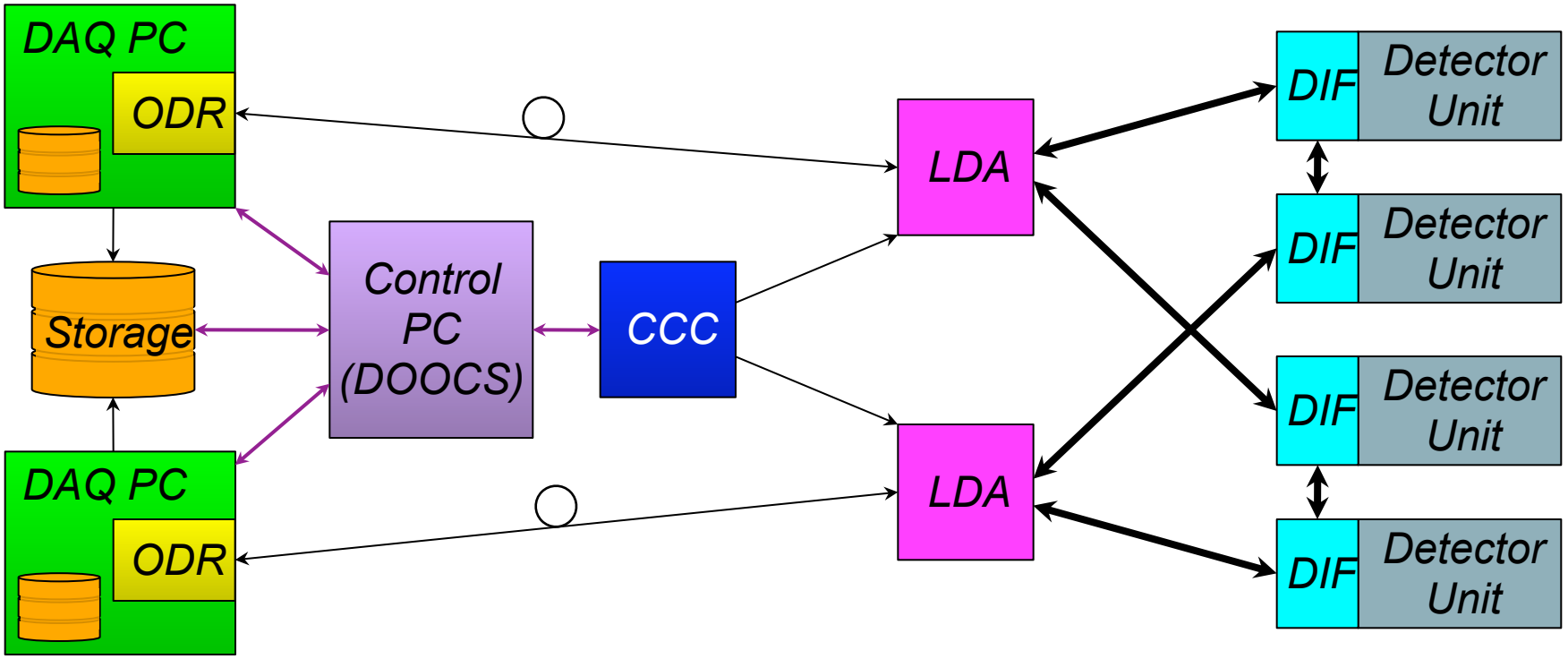
DIF: Detector InterFace connects generic DAQ and services

LDA: Link/Data Aggregator fansout/in DIFs and drives links to ODR

ODR: Off-Detector Receiver is PC interface

CCC: Clock and Control Card fans out to ODRs (or LDAs)

Control PC: Using DOOCS



DAQ system links

- DIF ⇔ LDA
  - synchronous, serial link with additional asynchronous pairs. 8b/10b encoded data
  - runs at N*machine clk: frequency 5..150MHz (assume 100MHz)
  - HDMI cabling and connectors
- LDA ⇔ ODR
  - Gigabit Ethernet (and TLK2501) serial protocol
  - SFP cage connector supports optical fibre
- CCC ⇔ LDA
  - compatible with LDA ⇔ DIF interface
  - CCC & DIF capable of stand-alone operation

Overall status

Hardware and firmware for all components at an advanced stage. Have been concentrating on :

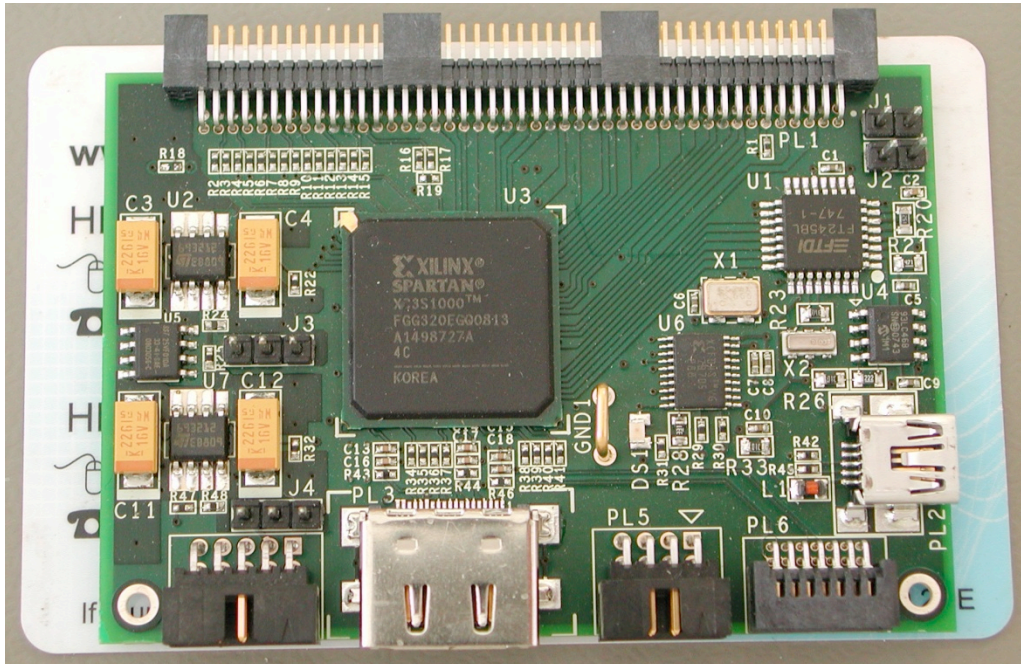
- firmware improvements and finalisation;
- final hardware tweaks and production versions of relevant components;
- hardware orders to have enough systems available for lab and beam tests;
- having (parts of) system available now to detector groups;
- acting on feedback from detector groups;
- further addition of documentation put on the CALICE twiki;
- design and writing DAQ software;
- DAQ component integration.

We need to (according to EUDET) have a working system by June 2009; it would be good for the detectors for the DAQ system to be available asap; we want to get a working system done asap and passed onto detector groups.

ECAL DIF

The ECAL DIF is being developed by the Cambridge group :

- AHCAL and DHCAL DIFs developed by other groups, but all within the DIF task force;
- involves board design and manufacture and firmware development;
- produced a prototype board which worked well, one in use at LLR. Have reduced number of components, whilst maintaining functionality (e.g. FPGA);
- two DIFs have been produced and were powered up;
- firmware is now being ported for extensive testing;
- can then produce full run of 40 ECAL DIFs—all PCBs and components in-house.
- Stable version of firmware for DAQ tests;
- Tested using pseudo-LDA, now ongoing with real LDA;
- Updated according to proposed data format within the DIF task force.



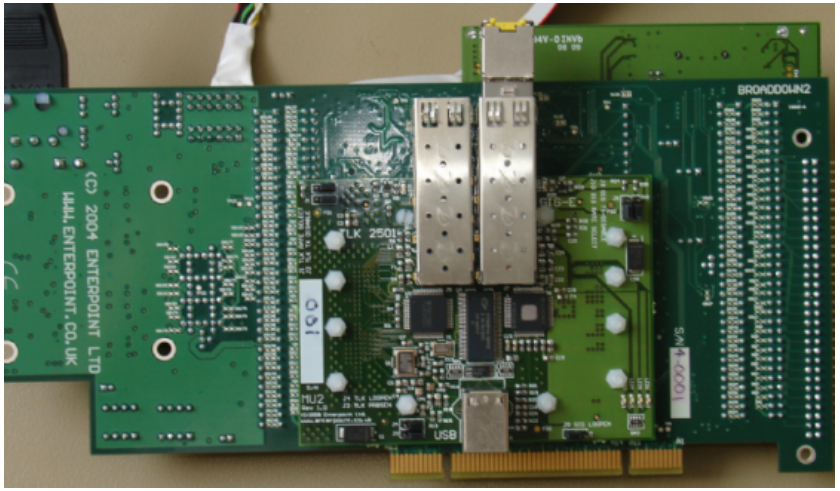
See B. Hommels, “DIF status”, Electronics/DAQ meeting, 31/03/09, DESY

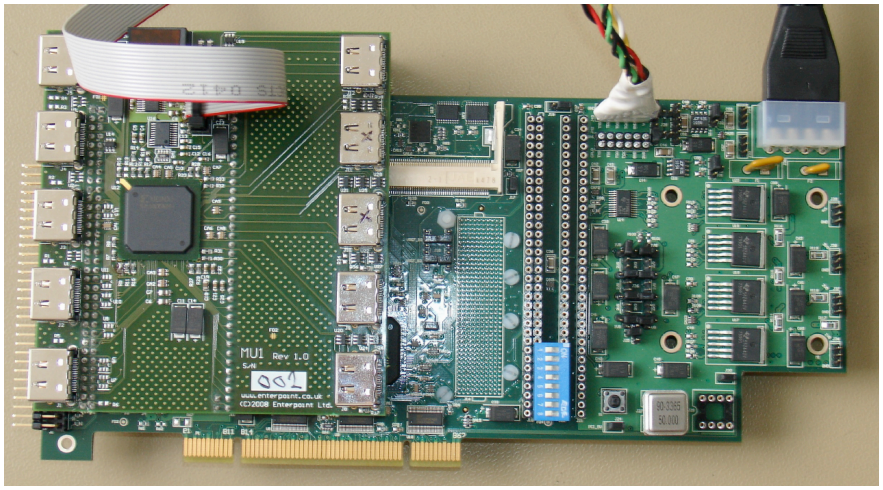
LDA

Essentially a concentrator card, recall the LDA hardware, from Enterpoint, consists of :

- a (Broaddown2 → Mulldonoch2) baseboard;
- an add-on HDMI board to connect to 10 DIFs;
- an add-on ethernet board to connect to an ODR.

So this is an example of commercially-available, off-the-shelf equipment ... all of which needed some corrections/additions/modifications from ourselves...





- Have 20 baseboards in-house ready for use;
- Have 5 ethernet boards in-house ready for use, with 15 being manufactured;
- Have 5 HDMI boards in-house which can be used, with 20 (AC coupled) being manufactured.

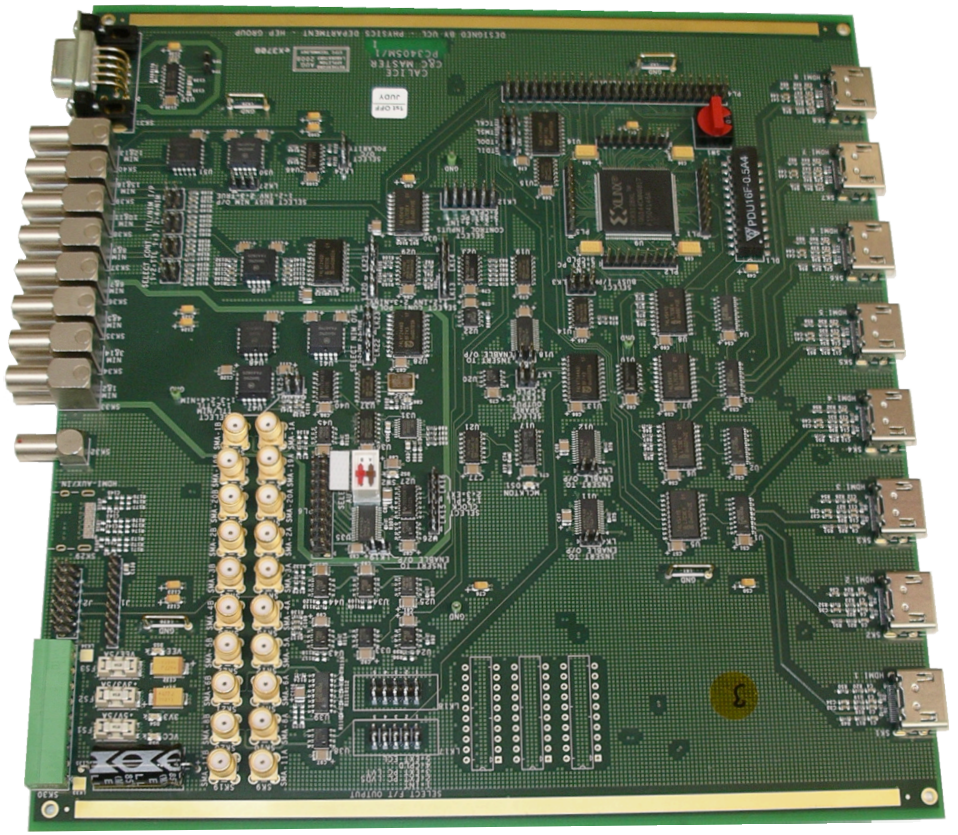
LDA firmware

- Firmware and software development continued whilst hardware issues were being sorted out.
- A LODDAR was developed which made an ODR “look” like an LDA :
  - This could verify the basic firmware functionality;
  - Not a complete test as specs not exactly the same;
  - But could establish path in both directions.
- Now with real LDAs, testing communication with the DIF.
- As the LDA is in the middle, its readiness has been crucial in allowing full system tests to be started.
- Getting some ready for distribution to detector groups.

See M. Kelly, “Status of LDA”, Electronics/DAQ meeting, 31/03/09, DESY

CCC

- A simple(ish), custom board which fans out machine clock to 8 LDAs.
  - Multiple types of signal input.
  - Provision for async scintillator type signals
  - Also capable of aggregating and generating Busy feedback.
- After building and testing two prototypes, had a further eight manufactured.
- Now have five working and tested CCCs all boxed up with power supplies, etc.
- One has been in use at LLR.
- Problem found (at LLR), the serial interface clock changes when you would hope it to be stable.

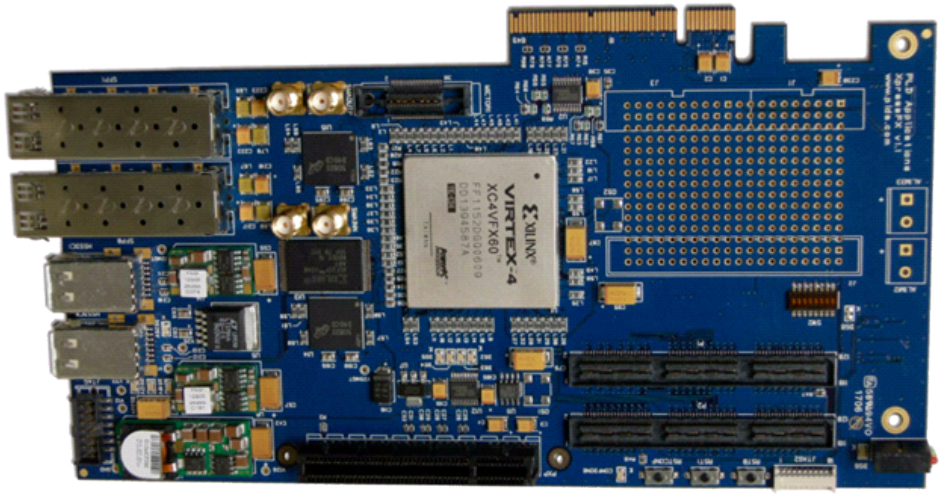


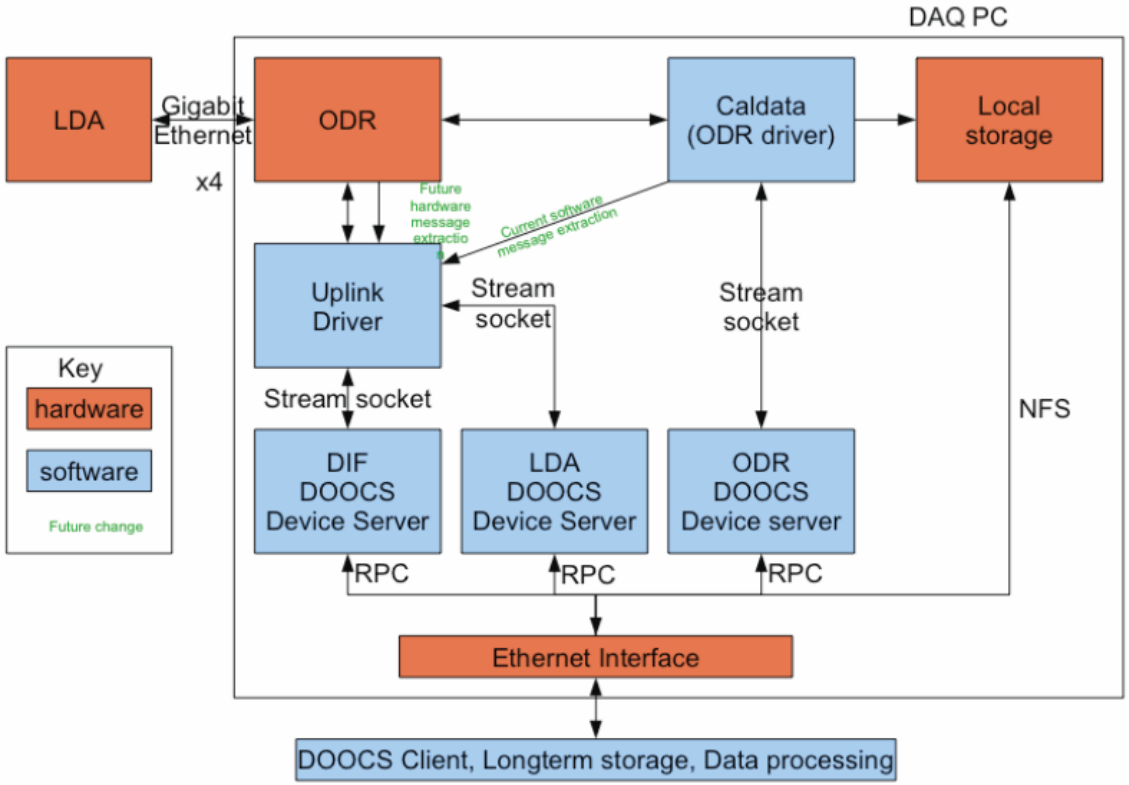
- Simple hardware modification to all boards.
- Extensive documentation and manual being twiki'ed.
- Available for use by detector groups.

See M. Postranecky, "Status of the clock and control", Electronics/DAQ meeting, 31/03/09, DESY

ODR and DAQ PC

- The ODR is a commercial FPGA board with high speed links and PCIe bus.
- Receives data on 4x fibres (RX)
- Writes to disk fast (> 150 MB)
- Sends data up fibre (TX)





- Housed in DAQ PC.
- Customised firmware and software, interfaced with the DAQ software.
- Optimised for performance.

ODR and DAQ PC

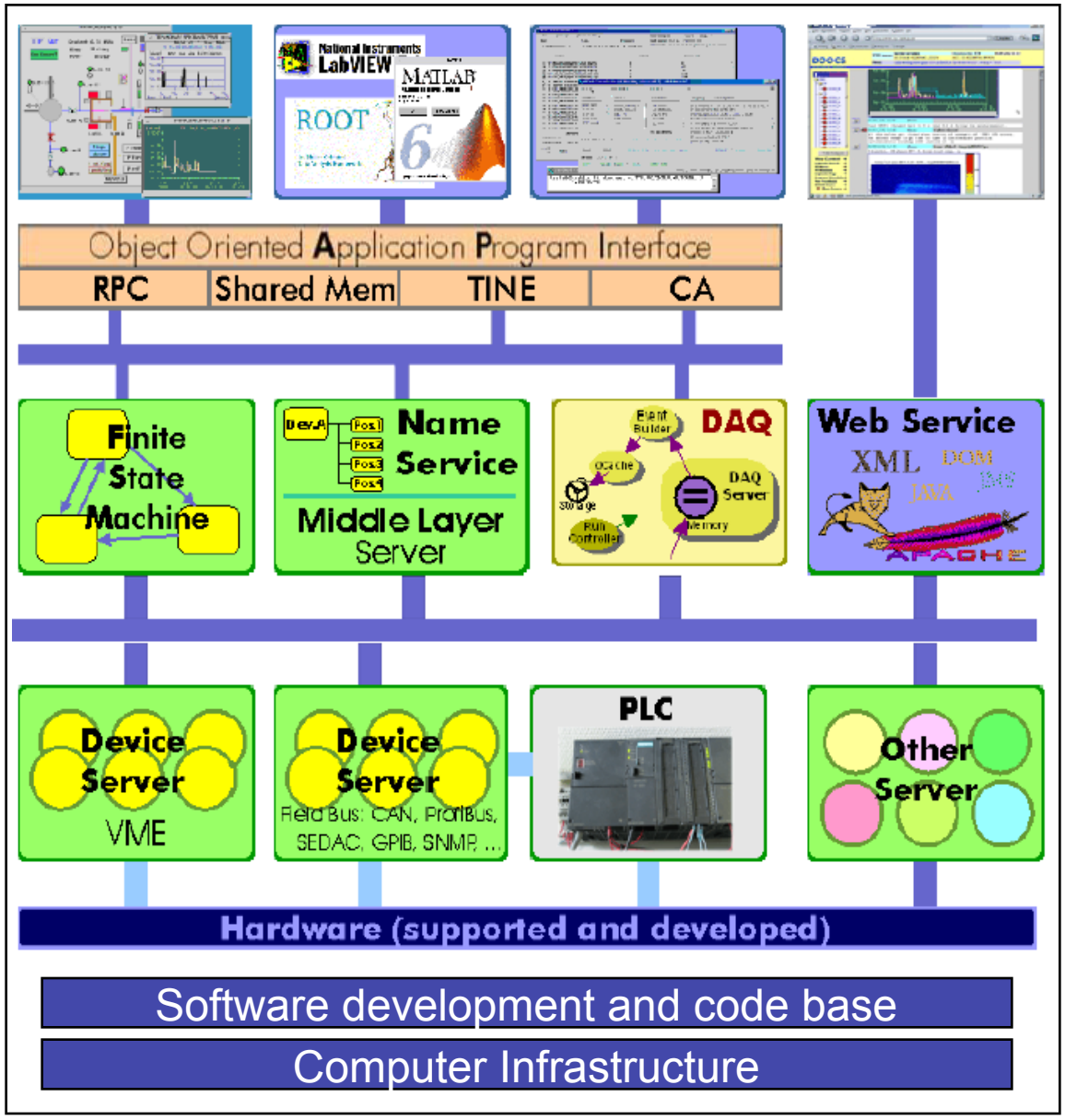
- System has generally been stable for a while : firmware written, linked to DOOCS, talk to an LDA emulator and a LODDAR, etc..
- Had problems with different versions of boards—essentially the same Virtex4 boards, with small modifications V1 → V2.
- Everything was stable on V1 for a long time, but could not get firmware to work on V2 boards and eventually traced down to faulty boards.
- Have received replacement V2 boards and all works fine.
- Now have 3 V1 and 2 V2 boards working and have ordered three more V2 boards (expect in a couple of weeks). It would be nice to have all V2s...
- Have three DAQ PCs with raid arrays and in process of building up three more with smaller disks for small-scale tests.

See M. Warren, “DAQ status and overview”, Collaboration meeting, Manchester, 09/09/08 and elsewhere.

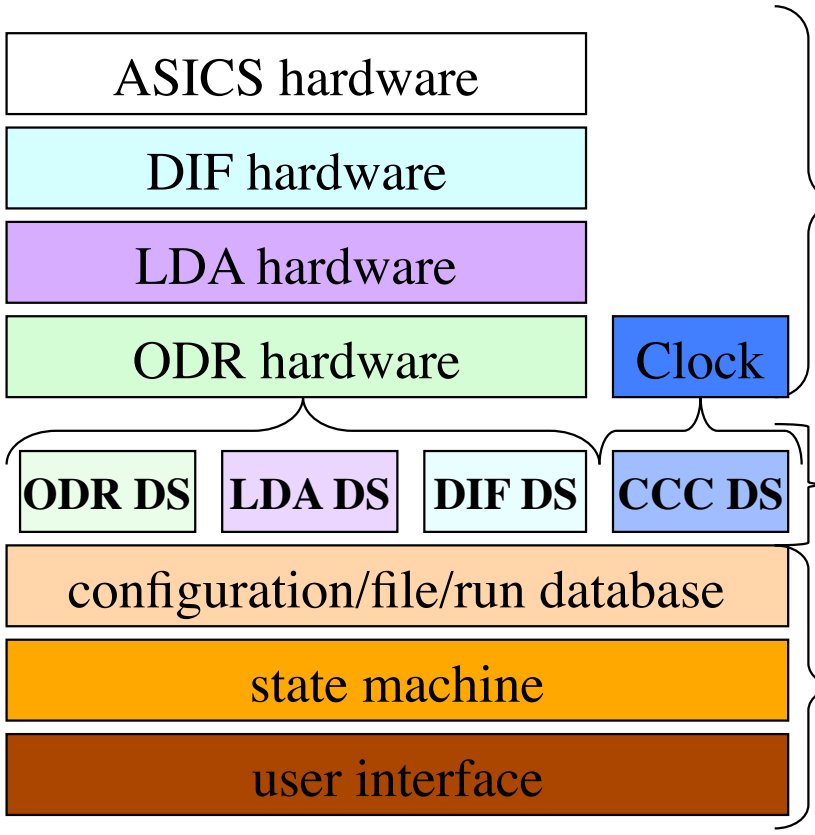
DAQ software

- Several calorimeter types each of significant complexity: O(10^4) channels, O(10^3) ASICs, O(10^2) DAQ electronics boards
- Need control software which can handle these numbers and has a large functionality and preferably already written (and supported)
- Chose DOOCS being developed at DESY for XFEL

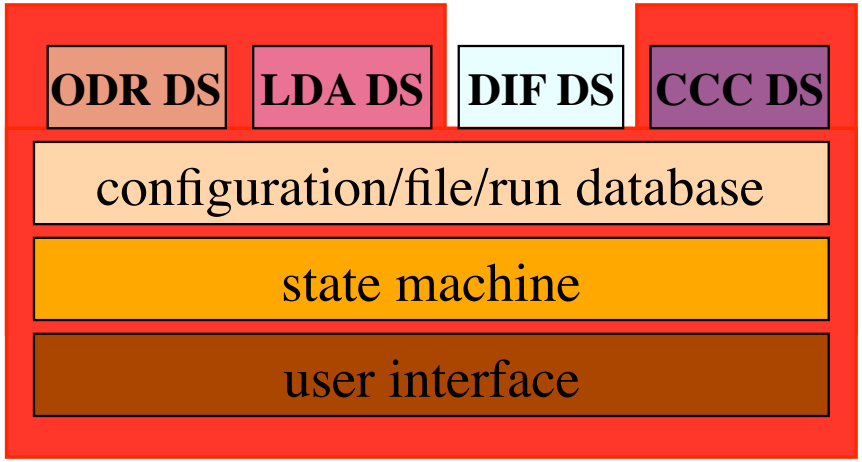
url : tesla.desy.de/doocs/doocs.html!



DAQ software



- Development started on almost all of the main software components.
- Emulator for the LDA, DIF development not yet started.
- User interface, ODR interface and CCC device server done.
- Database and state machine started.



See V. Bartsch, “DAQ software”, Electronics/DAQ meeting, UCL, 09/06/09

Hardware numbers needed

Detectors' requirements :

- ECAL : 30 layers ⇒ 30 DIFs, 3 LDAs, 1 ODR and DAQ PC, with 1 CCC
- AHCAL : 48 layers ⇒ (48 DIFs), 5 LDAs, 2 ODRs and 1 DAQ PC, with 1 CCC
- DHCAL : 40 layers ⇒ (120 DIFs & 14 DCCs), 2 LDAs, 1 ODR and DAQ PC, with 1 CCC

In general DAQ groups have to provide :

- 30 ECAL DIFs, 10 LDAs, 4 ODRs, 3 DAQ PCs, 3 CCCs;
- sufficient spares for test-beam running;
- additional systems for tests in labs.

Our procurement plan is :

- 40 ECAL DIFs
- 20 LDAs
- 8 ODRs and 8 DAQ PCs
- 10 CCCs

Hardware in-house

- 40 ECAL DIFs :
  - All components and PCBs in-house for full complement of production DIFs;
  - Building and testing 2 (1 for LLR tests who have a prototype DIF) of them before doing production run;
- 20 LDAs :
  - Have 5 full LDAs in house—baseboards, ethernet (to ODR) and HDMI boards (to DIF);
  - Have all 20 baseboards in-house;
  - Ethernet boards (few weeks) and HDMI boards (1−2 months) on order;
- 8 ODRs and 8 DAQ PCs :
  - 5 ODRs (3 V1 and 2 V2) with 3 (V2) to receive in couple of weeks;
  - 3 DAQ PCs in-house, 3 being ordered and built.
  - 1 of the V1 ODRs and DAQ PC is at LLR
- 10 CCCs :
  - All in-house.
  - 5 tested and working, 3 to be done (2 not planned to be used—prototypes—only if needed).
  - 1 CCC is in LLR.

Summary

- Progress being made (firmware, purchasing, developing) for all components.
- We are gradually building up a stock of components which should be sufficient for lab and beam tests. Complete in couple of months.
- In the meantime we should have enough for needs of detector groups now.
- We “just” need to give an LDA to LLR for them to have a complete system.
- Crucial to all of this are system tests.
- We need to finish quickly, so during the summer, we hope to have fulfilled our EUDET goal and have a robust system for use.