Status of the DCC and DAQ Test Bench at LLR

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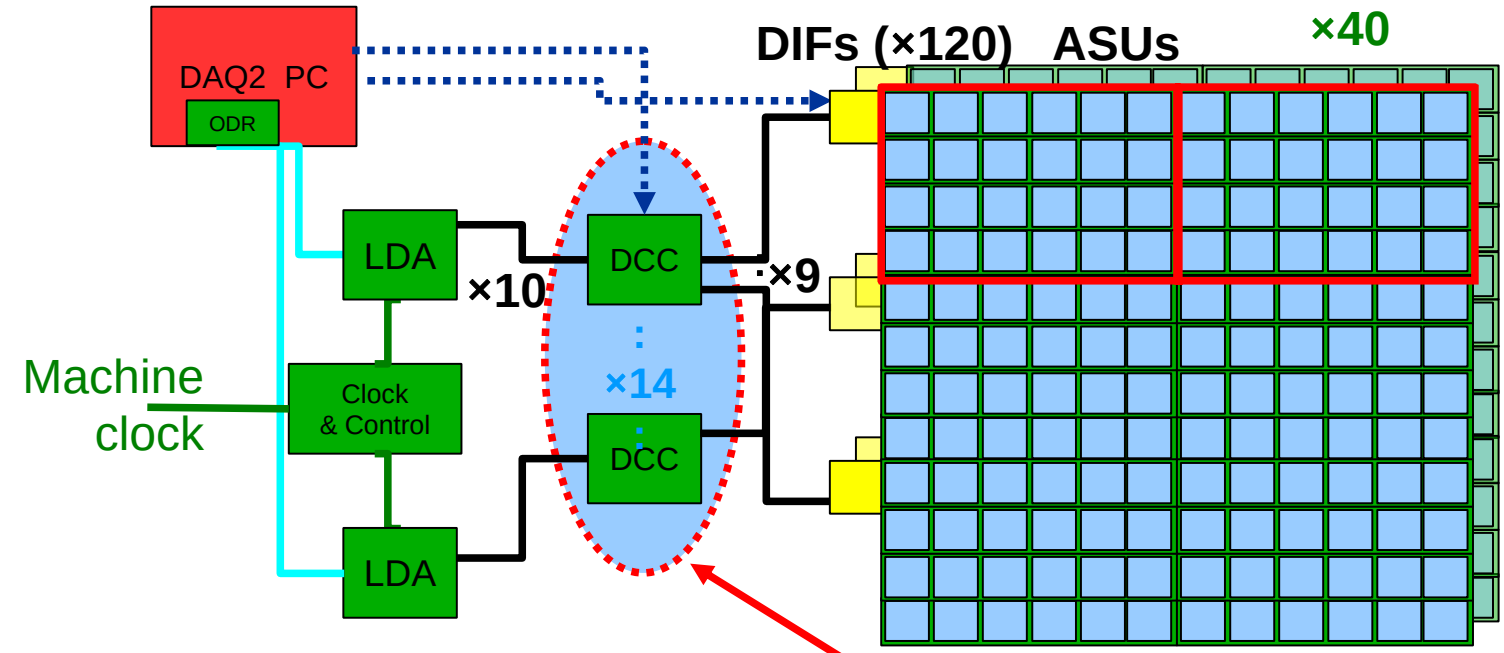
DAQ overview



Digital (Config, Control, Data, trigger, spill) over HDMI

Clock & Sync over HDMI

Optique GigE

Debug USB

DCC being developped at LLR

120 DIF → 12 LDA → 4 ODR

120 DIF → 14 DCC → 2 LDA → 1 ODR

Gain for DCC ≤ 1600€

Everything is resumed here

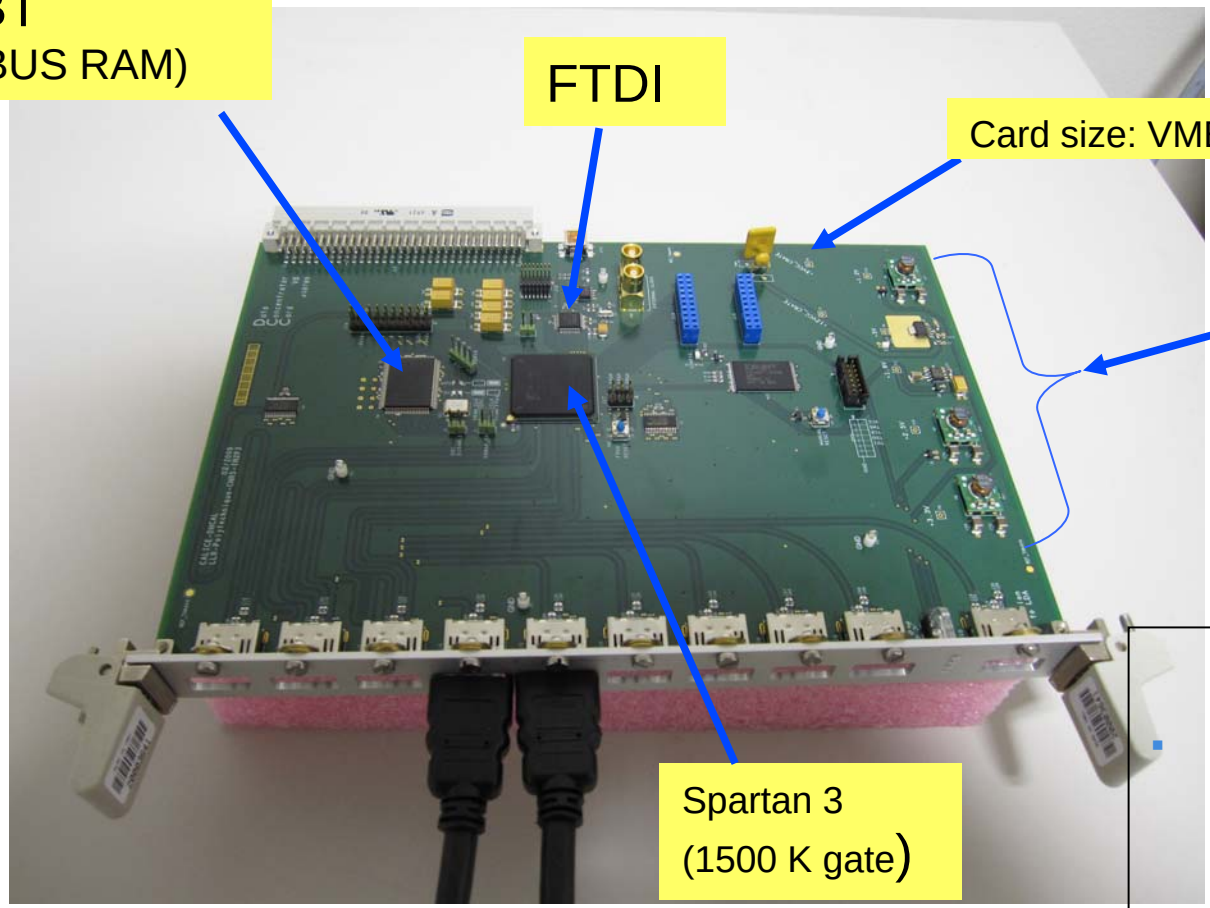
- Main specification :

Reduce the number of LDA and ODR for the DHCAL & optimize the data flux

- Without DCC :
  - 3 Difs/layer (40 Layers)
  - 10 Difs/LDA => 12 LDA and 3 ODR
- With DCC, we need :
- 9 DIFs/DCC => 14 DCC => 2 LDA and 1 ODR
- Characteristics :
  - To be transparent between DIF and LDA
  - Broadcast all fast commands from LDA to all DIFs
  - Send the packet R/O one after the other
  - Read 9 DIFs (objective)
  - Availability of USB access
- Firmware : Re-use as far as possible existing VHDL blocks (Marc)
- Homemade card
  - Cheaper: objective (max 600 € /card) for the production

DCC picture

16×1M ZBT
(no latency BUS RAM)



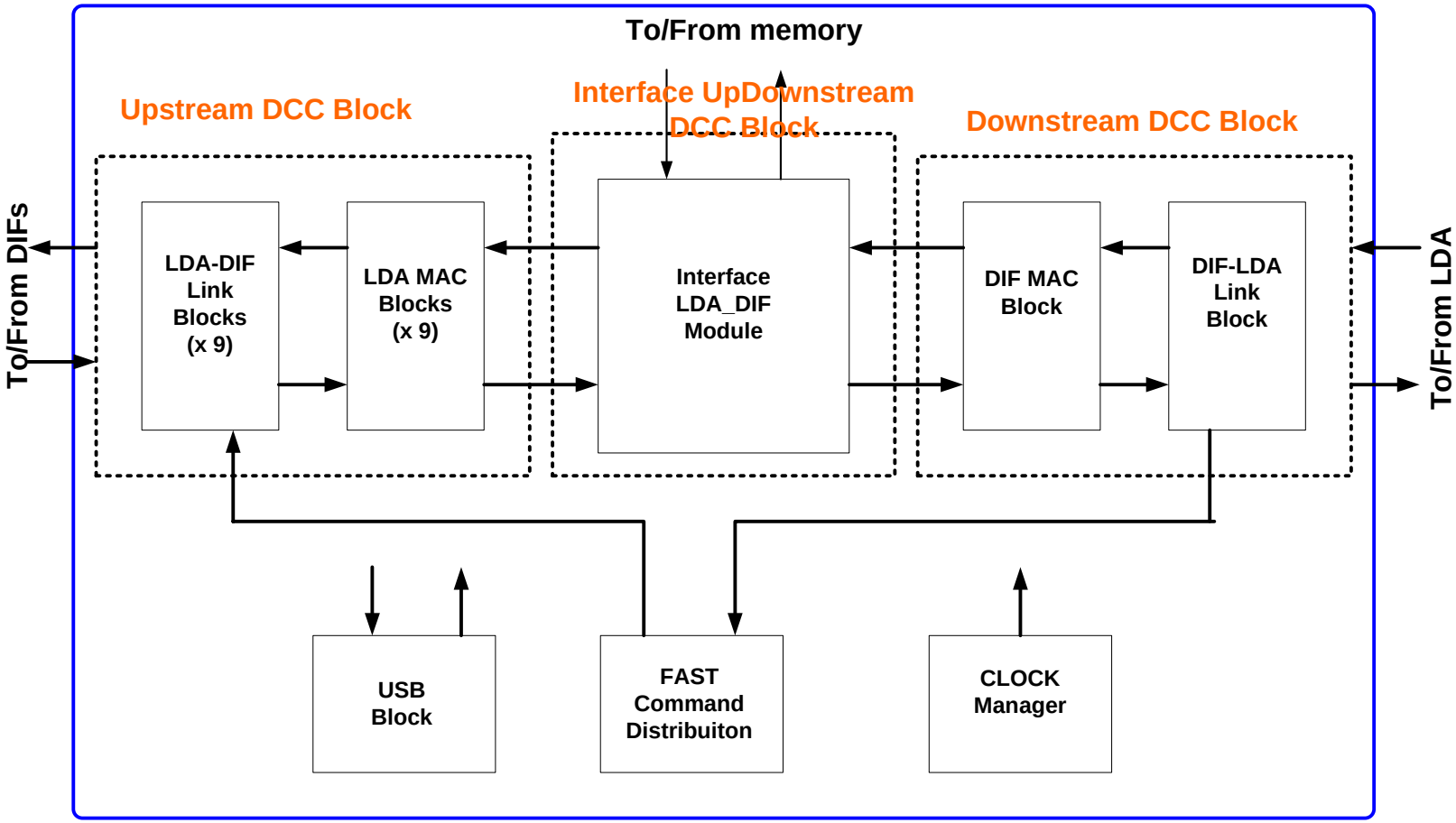
Cost proto I:

- 2 protos: ~ 19**00**€/card

Cost est.:

- 20 prods: ~**600**€/card

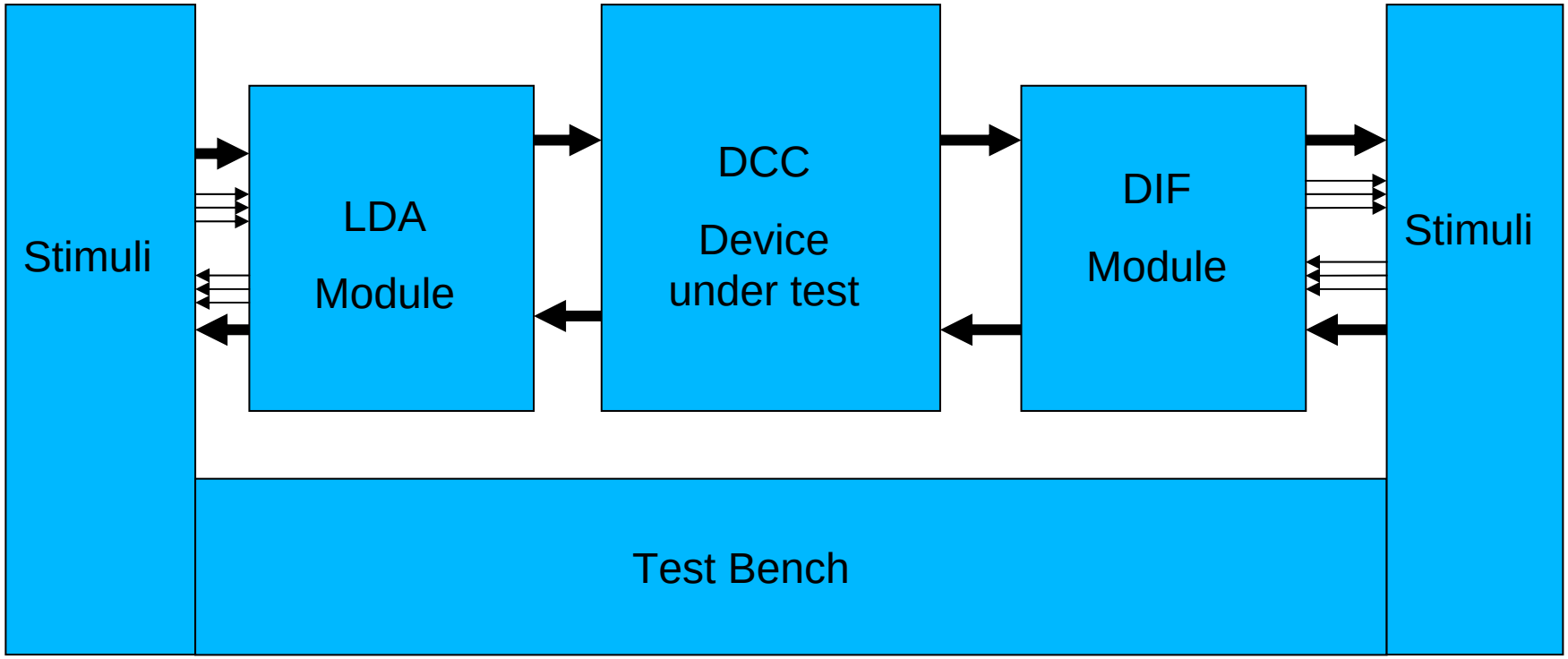
FPGA architecture by functionalities



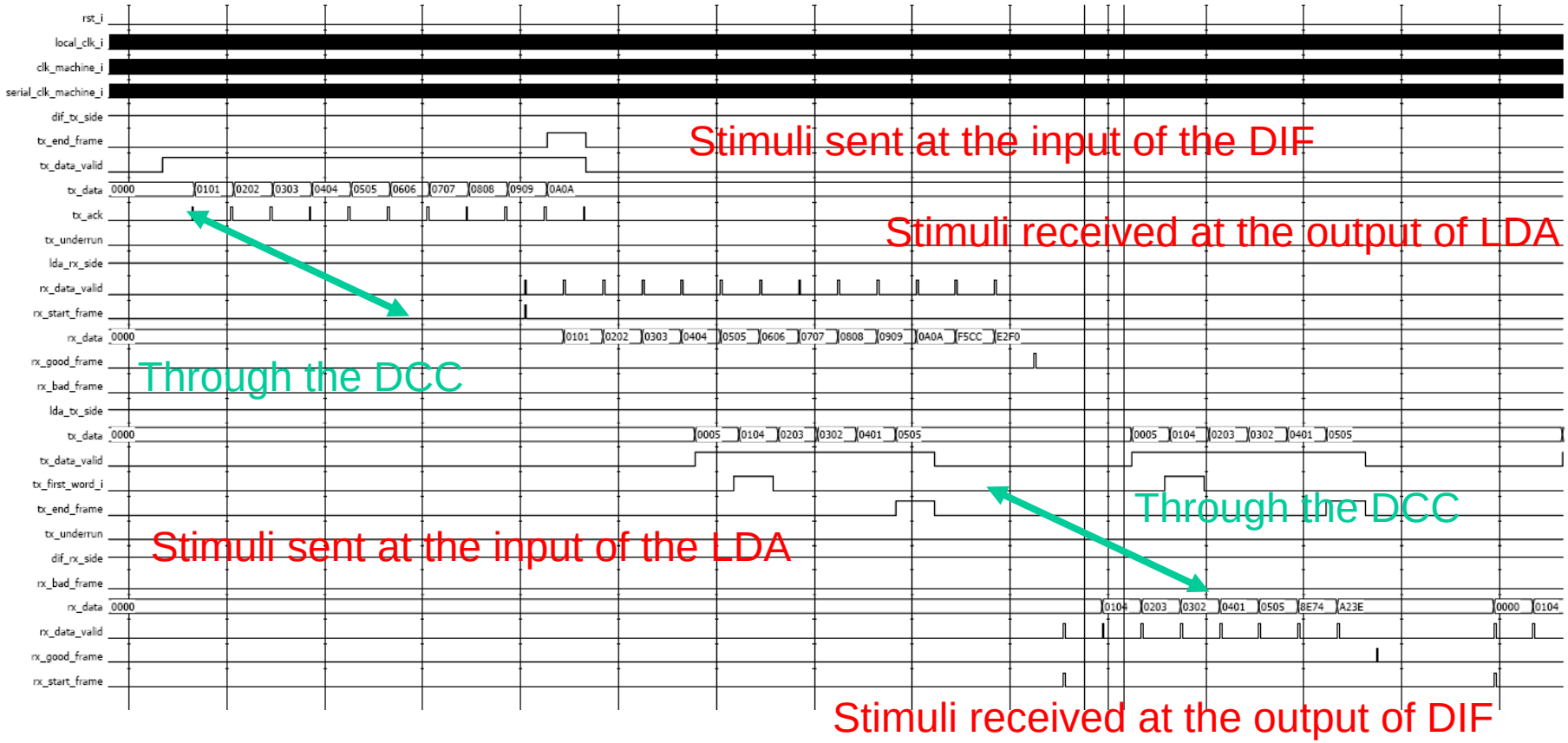
VHDL Blocks

- All VHDL blocks are designed
- Some bugs are still present but all are identified
  - End Oct. : Bug resolved
  - End Nov. : Validation of VHDL in test bench
  - End Dec. : Full validation of DCC

VHDL Test Bench



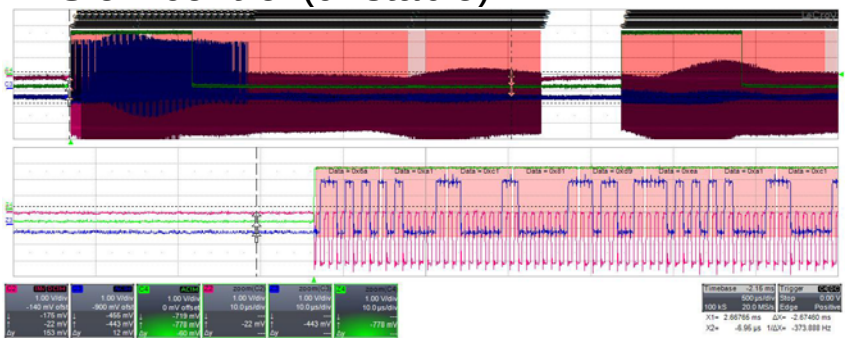
Example of simulation

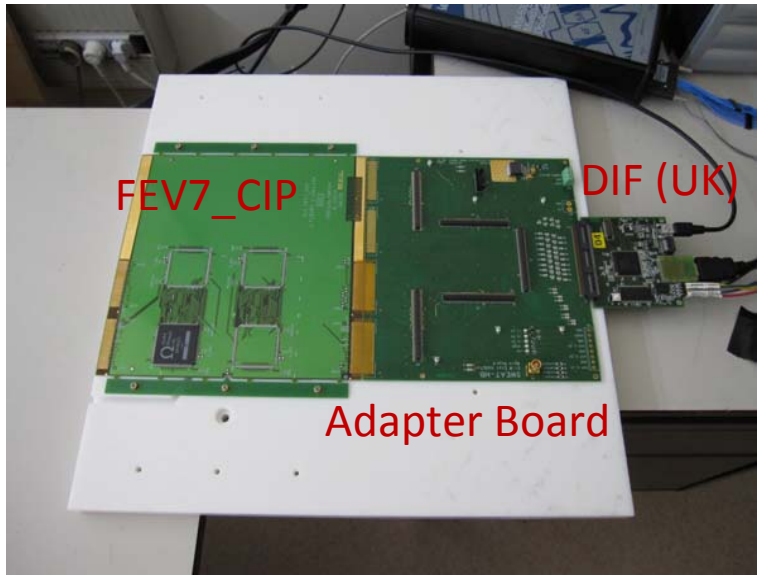


ECAL : First SLAB prototype assembled (03/07/09)

- Basic firmware for the DIF is developed
- 50 MHz
- HDMI/USB multiplexed
- Unique interface inside DIF
- Hardware test have started by the end of August
  - FCMD
  - BTCMD

  } From HDMI
  - Slow control (unstable)





- Connexion to SPIROC2 should be effective within 2 weeks
- More details in ECAL session

Test bench at LLR

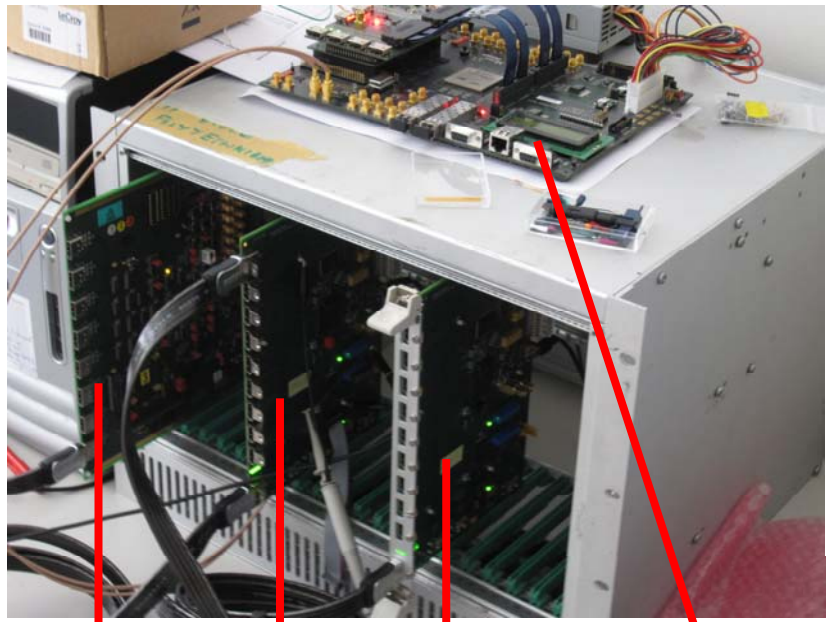
Test Bench overview

DIF part

LECROY SDA scope

DCC Chassis

CCC & DCC Chassis



CCC card

DCC 1

DCC 2

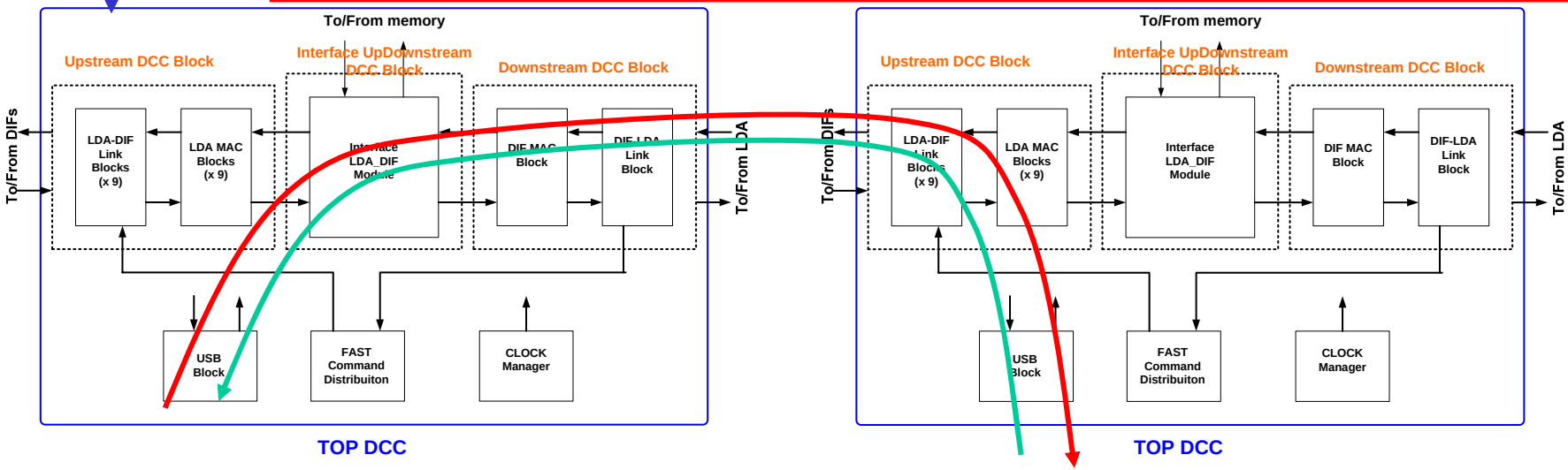
CLK generator

Test with two DCC

CLK

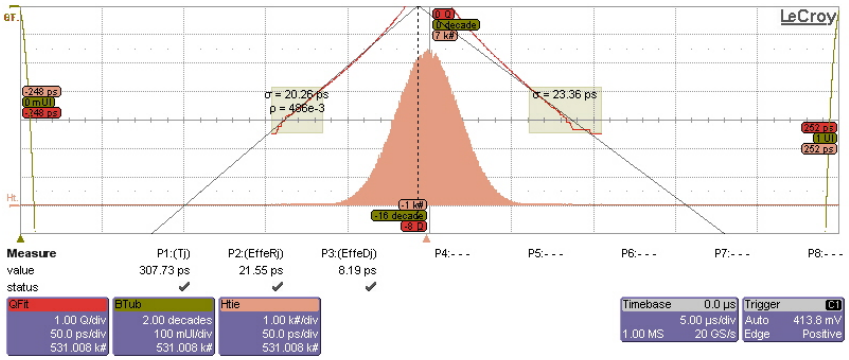
sent by the CCC

Everything is controlled via USB
Data sent by the DCC (Lda) or DCC (Dif) and controlled by a probe on serial link
Serial data decoded with a serial data analyzer

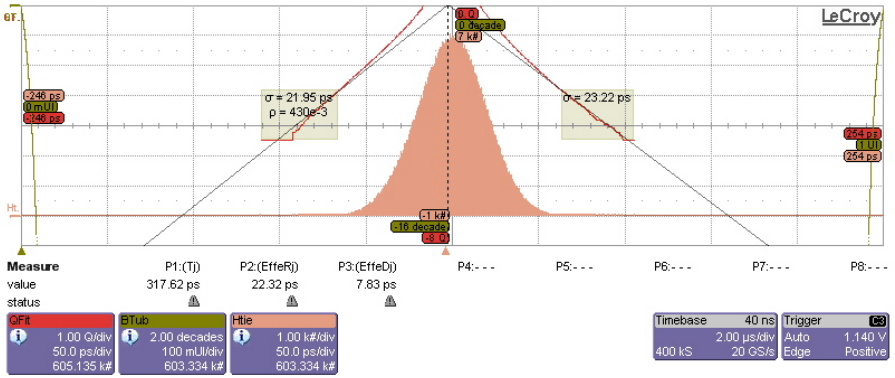


Link DCC(LDA) to DCC(DIF) via USB
Link DCC(DIF) to DCC(LDA) via USB

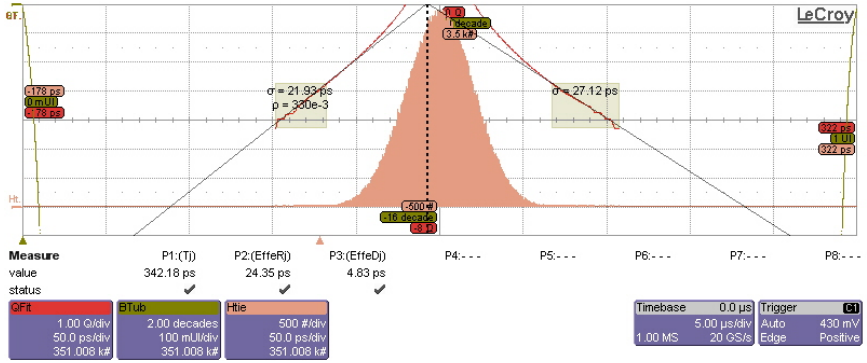
First test (clock)
ccc => dcc => dif



Jitter at the input of CCC : Tj = 307 ps



Jitter at the input of DCC : Tj = 317 ps

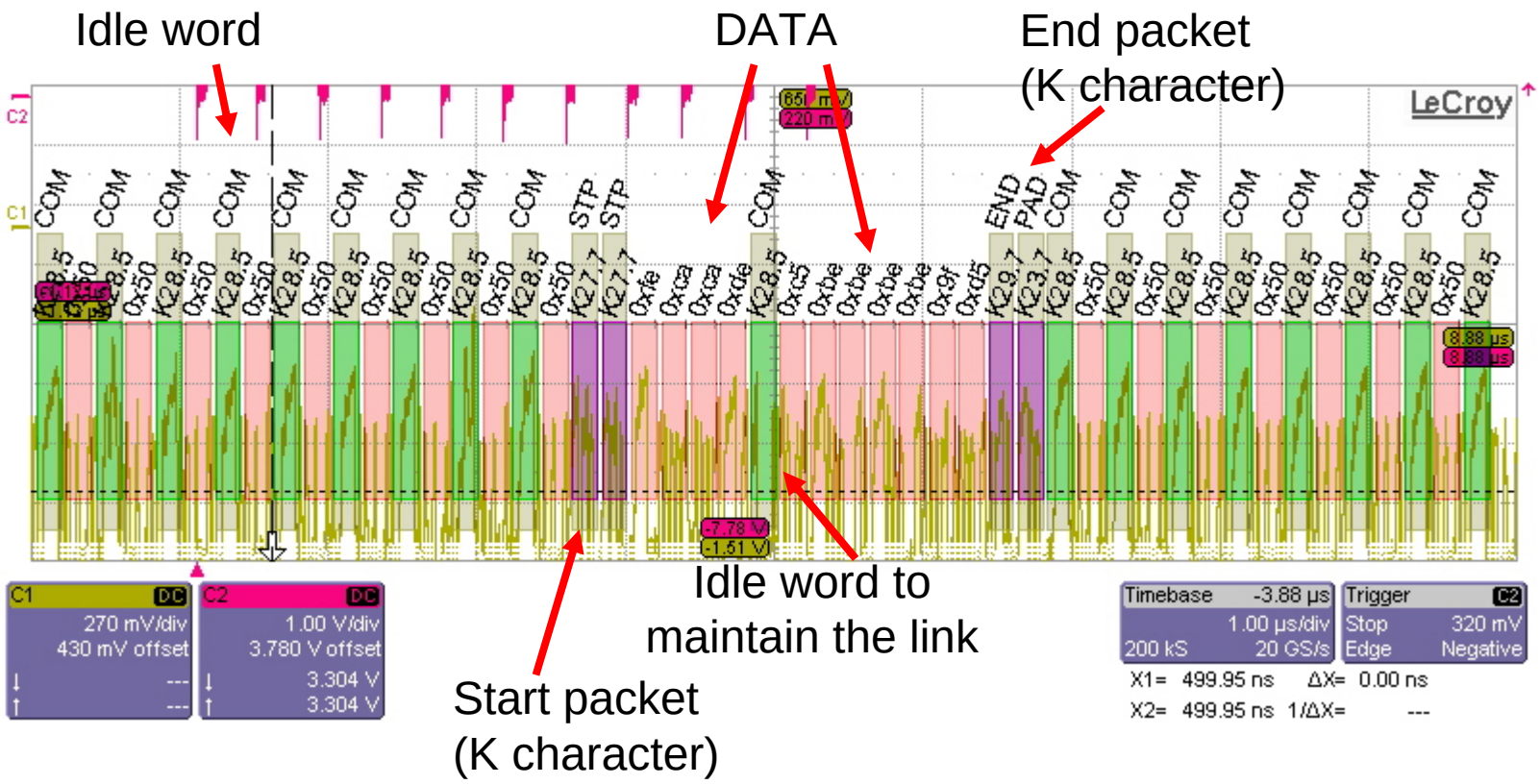


Jitter at the input of DIF : Tj = 342 ps

Jitter induce by the DCC
Jitter ~ 35 ps

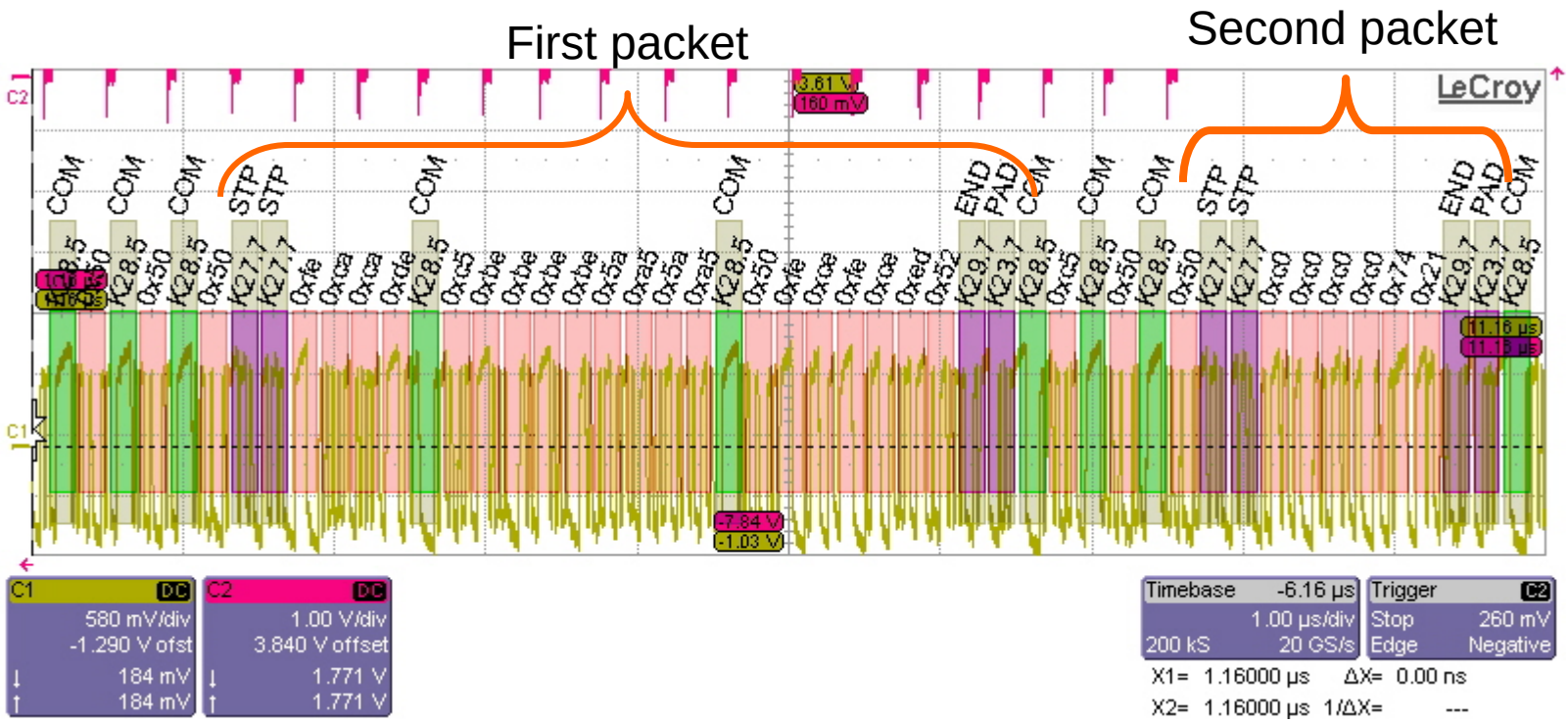
Some results on serial link

Data sent from DCC(DIF) to DCC(LDA)



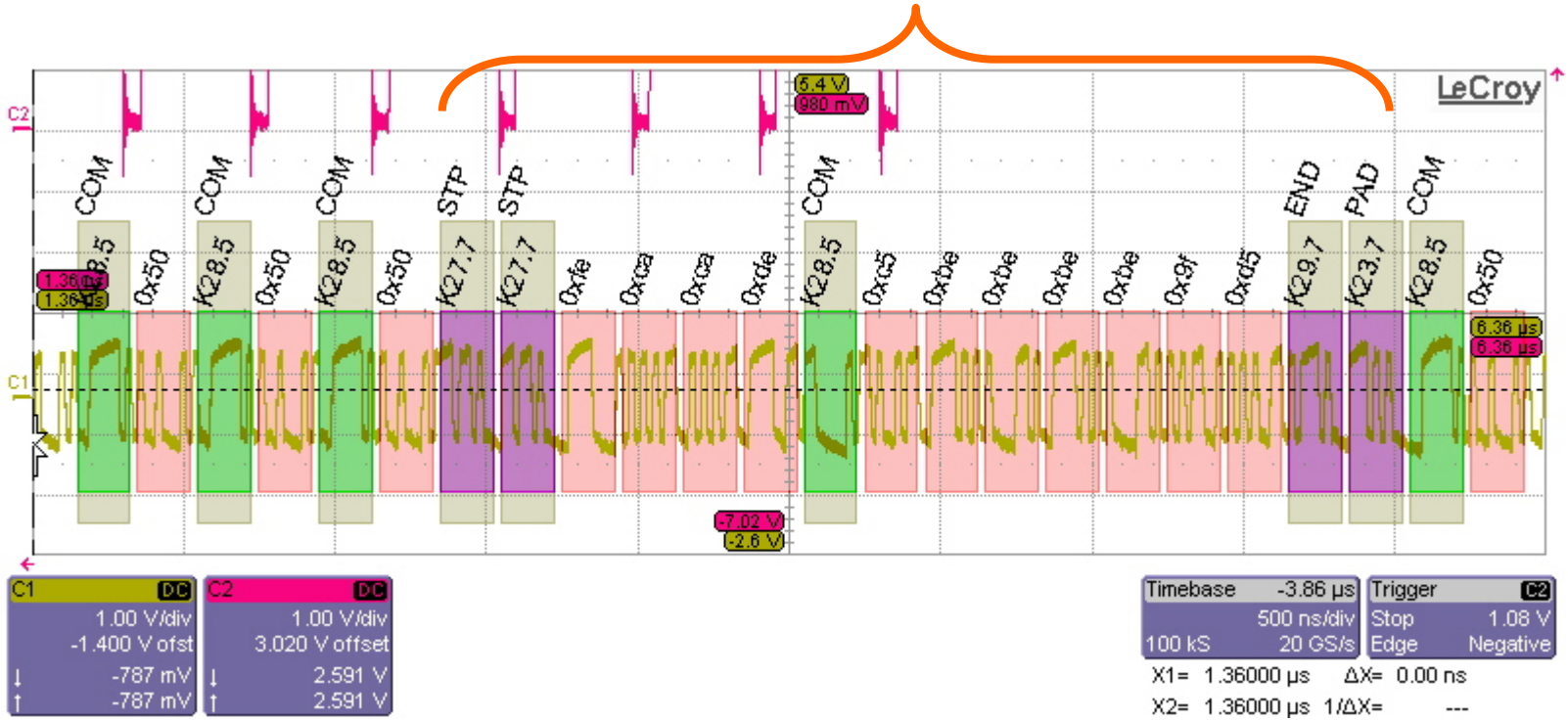
Data sent from DCC(DIF) to DCC(LDA)

2 packets data sent

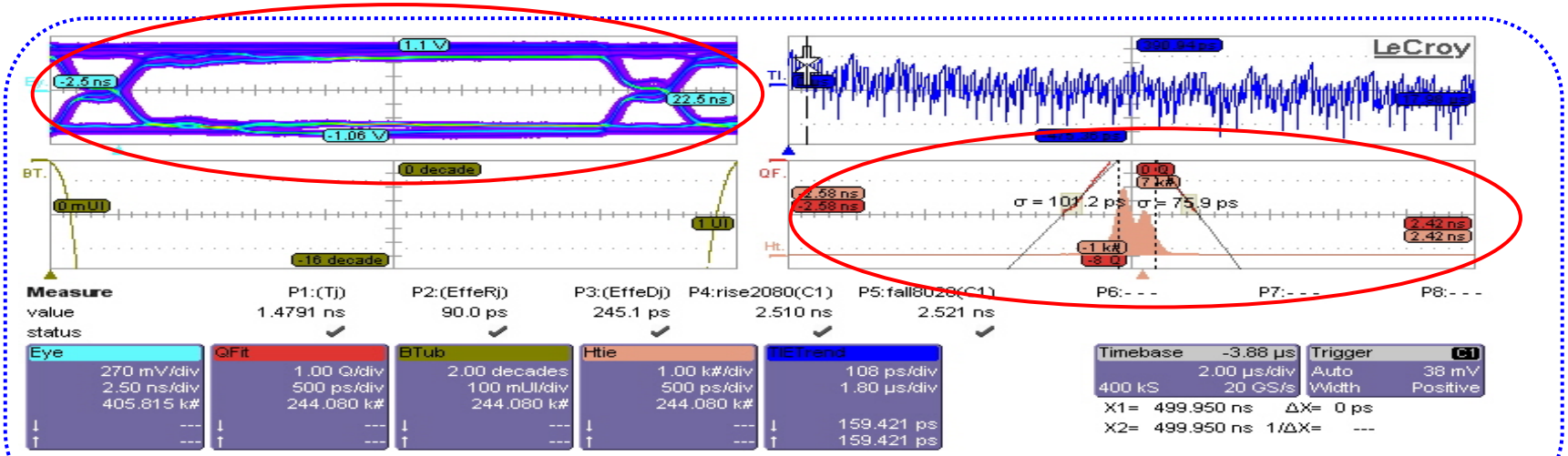


Data sent from DCC(LDA) to DCC(DIF)

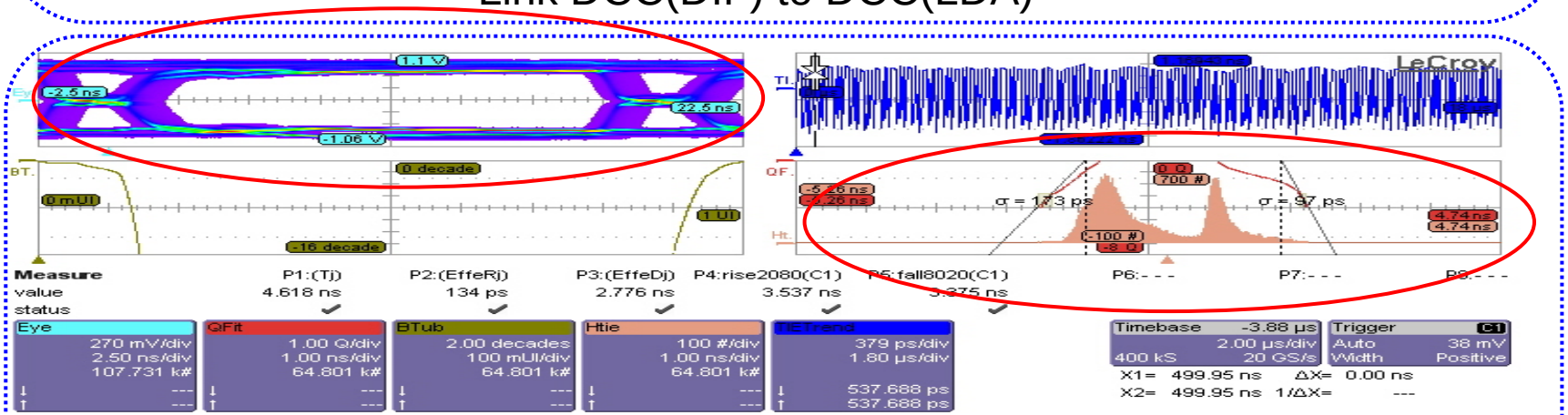
One packet sent correctly



Summary of tests

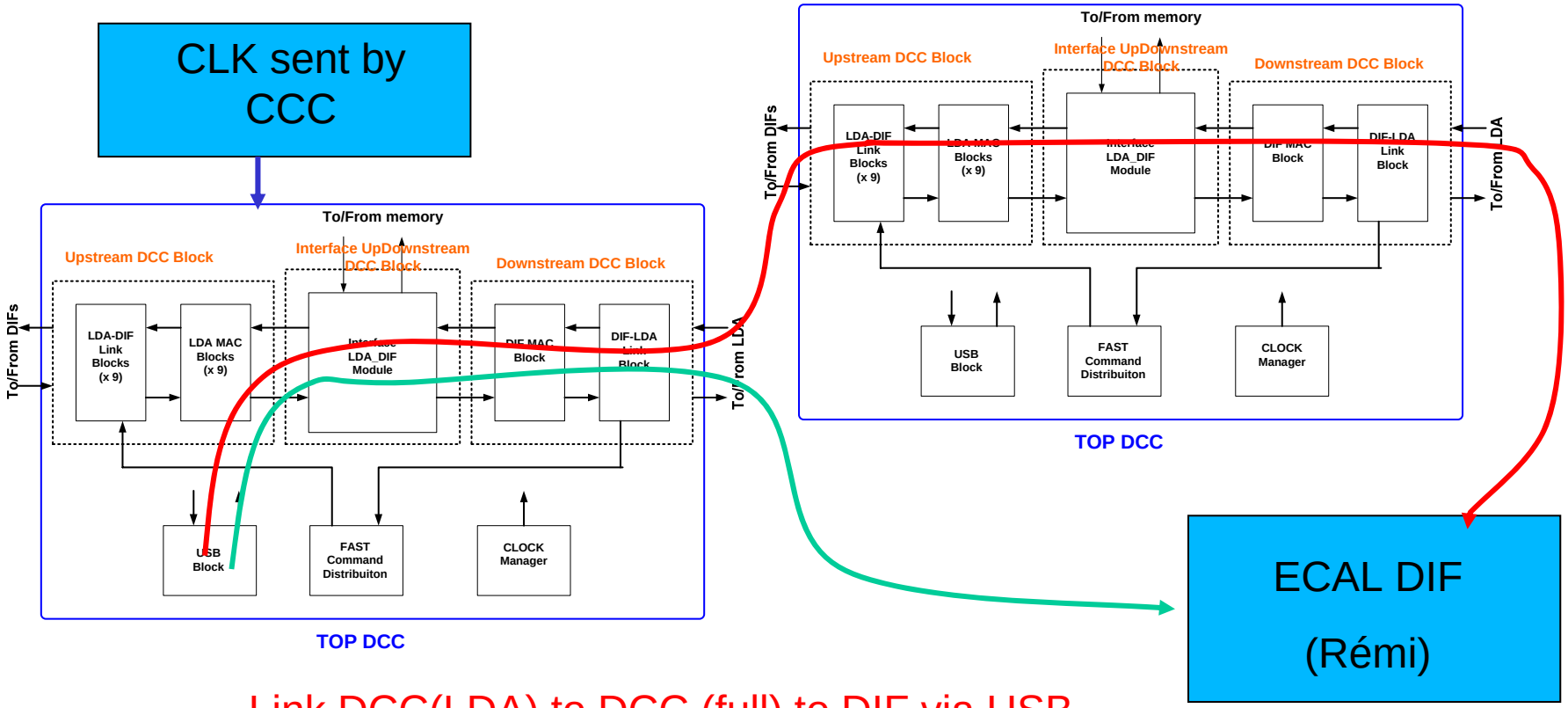


Link DCC(DIF) to DCC(LDA)



Link DCC(LDA) to DCC(DIF)

Test with two DCC and one DIF



Results

Link \ Status	Fast Command	Block Transfer	Data
DCC (lda) →DIF	✓	✓	
DCC (lda) → DCC (full) → DIF	✓	✓	
DIF → DCC (Lda)			To do
DIF → DCC (full) → DCC (Lda)			To do
DIF → DCC → LDA	To do	To do	To do
LDA → DCC → DIF	To do	To do	To do

✓ : Validate

✓ : do not work for the moment

Conclusion

- Firmware is running on the DCC
- Until end of year:
  - Tests & validation of VHDL code implemented on the DCC
  - Test of Multi-channel on the DCC
  - Test of a real DAQ Chain (ODR,LDA,DCC,DIF)
  - Improvement of DCC card (layout) before production
- DCC Production (early of next year)
  - February 2010 : PCB production
  - March 2010 : PCB cabling
  - April – June 2010: tests at LLR
- Full DAQ : summer 2010

Remarks for the thinking

- Where the LDA will be installed in test beam?
- What is the optimal length between the DIF and the DCC or LDA chassis ?

  (→ the length of HDMI cable)
- Should we use a special HDMI cable ?
- Who is responsible for power distribution ?
  - Should we go with our power supply ?
- Should we think of EMC and grounding problem ?

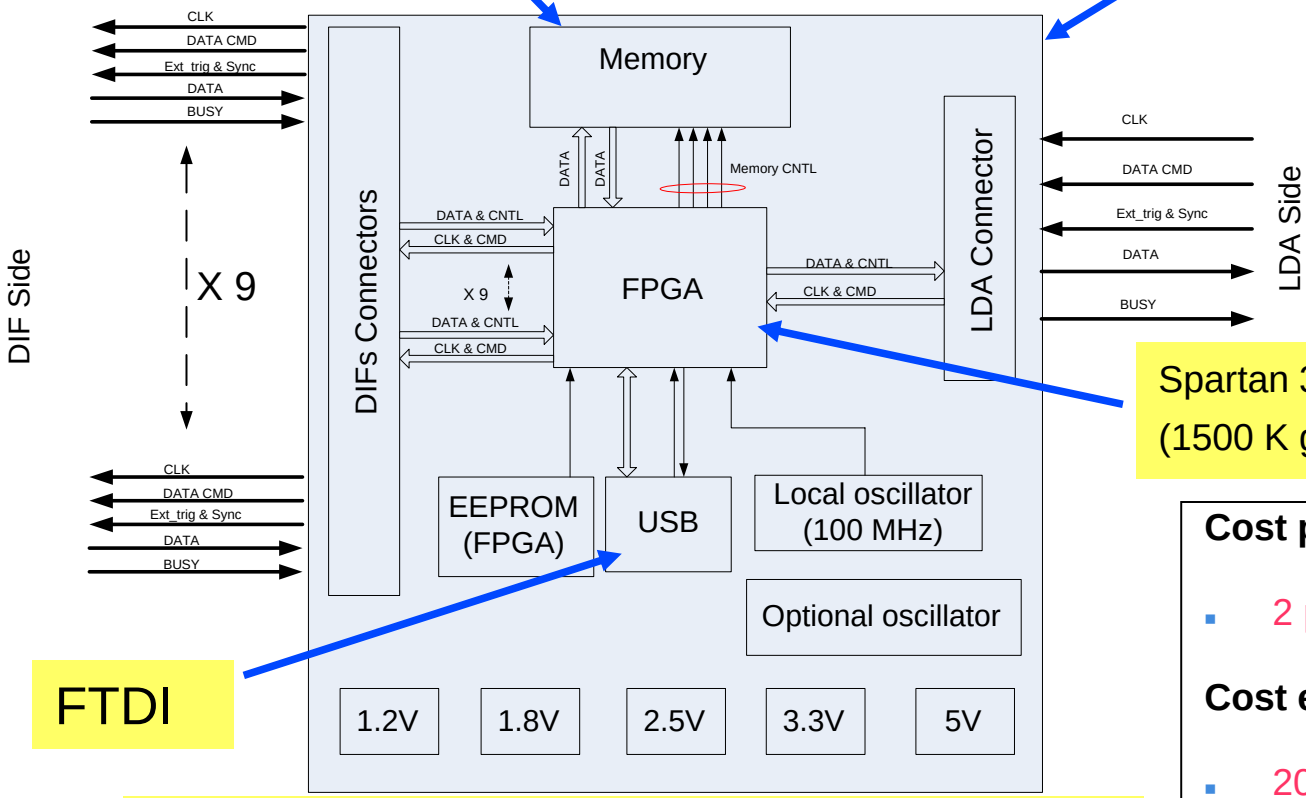
Back up

Card overview

16×1M ZBT
(no latency BUS RAM)

DCC

Card size: VME 6U



Spartan 3
(1500 K gate)

FTDI

Cost proto I:

- 2 protos: ~ 19**00**€/card

Cost est.:

- 20 prods: ~**600**€/card

Est: 1.2A 10mA 400mA 2.25A 30mA