



Laboratoire d'Anney-le-Vieux
de Physique des Particules

Micromegas m2 ASU and DIF

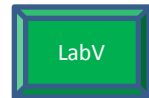
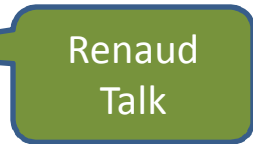
Cyril.Drancourt@lapp.in2p3.fr

17th September 2009



Summary

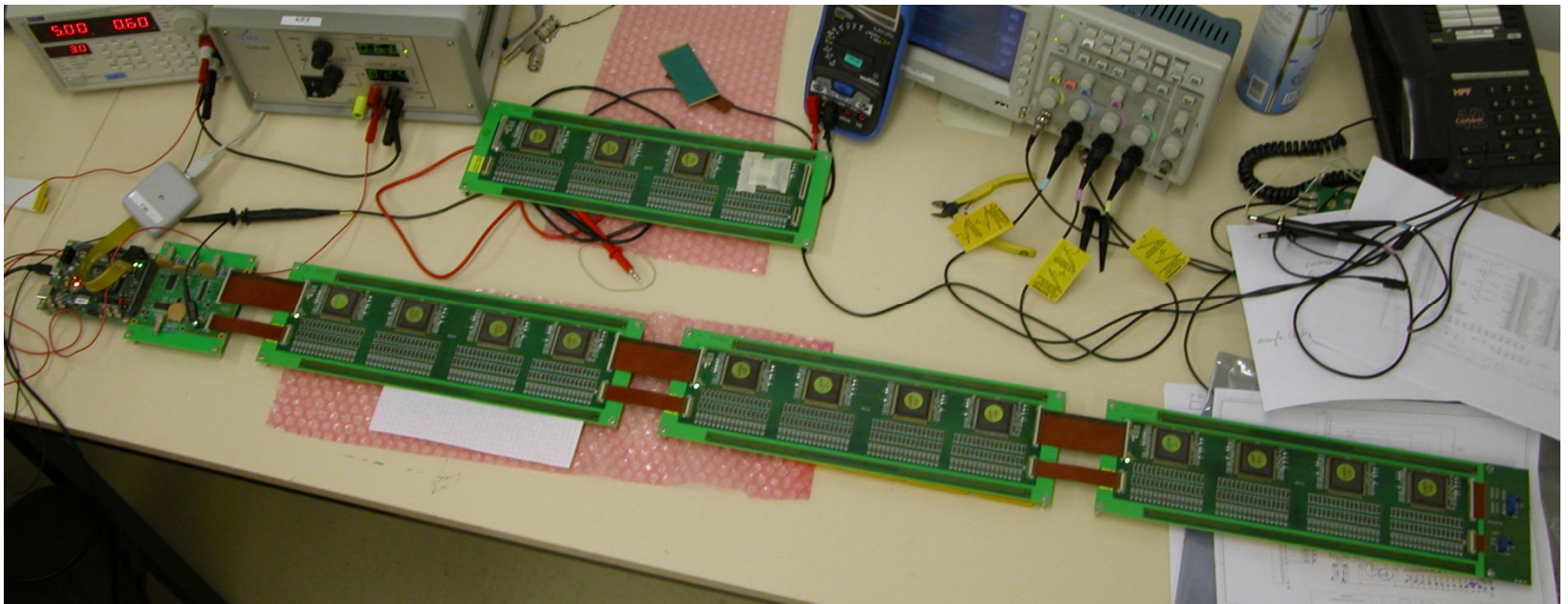
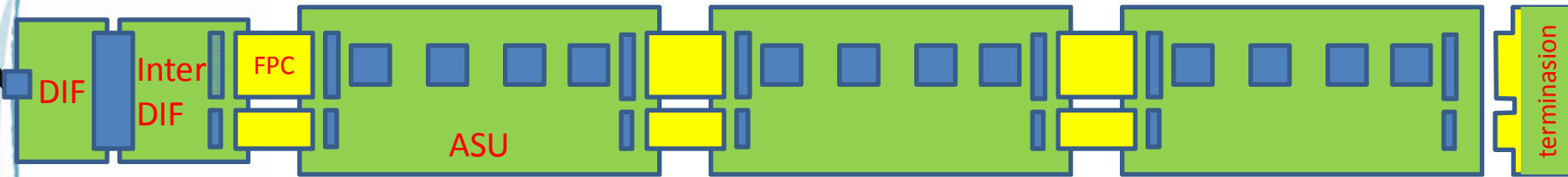
- Electronic board with Hardroc1 readout
- Electronic board with Hardroc2 readout
- Electronic board with Dirac2 readout
- LabVIEW test support
- DIF development



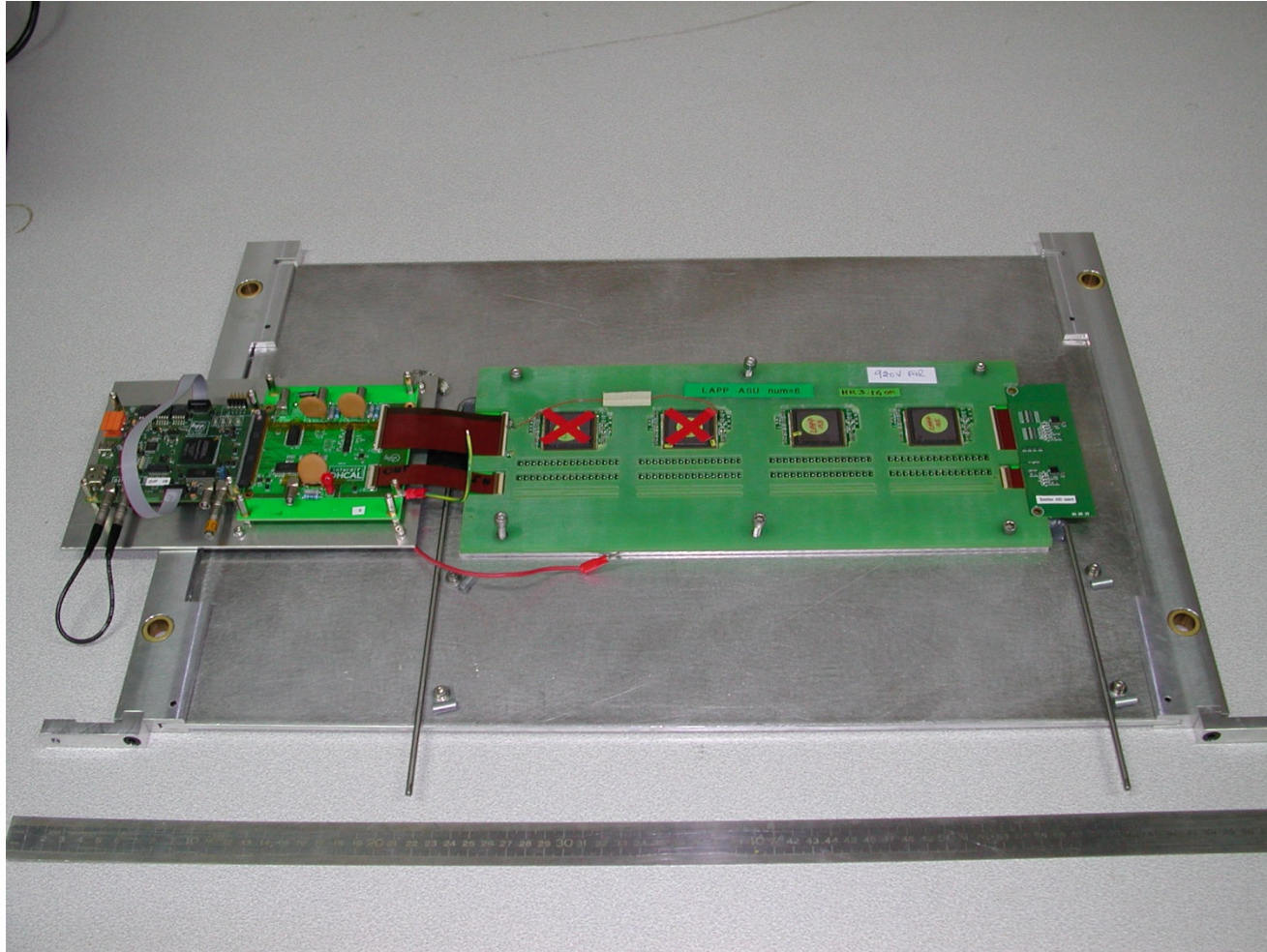


board with Hardroc1

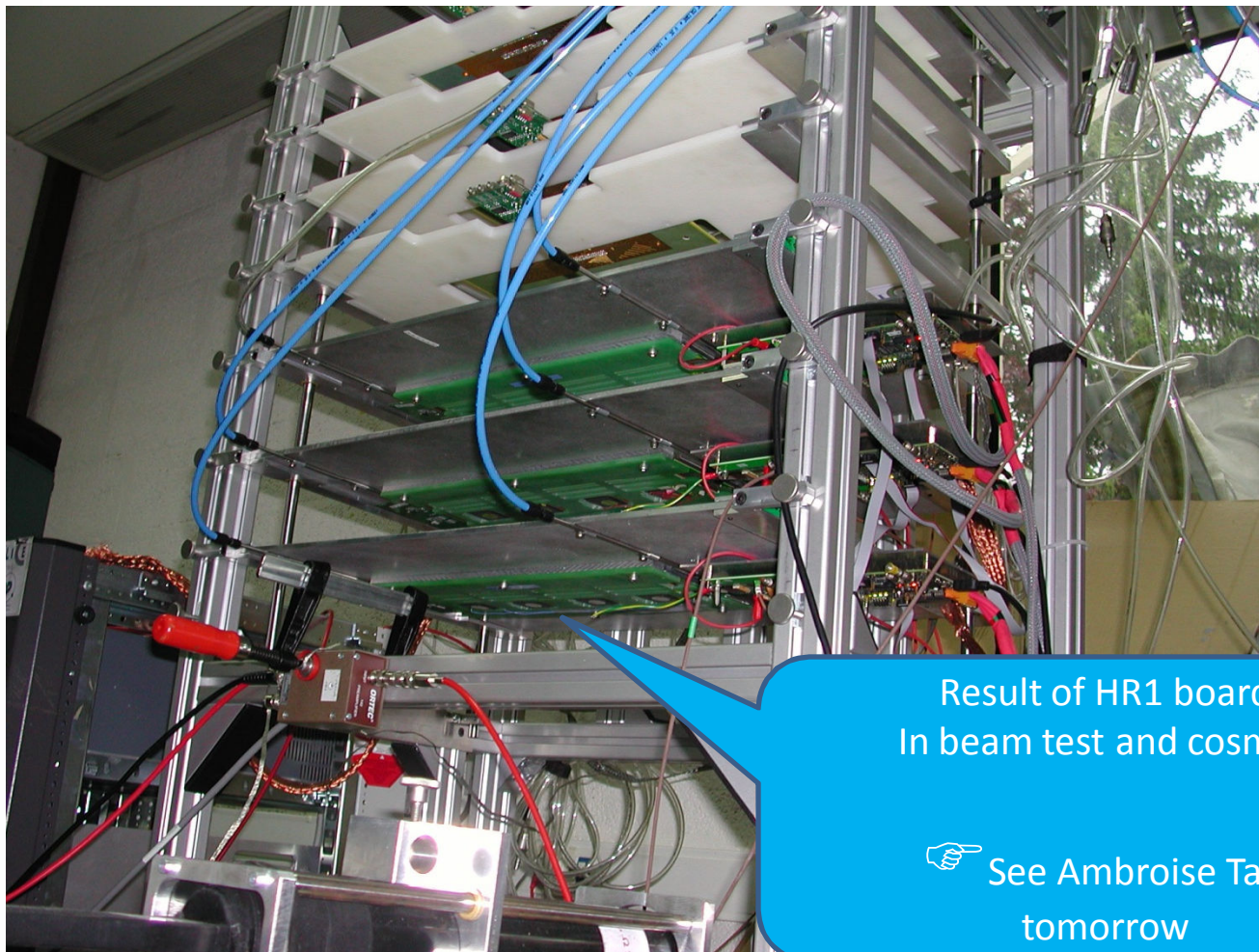
USB




detector with Hardroc1



detectors with Hardroc1

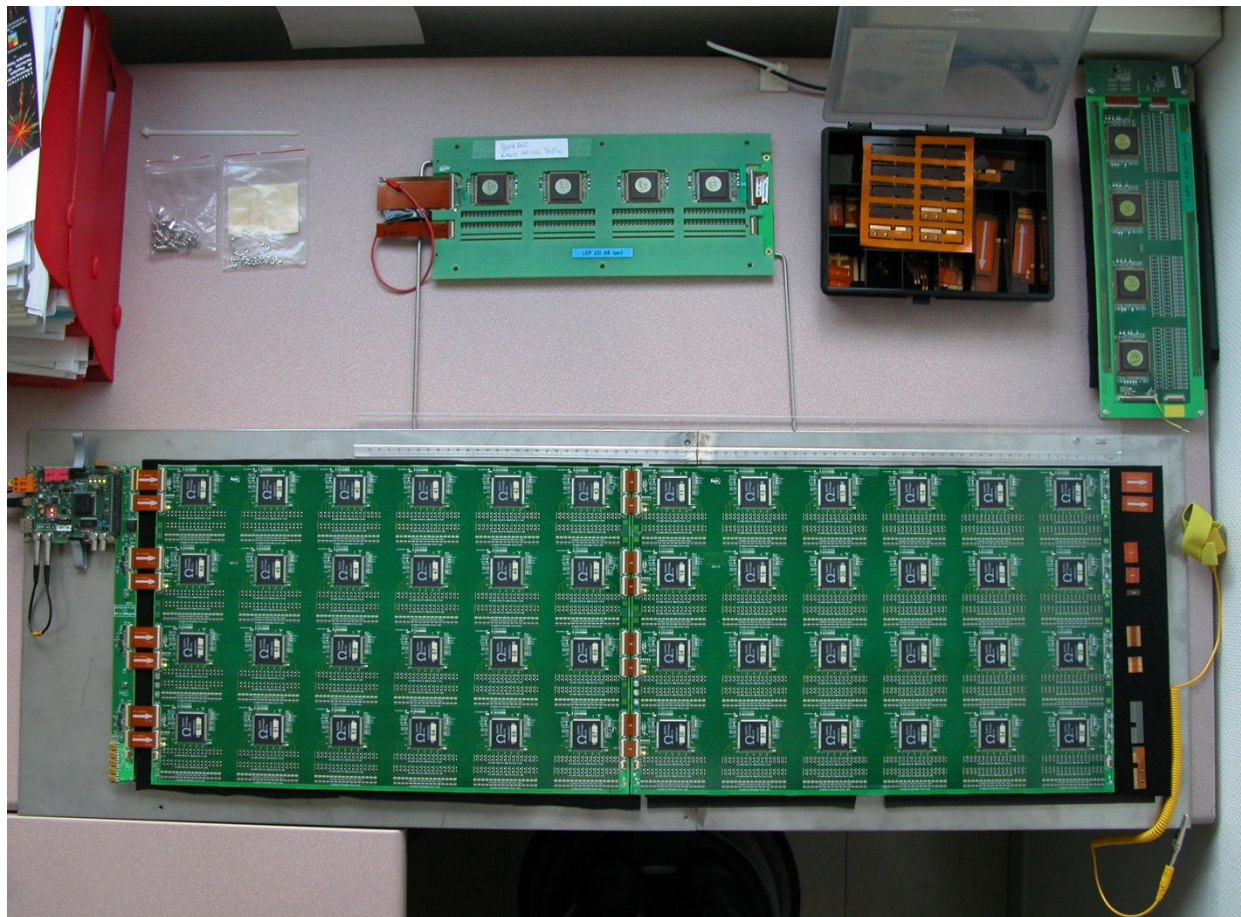


Result of HR1 board
In beam test and cosmic:

 See Ambrose Talk
tomorrow

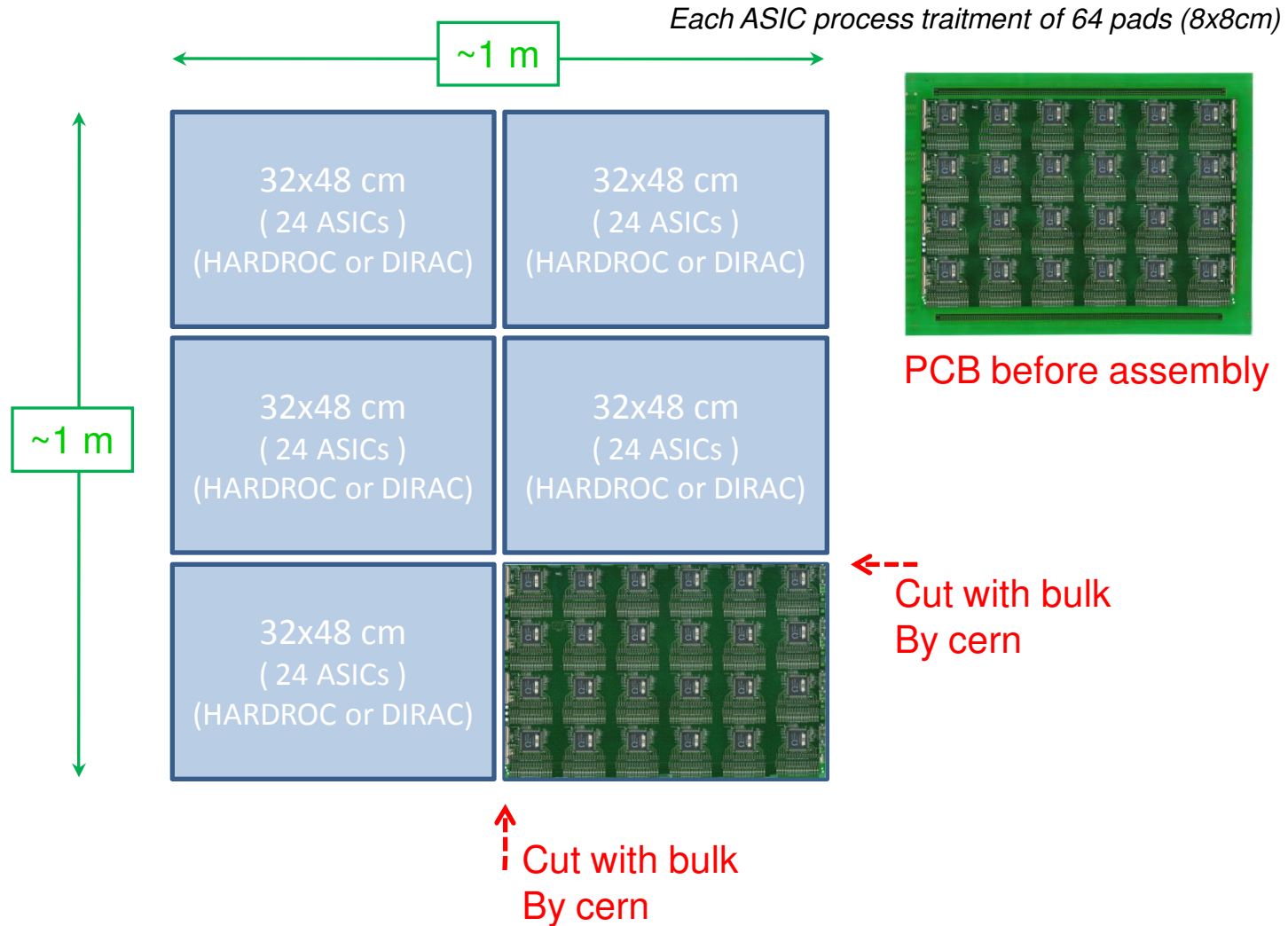
Boards with Hardroc2

~1 m

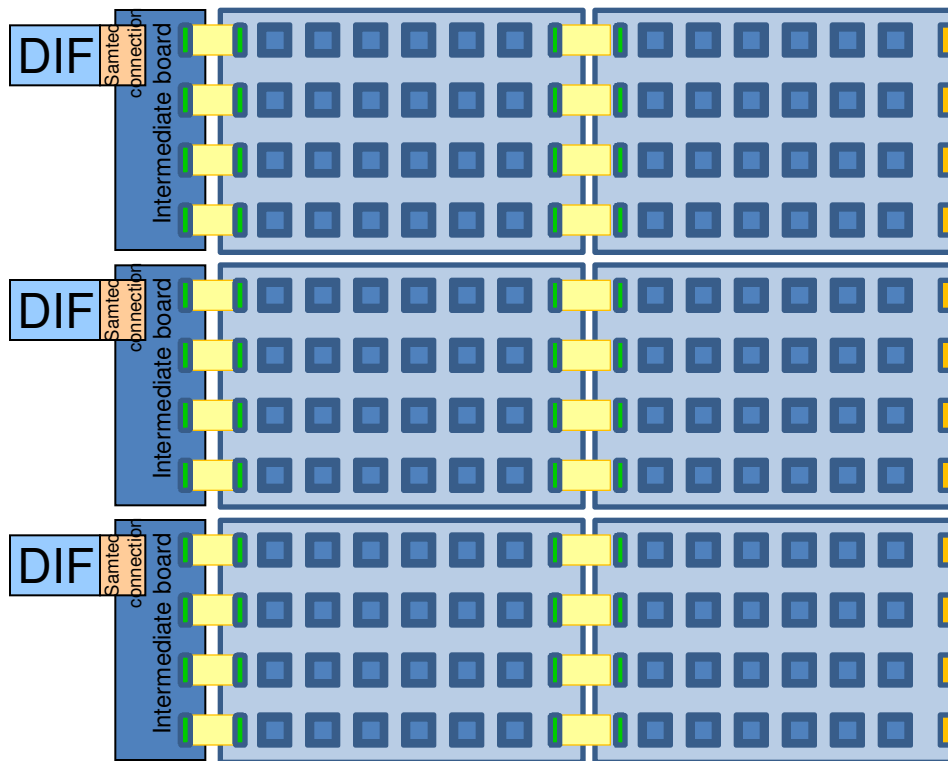


~0.33 m

Detector module in M²



Link in M²



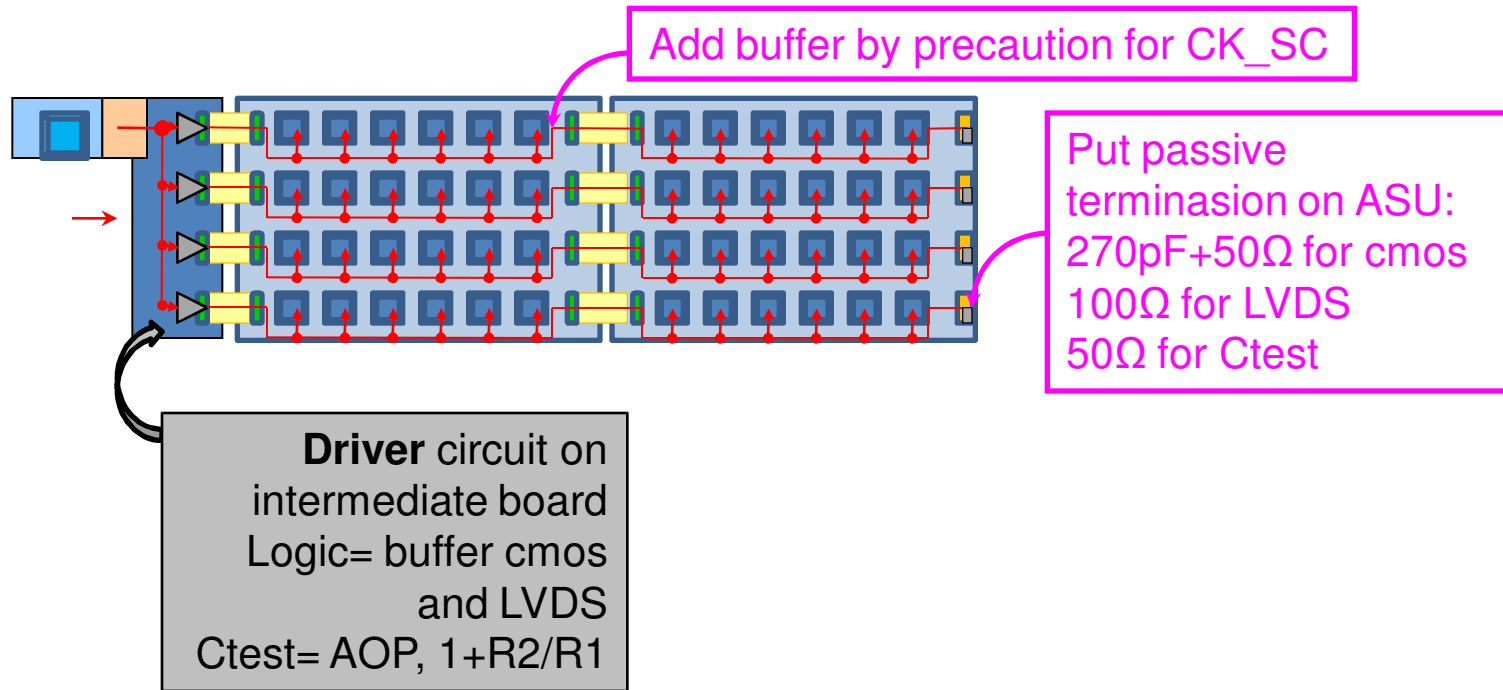
Flat Printed Circuit

ASIC chip (64 channels)

Hirose connector

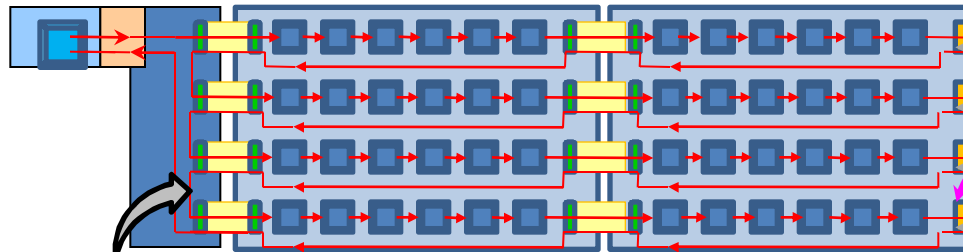
Termination component

Data flow: DIF → ASIC



■ = FPGA on DIF

Data flow: DIF \Rightarrow ASIC

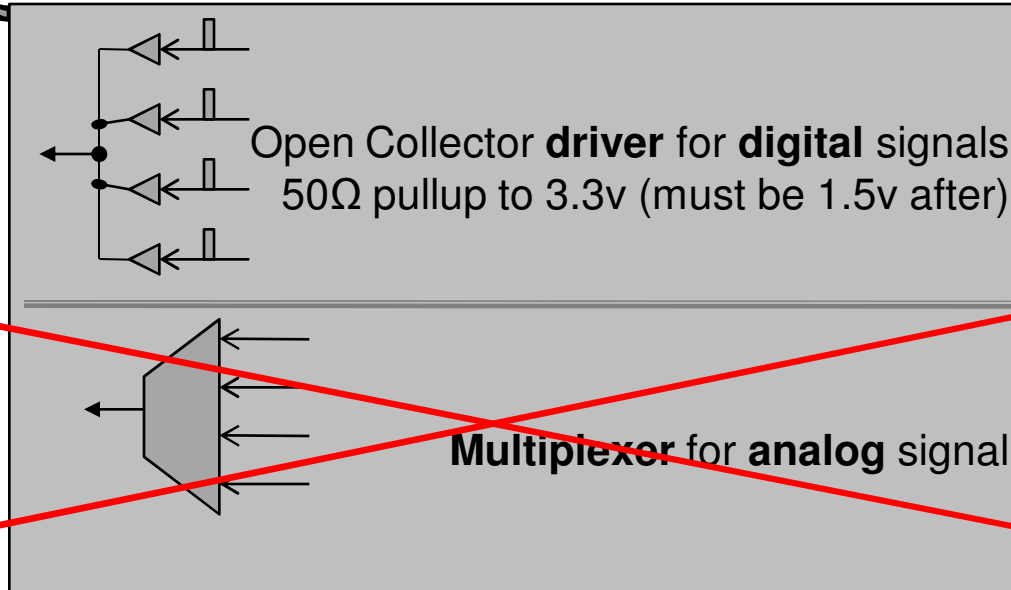
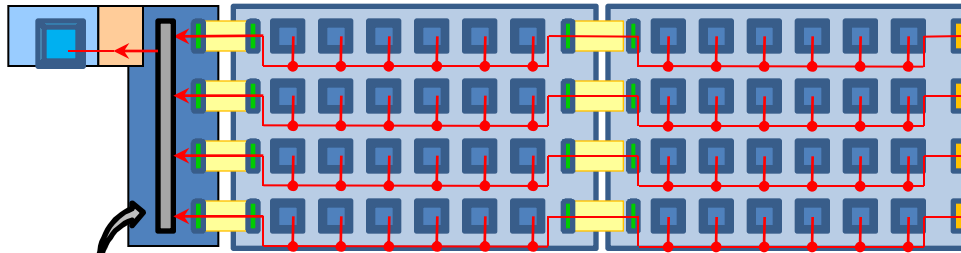


Put shunt and driver on ASU

Shunt chain and driver on intermediate board

 = FPGA on DIF

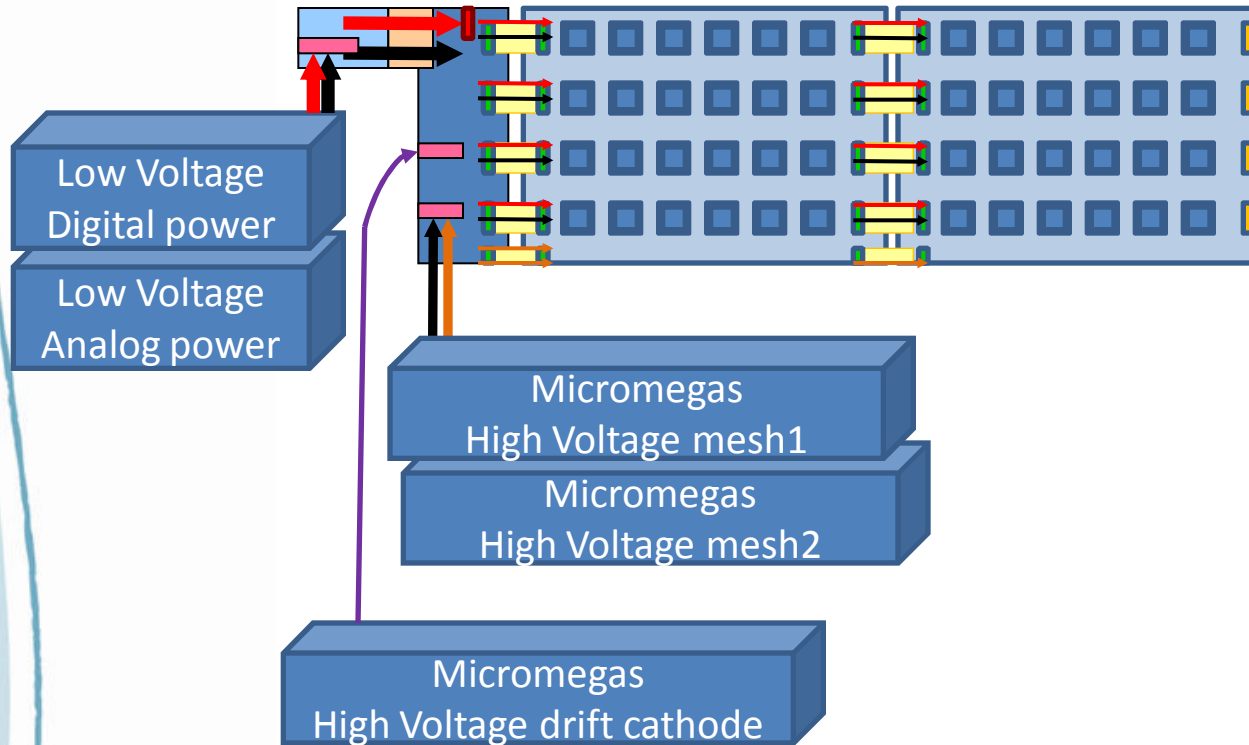
Data flow: DIF ← ASIC



Remove
Because
Bugg on
Hardroc2

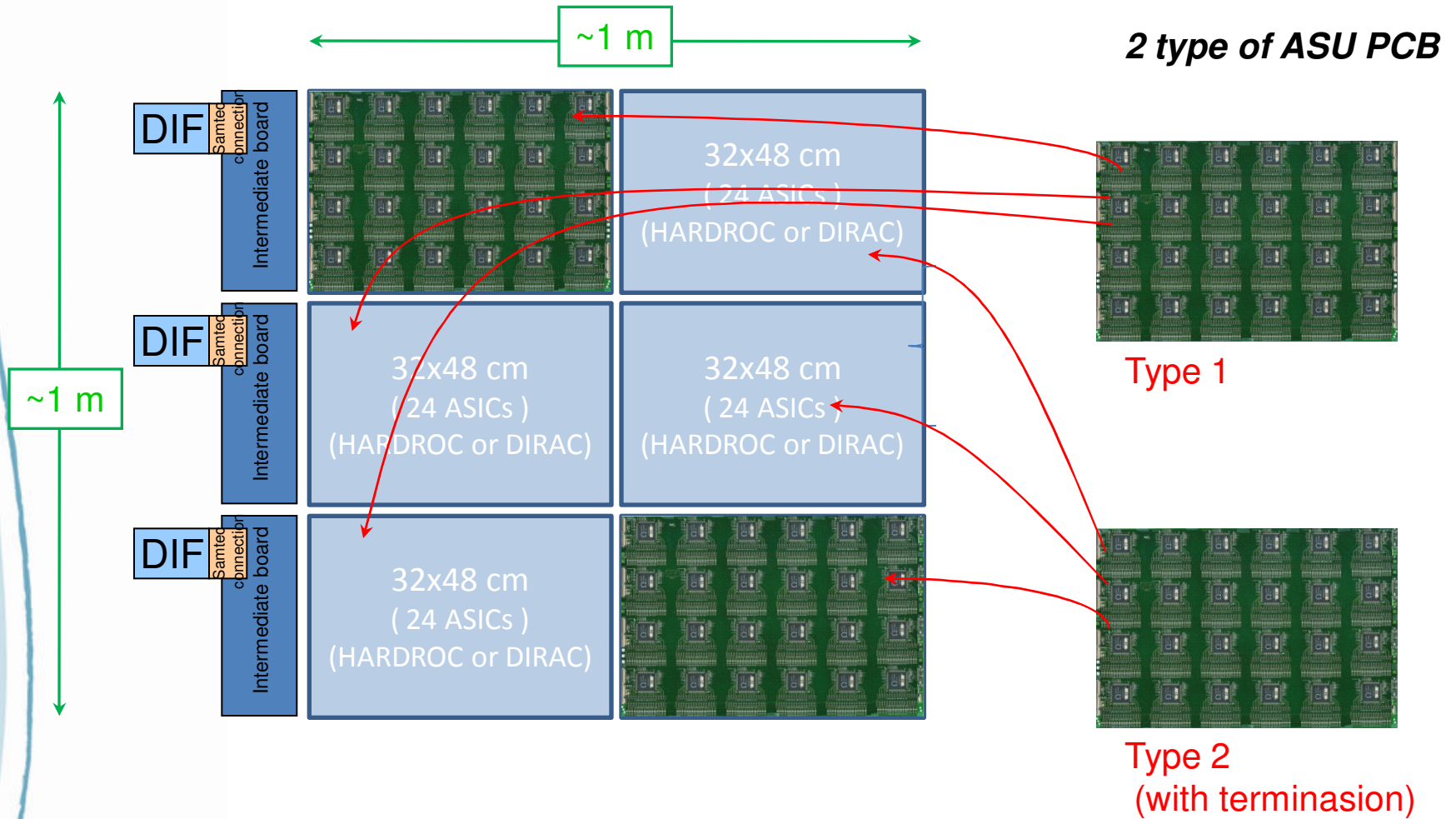
Power distribution: DIF → ASIC, detector

Adjust temporary digital 4v for Slow-control frame transfert



—: Power connector

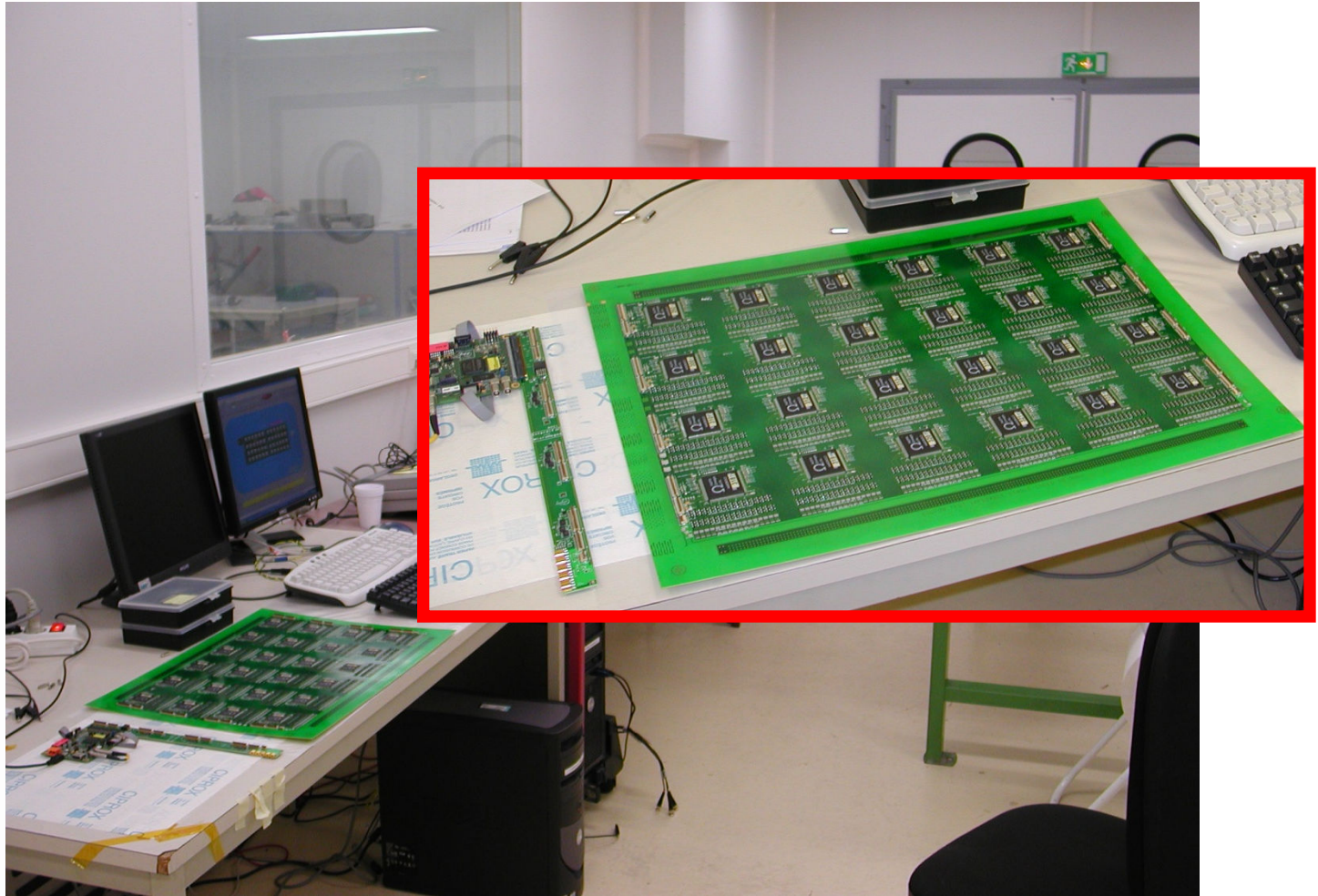
Detector module in M²



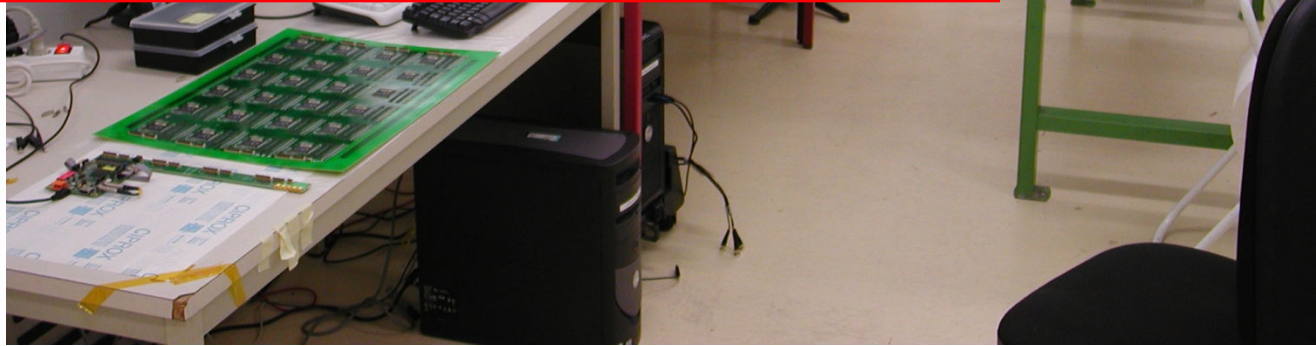
Boards with Hardroc2



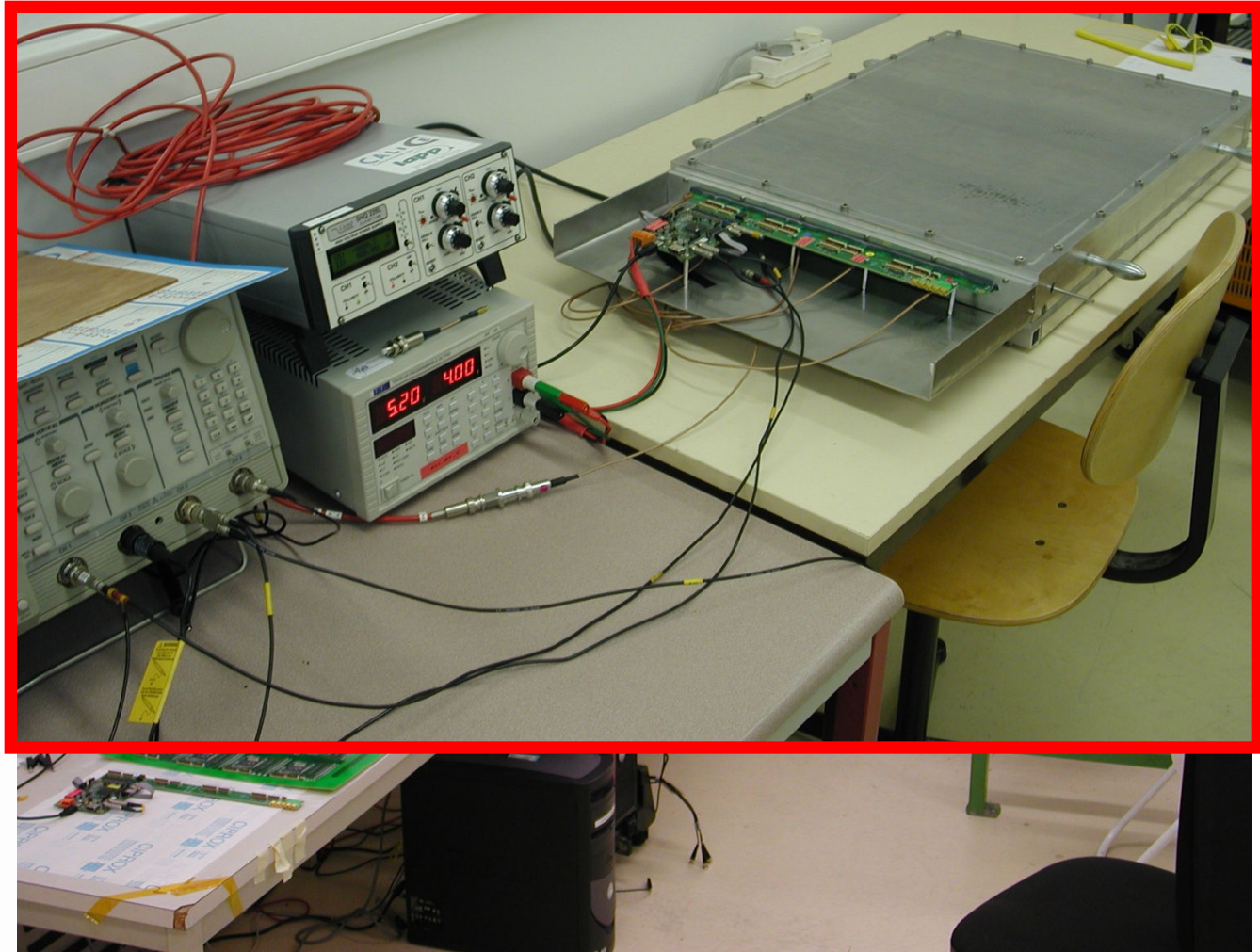
Board without detector



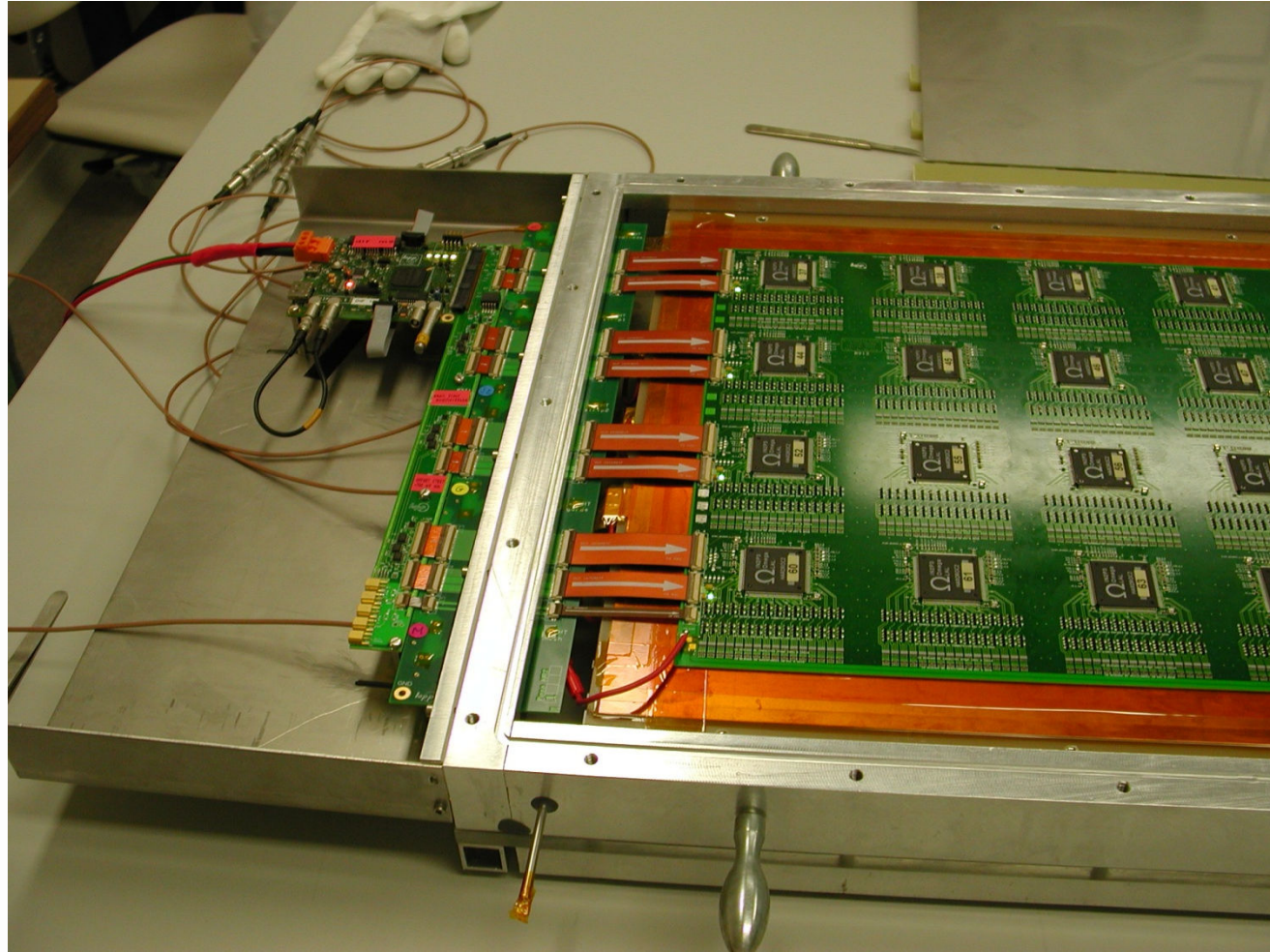
Board with Detector



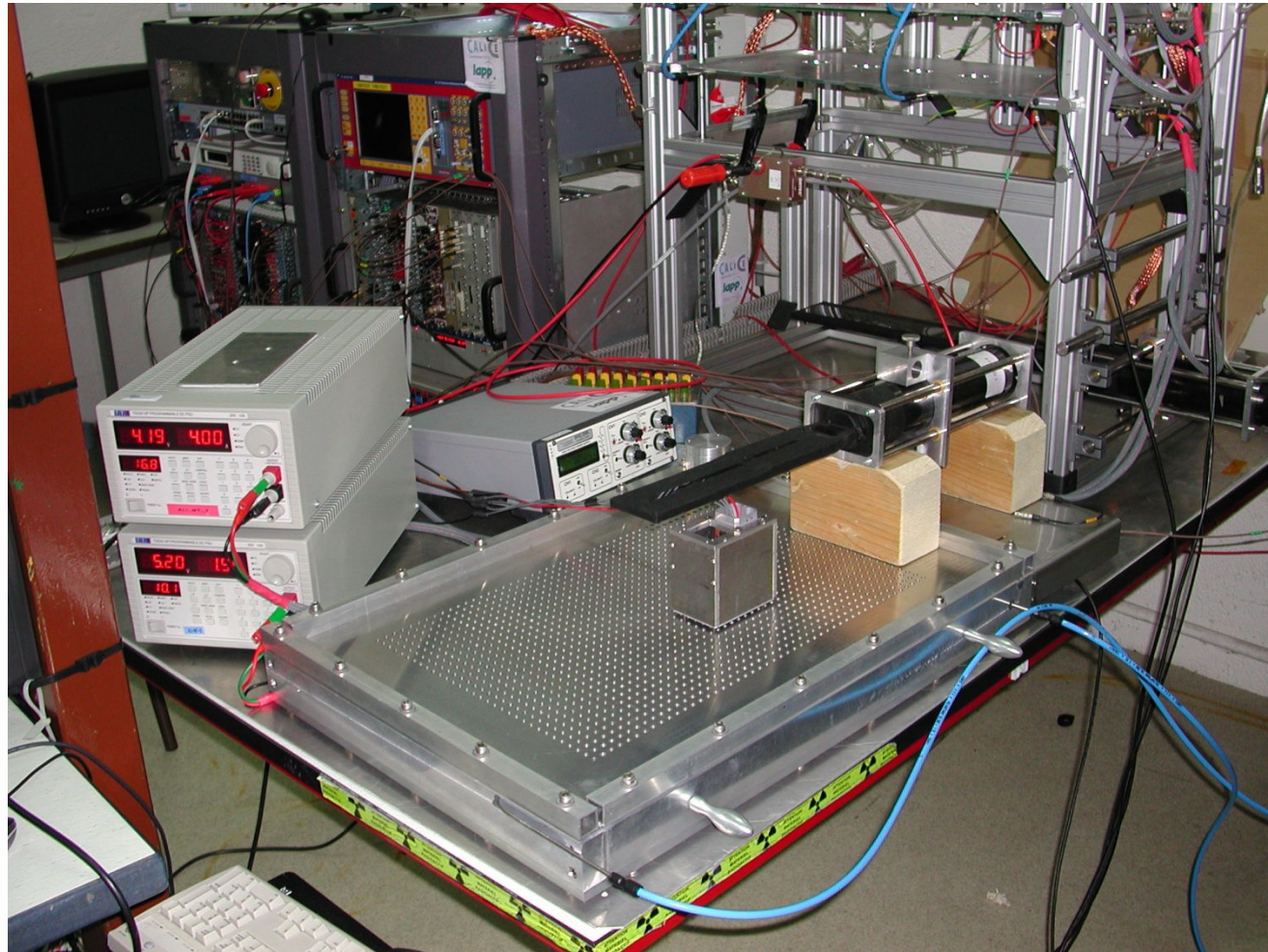
Board in test box



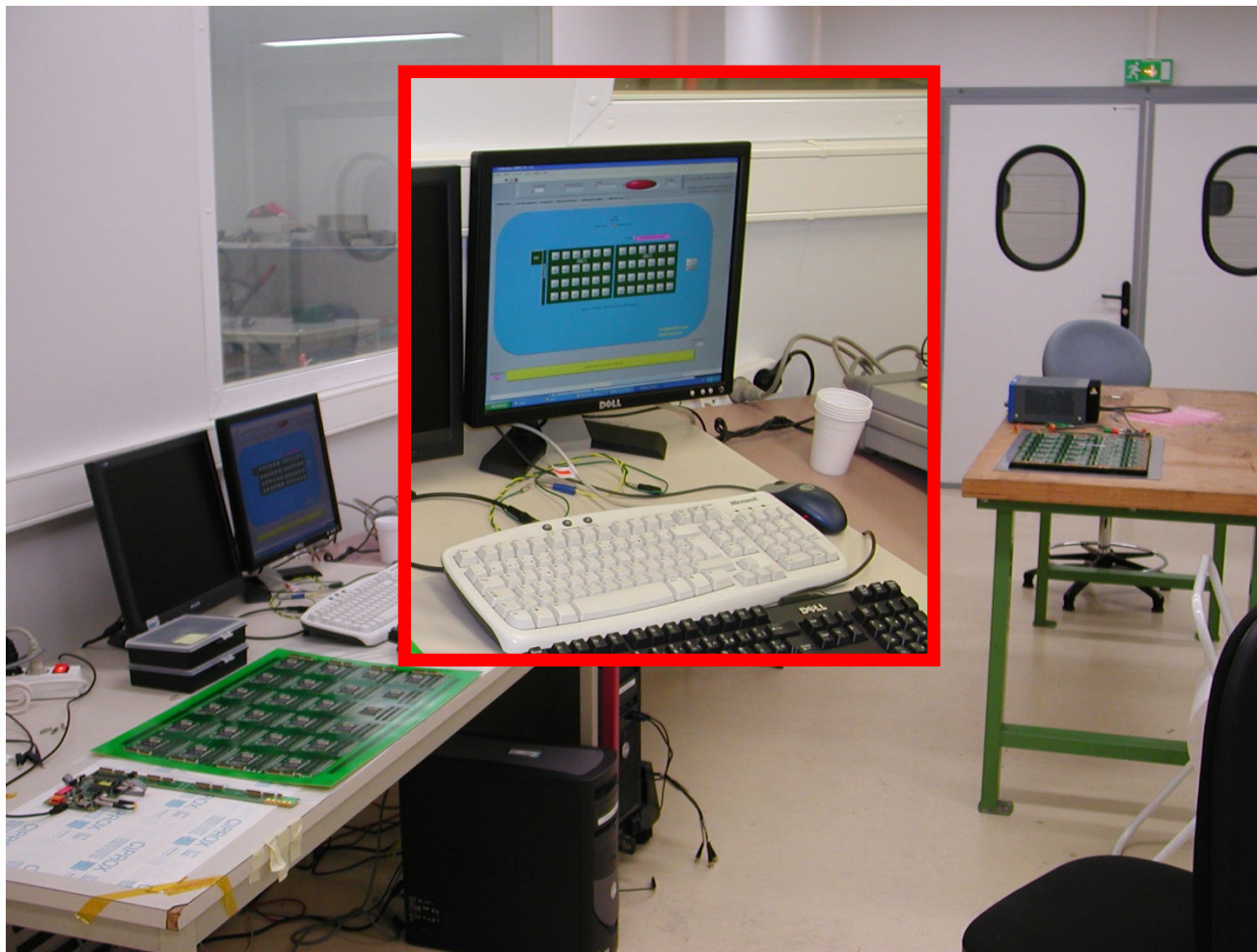
Board in test box



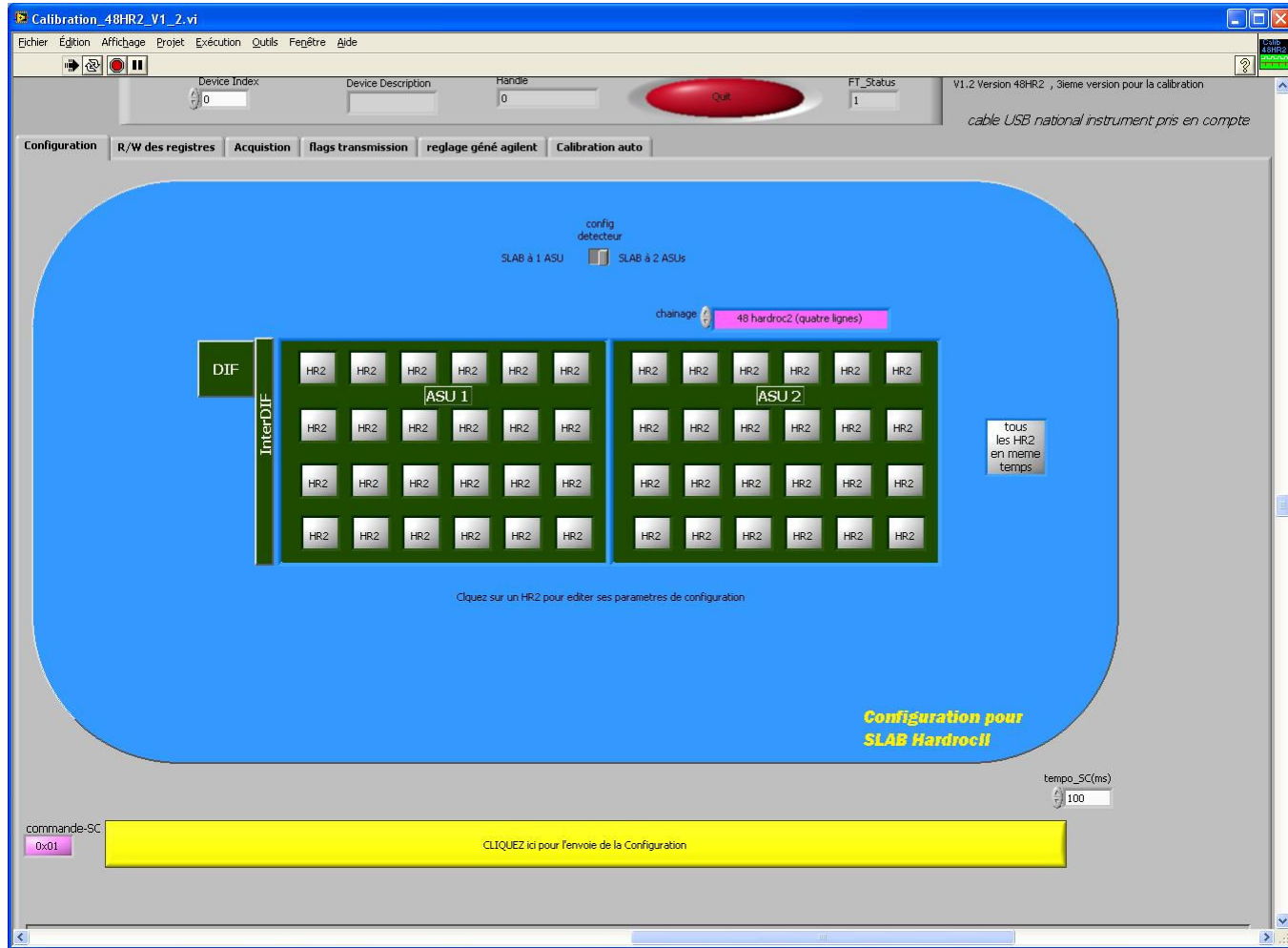
Board in test box



LabVIEW with Hardroc2



LAPP LabVIEW support



LAPP LabVIEW support

The screenshot displays a LabVIEW configuration window titled "param_slow_control_pc_portable.vi". The window is divided into several sections:

- Individual Channel PreAmplifier Gain:** A grid of 64 channels (Ch 0 to Ch 63) with gain values set to 128.
- PreAmplifiers Gain:** Sliders for "Individual Ch. PreAmp Gain" and "All Channel Gain except Ch. XX".
- All Channel Gain:** A slider set to 128.
- Channel XX:** A dropdown menu set to 1.
- Channel XX Gain:** A slider set to 128.
- Discriminators Masks Disable = Enable Channel Discriminator:** Three grids for Discriminator 0, 1, and 2, each with 64 channels. All indicator lights are green.
- Internal Test Capacitor:** A section with "Internal Test Capacitor Enable" and "Discriminator Masks" sub-sections, each with a grid of 64 channels and indicator lights.
- Buttons:** "OK" (green) and "Cancel" (yellow) buttons at the bottom.

On the left side of the window, there is a large blue area labeled "DIF". At the bottom left, there is a "commande-SC" field with the value "0x01".

LAPP LabVIEW support

Calibration_48HR2_V1_2.vi

Echier Edition Affichage Projet Exécution Outils Fenêtre Aide

Device Index: 0 Device Description: Handle: 0 FT_Status: 1

QUIT

V1.2 Version 48HR2 , 3ieme version pour la calibration

cable USB national instrument pris en compte

Configuration R/W des registres Acquisition flags transmission reglage généré Calibration auto

config detecteur

SLAB à 1 ASU SLAB à 2 ASUs

chainage

- 12 hardroc2 (une ligne)
- 24 hardroc2 (deux lignes)
- 36 hardroc2 (trois lignes)
- ✓ 48 hardroc2 (quatre lignes)

DIF InterDIF ASU 1 ASU 2

HR2

tous les HR2 en meme temps

Clquez sur un HR2 pour editer ses parametres de configuration

Configuration pour SLAB HardrocII

tempo_SC(ms) 100

commande-SC 0x01

CLIQUEZ ici pour l'envoi de la Configuration

LAPP LabVIEW support

LAPP LabVIEW support

Calibration_48HR2_V1_2.vi

Fichier Édition Affichage Projet Exécution Outils Fenêtre Aide

Device Index: 0 Device Description: Handle: 0 FT_Status: 1

Quit

V1.2 Version 48HR2 , 3ieme version pour la calibration
cable USB national instrument pris en compte

Configuration R/W des registres Acquisition flags transmission reglage généré agilent Calibration auto

type de géné: généré agilent 81110A

nombre de boucle: 40, 50, 60, 70, 80, 90, 100

max: 200 mV

nombre de pulse C'est

visualisation de la première calibration

Mesure de piedestaux
Calibration sur un chip
Un chip , toutes les lignes ensemble
Calibration chip par chip
/ chip par chip , toutes les lignes ensemble
Calibration sur tous les hardrocs ensemble

config ASU

choix de mesure

motif du "Test Capacitor"

0 1 2 3 4 5 6 7 1023 =
750 -
500 -
250 -
0 -
DAC2

max: 70
step: 5
min: 50

32 33 34 35 36 37 38 39 1023 =
750 -
500 -
250 -
0 -
DAC1

max: 65
step: 5
min: 50

40 41 42 43 44 45 46 47 1023 =
750 -
500 -
250 -
0 -
DAC0

max: 60
step: 2
min: 50

liste des hardrocs à calibrer

0 1
13
25
37
2
14
26
38
3

Calibration pour 1 slab de 1 ASU 24HR2 ou pour 1 slab de 2 ASU 24HR2

numéro du RUN: 002

dernier stockage: E:\cyril\lapp\DHICAL\labview_dir\portable\labview_cyril\hardroc2\DATA\ASU6_run1_200mV_chip1_m00000000000000FF_DAC_0.txt

time_out reception(ms): 50

numéro de l'ASU: 006

Cliquez ici pour le Lancement de la Calibration

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V1.2 Cyril, 14 sept 2009

LAPP LabVIEW support

Face-avant de Calibration_4HR1_V1_7.vi

Echier Édition Affichage Projet Exécution Outils Fenêtre Aide

Police de l'application 18pts

Device Index: 0, Device Description: , Handle: 0, FT_Status: 1, Quit

Configuration | R/W des registres | Acquisition | flags transmission | Calibration auto

nombre de boucle: 40, 50, 60, 70, 80, 90, 100

type de géné: signal par fpga dif

Géné Ctest: max 3300 mV, step 10 mV, min 3300 mV

nombre de pulse Ctest: 100

config ASU 4HR1

choix de l'asic: chip3

motif du "Test Capacitor"								1023-
0	1	2	3	4	5	6	7	750-
8	9	10	11	12	13	14	15	500-
16	17	18	19	20	21	22	23	250-
24	25	26	27	28	29	30	31	0-
								DAC1
32	33	34	35	36	37	38	39	1023-
40	41	42	43	44	45	46	47	750-
48	49	50	51	52	53	54	55	500-
56	57	58	59	60	61	62	63	250-
								DAC0

nbre decalage du motif: 1, increment du motif: 32

Cablage de l'ASU: chip1 (bypass), chip2 (HR OK), chip3 (HR OK), chip4 (HR OK)

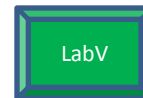
Calibration pour ASU 4HR1

numéro du RUN: 010, dernier stockage: E:\cyril\lapp\micromegas\dif\labview_cyril\hardroc1\DATA\ASU3_run10_3300mV_mFFFFFFFFFFFFFFFF_DAC_1.txt, time_out reception(ms): 200

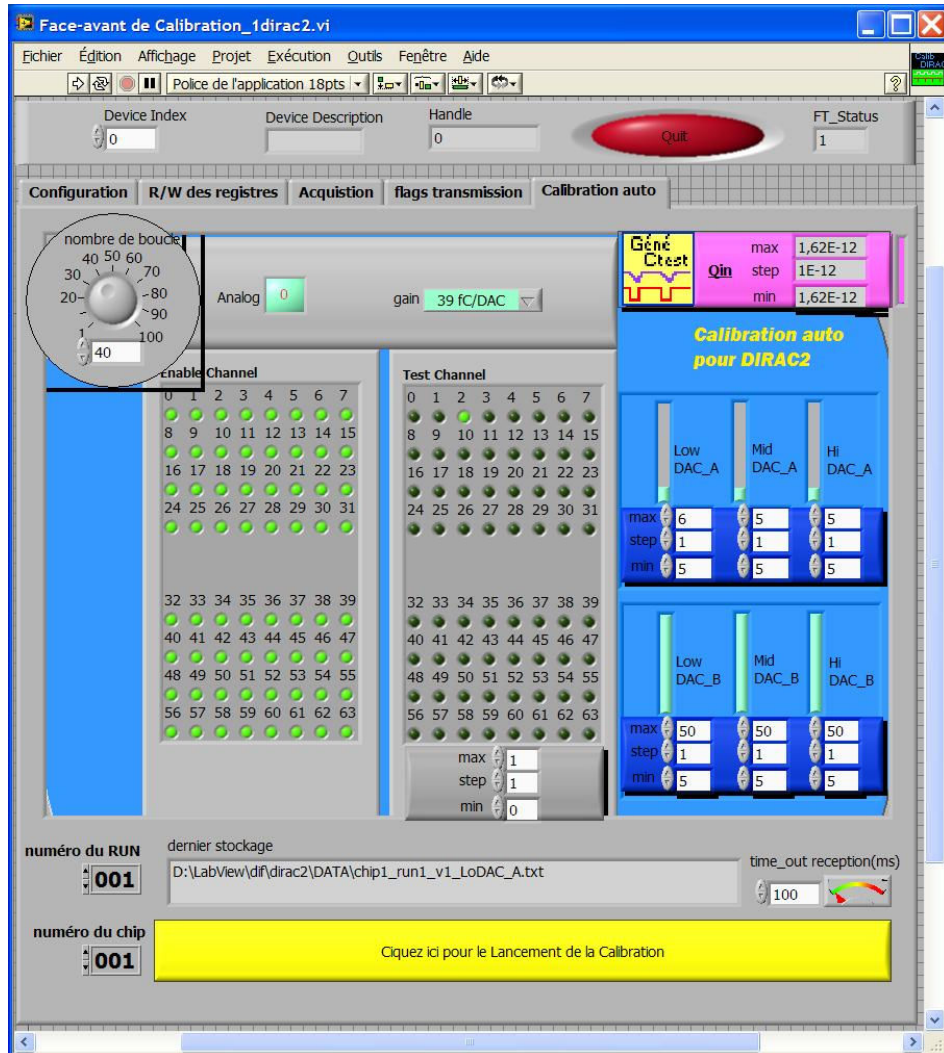
numéro de l'ASU: 003

Cliquez ici pour le Lancement de la Calibration

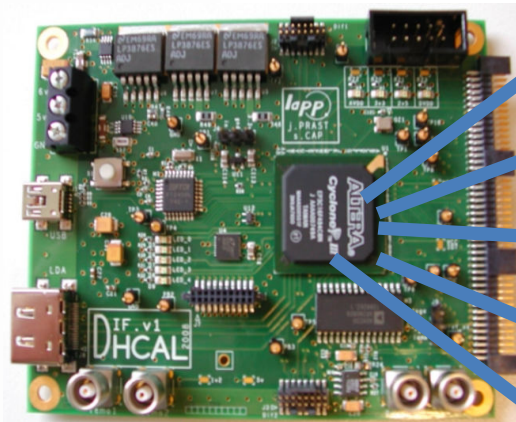
LAPP
Laboratoire d'Anney-le-Vieux de Physique des Particules
V1.7 Cyril, 4 Sept 2009



LAPP LabVIEW support



DIF



VHDL firmware1 for Hardroc1 Micromegas

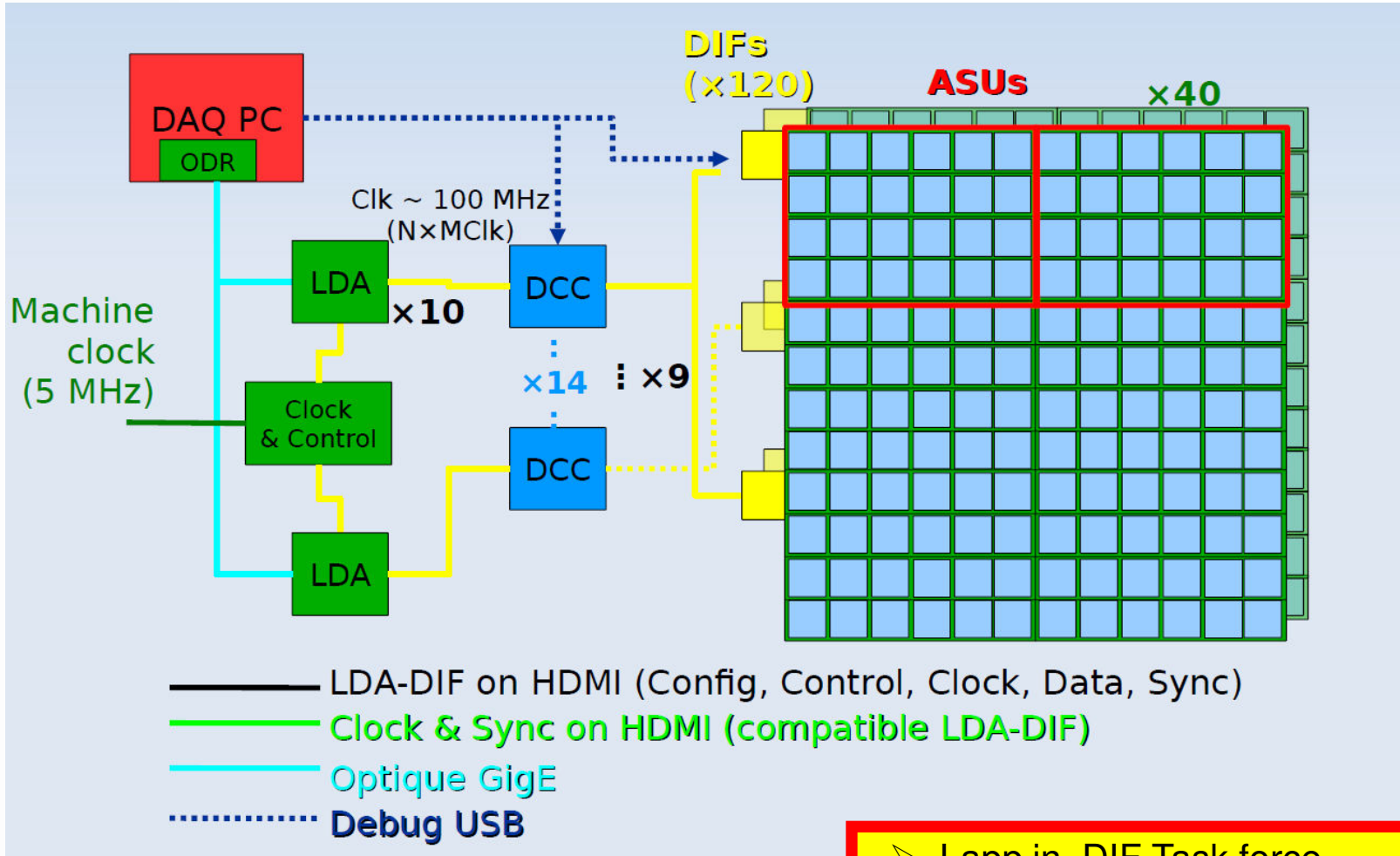
VHDL firmware2 for Hardroc1 RPC

VHDL firmware3 for Dirac2 Micromegas

VHDL firmware4 for Hardroc2 Micromegas

VHDL firmware5 for Calice DAQ Test

CALICE DAQ



➤ Lapp in DIF Task force

Electronic LAPP team

- **Julie Prast:** DIF conception, DIF Link Study
- **Guillaume Vouters:** DIF firmware development, ASU test, integration
- **Sebastien Cap:** DIF CAO, interDIF Conception&CAO, integration
- **Renaud Gaglione:** Dirac conception(ASIC&ASU), R&D protection inside PCB
ASU test, integration
- **Alexandre Dalmaz:** ASUs CAO (Hardroc&Dirac), R&D protection inside PCB
- **Cyril Drancourt:** ASU Hardroc conception, ASU test, LabVIEW, integration