Laboratoire d'Annecy-le-Vieux
de Physique des Particules

# Micromegas m2 ASU and DIF

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CHAMBERY ANNECY

# Summary

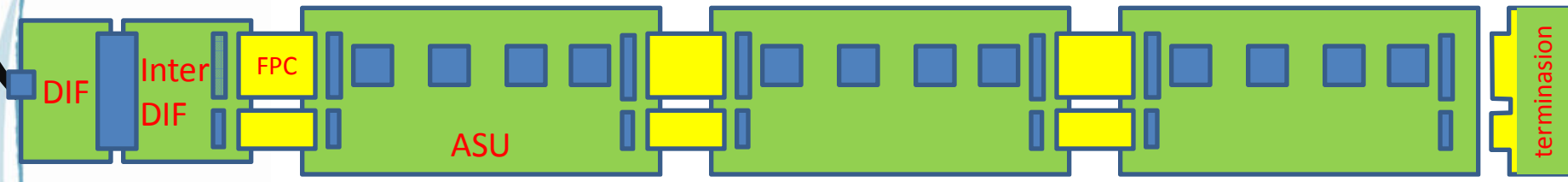
- Electronic board with Hardroc1 readout
- Electronic board with Hardroc2 readout
- Electronic board with Dirac2 readout
- LabVIEW test support
- DIF development

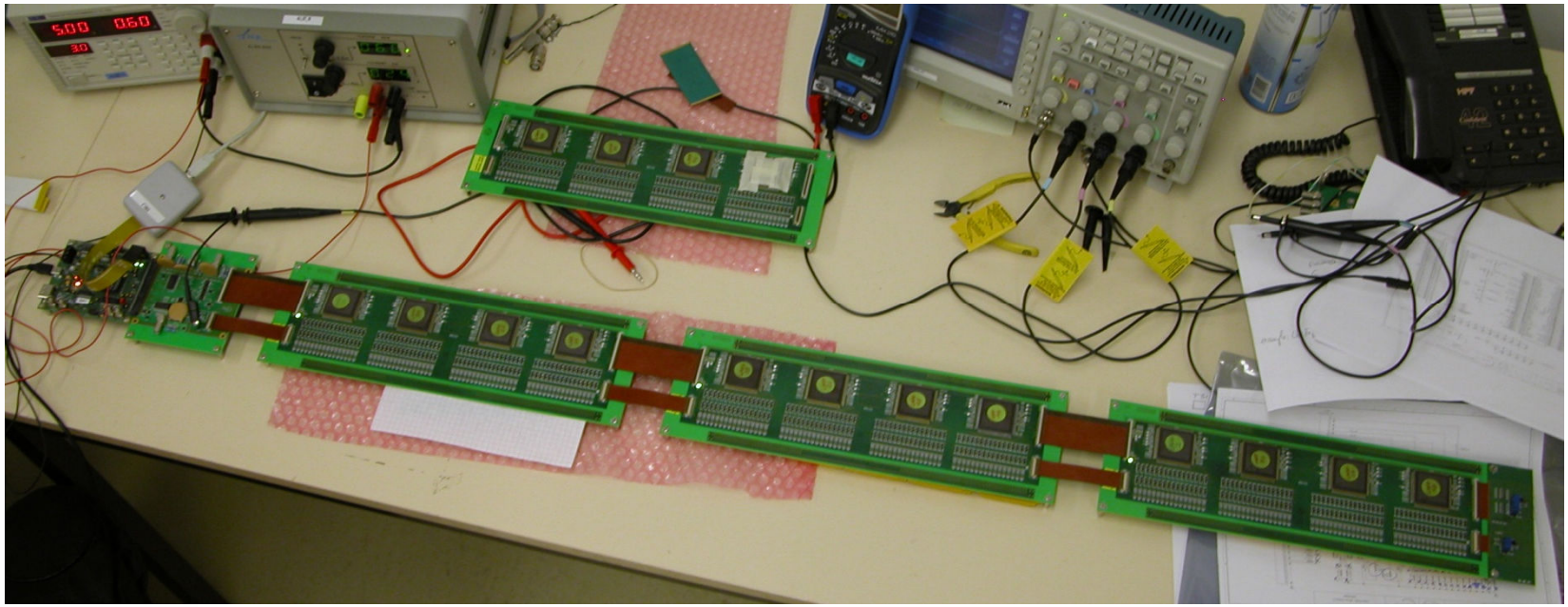




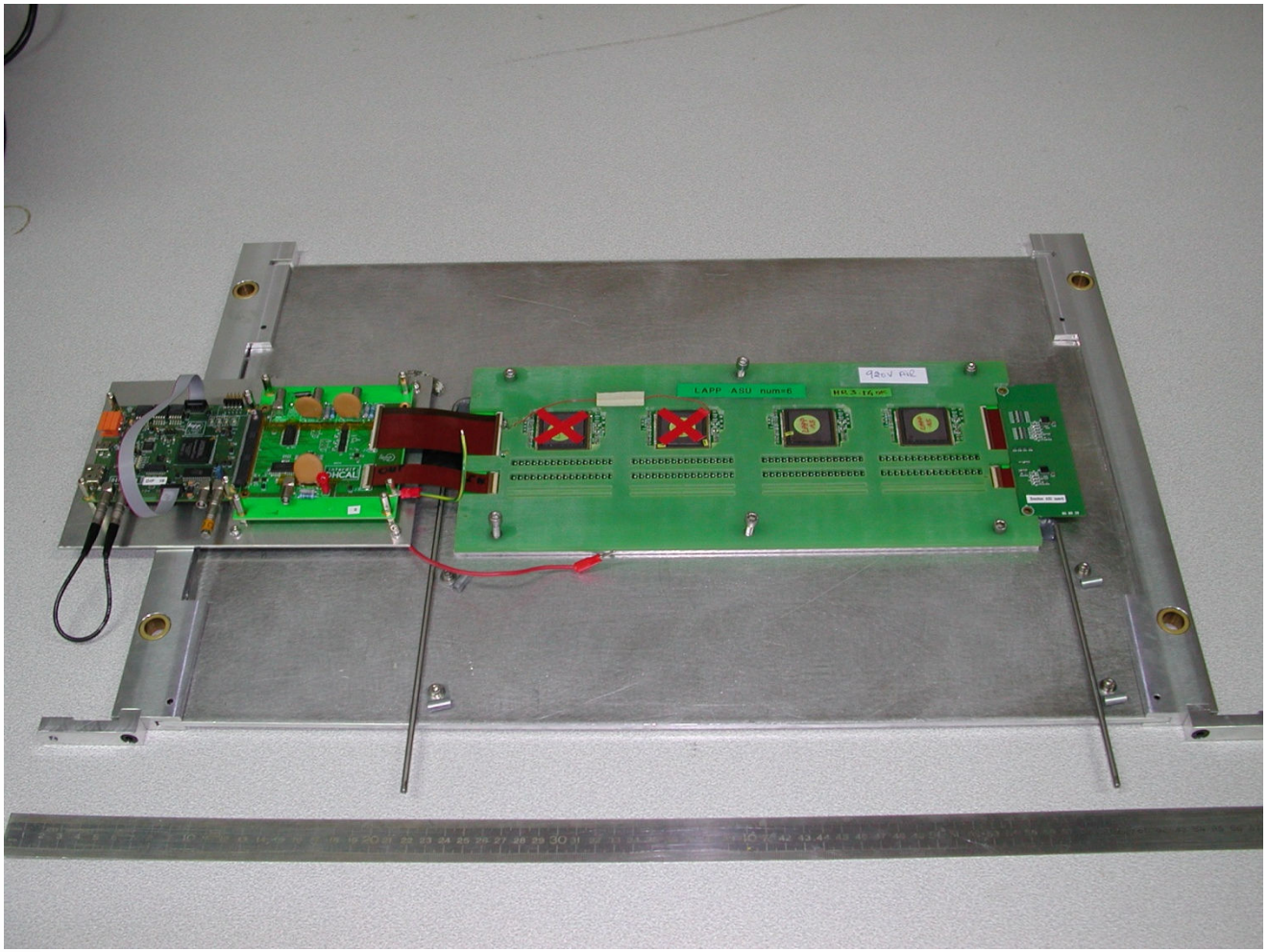
# board with Hardroc1

USB

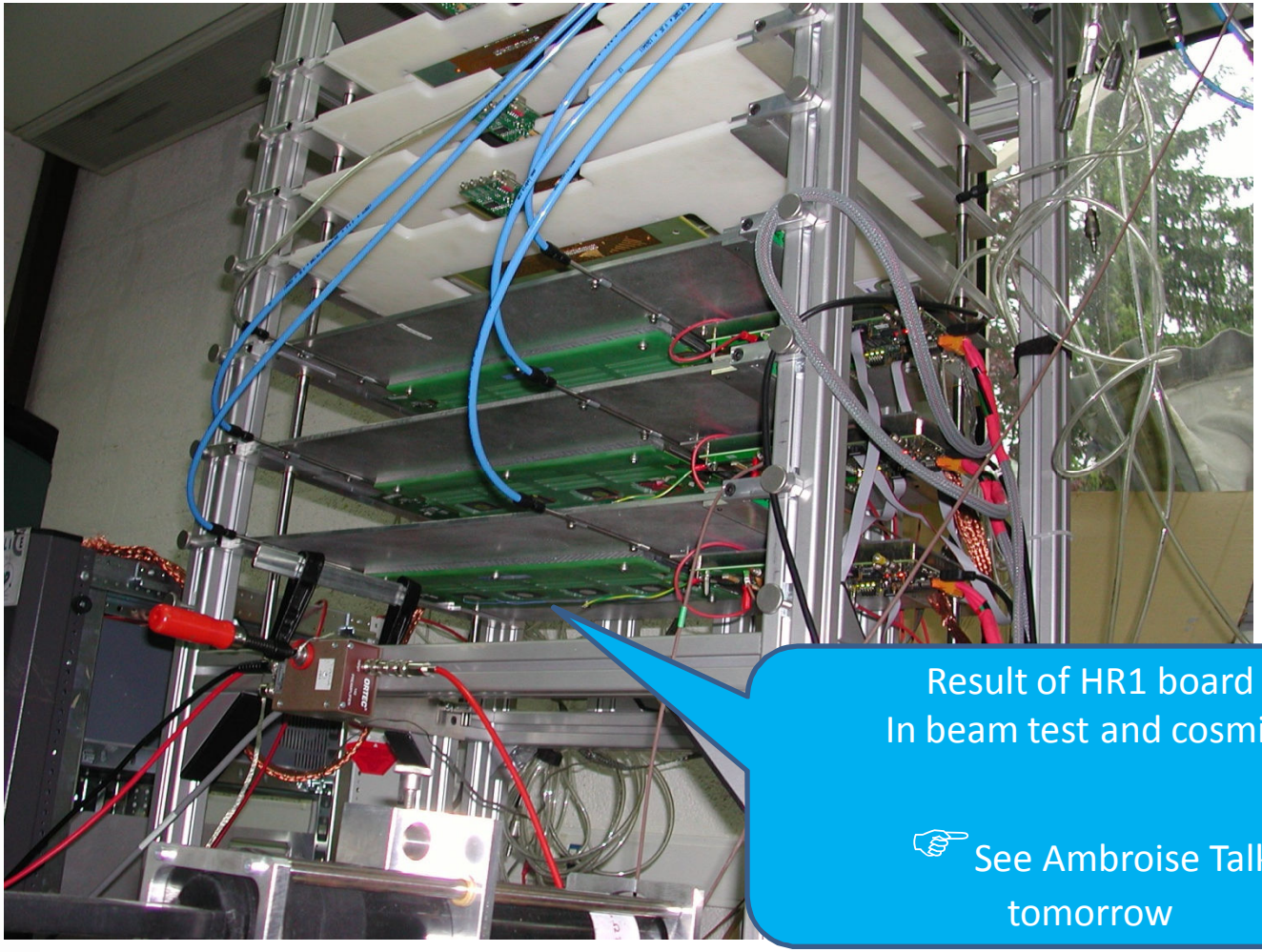


# detector with Hardroc1



# detectors with Hardroc1

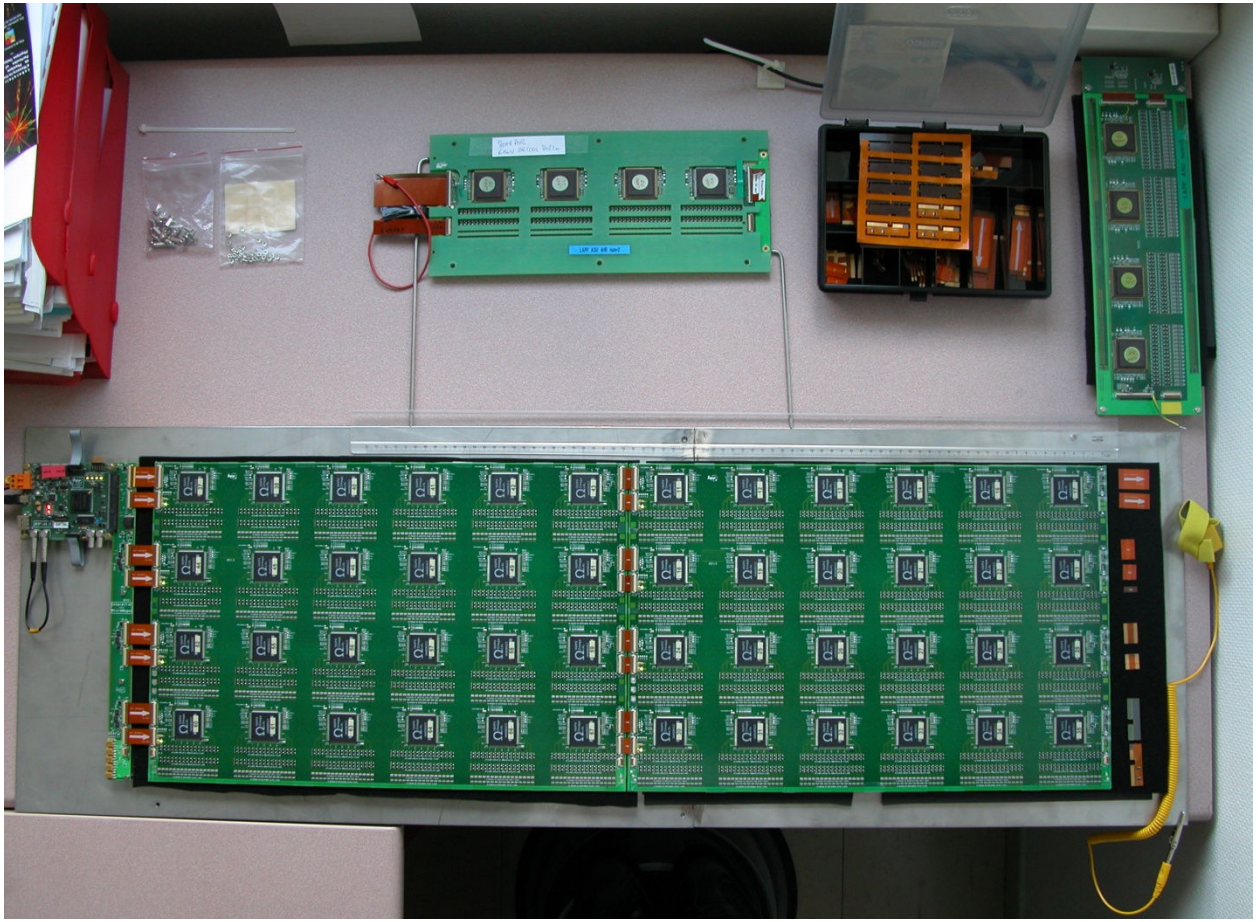


Result of HR1 board
In beam test and cosmic:

☞ See Ambroise Talk tomorrow

# Boards with Hardroc2

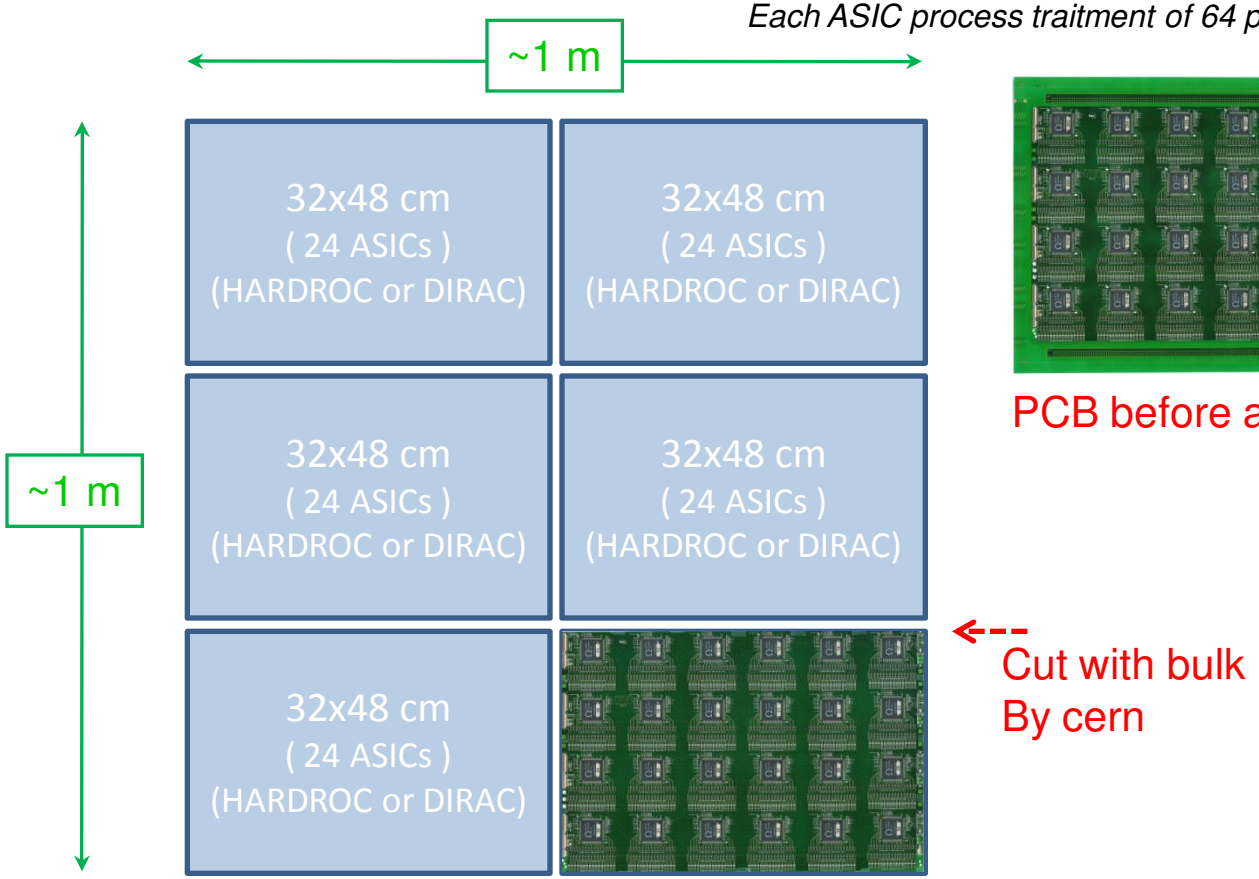
~1 m



~0.33 m

# Detector module in $M^2$

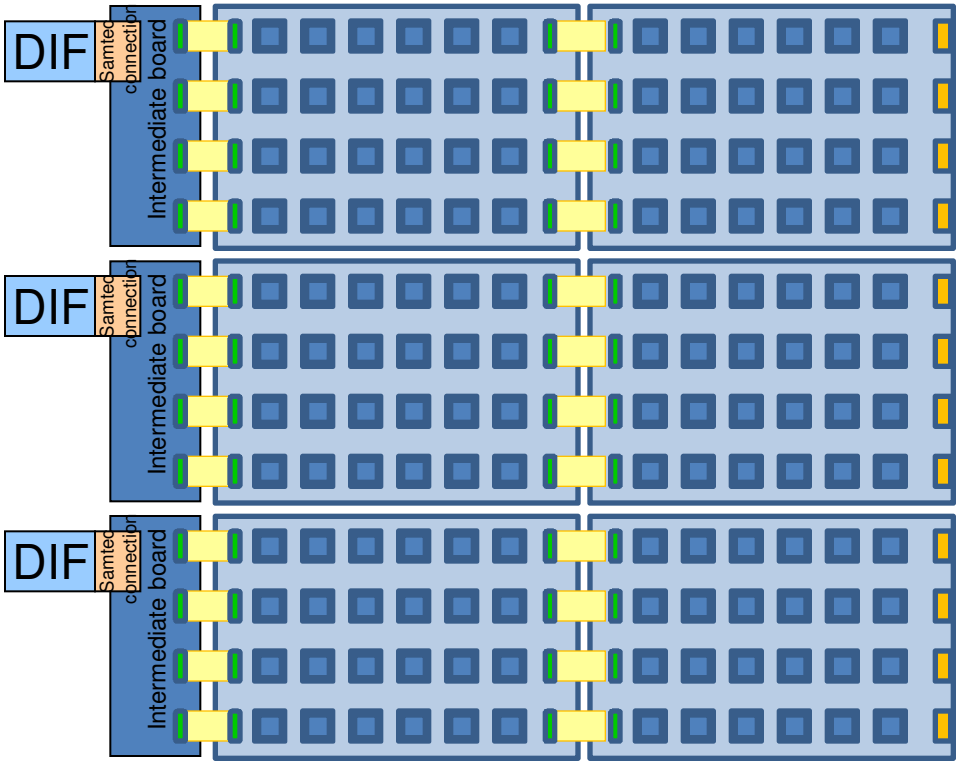
*Each ASIC process traitment of 64 pads (8x8cm)*






PCB before assembly

# Link in $M^2$



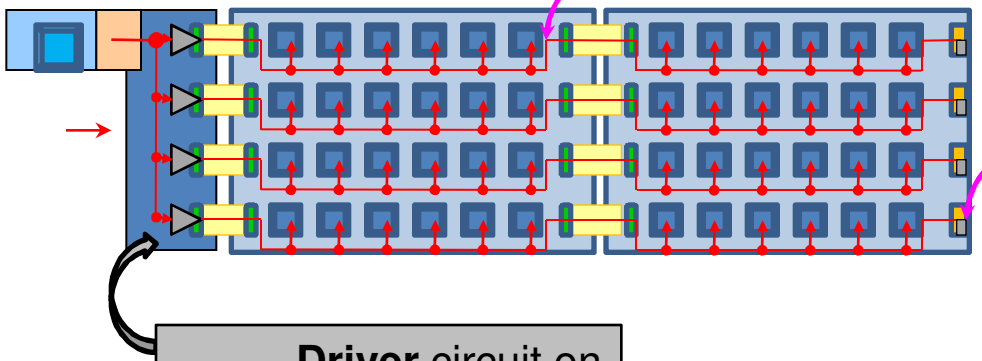

: Flat Printed Circuit

: ASIC chip (64 channels)

: Hirose connector

: Terminasion component

# Data flow: DIF ➡ ASIC



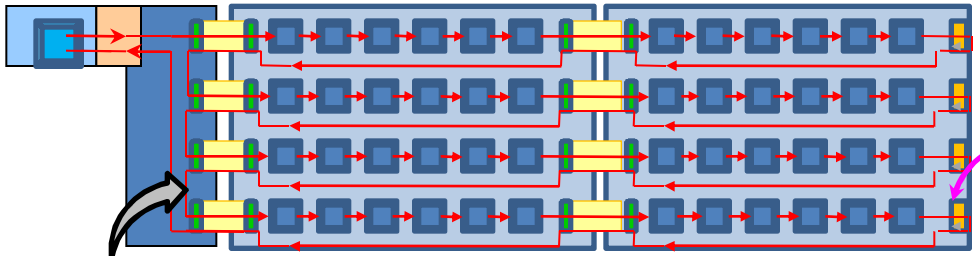
Add buffer by precaution for CK_SC

Put passive terminasion on ASU:
270pF+50Ω for cmos
100Ω for LVDS
50Ω for Ctest

**Driver** circuit on intermediate board
Logic= buffer cmos and LVDS
Ctest= AOP, 1+R2/R1

= FPGA on DIF

# Data flow: DIF ⇄ ASIC

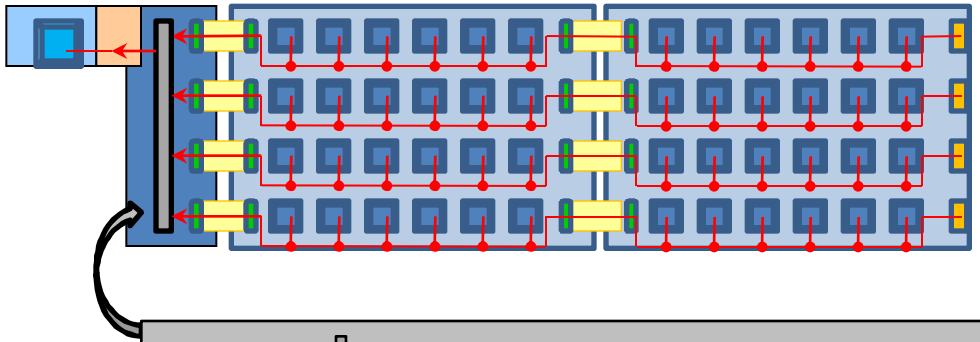


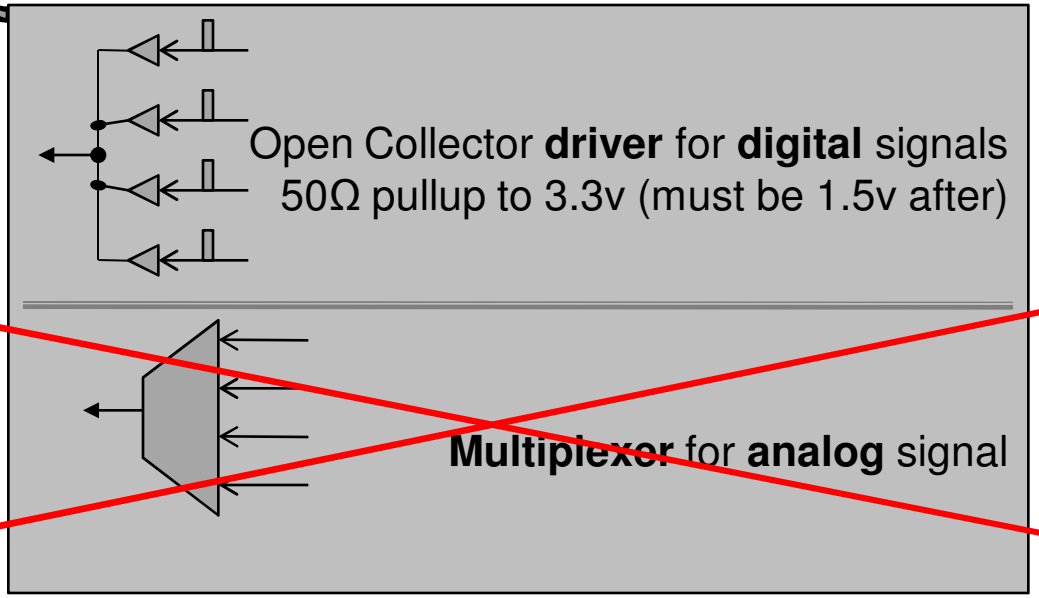
Put shunt and driver on ASU

**Shunt** chain and driver on intermediate board

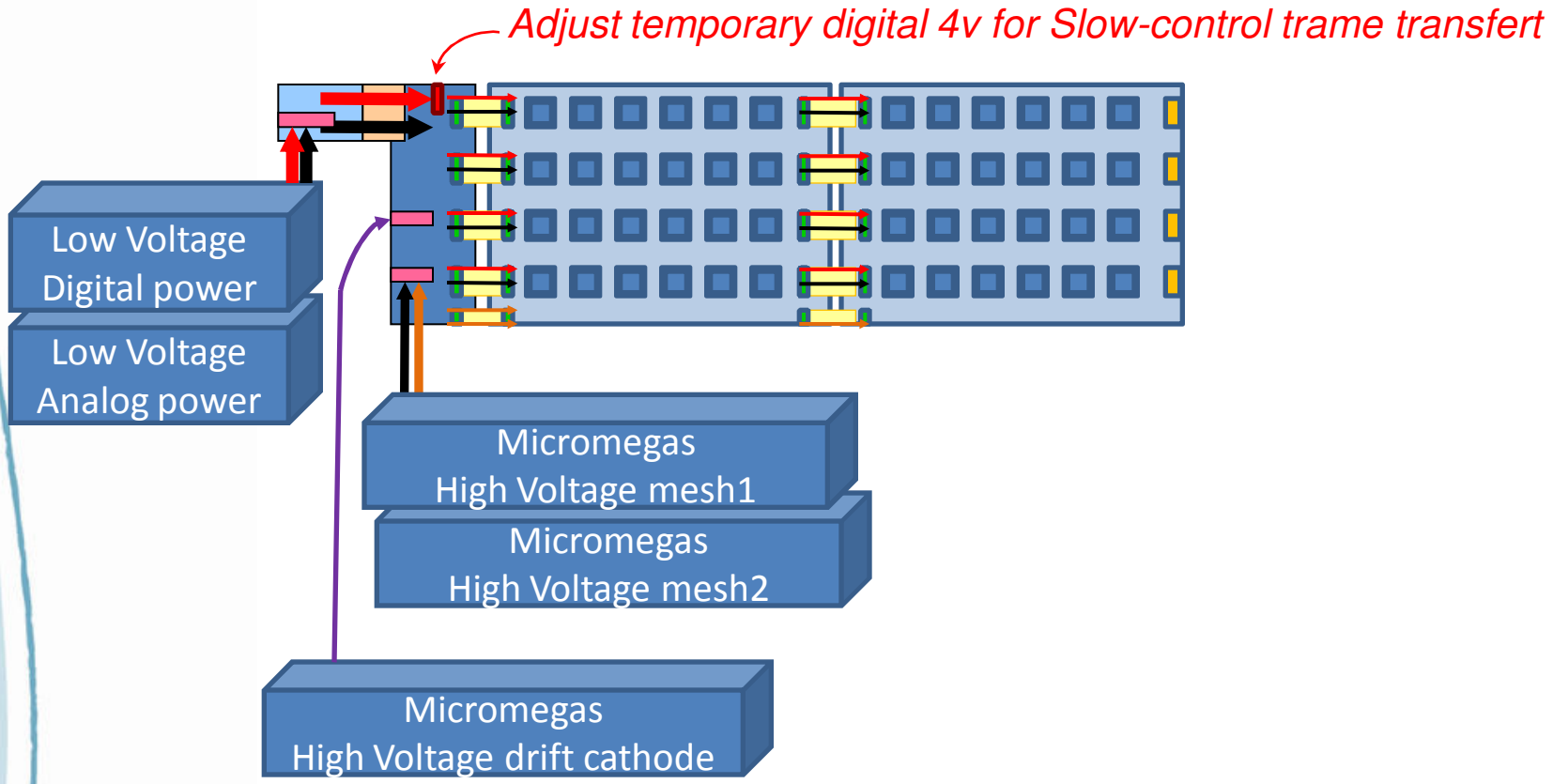
= FPGA on DIF

# Data flow: DIF ⟸ ASIC



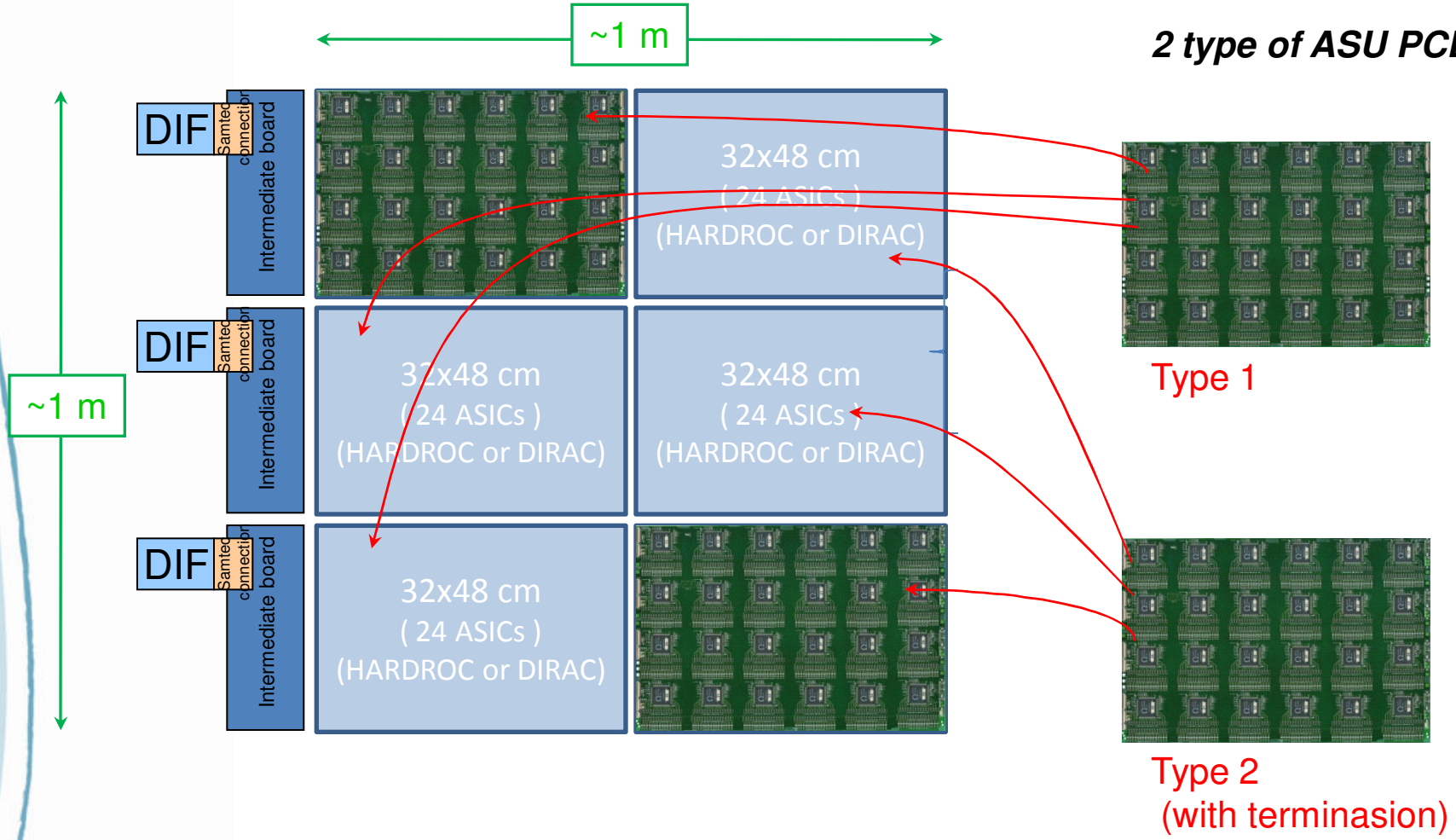


# Power distribution: DIF ⟹ ASIC, dectector



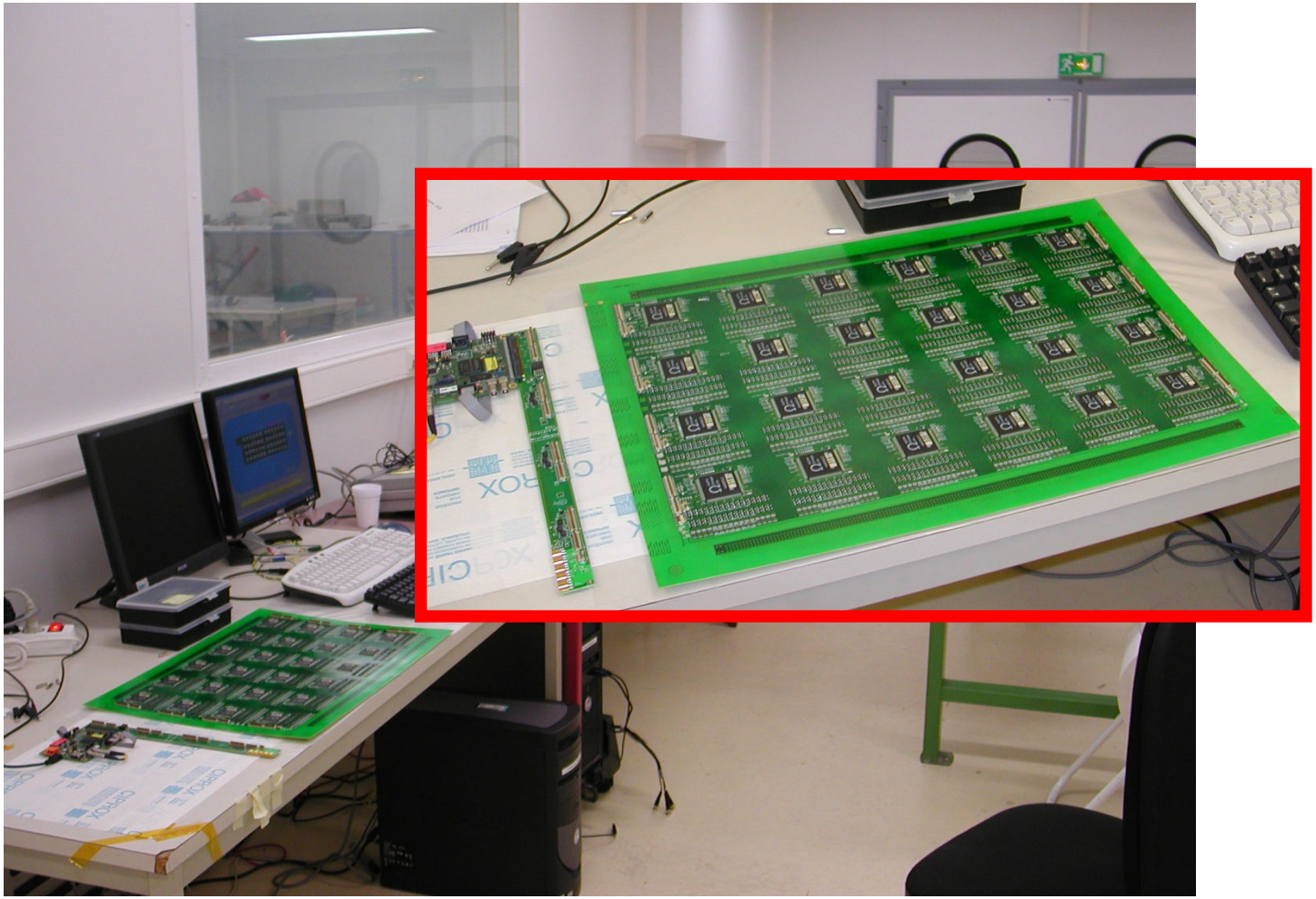

▭: Power connector

# Detector module in $M^2$



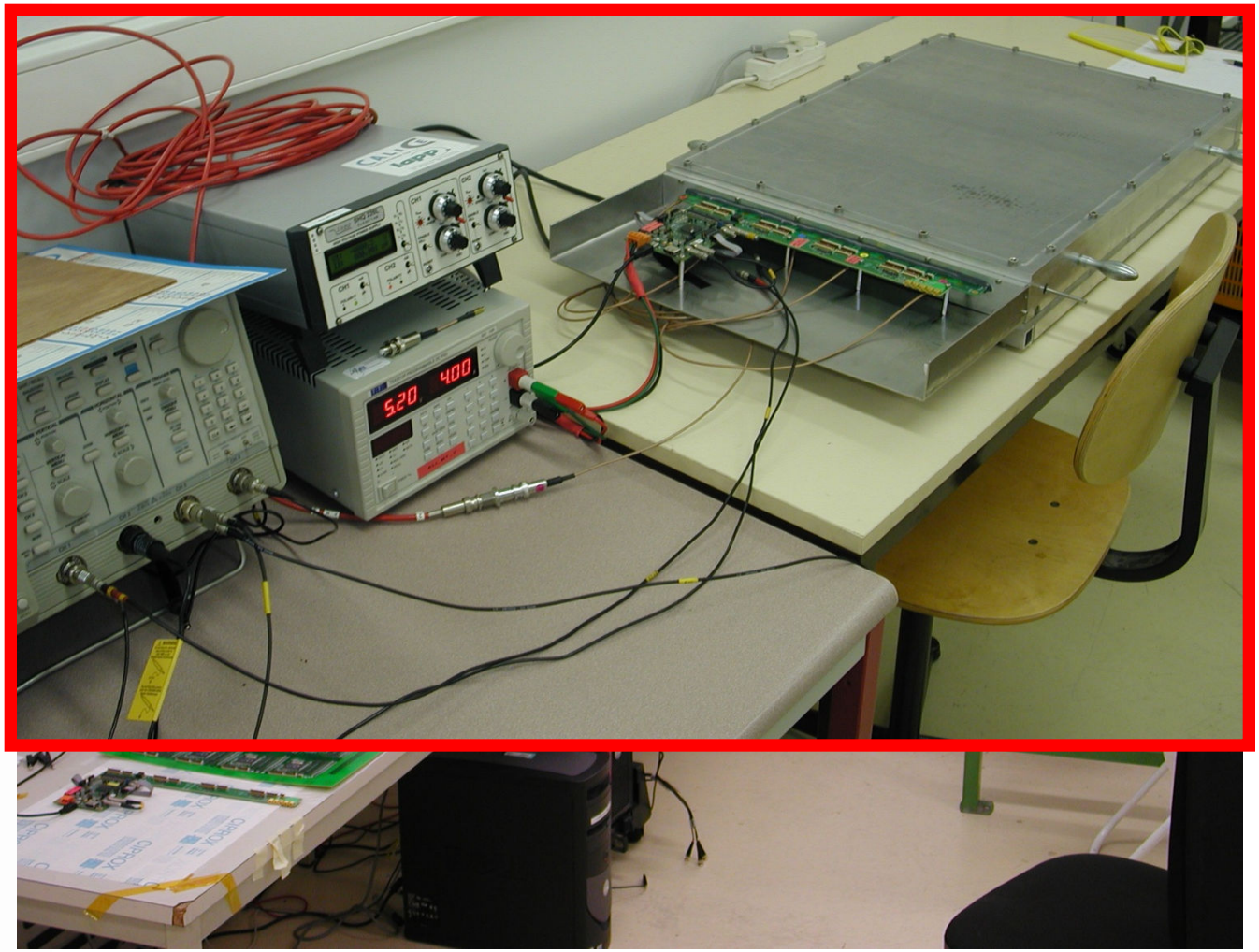
# Boards with Hardroc2

# Board without detector

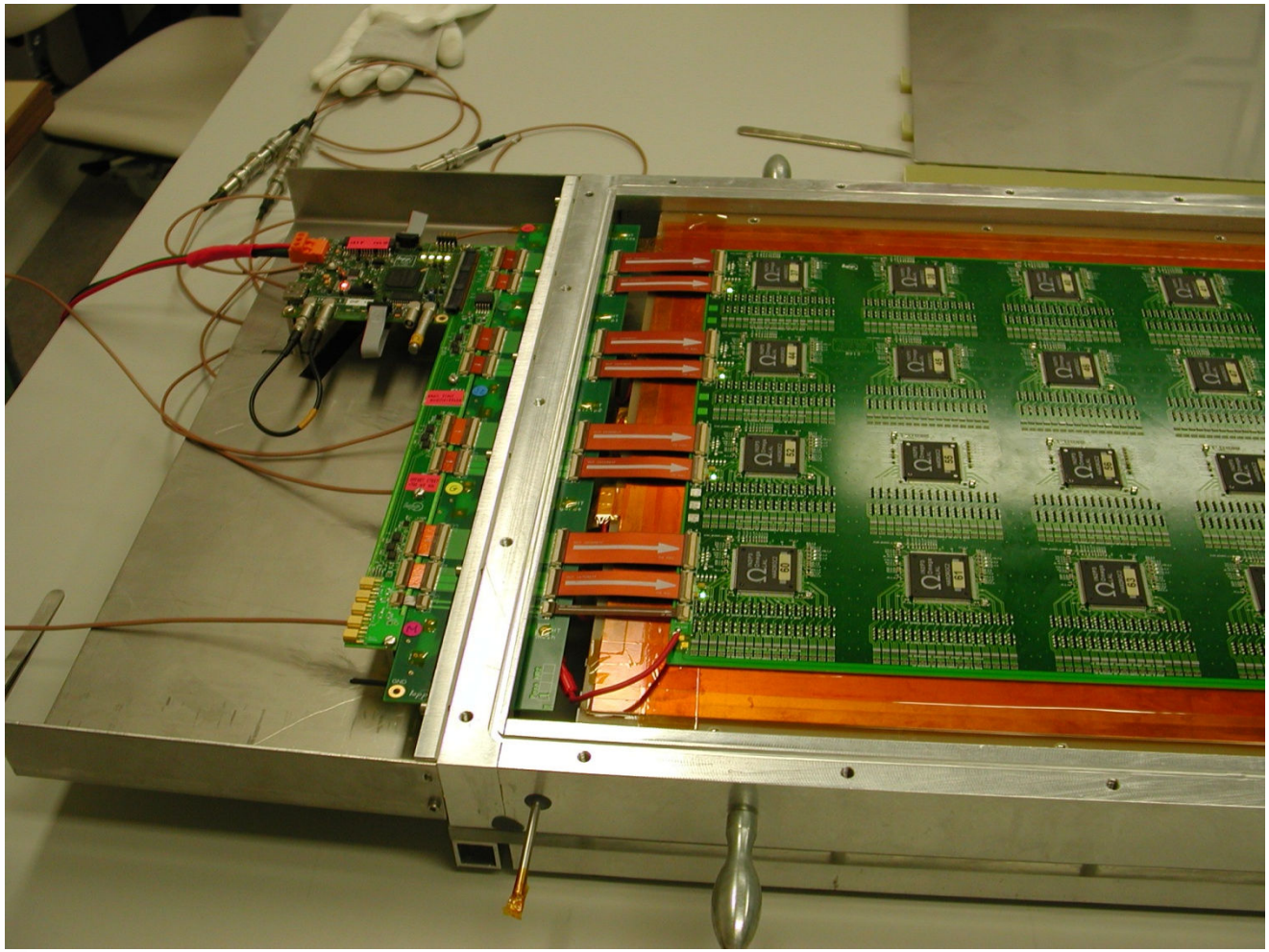


# Board with Detector

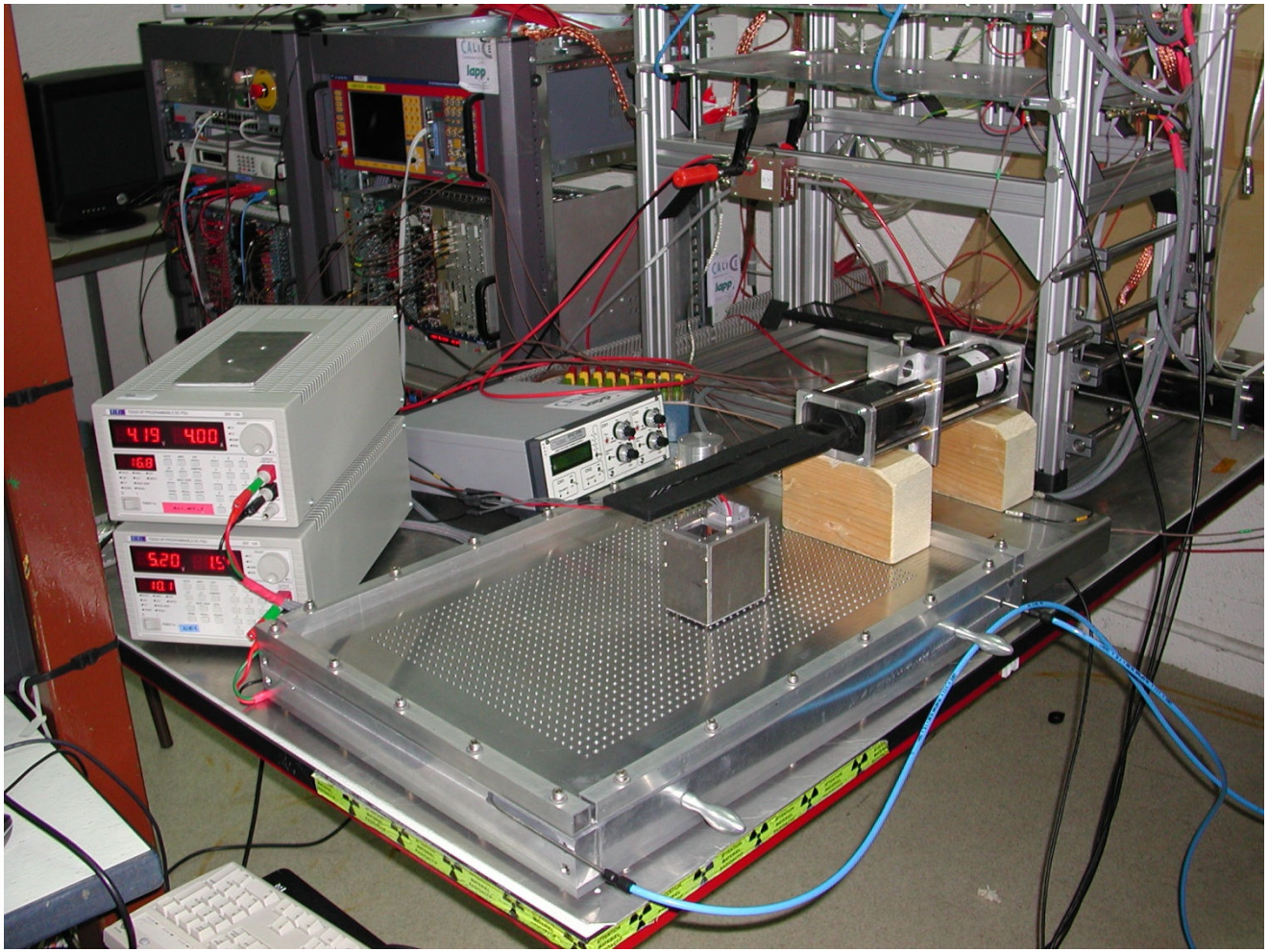
# Board in test box



# Board in test box

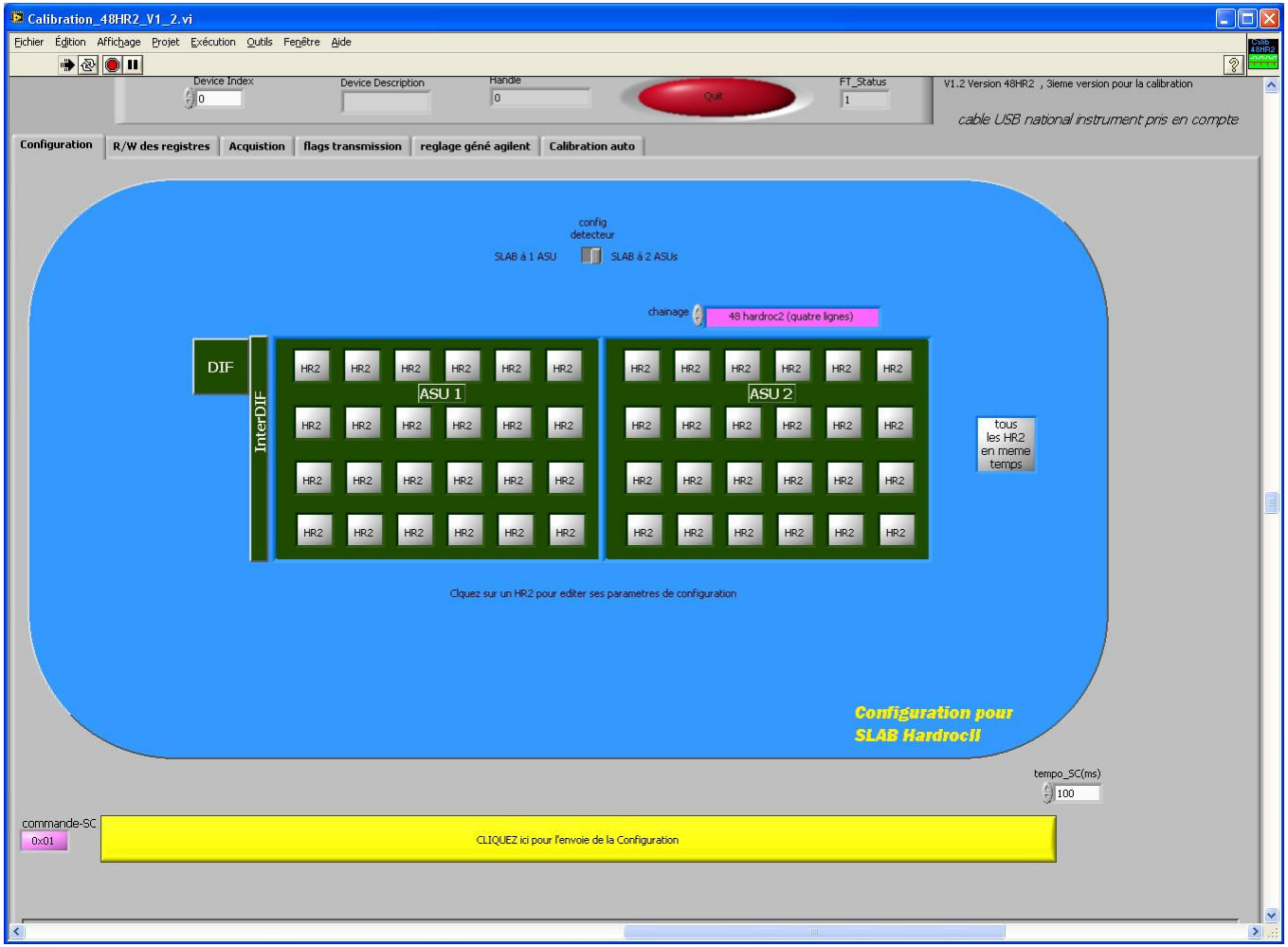


# Board in test box

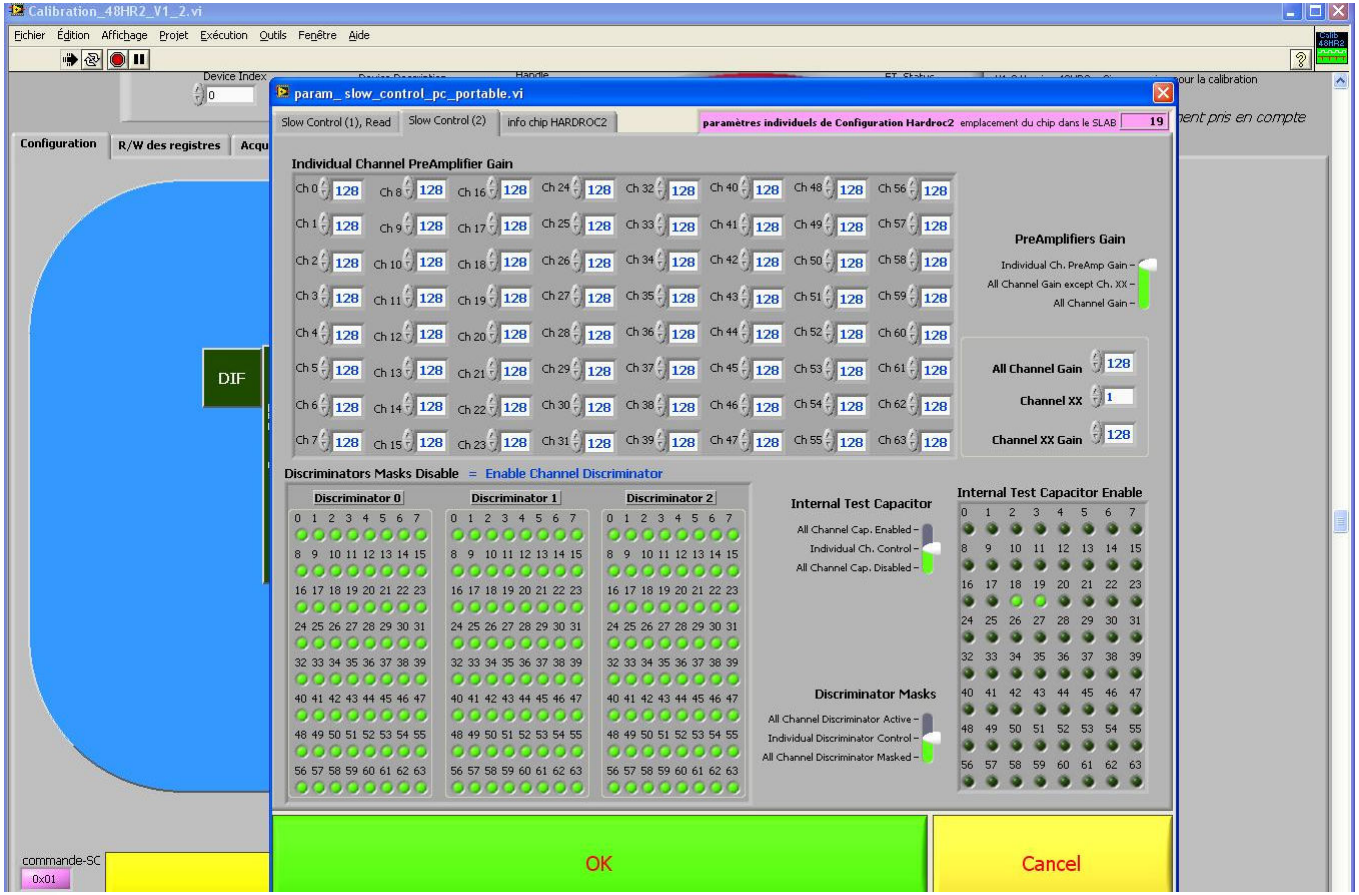


# LabVIEW with Hardroc2

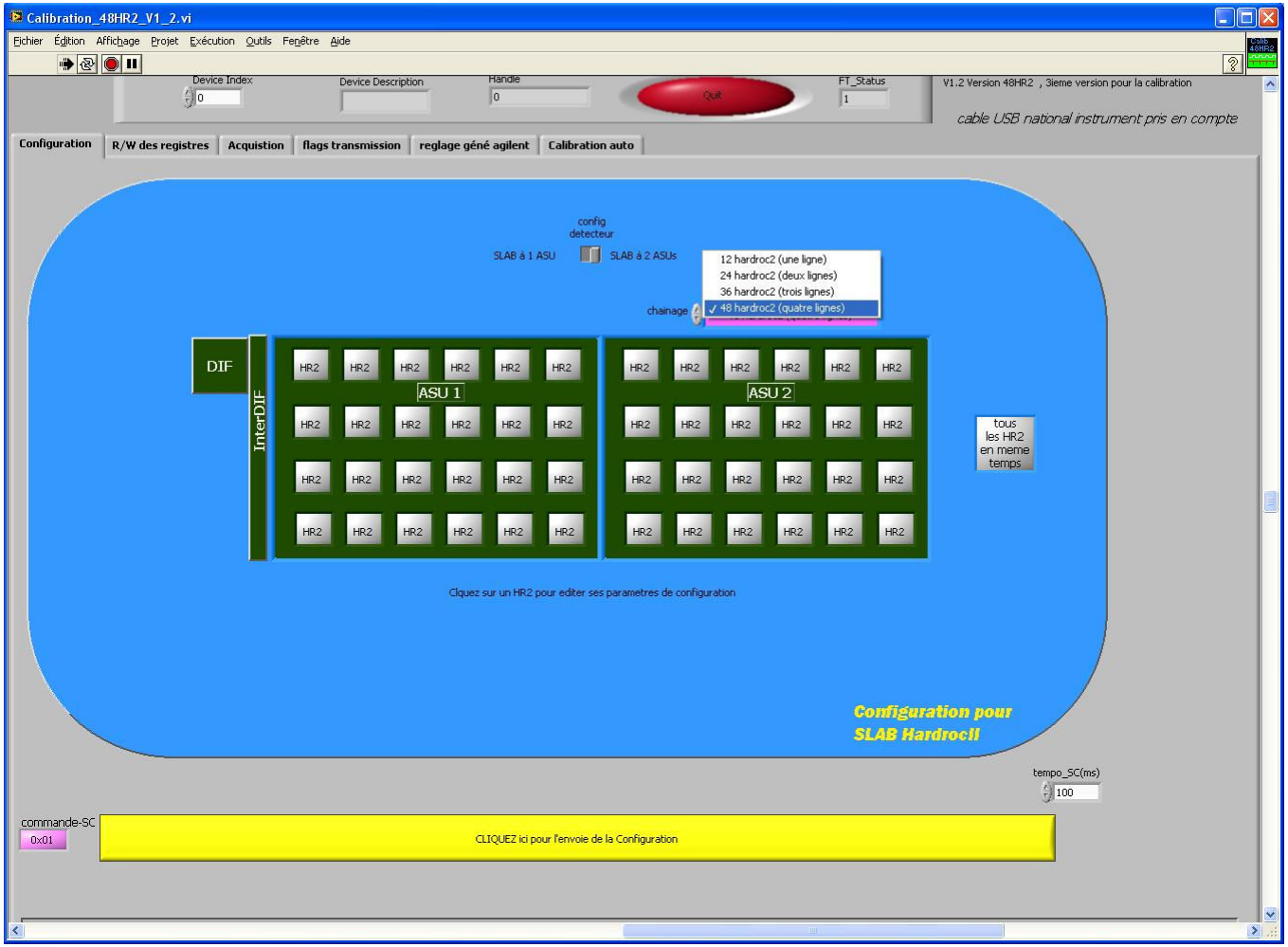
# LAPP LabVIEW support



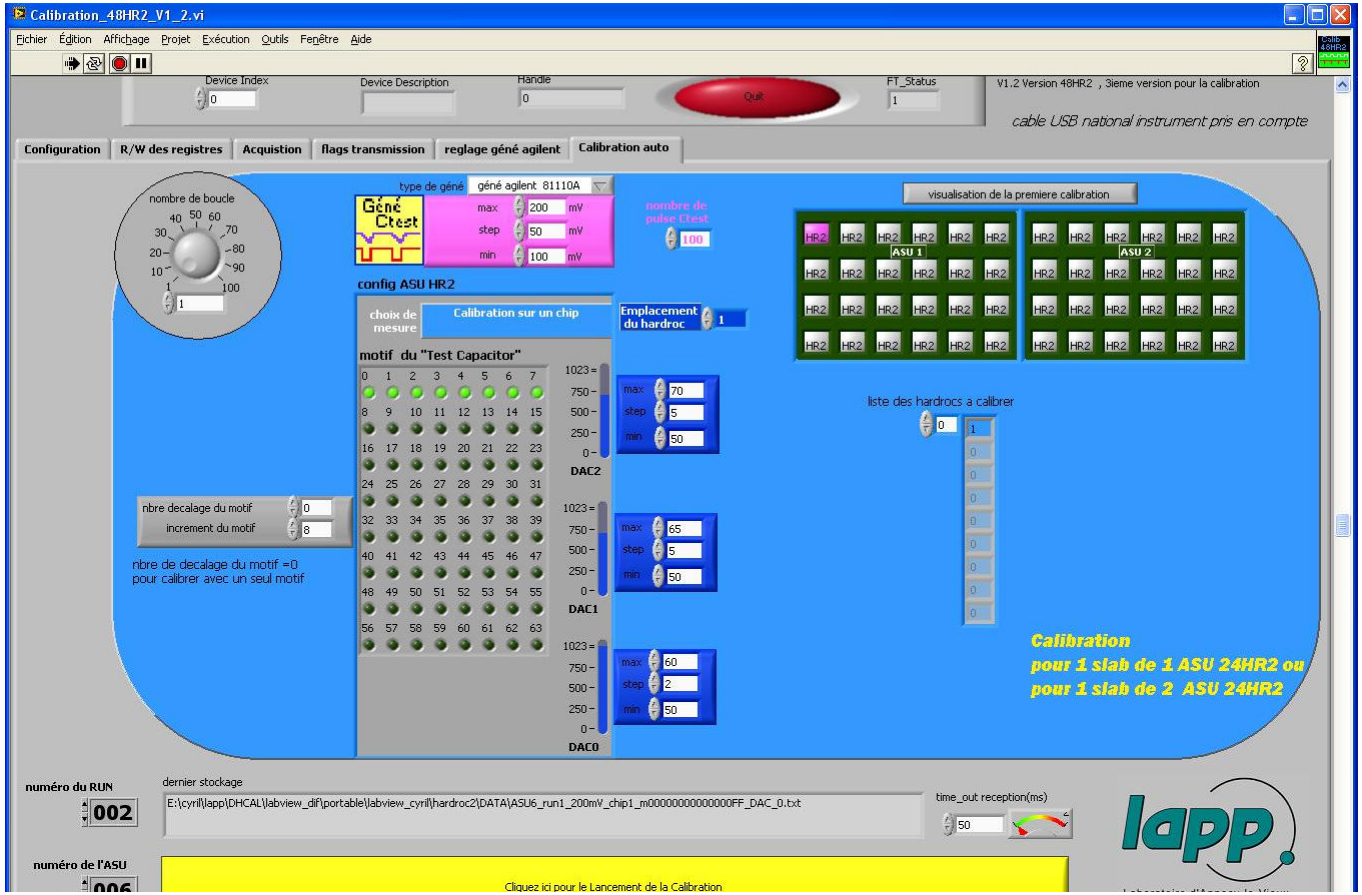
# LAPP LabVIEW support



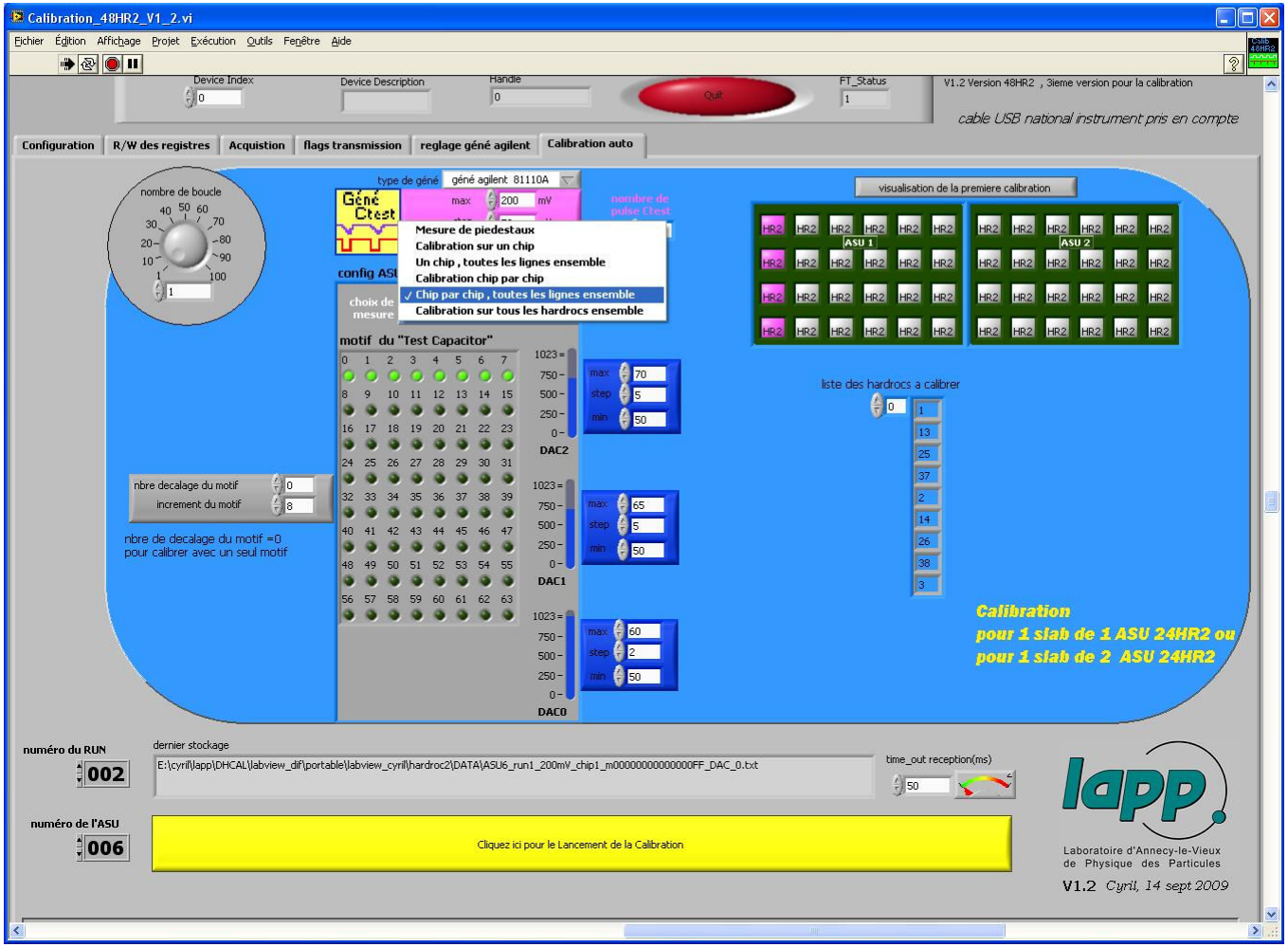
# LAPP LabVIEW support



# LAPP LabVIEW support



# LAPP LabVIEW support



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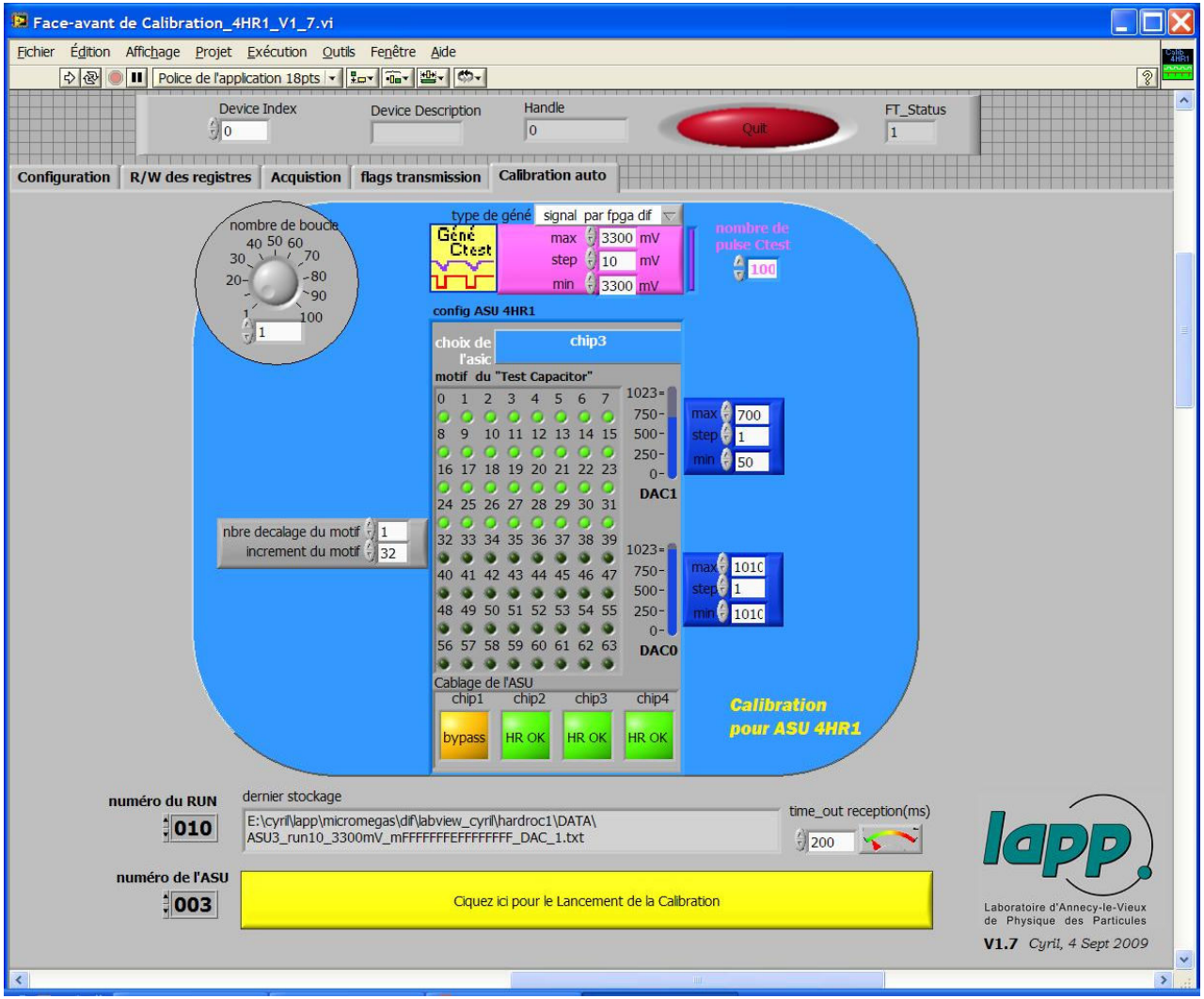
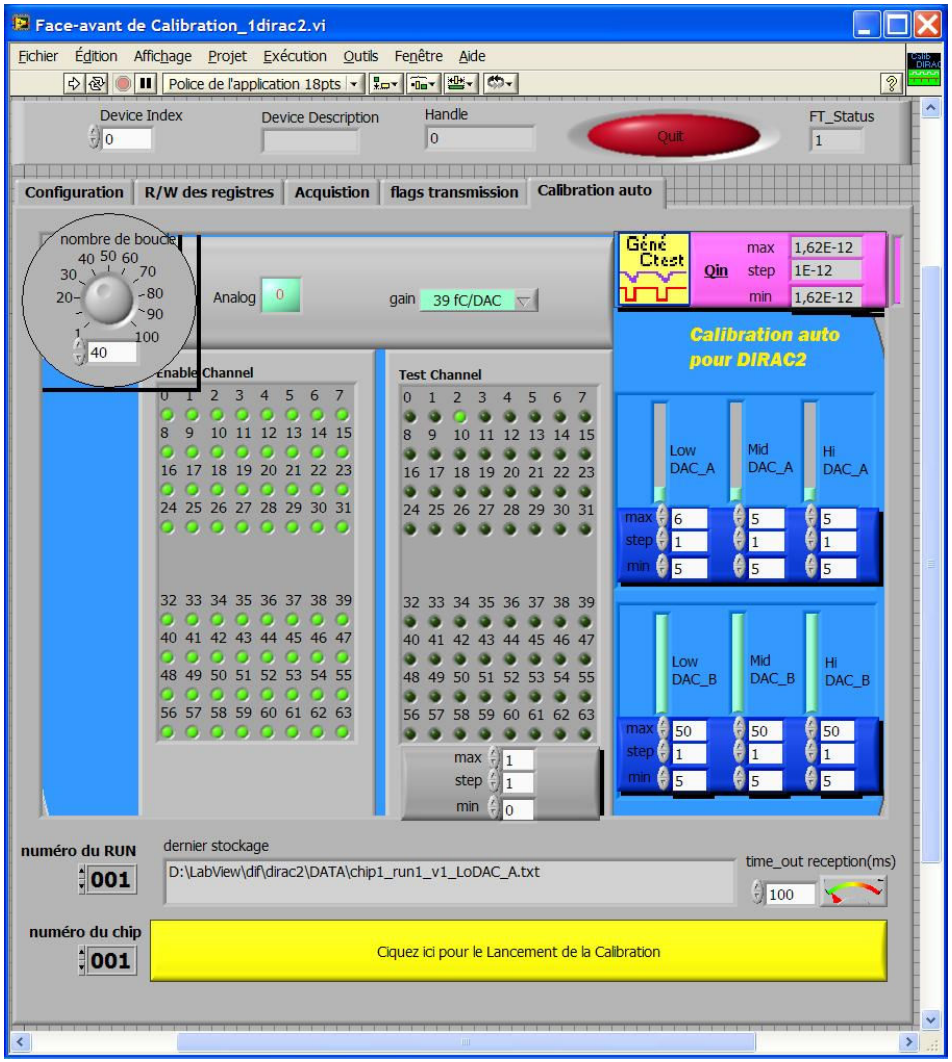
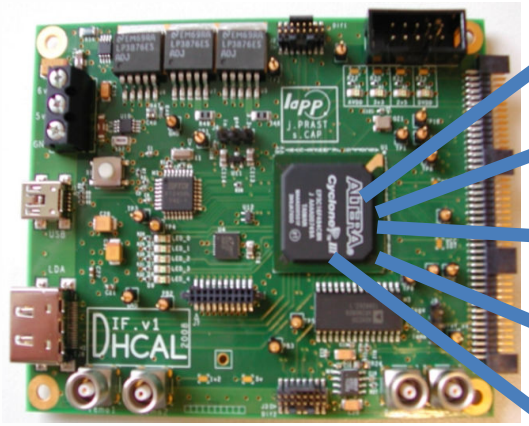


# LAPP LabVIEW support



# DIF




VHDL firmware1 for Hardroc1 Micromegas

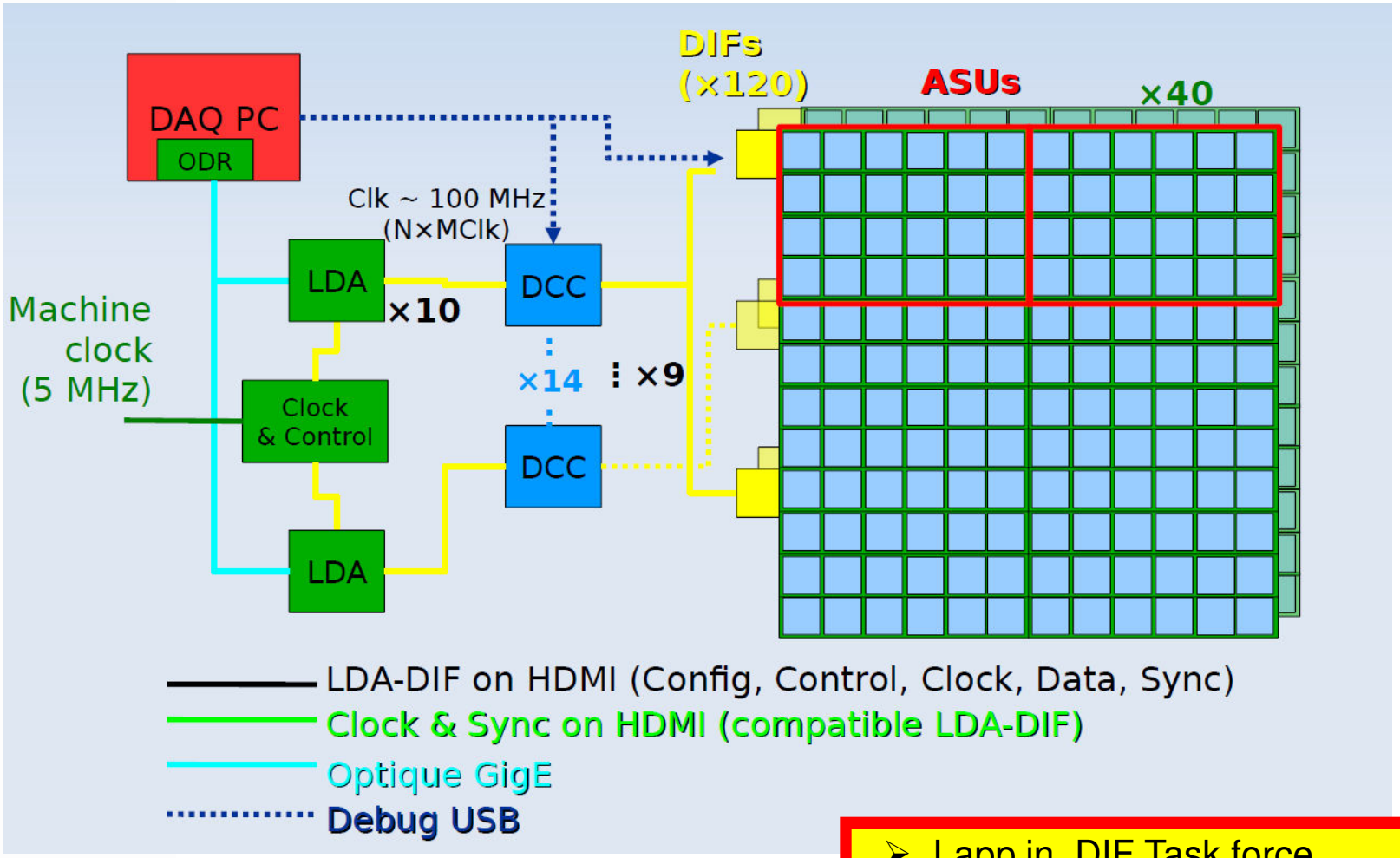
VHDL firmware2 for Hardroc1 RPC

VHDL firmware3 for Dirac2 Micromegas

VHDL firmware4 for Hardroc2 Micromegas

VHDL firmware5 for Calice DAQ Test

# CALICE DAQ




- Lapp in DIF Task force

# Electronic LAPP team

- **Julie Prast**: DIF conception, DIF Link Study
- **Guillaume Vouters**: DIF firmware development, ASU test, integration
- **Sebastien Cap**: DIF CAO, interDIF Conception&CAO, integration
- **Renaud Gaglione**: Dirac conception(ASIC&ASU), R&D protection inside PCB ASU test, integration .
- **Alexandre Dalmaz**: ASUs CAO (Hardroc&Dirac), R&D protection inside PCB
- **Cyril Drancourt**: ASU Hardroc conception, ASU test, LabVIEW, integration