# HARDROC2: Statistical measurements

http://omega.in2p3.fr/

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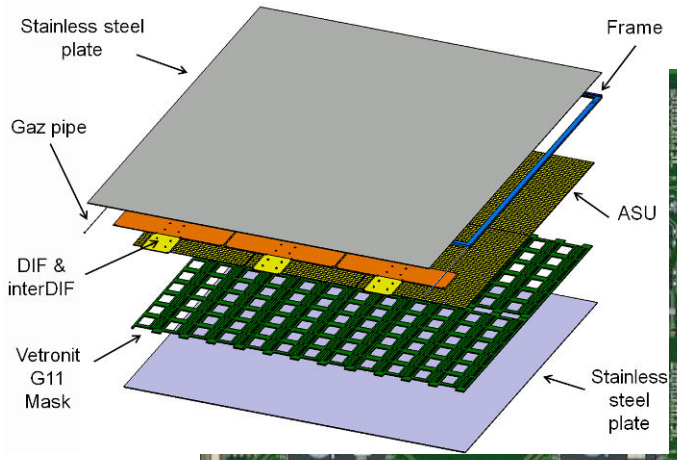
# TOWARDS A TECHNOLOGICAL PROTOTYPE




Slab #1 DIF #1

Slab #2 DIF #2

PC

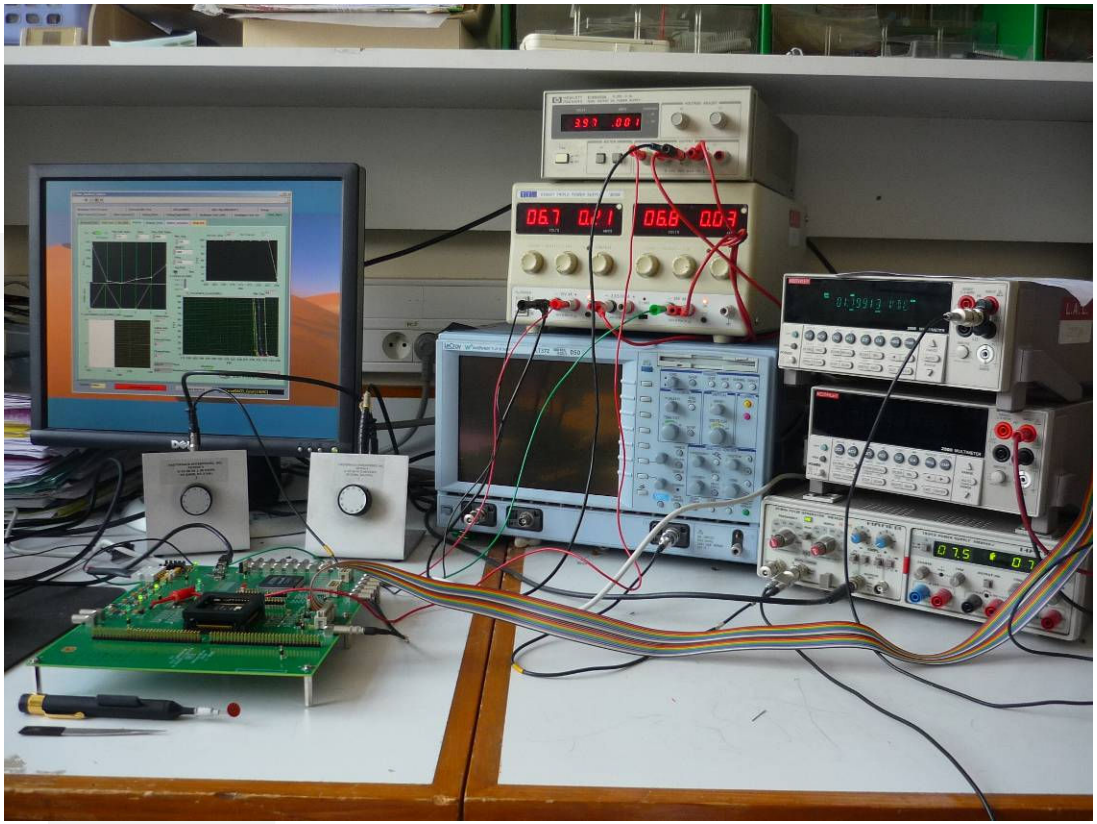
Slab #3 DIF #3

1m$^2$ scalable detector to be equipped and tested

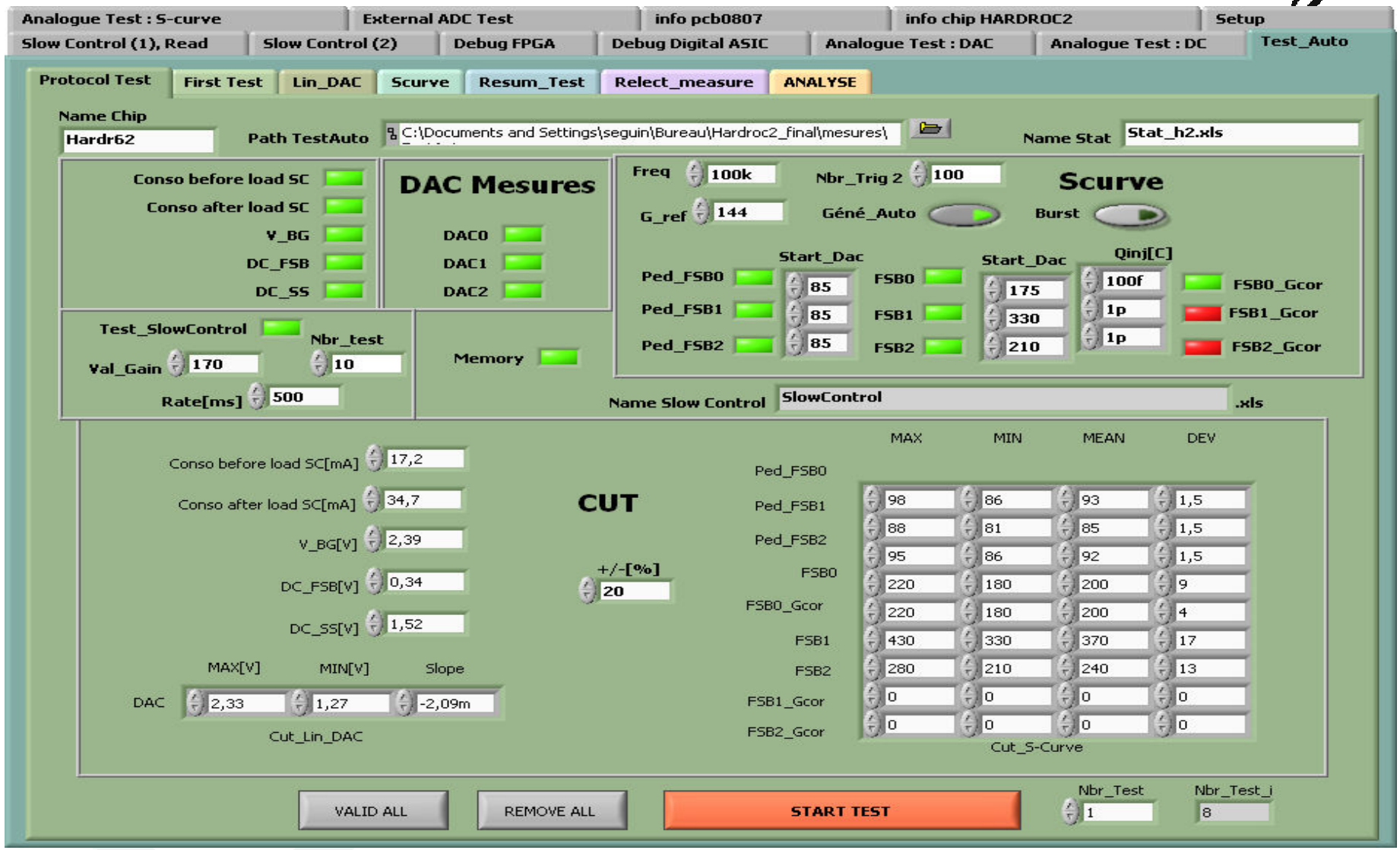
144 chips/m$^2$

# HR2 test

- 400 chips to be tested to equip 1m$^2$ RPC and µmegas detectors
- ≈300 chips tested this summer in ORSAY and in Lyon
- Good exercise before tests of productions (5000 chips)

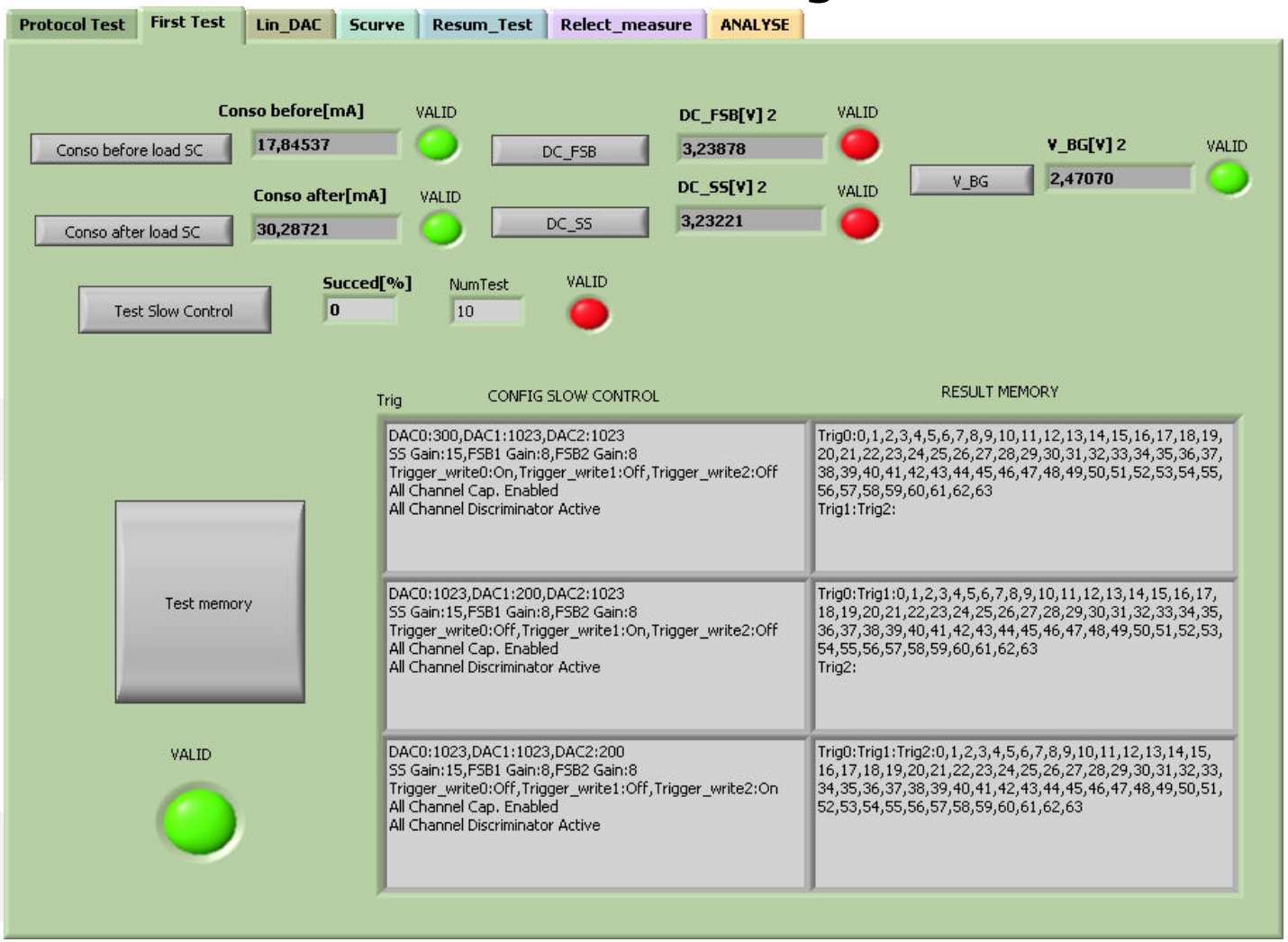


# LABVIEW SETUP @Rodolphe Della Negra (IPNL)

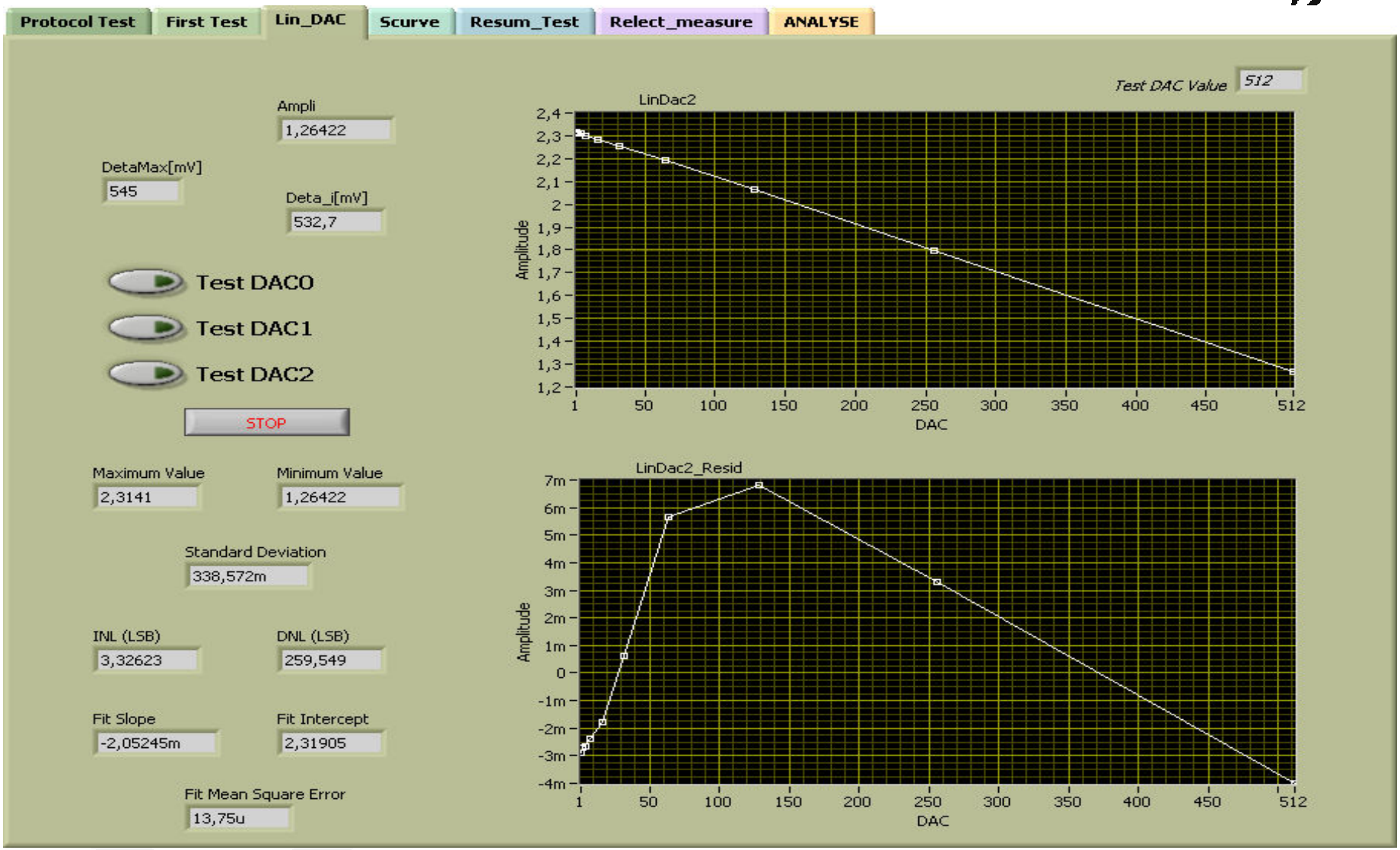


# LABVIEW SETUP @Rodolphe Della Negra (IPNL)

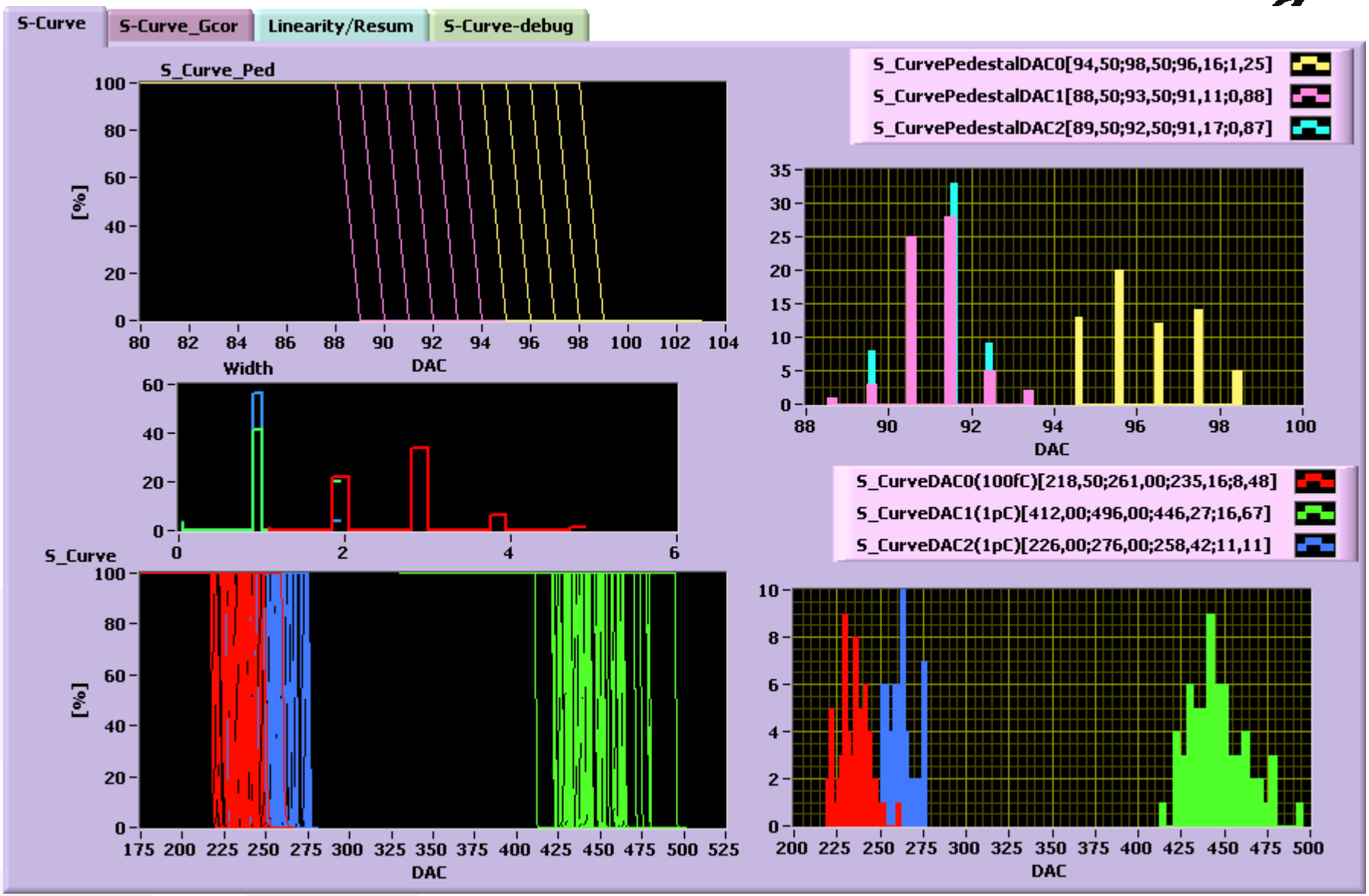
- DC levels, power consumption, VBG, memory test, SC test with a « difficult config »



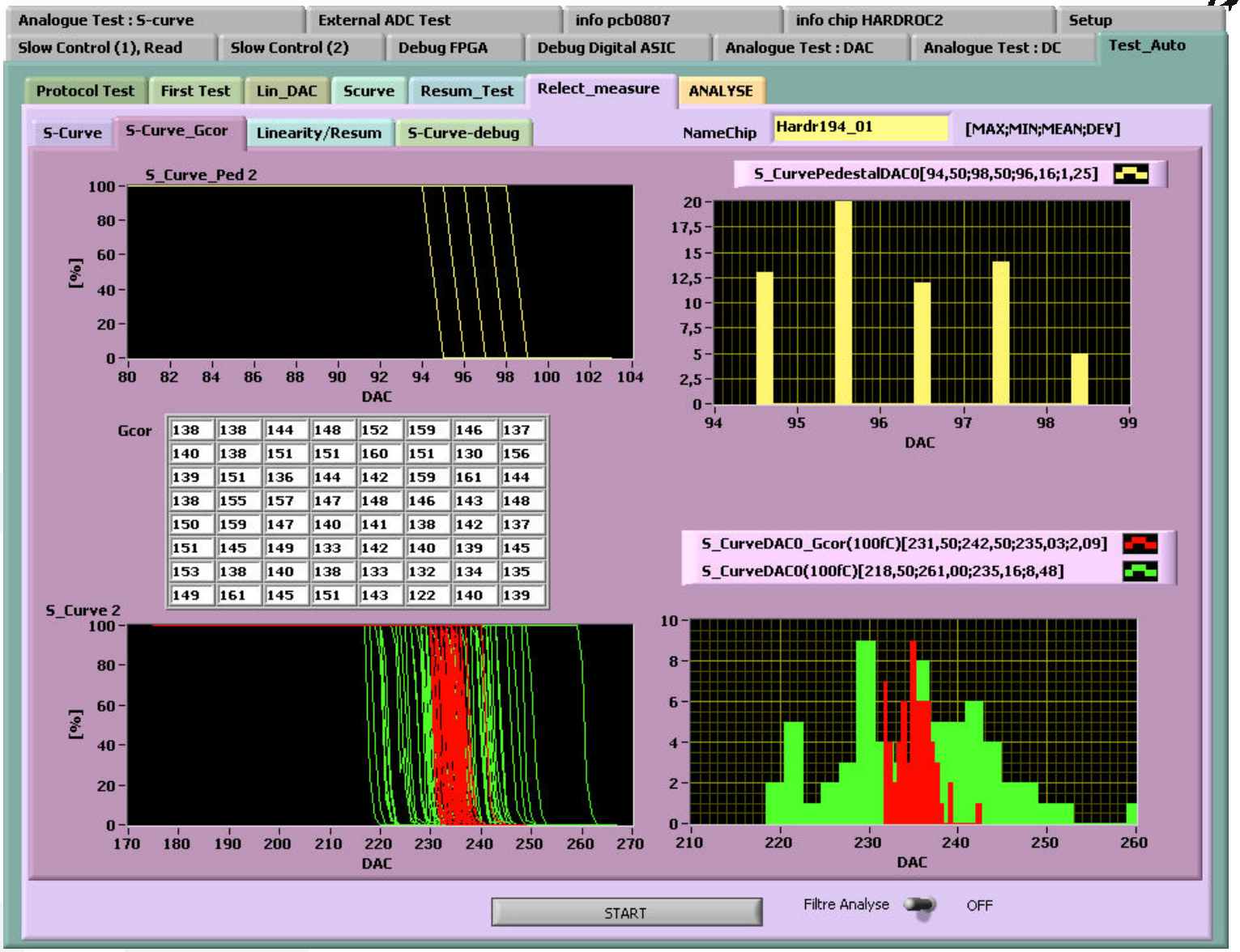
# 3 DACs linearity



# SC measurements: pedestal, 100fC, 1pC

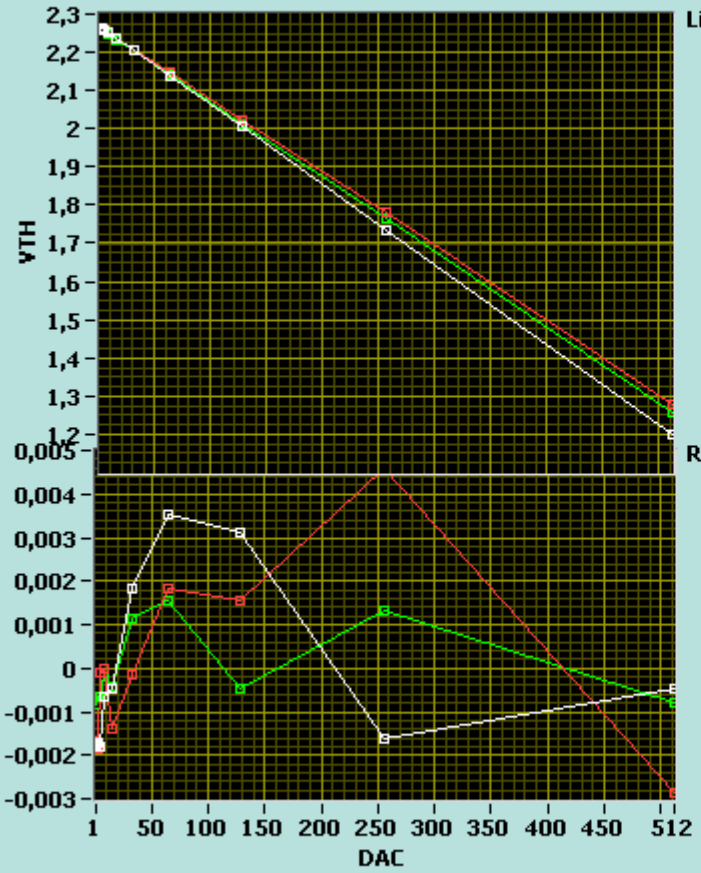


# FSB0 Gain Correction



# Read back of the measurements

S-Curve | S-Curve_Gcor | Linearity/Resum | S-Curve-debug




Linearity

LinDac0
LinDac1
LinDac2

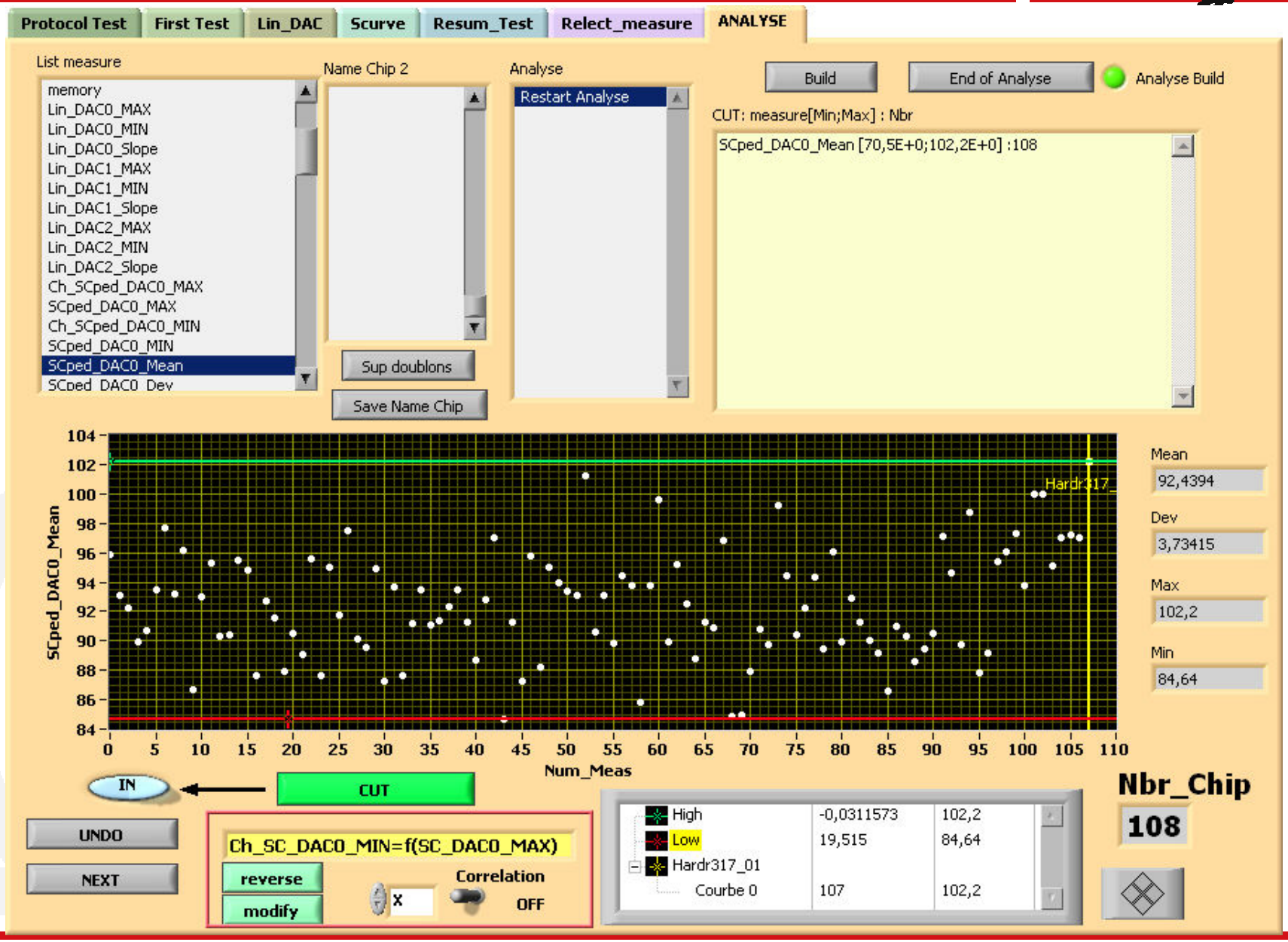
Residual

Res_LinDac0
Res_LinDac1
Res_LinDac2

Resum

```
Hardr211
11/09/2009 08:54:56
-------------------------
Name_SlowControlRef : SlowControl
-------------------------
Conso before load SC
Delay=0:5:887

Value : 13,94 mA
..... Valid .....
-------------------------
Conso after load SC
Delay=0:6:343

Value : 27,61 mA
..... Failed .....
-------------------------
V_BG
Delay=0:3:886

Value : 2,42 V
..... Valid .....
-------------------------
DC_FSB
Delay=0:3:880

Value : 3,24 V
..... Failed .....
-------------------------
DC_SS
Delay=0:3:743

Value : 3,23 V
..... Failed .....
```

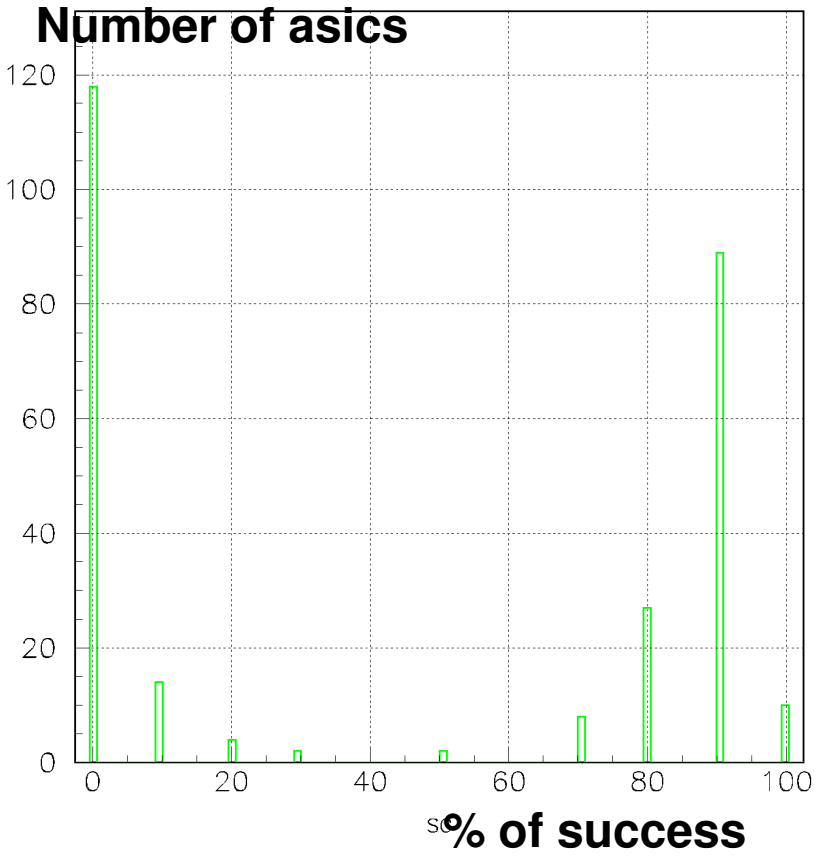
# DATA ANALYSIS



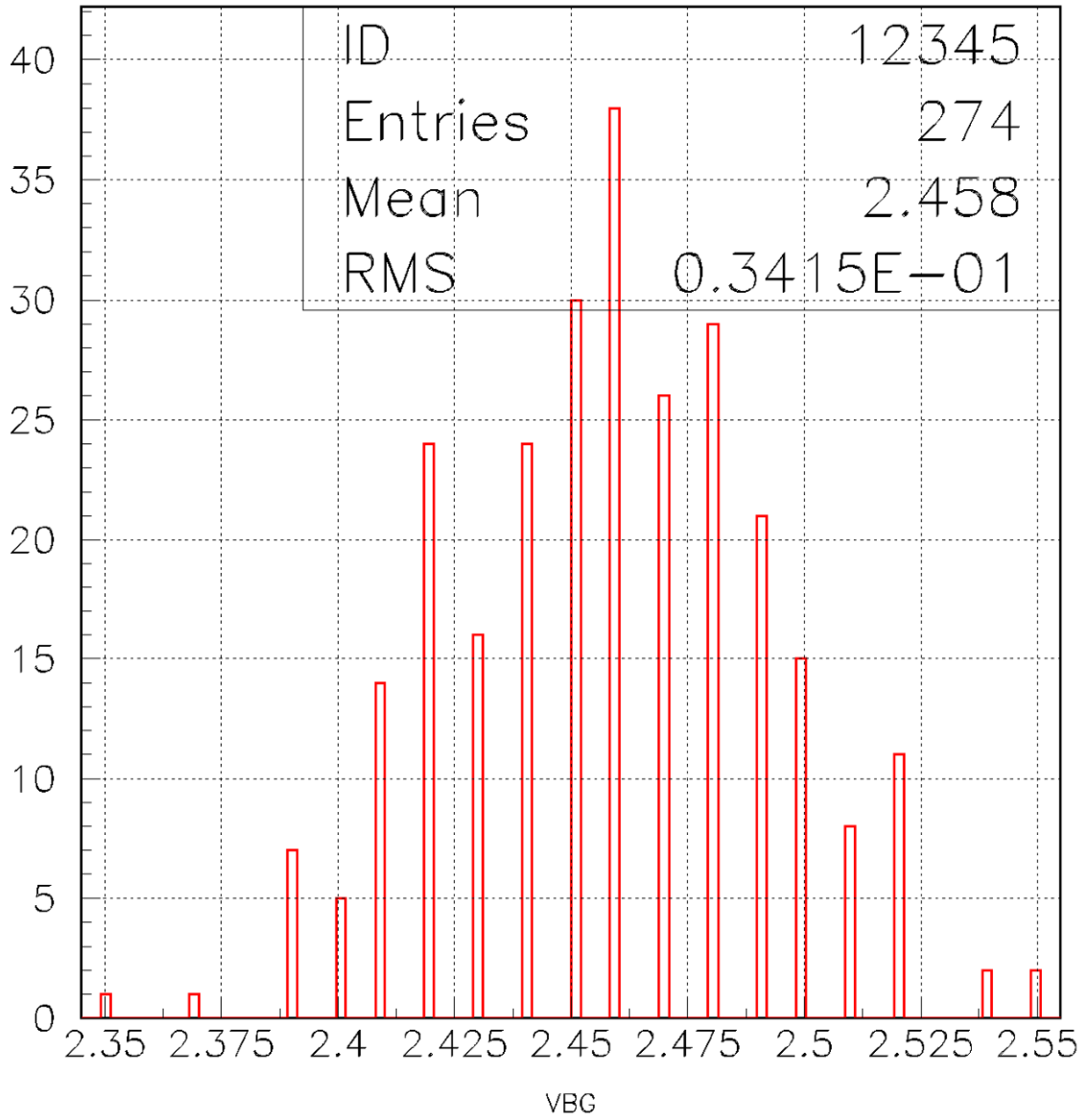
# Results of the SC test performed on 274 chips

- Some gain configurations are sometimes difficult to load in hardroc2
  - Due to long connections between flip flops inside the chips: can be corrected with additional buffers on clk and data signals
  - **necessity to increase digital vdd to 4V**.

- But still, ≈50% of the chips exhibit pb with the loading of « difficult » SC config.
  - Gain=170 = 10101010 loaded 10 times, calculation of the ratio of success.
  - **Anyway 90% of the chips OK for the other tests performed with various SC configs have to be loaded**

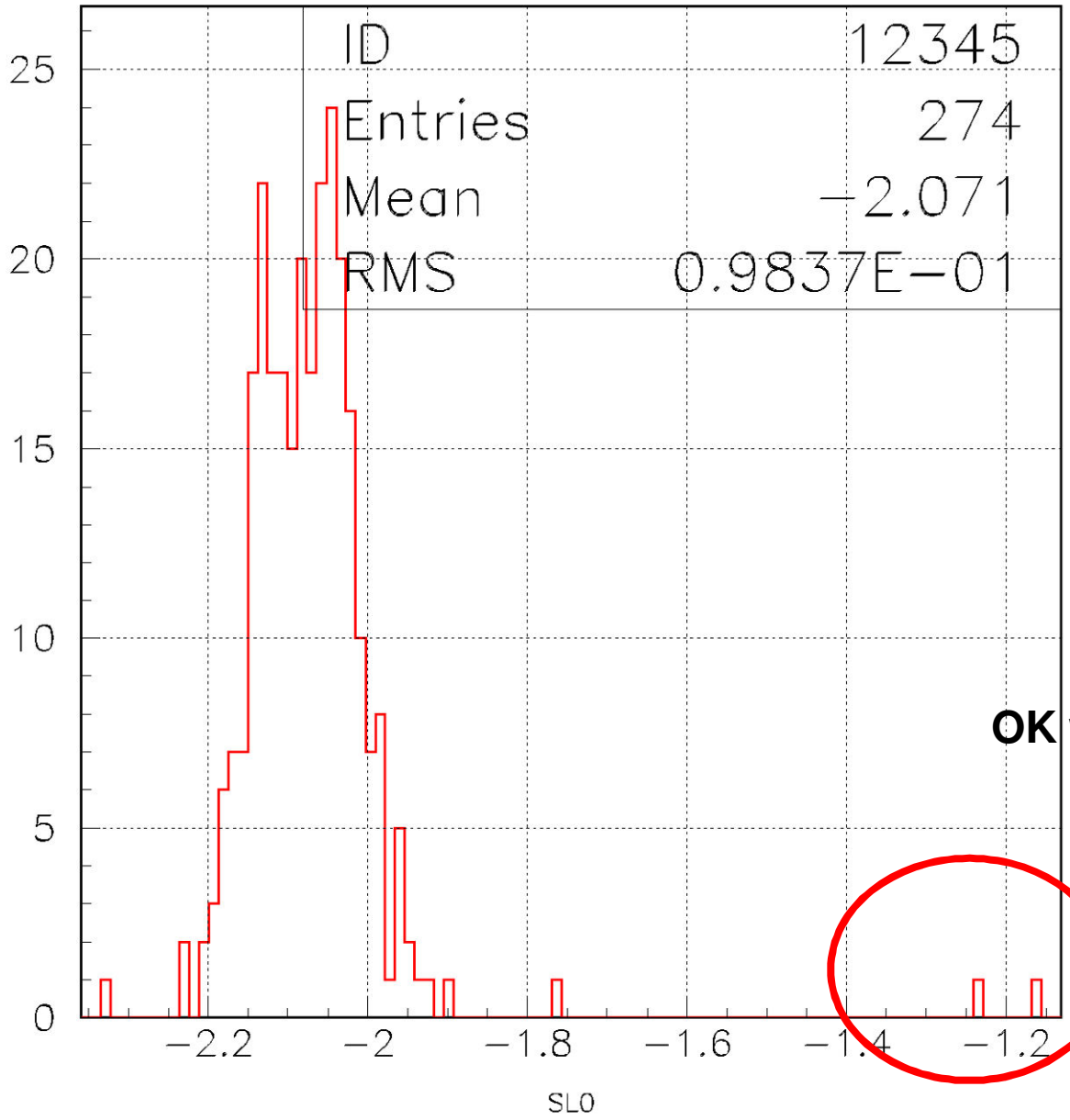


# VBG



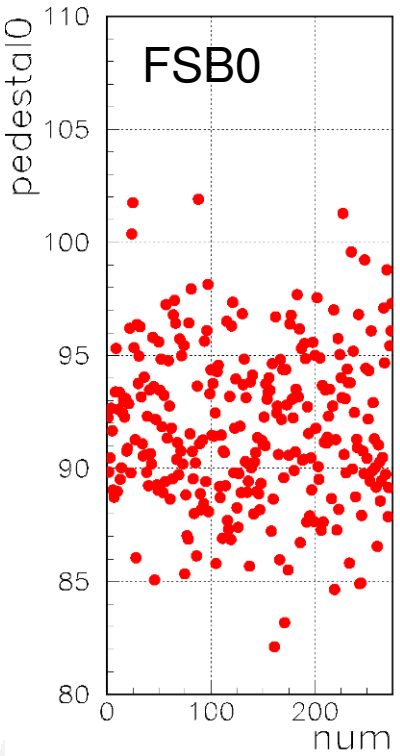

**Rms=34 mV**
**Offset to be improved**

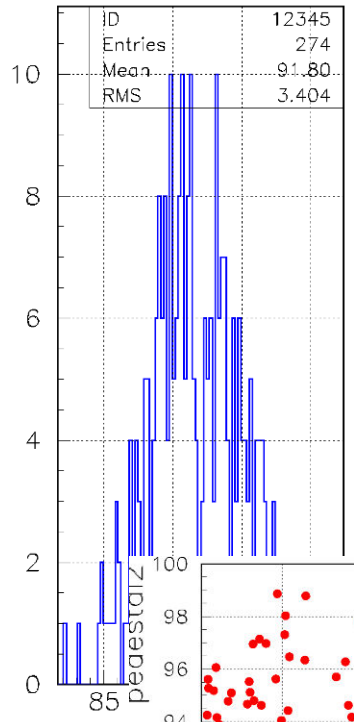
# DAC0 slope

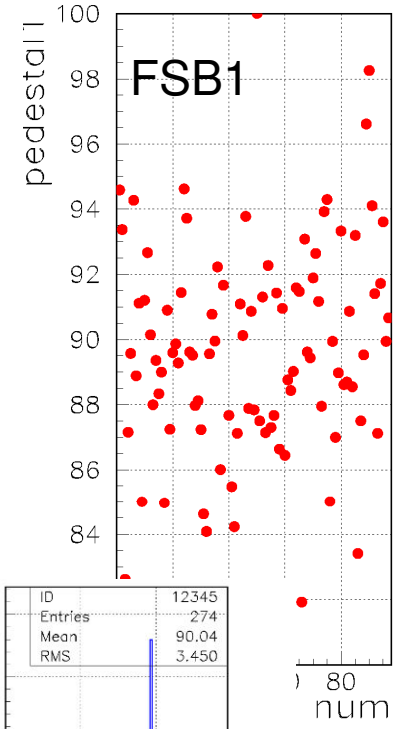


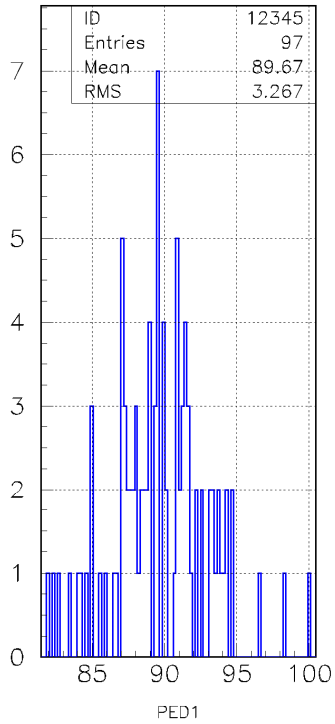

**OK when redone**

# FSB0,1,2 PEDESTALS dispersion between chips

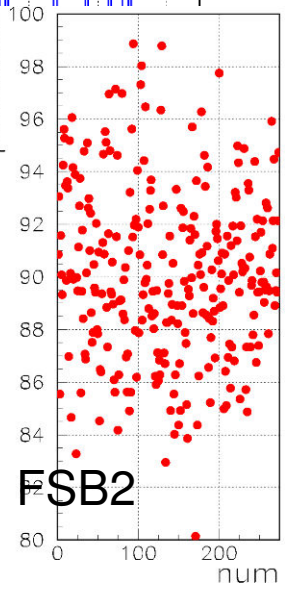


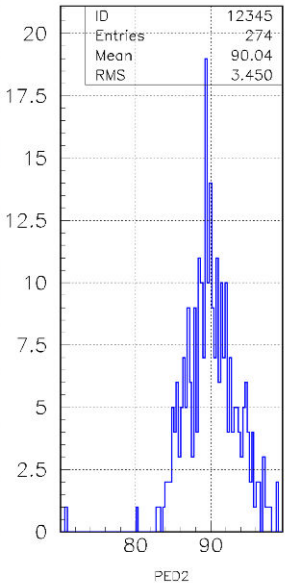



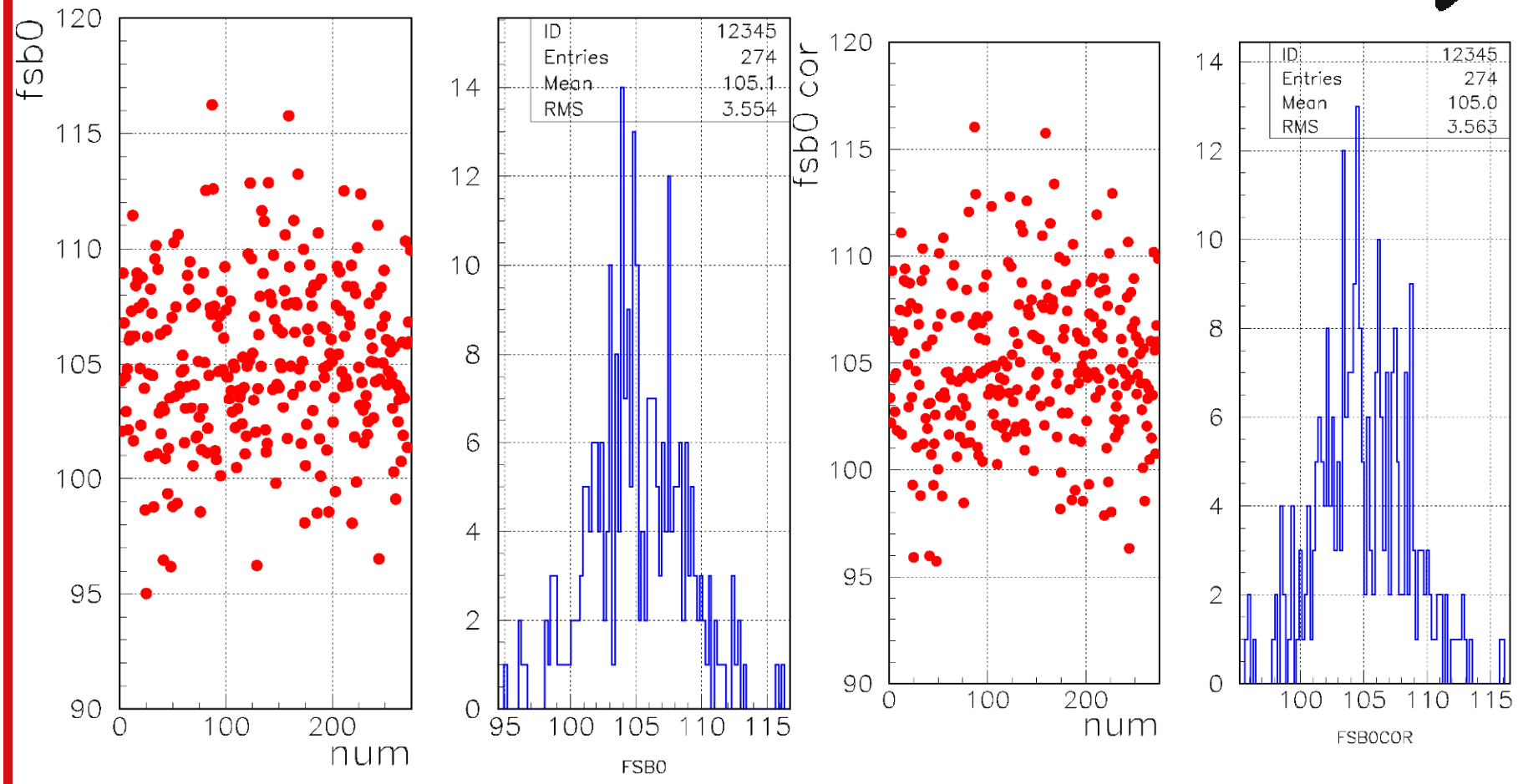




**Mean=90, rms=3**



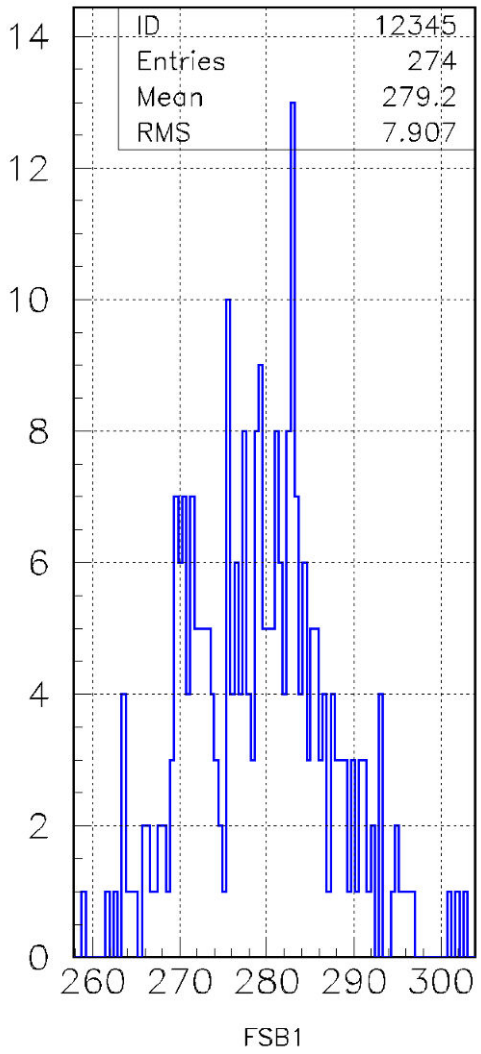



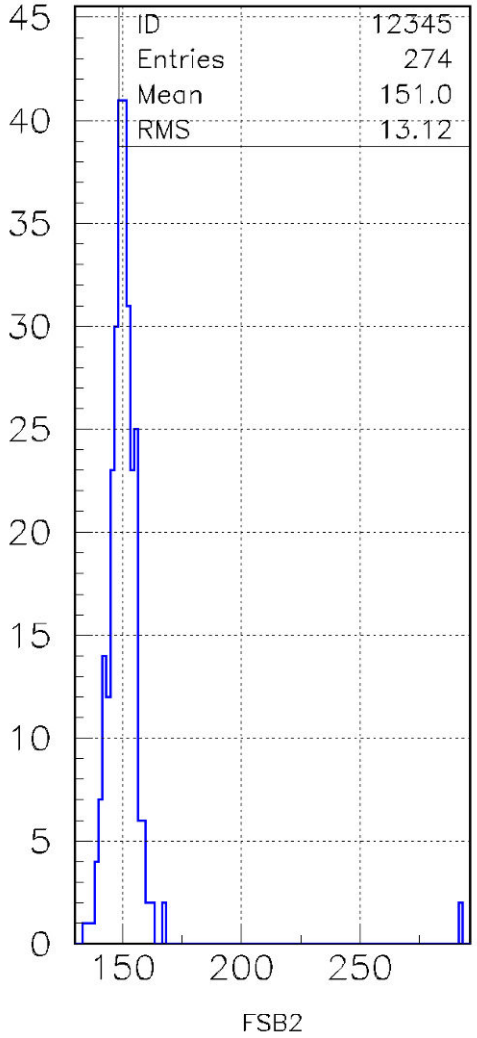
# FSB0: before and after gain cor




pedestal substracted

# FSB1 and 2 (pedestal subtracted)



# CONCLUSION

- 274 chips tested: Yield=90%
  - SC loading pb (Gain=170) => about 40% of the chips
  - 3: memory pb
  - 3: scurves pb
  - 4: minor pb (std slightly too high, pb of pins…)
- Hardroc2b submitted mid June for a medical application, minor modifications
  - Pinout UNCHANGED
  - Bandgap: offset minimised
  - Read/SC selection bug corrected
  - SC control register: buffers added on the Clk
  - Reception: in September => measurements before production submission
- Production foreseen end 2009/beginning 2010 for technological prototypes