

Omega

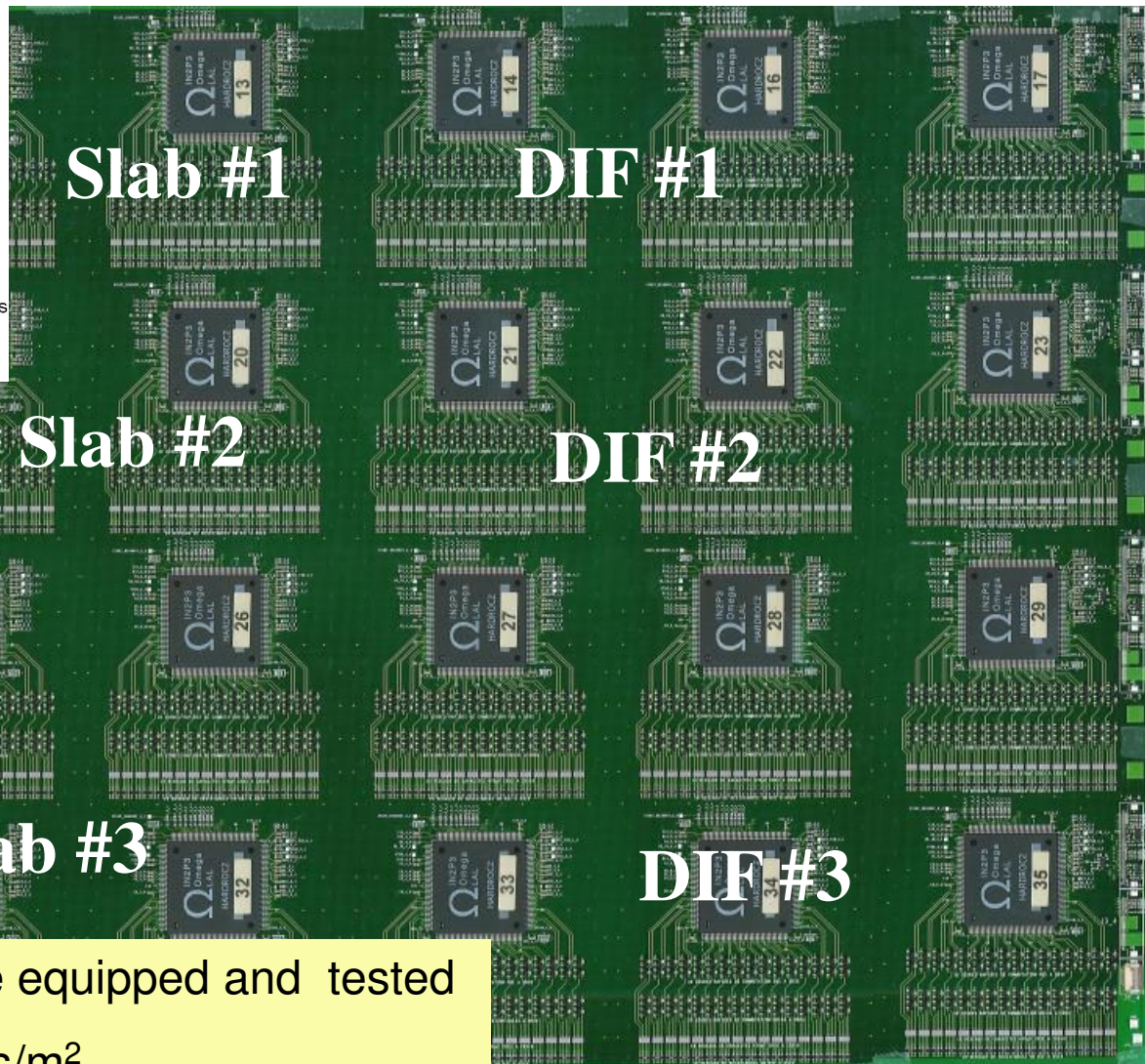
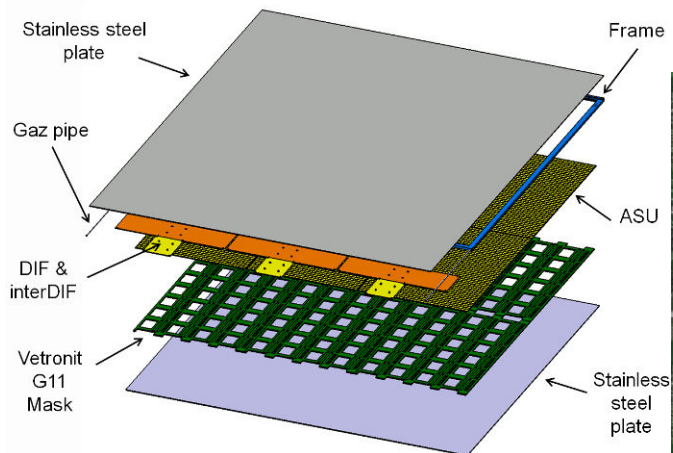
HARDROC2: Statistical measurements

<http://omega.in2p3.fr/>

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Orsay MicroElectronic Group Associated

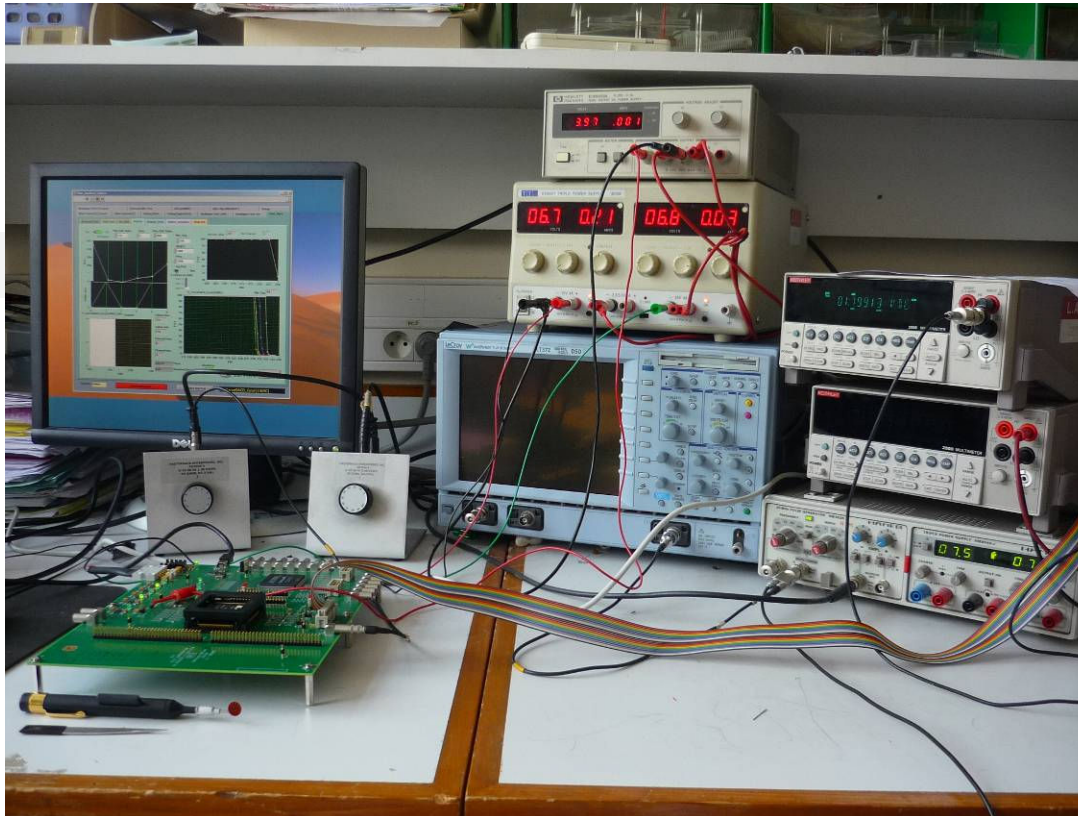


PC

1m² scalable detector to be equipped and tested

144 chips/m²

- 400 chips to be tested to equip 1m² RPC and μ megas detectors
- \approx 300 chips tested this summer in ORSAY and in Lyon
- Good exercise before tests of productions (5000 chips)





Analogue Test : S-curveExternal ADC Testinfo pcb0807info chip HARDROC2SetupSlow Control (1), ReadSlow Control (2)Debug FPGADebug Digital ASICAnalogue Test : DACAnalogue Test : DCTest_Auto

Protocol TestFirst TestLin_DACScurveResum_TestRelect_measureANALYSE

Name ChipHardr62Path TestAutoC:\Documents and Settings\seguin\Bureau\Hardroc2_final\mesures\Name StatStat_h2.xls

Conso before load SCConso after load SCV_BGDC_FSBDC_SSTest_SlowControlNbr_testVal_GainRate[ms]

DAC Mesures

DAC0DAC1DAC2Memory

Scurve

FreqNbr_Trig 2G_refGéné_AutoBurst

Ped_FSB0Ped_FSB1Ped_FSB2

Start_DacFSB0Start_DacFSB1Start_DacFSB2

Qinj[C]FSB0_GcorFSB1_GcorFSB2_Gcor

Conso before load SC[mA]Conso after load SC[mA]V_BG[V]DC_FSB[V]DC_SS[V]MAX[V]MIN[V]SlopeDACCut_Lin_DAC

CUT

+/-[%]

	MAX	MIN	MEAN	DEV
Ped_FSB0	98	86	93	1,5
Ped_FSB1	88	81	85	1,5
Ped_FSB2	95	86	92	1,5
FSB0	220	180	200	9
FSB0_Gcor	220	180	200	4
FSB1	430	330	370	17
FSB2	280	210	240	13
FSB1_Gcor	0	0	0	0
FSB2_Gcor	0	0	0	0

VALID ALLREMOVE ALLSTART TEST

Nbr_TestNbr_Test_i

CALICE meeting, IPN Lyon

HARDROC2 measurements

4

- DC levels, power consumption, VBG, memory test, SC test with a « difficult config »

Protocol Test

First Test

Lin_DAC

Scurve

Resum_Test

Relect_measure

ANALYSE

Conso before[mA]

VALID

DC_FSB[V] 2

VALID

V_BG[V] 2

VALID

Conso before load SC

17,84537

DC_FSB

3,23878

V_BG

2,47070

Conso after[mA]

VALID

DC_SS[V] 2

VALID

Conso after load SC

30,28721

DC_SS

3,23221

Test Slow Control

Succed[%]

NumTest

VALID

0

10

Test memory

VALID

Trig

CONFIG SLOW CONTROL

RESULT MEMORY

DAC0:300,DAC1:1023,DAC2:1023
SS Gain:15,FSB1 Gain:8,FSB2 Gain:8
Trigger_write0:On,Trigger_write1:Off,Trigger_write2:Off
All Channel Cap. Enabled
All Channel Discriminator Active

Trig0:0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,
20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,
38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,
56,57,58,59,60,61,62,63
Trig1:Trig2:

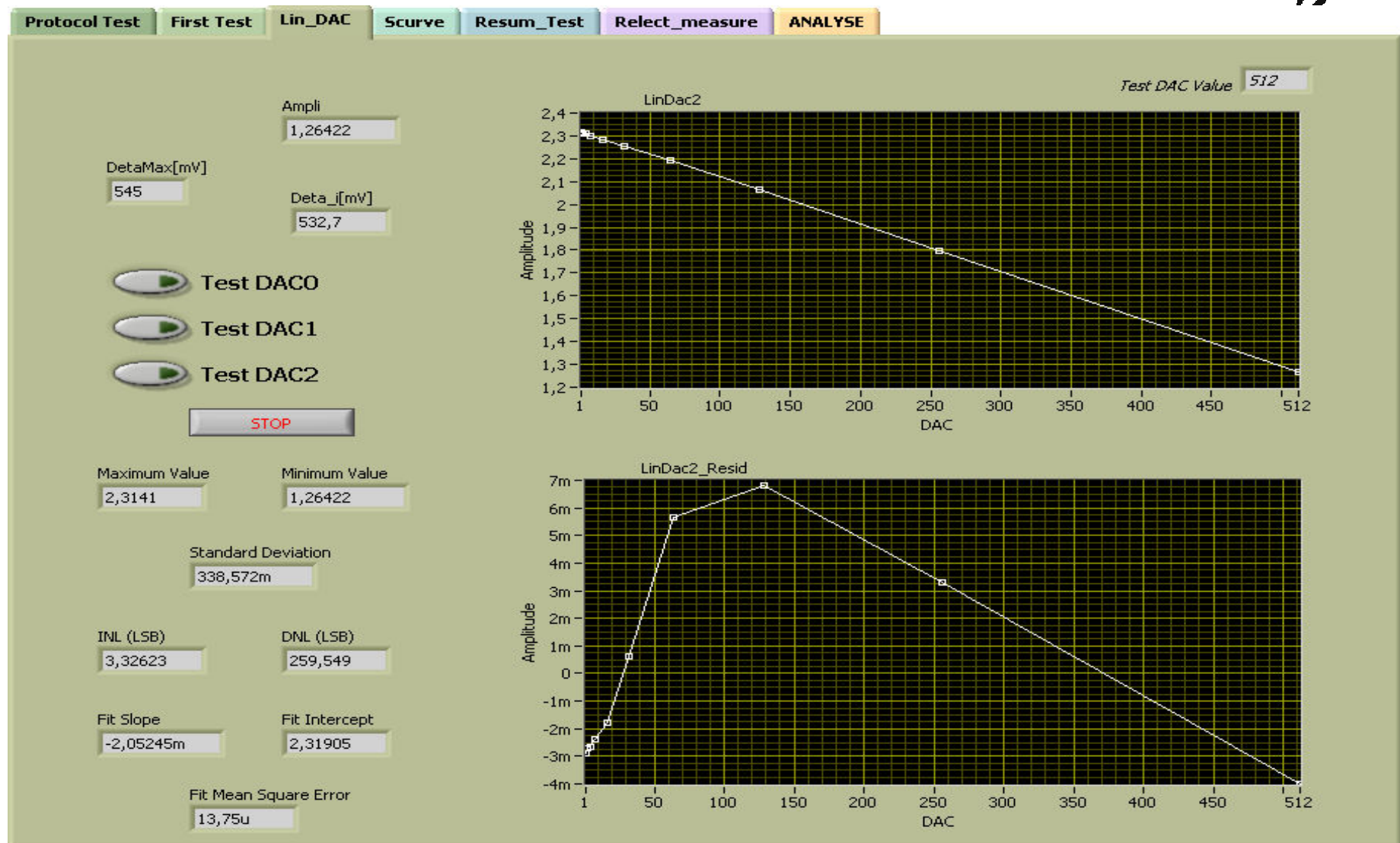
DAC0:1023,DAC1:200,DAC2:1023
SS Gain:15,FSB1 Gain:8,FSB2 Gain:8
Trigger_write0:Off,Trigger_write1:On,Trigger_write2:Off
All Channel Cap. Enabled
All Channel Discriminator Active

Trig0:Trig1:0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,
18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,
36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,
54,55,56,57,58,59,60,61,62,63
Trig2:

DAC0:1023,DAC1:1023,DAC2:200
SS Gain:15,FSB1 Gain:8,FSB2 Gain:8
Trigger_write0:Off,Trigger_write1:Off,Trigger_write2:On
All Channel Cap. Enabled
All Channel Discriminator Active

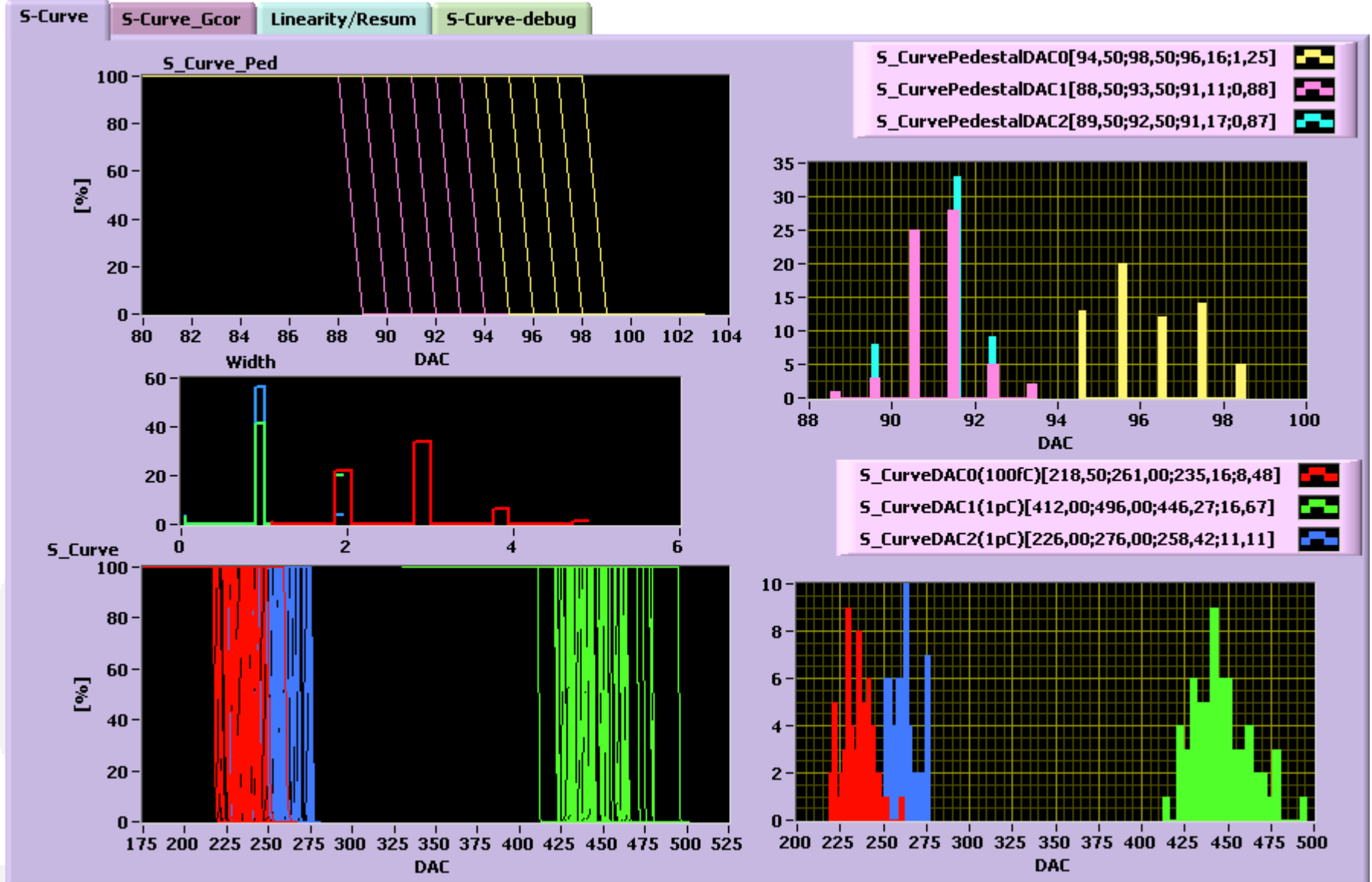
Trig0:Trig1:Trig2:0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,
16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,
34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,
52,53,54,55,56,57,58,59,60,61,62,63

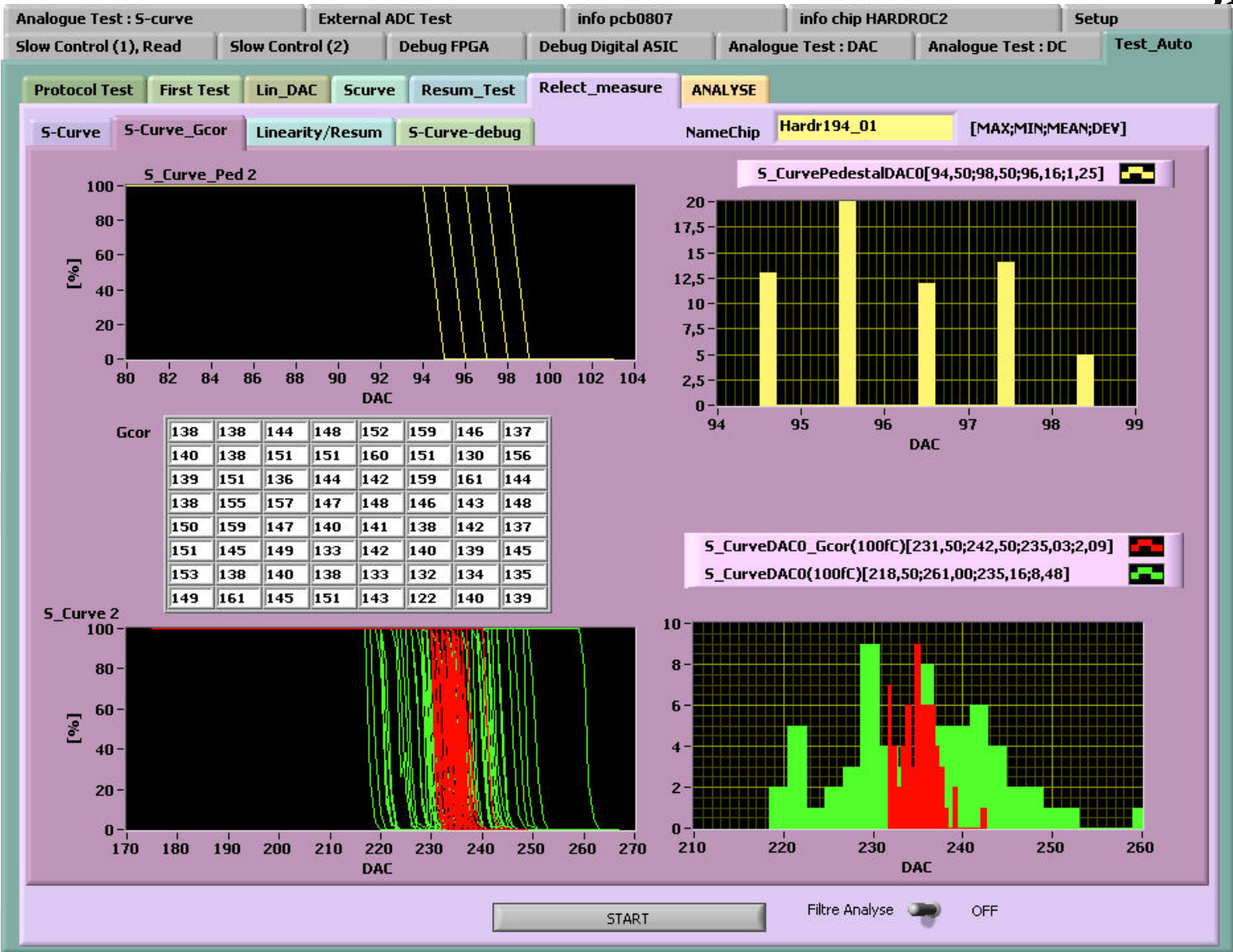
3 DACs linearity

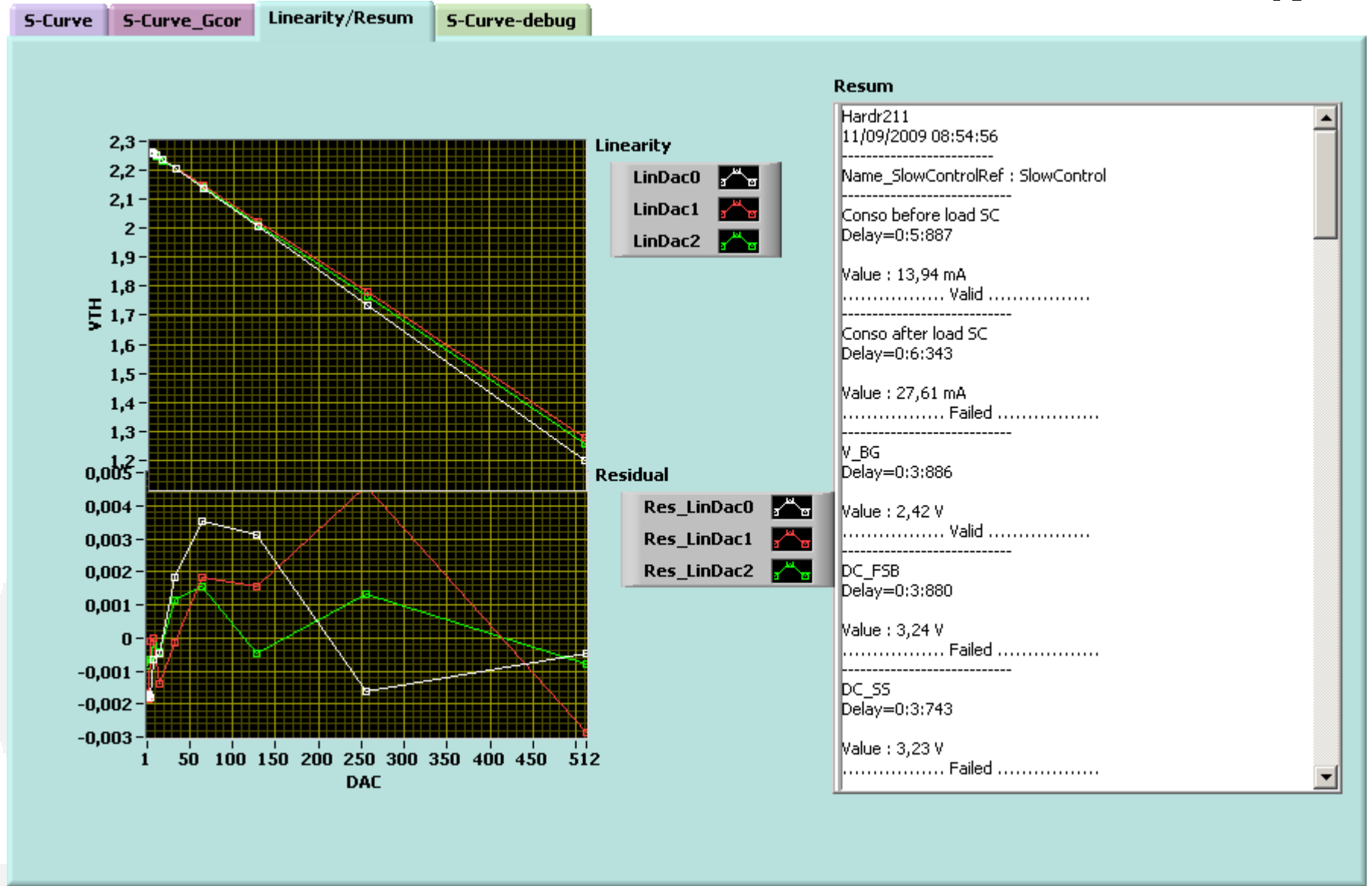


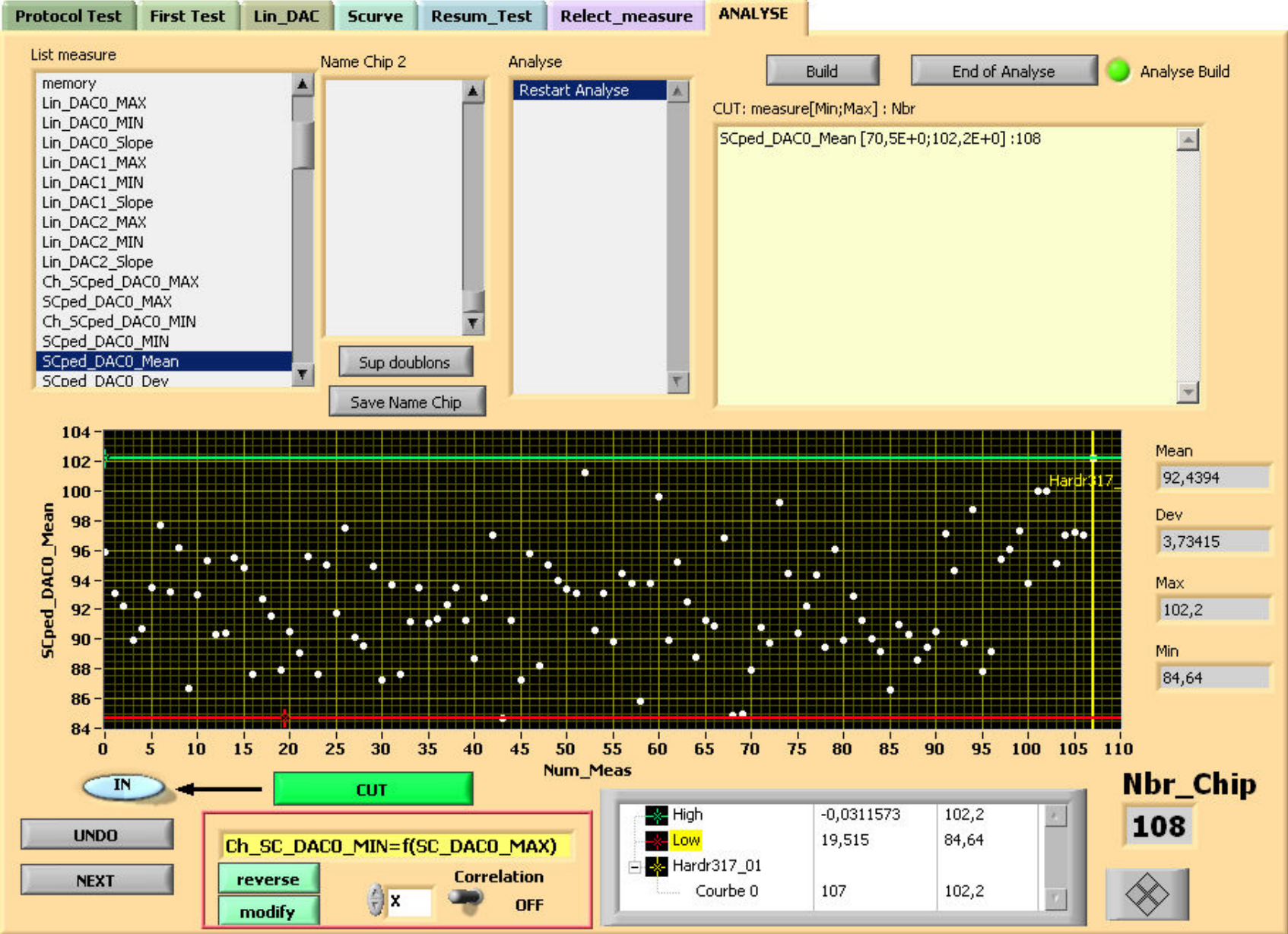
SC measurements: pedestal, 100fC, 1pC

Omega

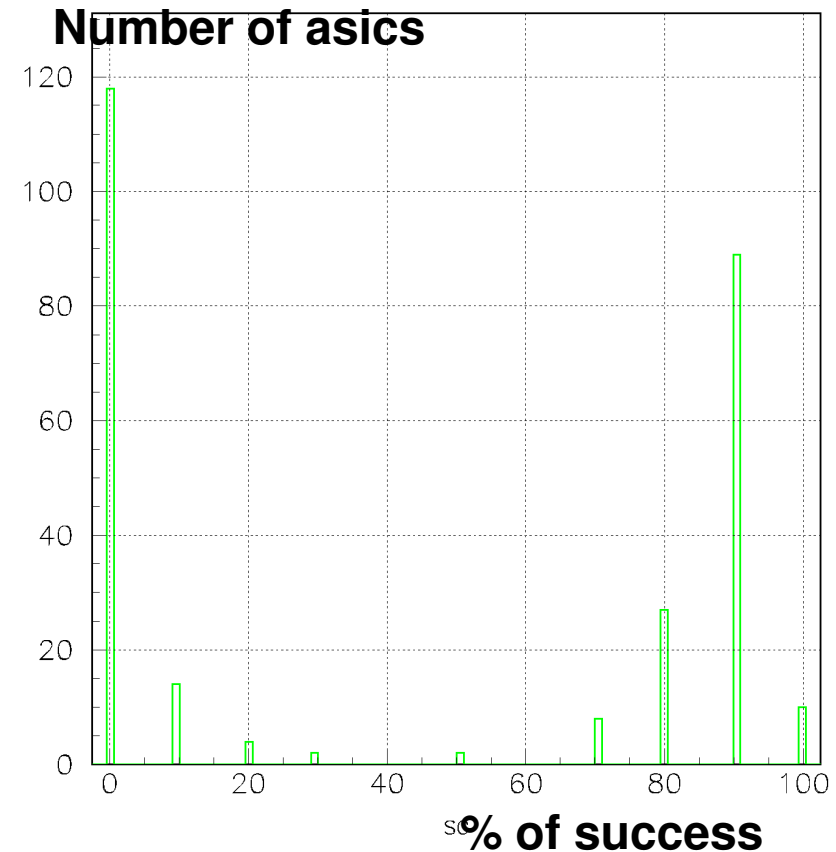


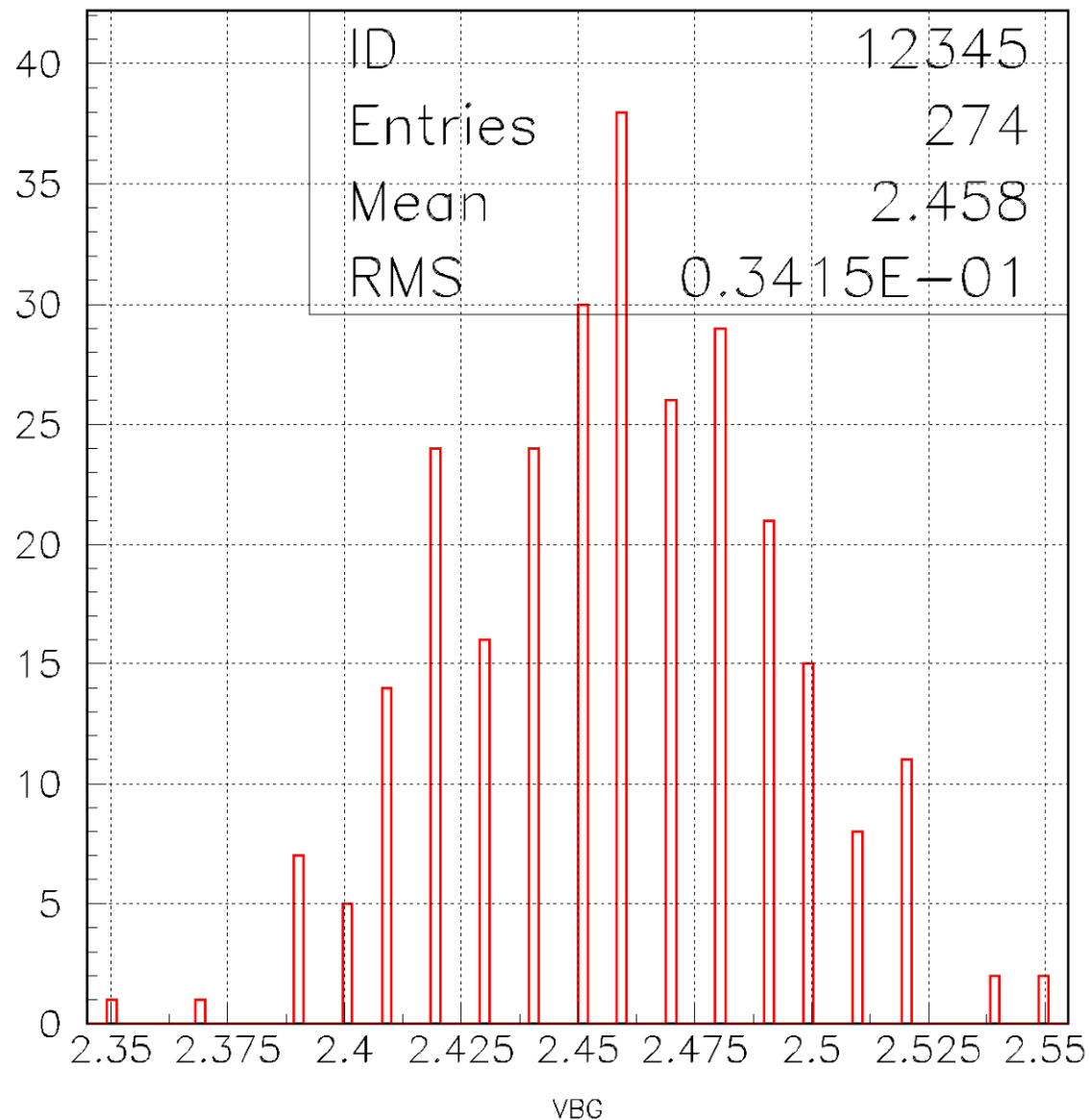




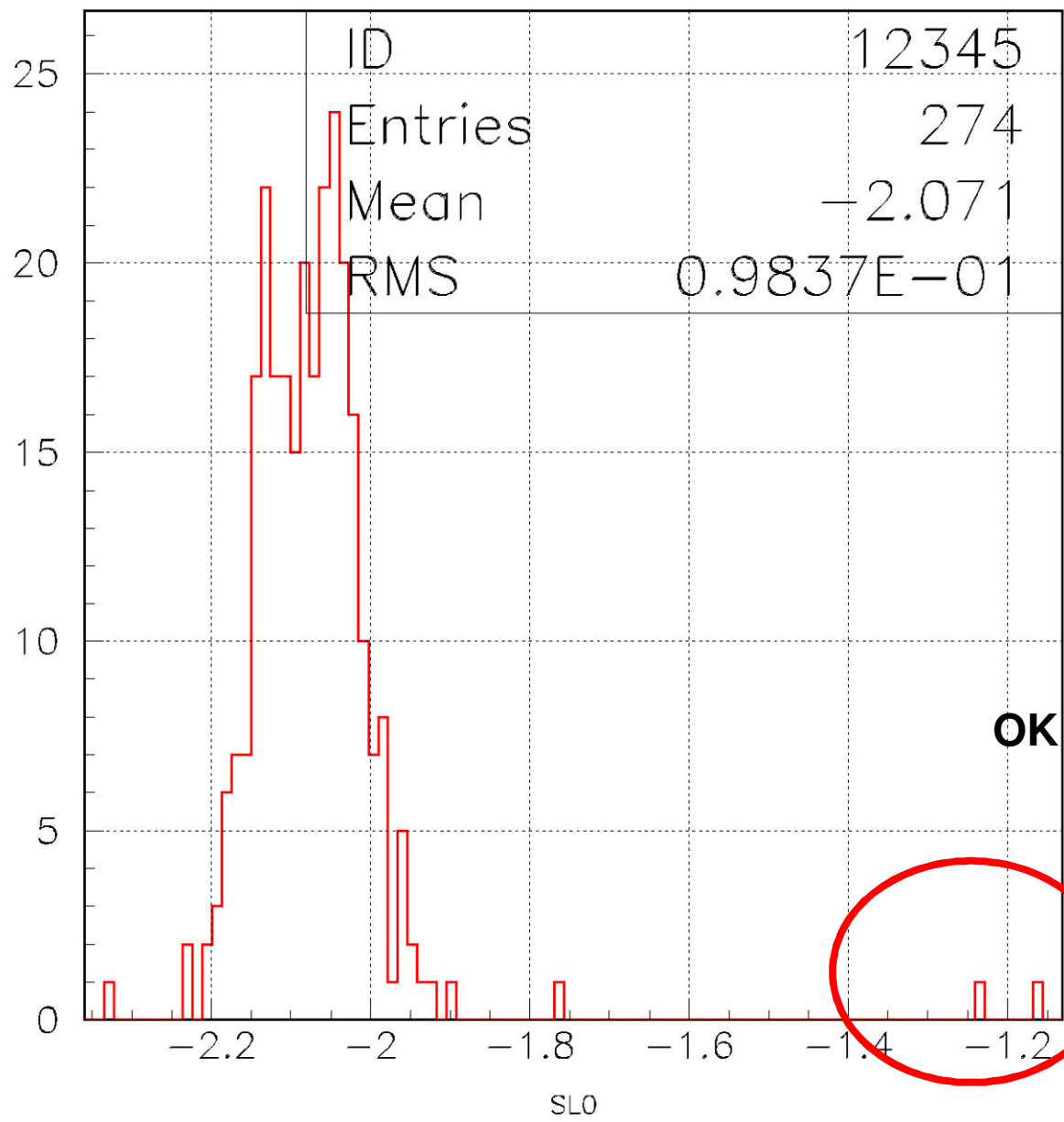


- Some gain configurations are sometimes difficult to load in hardroc2
 - Due to long connections between flip flops inside the chips: can be corrected with additional buffers on clk and data signals
 - **necessity to increase digital vdd to 4V.**
- But still, $\approx 50\%$ of the chips exhibit pb with the loading of « difficult » SC config.
 - Gain=170 = 10101010 loaded 10 times, calculation of the ratio of success.
 - **Anyway 90% of the chips OK for the other tests performed with various SC configs have to be loaded**



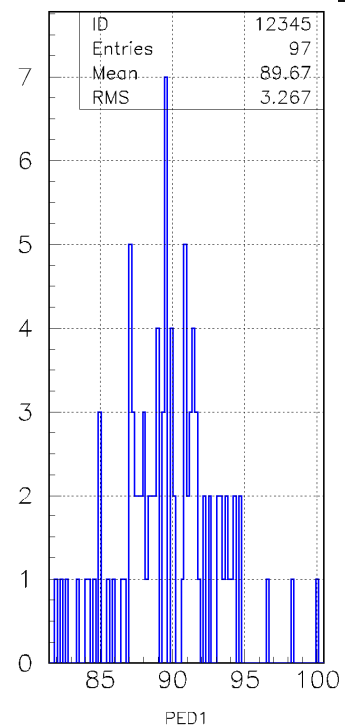
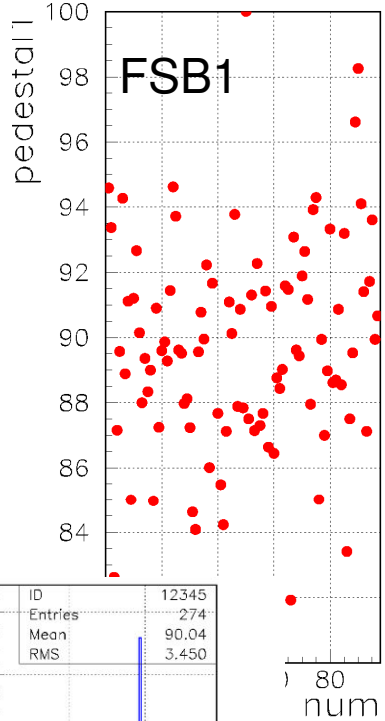
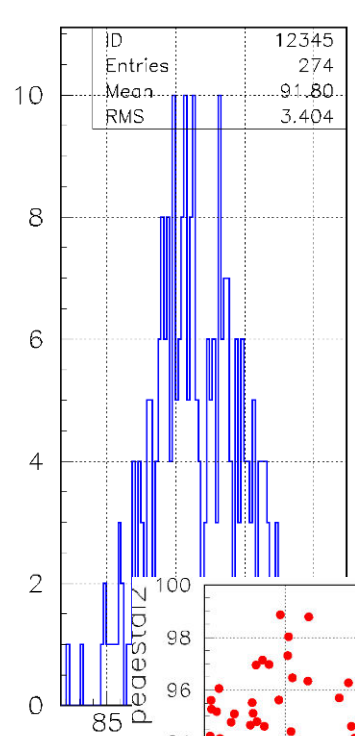
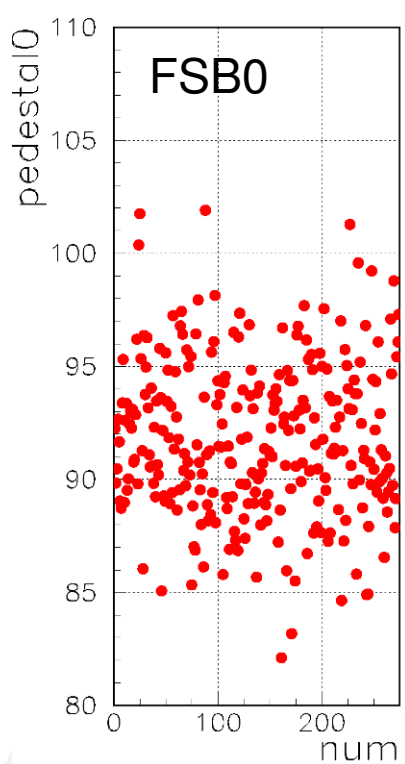


Rms=34 mV
Offset to be improved

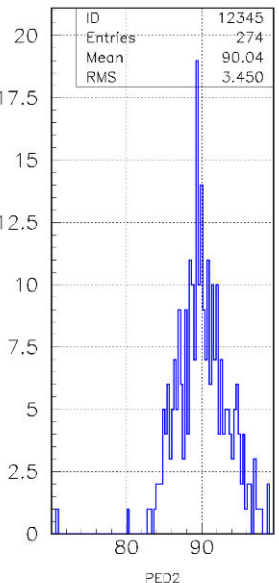
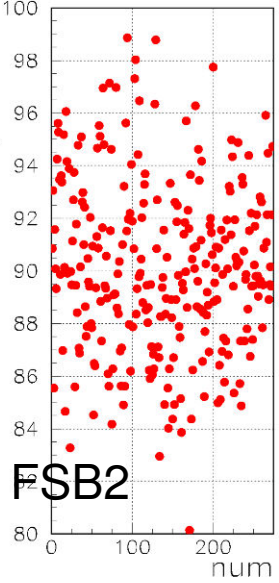


OK when redone

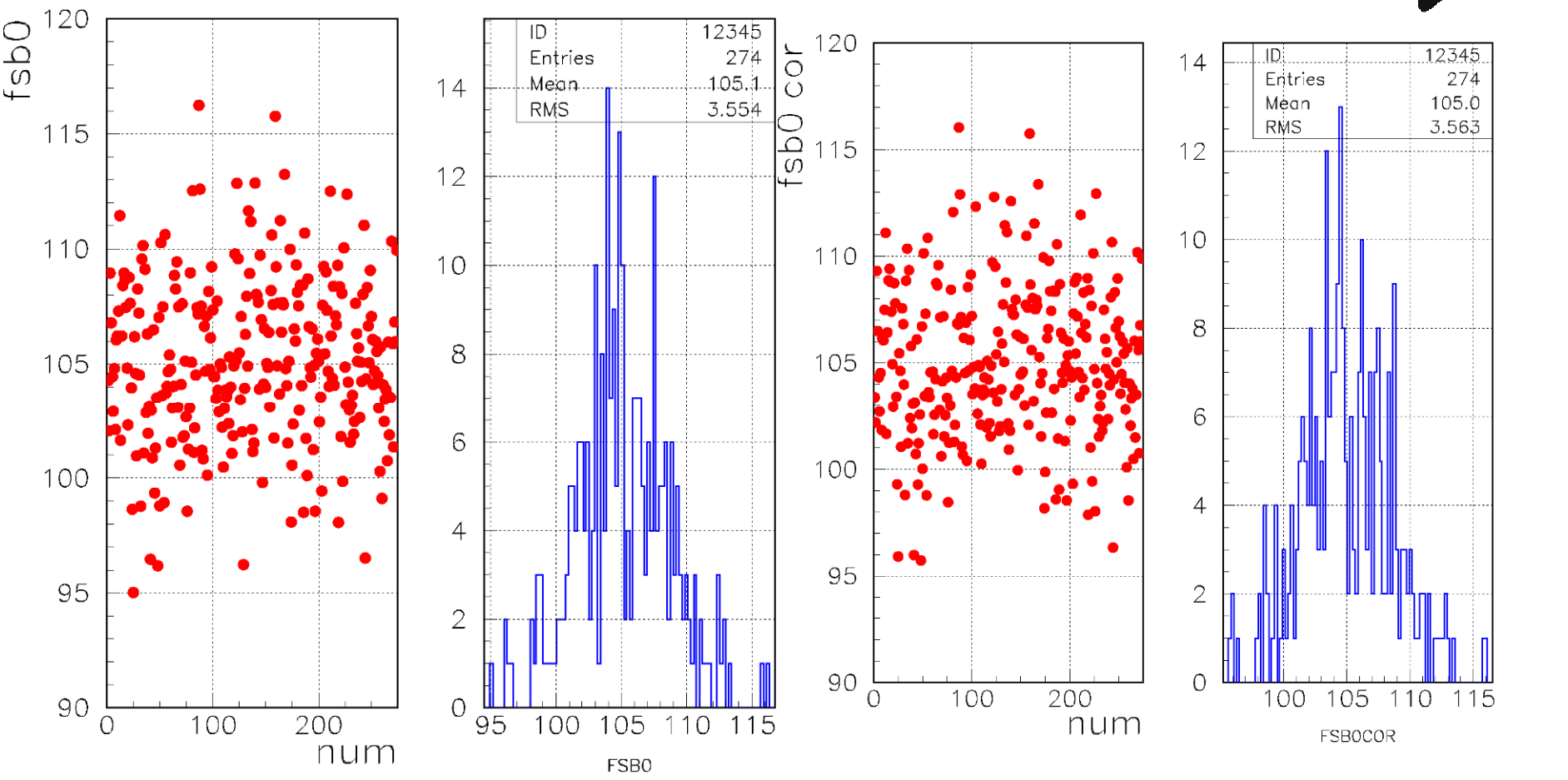
FSB0,1,2 PEDESTALS dispersion between chips



Mean=90, rms=3

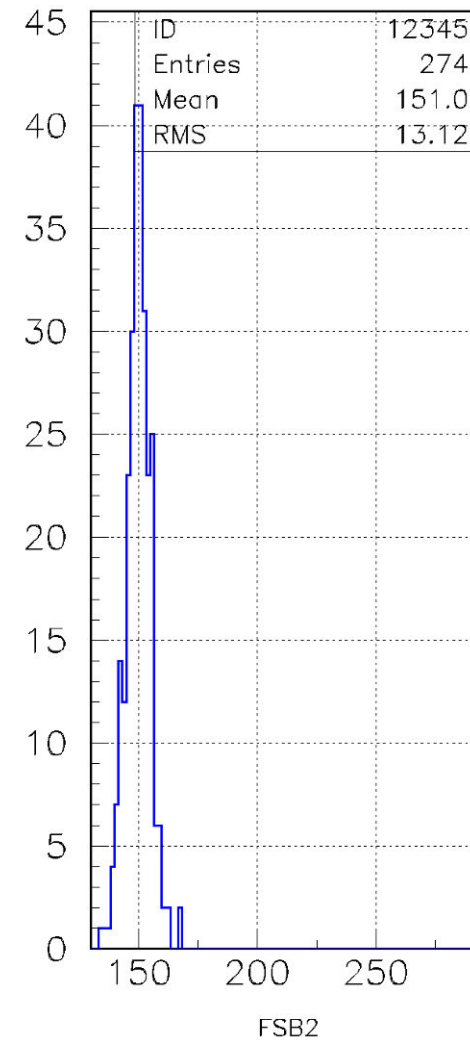
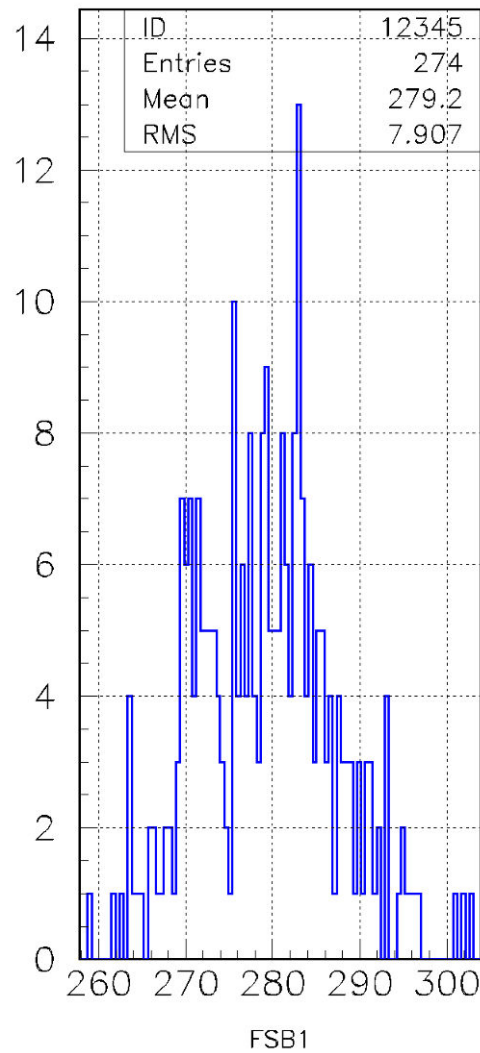


FSB0: before and after gain cor



pedestal substracted

FSB1 and 2 (pedestal subtracted)



- 274 chips tested: Yield=90%
 - SC loading pb (Gain=170) => about 40% of the chips
 - 3: memory pb
 - 3: scurves pb
 - 4: minor pb (std slightly too high, pb of pins...)
- Hardroc2b submitted mid June for a medical application, minor modifications
 - Pinout UNCHANGED
 - Bandgap: offset minimised
 - Read/SC selection bug corrected
 - SC control register: buffers added on the Clk
 - Reception: in September => measurements before production submission
- Production foreseen end 2009/beginning 2010 for technological prototypes