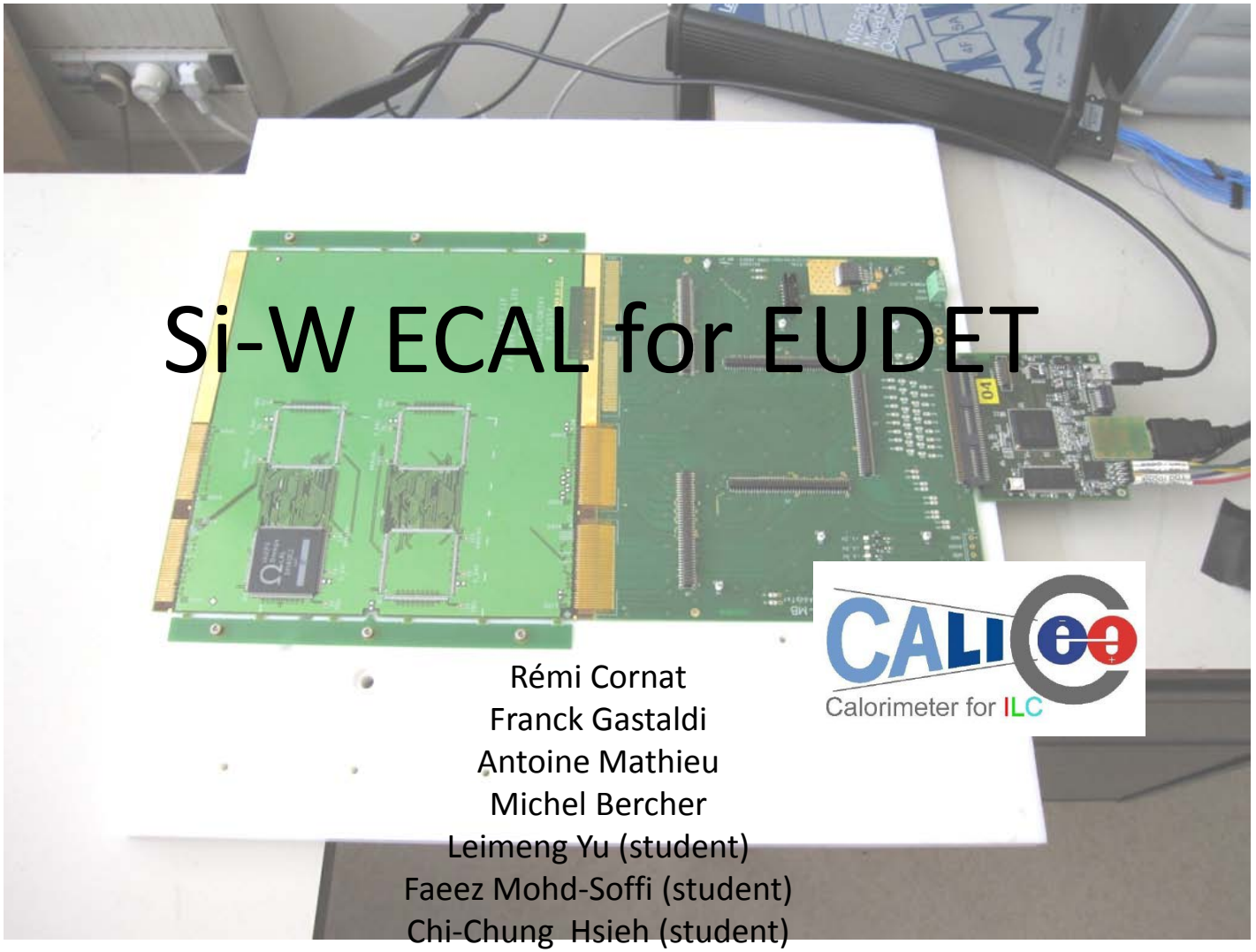

Si-W ECAL for EUDET

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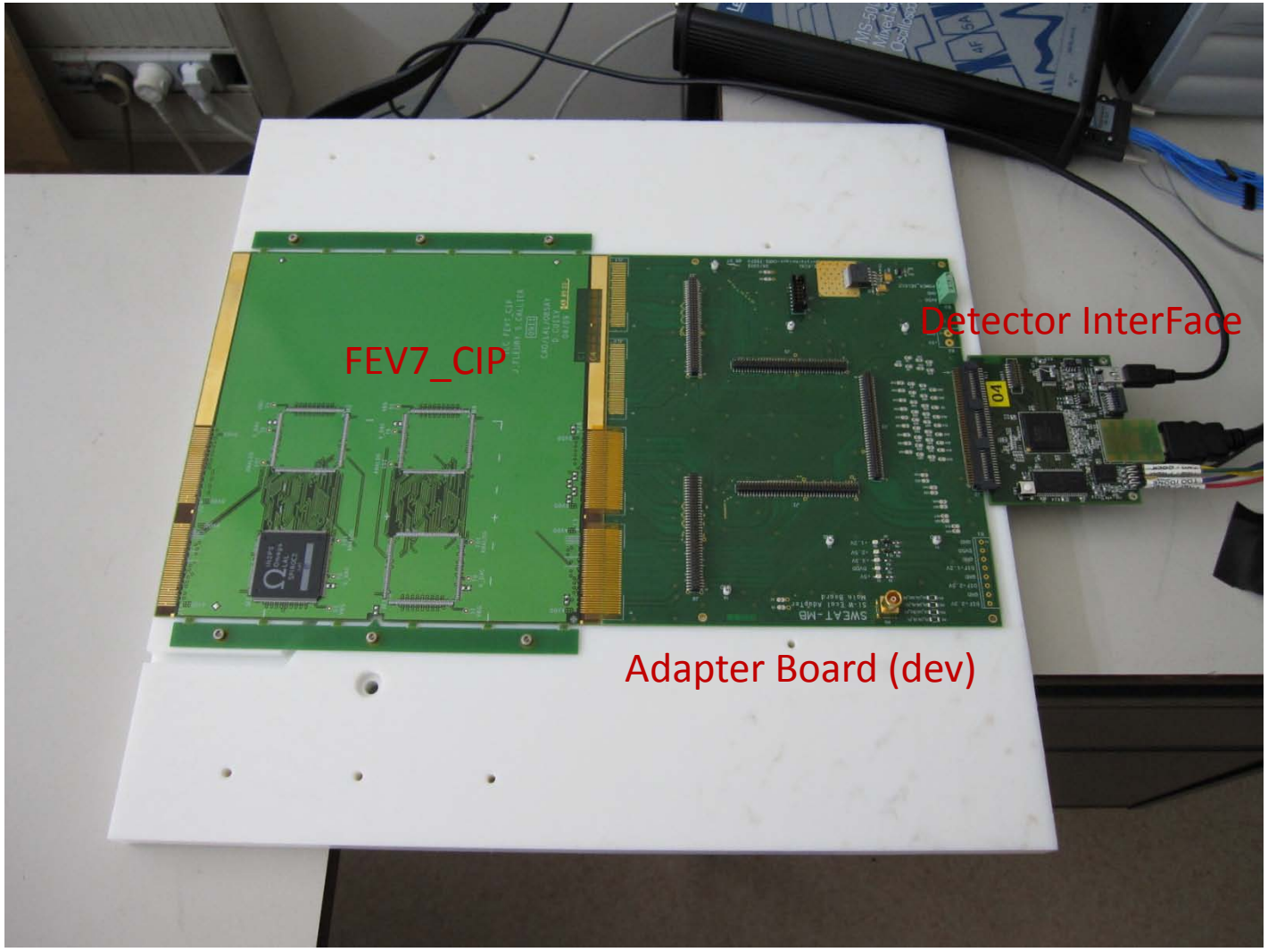
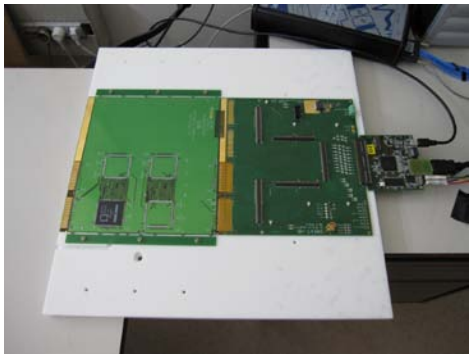
Antoine Mathieu
Michel Bercher
Leimeng Yu (student)
Faeez Mohd-Soffi (student)
Chi-Chung Hsieh (student)

First SLAB prototype assembled (03/07/09)



ECAL : First SLAB prototype assembled (03/07/09)

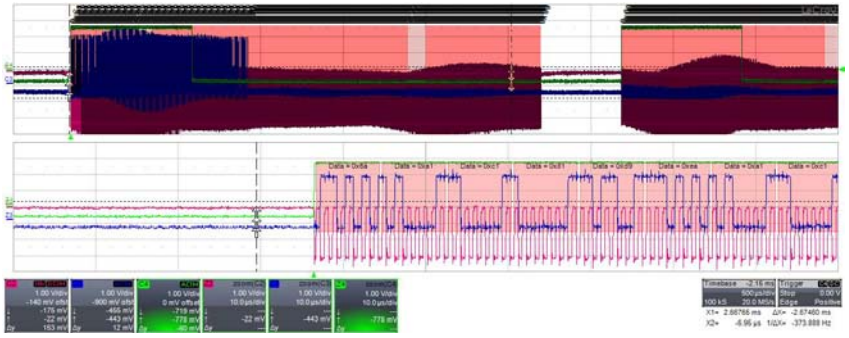


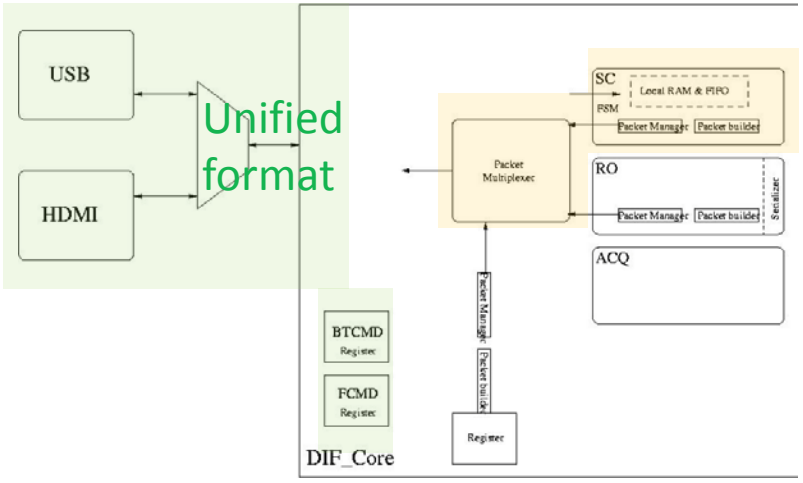
- Basic firmware for the DIF is developed
- 50 MHz
- Multiplexed HDMI/USB
  - USB tested over few millions 256 B transfers
  - Unique interface inside DIF
- Hardware tests have started by the end of August
  - FCMD
  - BTCMD
  - Slow control (unstable)

  } From HDMI
- Connection to SPIROC2 should be effective within 2 weeks

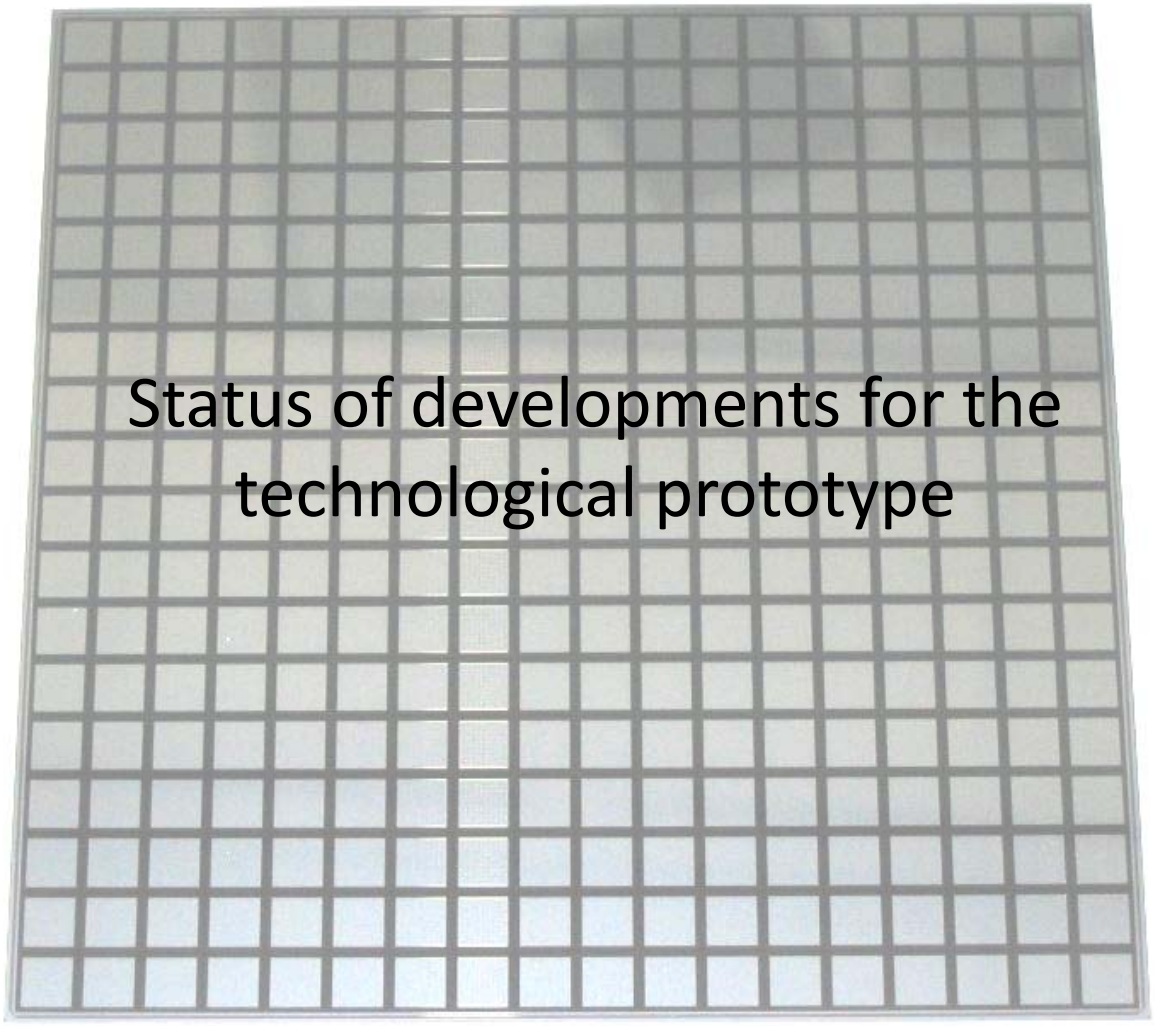
- Slow control interface to the ROCs
- Packet formatter and packet multiplexer

are being tested





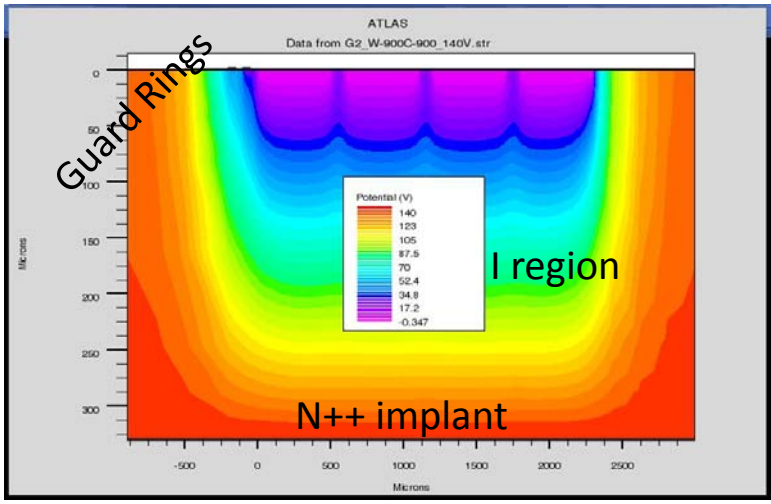
Silicon Sensors



Si design

- The simplest design to control the cost
  - Few thousands of m² needed for ILD
  - Minimize the number of steps of the processing procedure
  - Guard rings = same as pixels
  - Glued on PCB : Floating GR
- Drawbacks : lack of optimization
  - Large dead zone at the edges
  - Crosstalk (Square Events)
- But…cost is still too high
  - 70 keur (including NRE) for 40 pcs of this hamamatsu prototype = 22 € / cm2 (14 w/o NRE)
  - Cost estimate for ILD : ~2 € /cm²

P++ implants (pixels)



9x9 cm², 324 pixels

Si overview

- Experience with Czech, Russian and Korean sensors on the physics prototype
  - 500 nm, 6x6 cm², 36 pads
  - Square events : understood to come from guard rings
  - Dead area at the edges
- Search for new design techniques
  - Reducing crosstalk due to the GR
    - Segmented guard rings to avoid square events
  - Lowering Dead space (at the border)

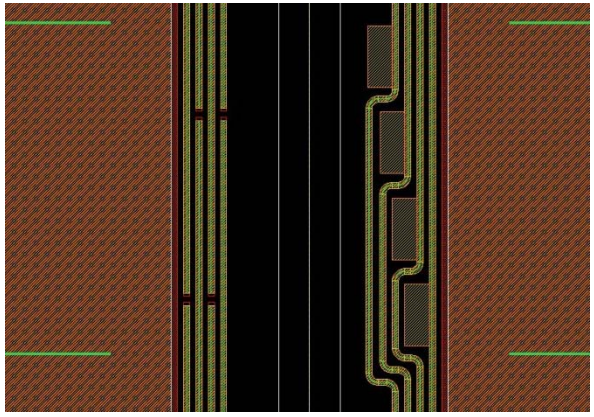
NEW : Prototypes are measured !

- Improved design for the technological prototype (& particle flow physics)
  - Hamamatsu design: 300 nm, 9x9 cm², 256 pads
  - Have guard rings ! External charge injection shows square events…
  - Large dead space
  - Behavior with glue checked over 8 months : OK
  - Cost of prototypes: 70 k€ = 40 wafers(EUDET needs 160)

NEW : Production batch received at LLR!

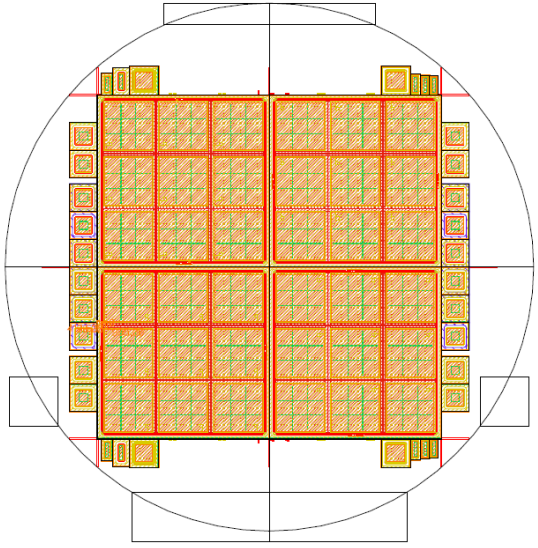
Segmented guard ring

- Should avoid the signal propagation along the border of the wafer



- Idea tested thanks to PCBs and test bench at LPC (CALOR'08, NSS'08 talks)
  - Segmented topology helps to prevent SqEvt (factor 50 on signal intensity)
  - What about current leakage & breakdown ?

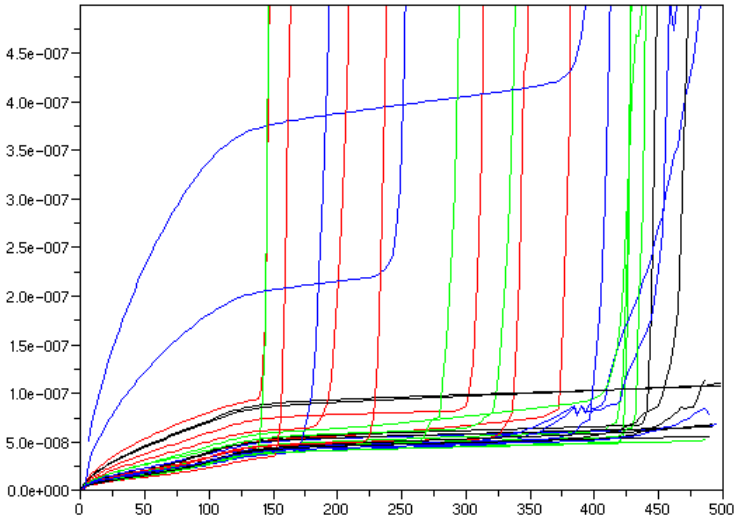
- Prototype wafers have been manufactured (LLR made layout)
  - OnSemi/Institute of Physics (Prague), Cz
  - BhaBha Atomic Research Centre, India
  - Tests are ongoing



NEW : Prototypes received at BARC !

R&D on segmented guard rings

I(V)

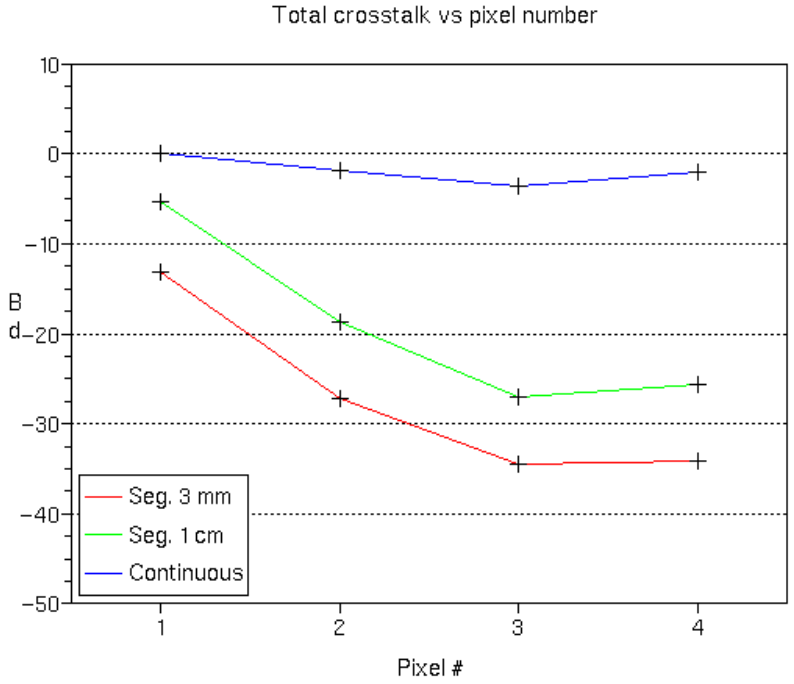


Yield (Breakdown >250V)

- Continuous: 100%
- 1 cm: 85%
- 3 mm: 40%
- Mixed: 70%

Sum of GRs contribution

Xtalk lowered by a factor 80 (with 3 mm segments (measurements made at LPC)



Next R&D prototypes of segmented guard rings

Vary Inter segment gap :
1 cm segment with 5, 10, 25 (actual: 50 um)

Distributed capacitance:
Mixed: inner 2cm, 1 cm , outer 3mm - 1mm

2 conferences
IEEE NSS'09
IEEE Sensors'09

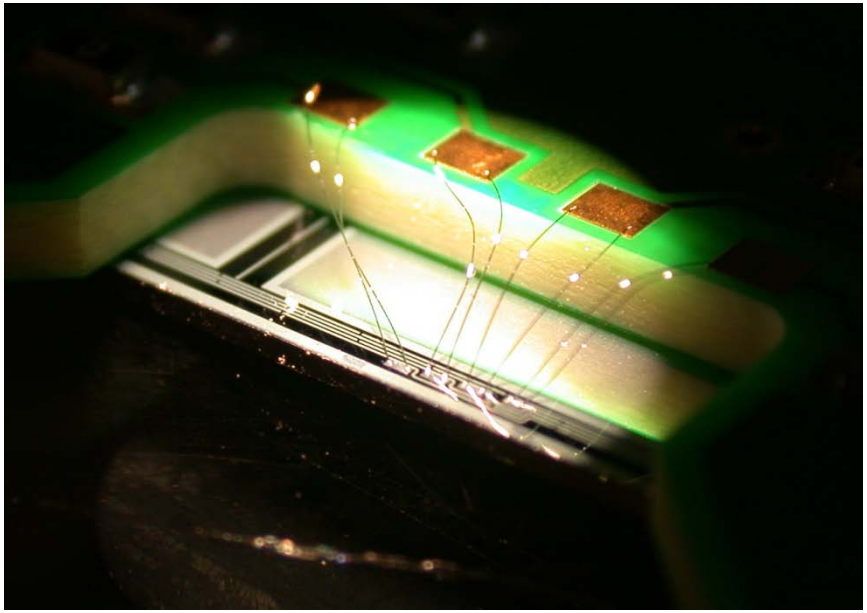
bounding attempt at CERN in order to ease the measurements
But it adds some Xtalk

S1

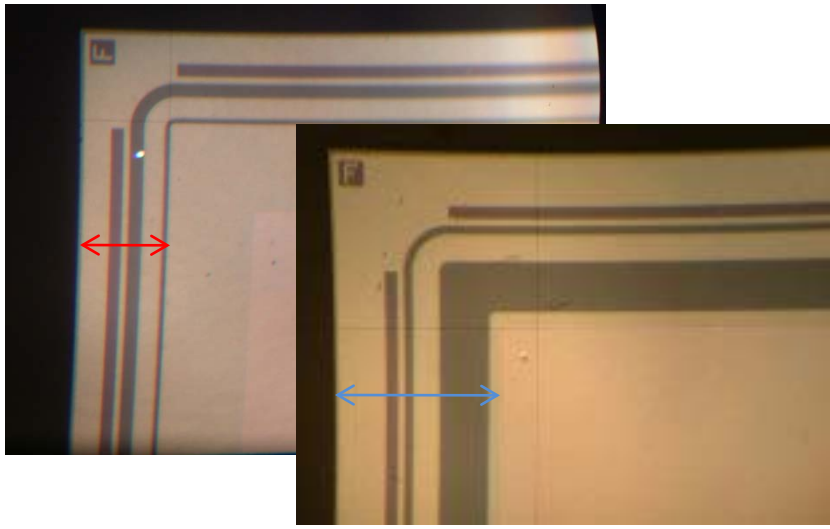
G1 800mV			
	128	29	28
	572	28	30
	59	30	30

S1

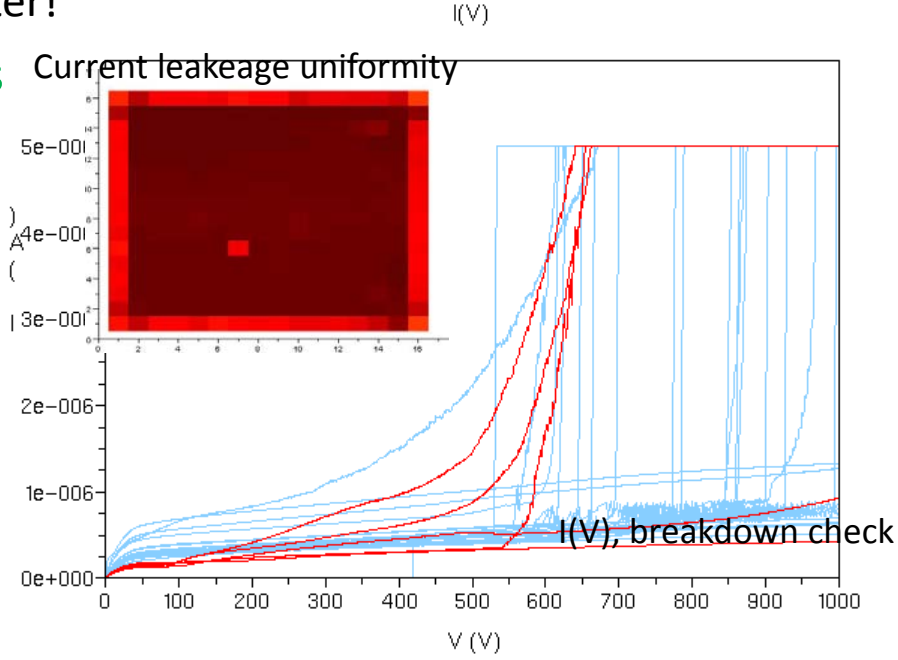
G4 800mV			
	64	67	69
	156	69	68
	216	90	70



Hamamatsu sensor V2

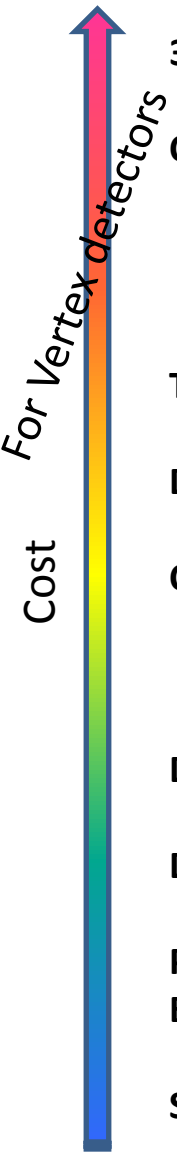


- Dead area decreased to 750 um (1200 µm previous)
- Leakage current issue seen at Hamamatsu
  - Level: x 5-10 wrt previous sensors , bad uniformity
  - They developed a new test setup : better!
- 5 samples + production batch of 35 pcs (received this week)
- Breakdown ok but seems to be slightly lower
- Have 40 sensors to start EUDET SLAB assembly (160 needed)



Silicon Sensors

Some optimizations



3D sensors : lower Vbias, internal current flow, low sensibility to edge effects : can be ~edgeless (100 um)

Cut through edge

same technology as for 3D but used only at the edge
no saw cuts, 3D edges
4-side abuttable ~*no dead space,* Deep trench etch, n doped polysilicon fill provides edge doping

Integration ☹

Trenches + saw cut : cost of trenching, post processing of every sensors, bad control of current.

Dry etching cut

Current terminating ring

two rings but biased : thin contact needed, gluing not applicable
edge width less than ½ wafer thickness

Integration ☹

Double sided GR

Doped edges

Punch-through biasing

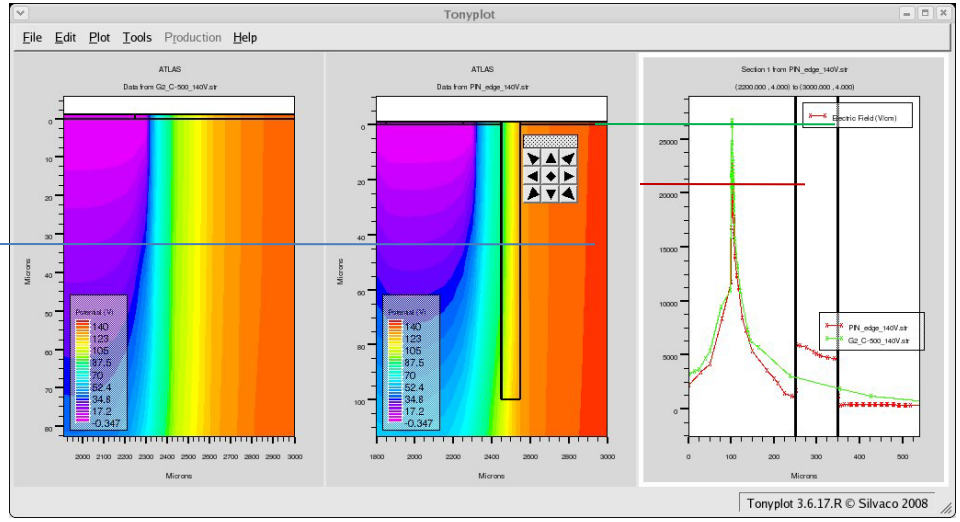
Biased GR Integration ☹

Crosstalk + ~edgeless ☺ (300 um)

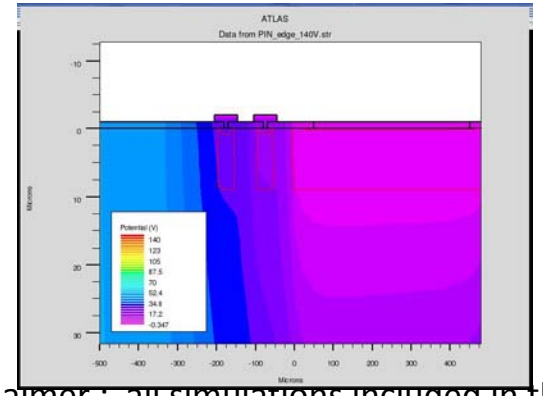
Segmented GR : need further tests

edge ☹ (800 um)

Simulation tools examples

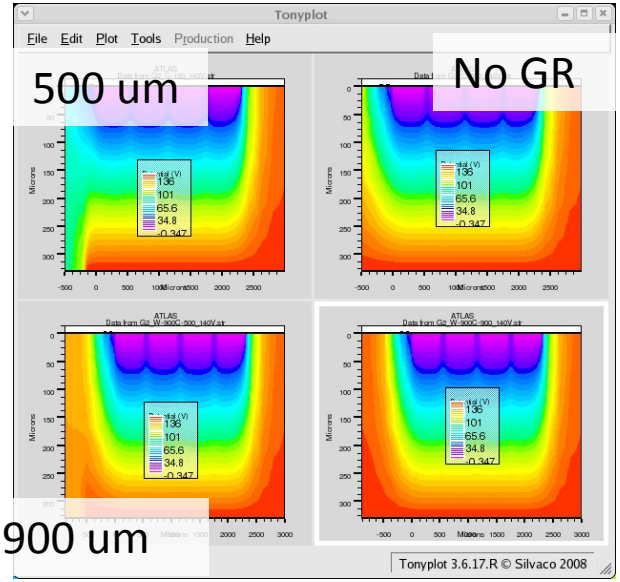


Lower Max E with a trench (red)



100 x 100 um

Double sided GR



Disclaimer : all simulations included in this talk are doubtful, simplistic and wrong

Contributors to the previous prototypes

ON Semiconductor®

HAMAMATSU

МГУ имени М.В.Ломоносова
1755

The cost issue

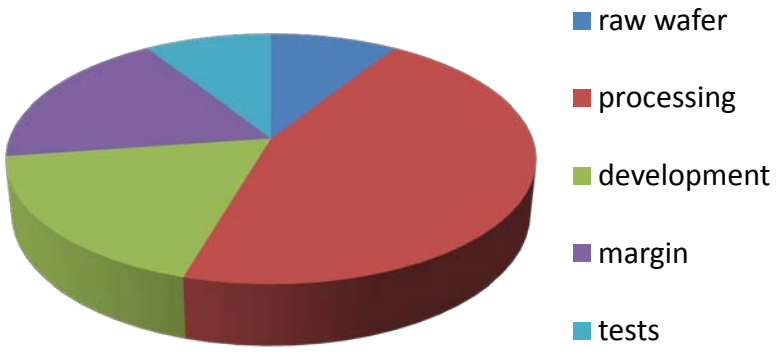
The cost estimate of a financially viable ECAL for ILD assumes this input :

A cost at the level 2 € / cm²

Now we are at the level of 10 to 20 €/cm²

About 2500 m² of sensors needed for SiW ECAL of ILD = 300 000 sensors (actual design)

price ?



What could we do / rely on?

Savings due to the change on scale ?

Create a competition between manufacturers ?

- specific production…
- financial weight of our orders

Do things ourselves ?

- manpower, equipment

Optimize financial impact being opportunistic ?

- order when markets are low
- share production among various small batches

Optimize the yield ?

Deal with consumer devices manufacturers ?

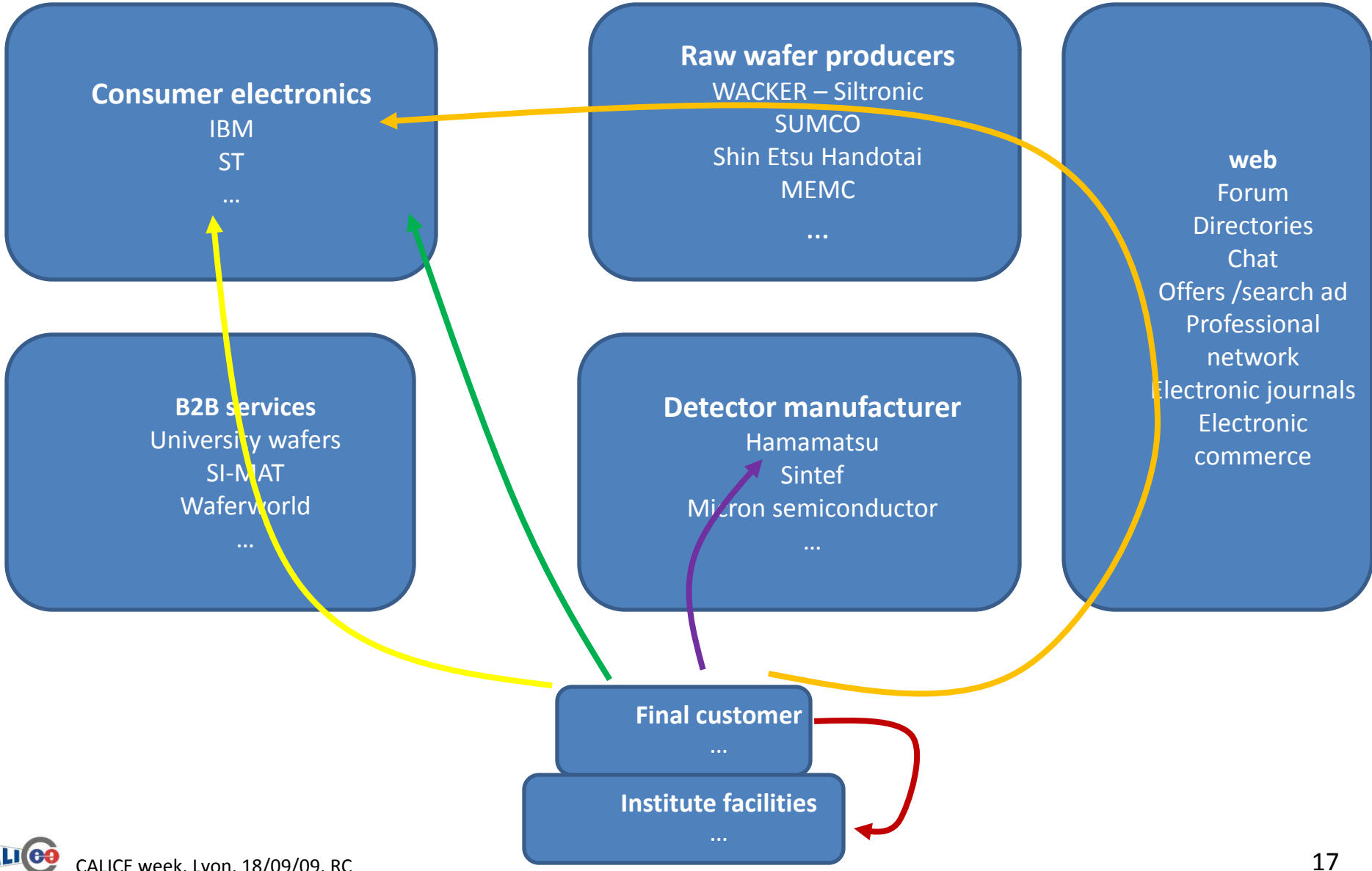
- eg. OnSemi

Some market trends

- High resistivity silicon : RF & wireless, power devices
- New method to produce HiRes silicon with CZ process
- Manufacturing tools for 300mm
- R&D to produce 300 mm FZ ingots : 4 sensors

- Market is dominated by electronics and photovoltaic silicon, resistivity below 10 Ohms.cm
- Our production is rather small
- Some specific features
  - Passivation (I_{leak}, compatibility with glue)
  - Guard rings

Si Market Overview



The cost issue

Commercial market

- Market analysis
- Increase our visible weight to start bargaining
- Develop our contacts in the industry
- Find the necessary funding to invest in R&D with a panel selected of manufacturers

Institutional organizations

- Have the necessary knowledge of the manufacturing processes, develop our own R&D or production facilities ?
  - Silicon factory at fermilab
  - Association with existing European platform for micro/nano tech
    - Eg. MINERVE at Orsay, CEA-LETI, …
    - European programs for technological platforms
  - Buy or loan an obsolete industrial production chain (eg. AMS 0.35 ?)
  - Show that we could do it ourselves

Seventh Framework Programme (FP7)

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Find project partners

Capacities

The Commission's proposals for the FP7 Capacities programme aim to enhance research and innovation capacities throughout Europe and ensure their optimal use. The Capacities programme is provided with a budget of EUR 4 097 million to operate in seven broad areas:

- Research infrastructures
- Research for the benefit of SMEs
- Regions of knowledge and support for regional research-driven clusters
- Research potential of Convergence Regions
- Science in society
- Support to the coherent development of research policies
- International cooperation

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Highlights

- ETP Conference, Gearing R&I to address societal challenges, 13 October 2009
- Fourth STATUS REPORT: Harvesting the potential, August 2009

Réseau de grandes centrales technologiques pour la Recherche Technologique de Base

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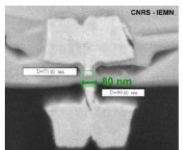
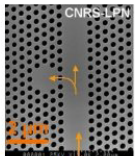
Bienvenue sur le réseau RENATECH des grandes centrales de technologie du CNRS

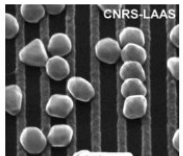
Le programme intitulé « Un réseau national de grandes centrales de technologie pour la RecherceTechnologique de Base (RTB) » a été initié en 2003.

La mise en place d'un réseau national de grandes centrales technologiques au sein du secteur public est une action d'envergure du Ministère de l'enseignement supérieur et de la recherche. Son objectif est de permettre à la recherche publique française (CEA, CNRS, Universités,...) de faire face dans de bonnes conditions aux formidables enjeux de micro et nanotechnologies et nanosciences pour les années à venir. Ce programme vise à disposer d'une infrastructure propre à fournir les technologies nécessaires à la réalisation des projets de recherche et de développement des laboratoires.

Ce projet est porté par l'Institut ST2I du CNRS (l'Institut de physique INP et des laboratoires universitaires étant concernées) et par le LETI du CEA (d'autres entités du CEA étant également concernées).







Conclusion

- Invest for future cost optimization
  - Funding (and manpower) for R&D
    - Opportunity of technological prototype
    - Several batches of sensors from various manufacturer
      - Establish relationship
      - Allow consumer devices manufacturers
  - Market study
- Avoid a dependence in a single design / manufacturer
- Increase our visible weight
  - Collaboration & network (CERN…)
  - Bargaining
  - Generate interest from consumer electronics manufacturers (ST, Samsung, OnSemi,…)
- Improve our tests / qualification procedure
  - Test beams
  - Test equipment
  - Exhibit a reasonable knowledge of the sensors to enable discussion and avoid the trap of dependence