AHCAL Integration.

Status and Outlook

Mathias Reinecke
for the AHCAL developers
CALICE week Lyon
IPNL, Sept. 16th – 18th, 2009

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

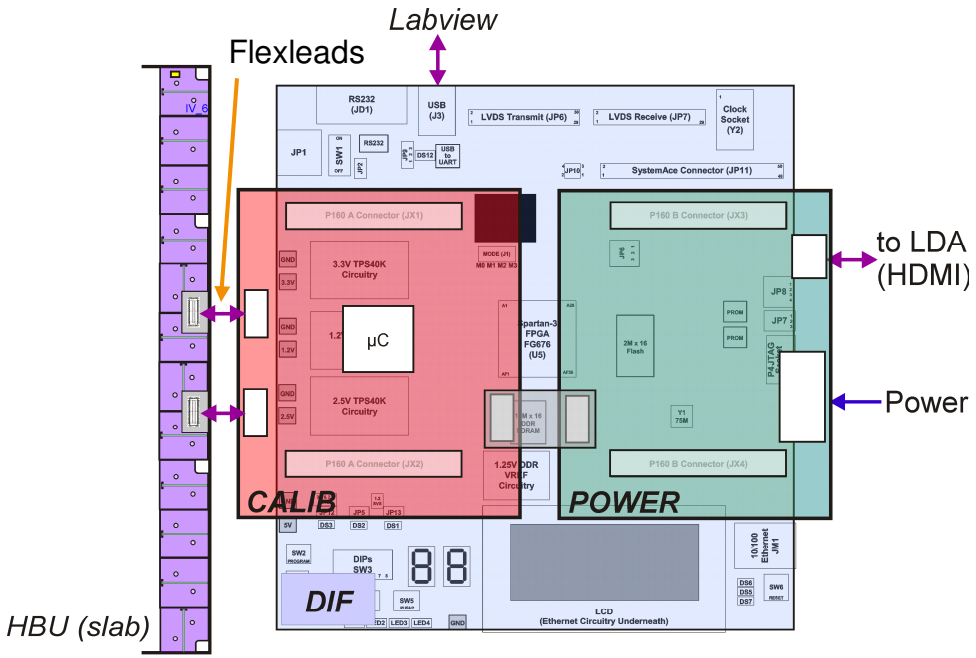
EUDET

DESY

Outline

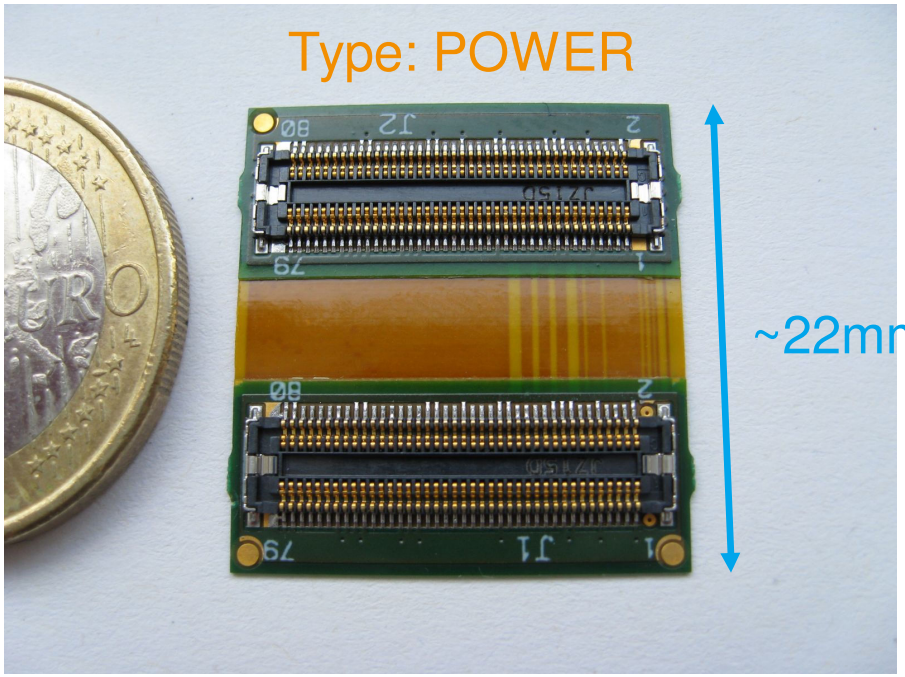
- Hardware Developments at DESY
  - CALIB, POWER, Flexleads
  - HBU0
  - DIF0 and DAQ interface (USB)
  - Tiles integration
- System Commissioning
- SPIROC analogue tests (see electronics session)
- The Next Generation
- Conclusions and Outlook

'old-fashioned overview'
CALICE week Manchester

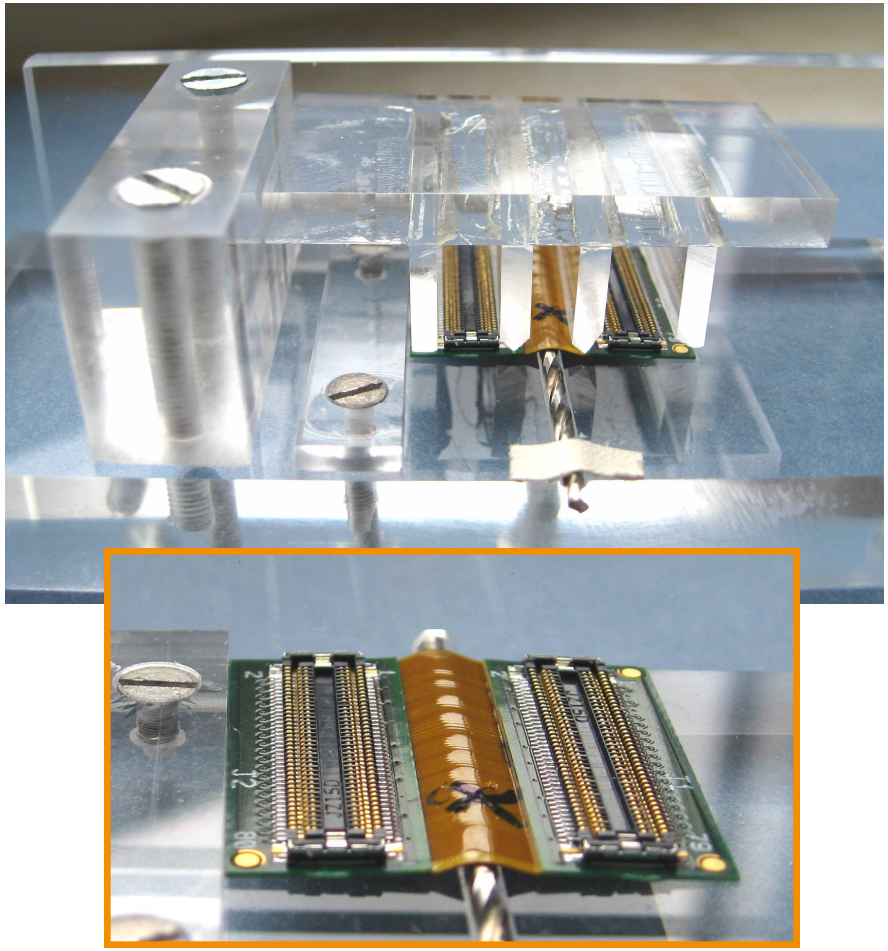


Flexleads – SIGNAL and POWER

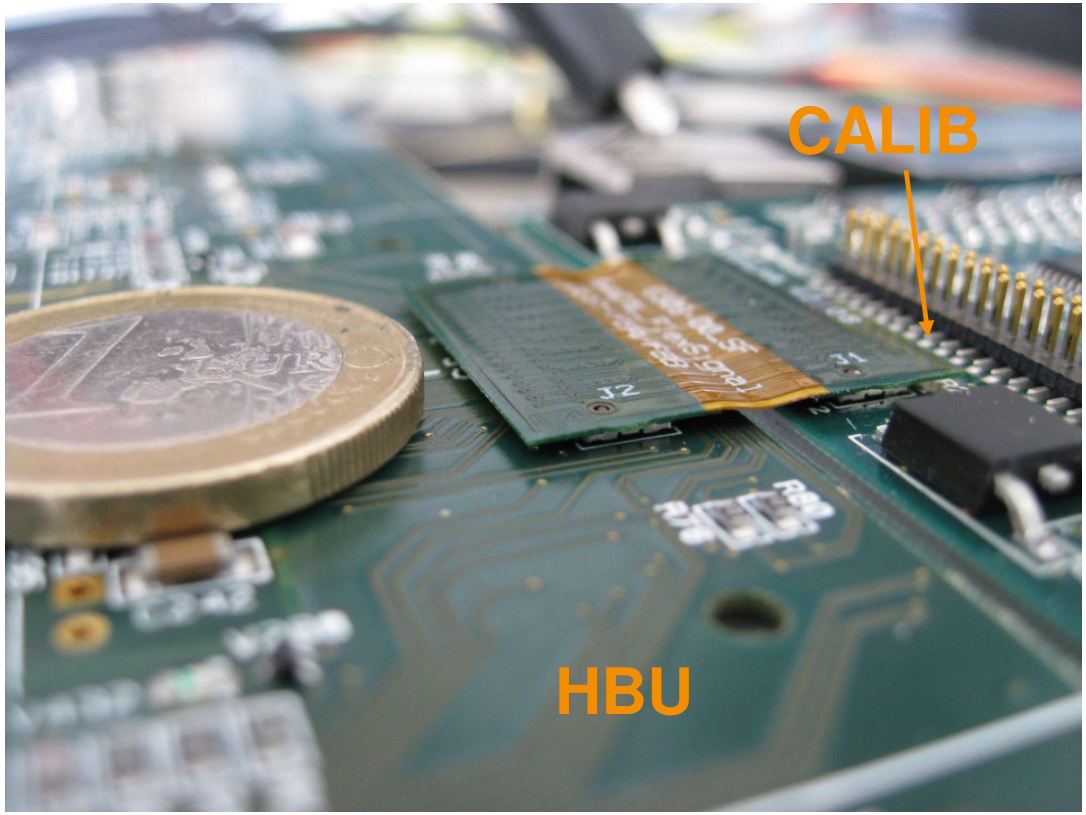
- 20 pieces of each type finished.
- Pre-bending procedure ok.



Flexlead Pre-Bending:



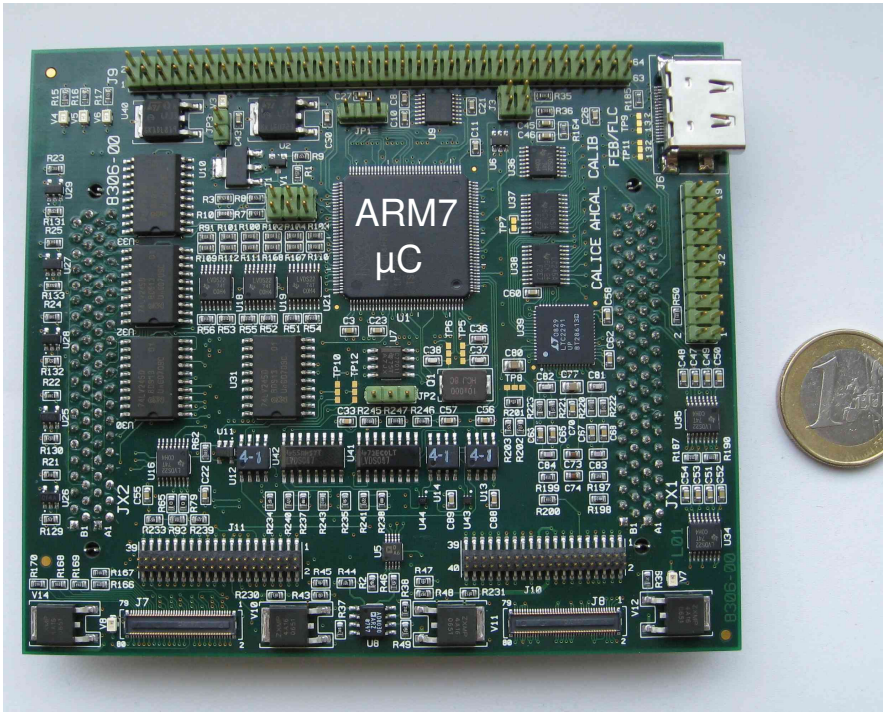
Flexleads – SIGNAL and POWER



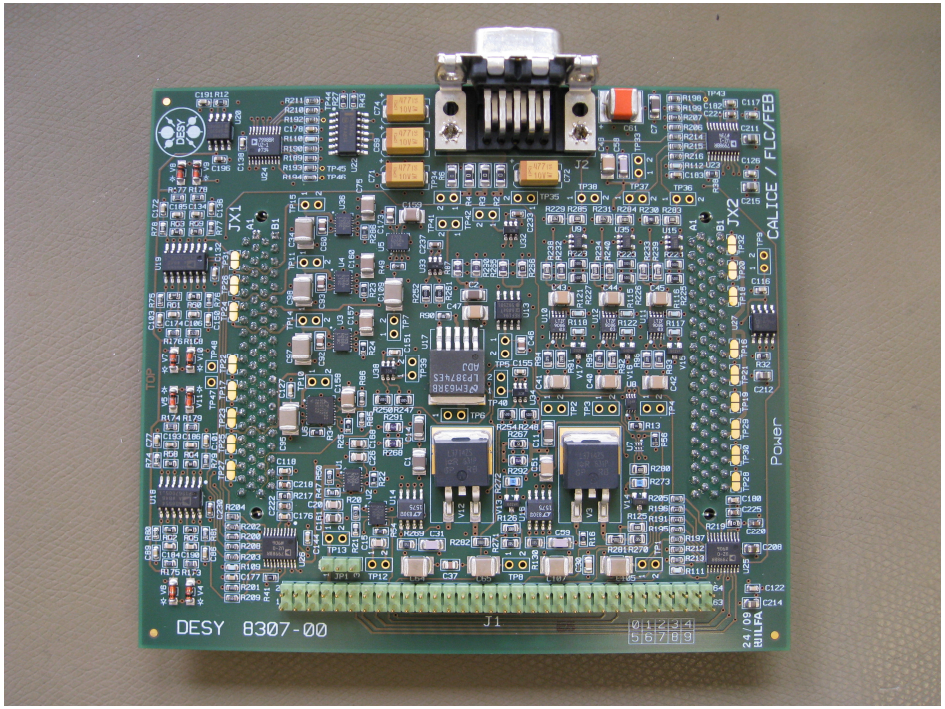
- About 80 connection cycles up to now - still ok.
- Compensate HBU misalignments in distance.
- Fulfill AHCAL height requirements.
- Tests ok concerning:
  - Signal allocation
  - Signal quality
  - Resistance for power

CALIB and POWER Modules

CALIB module: 11 x 10 cm²



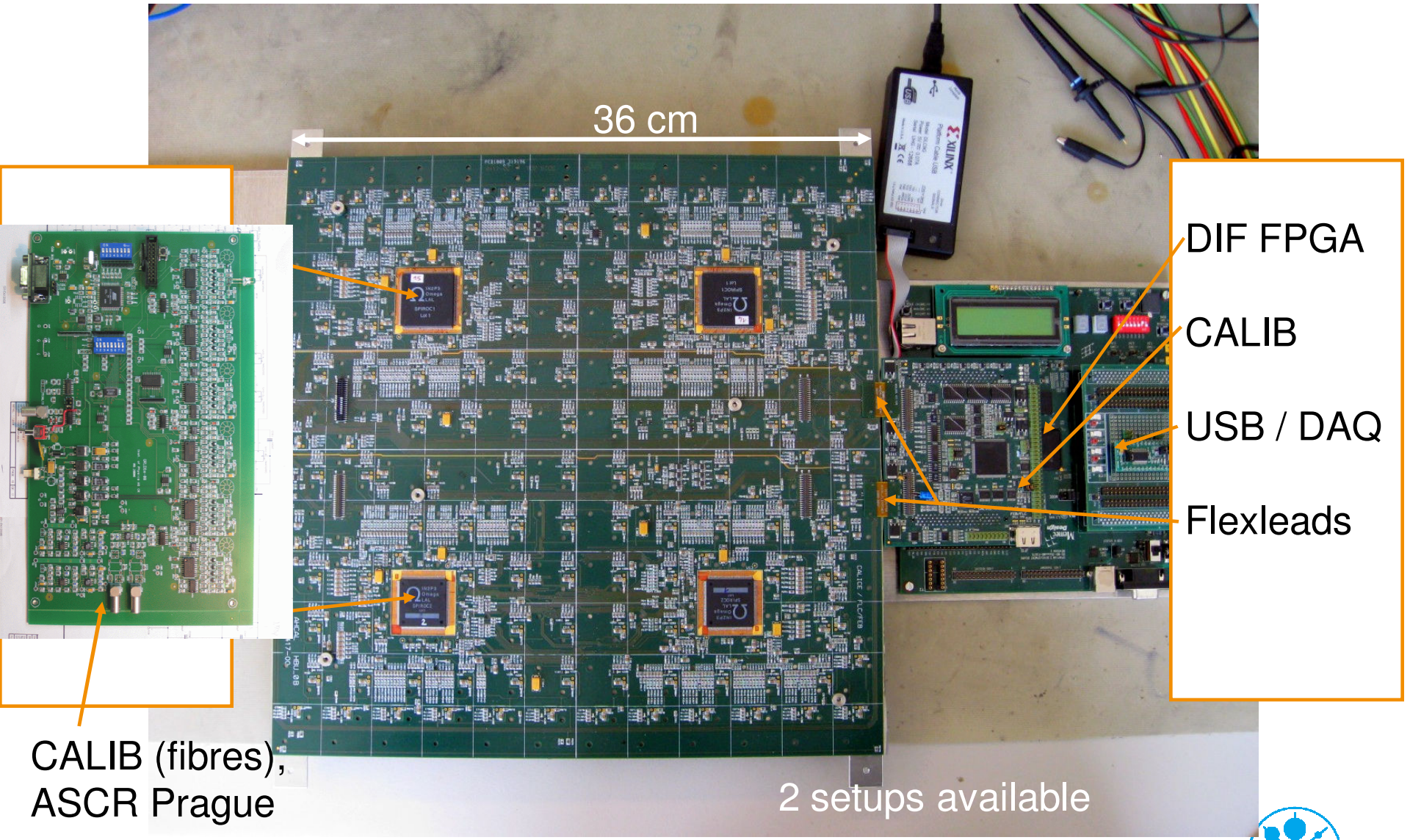
POWER module: 12.5 x 11 cm²



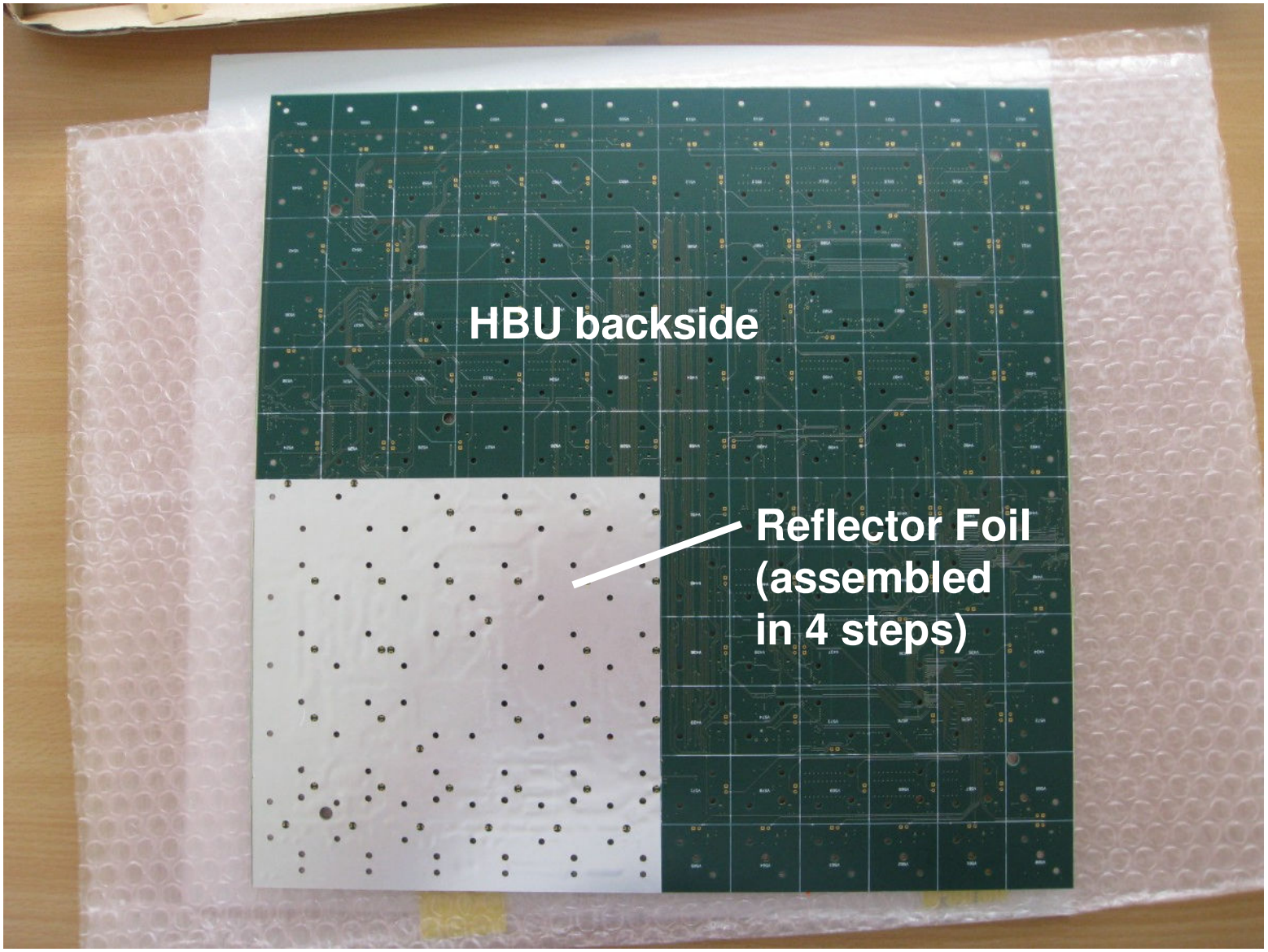
> 4 Modules of both types finished, in operation.
> First tests successful.

Sizes and heights: To be adapted to ILC mechanics later.

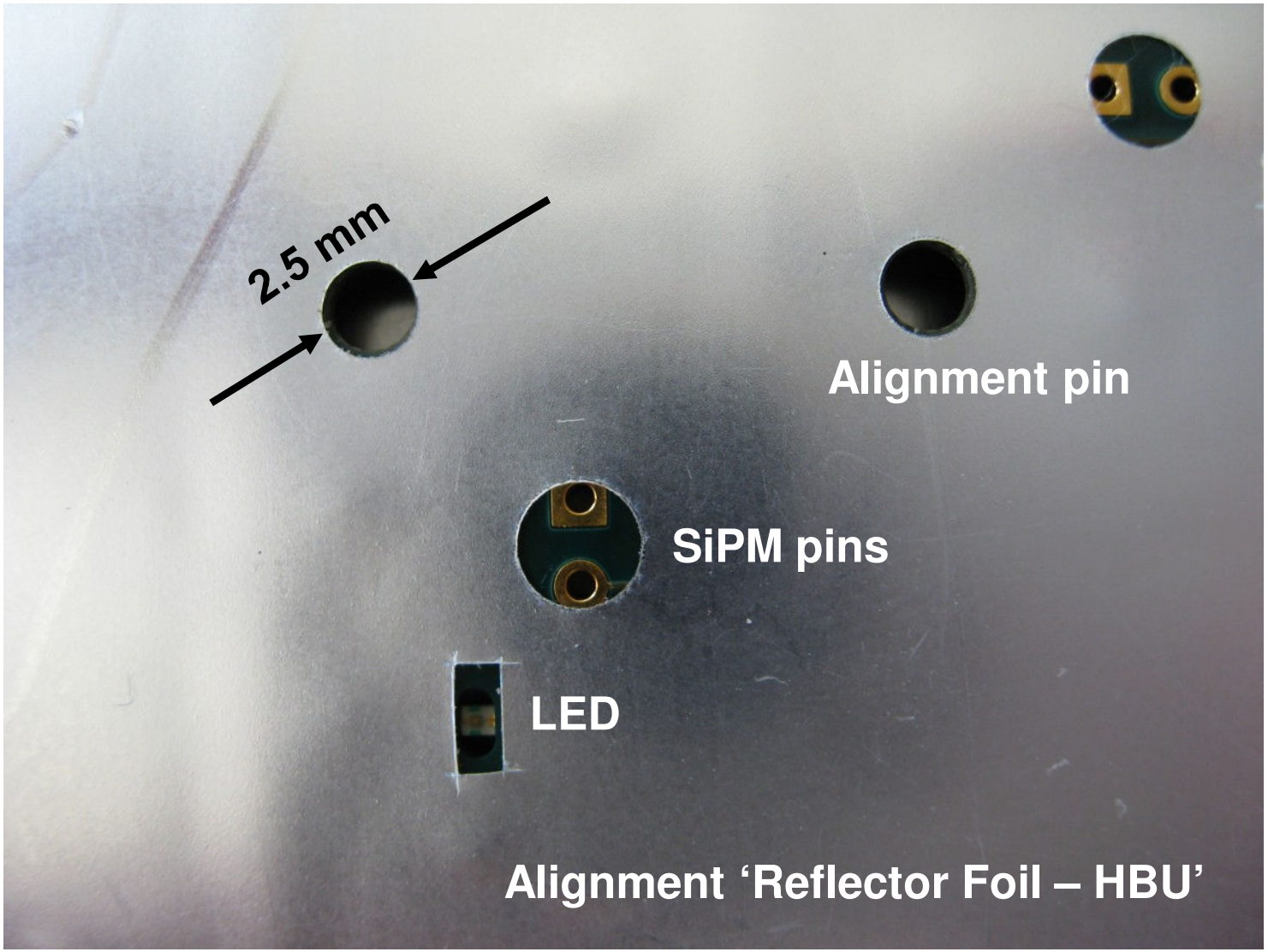
HCAL Base Unit (HBU) setup



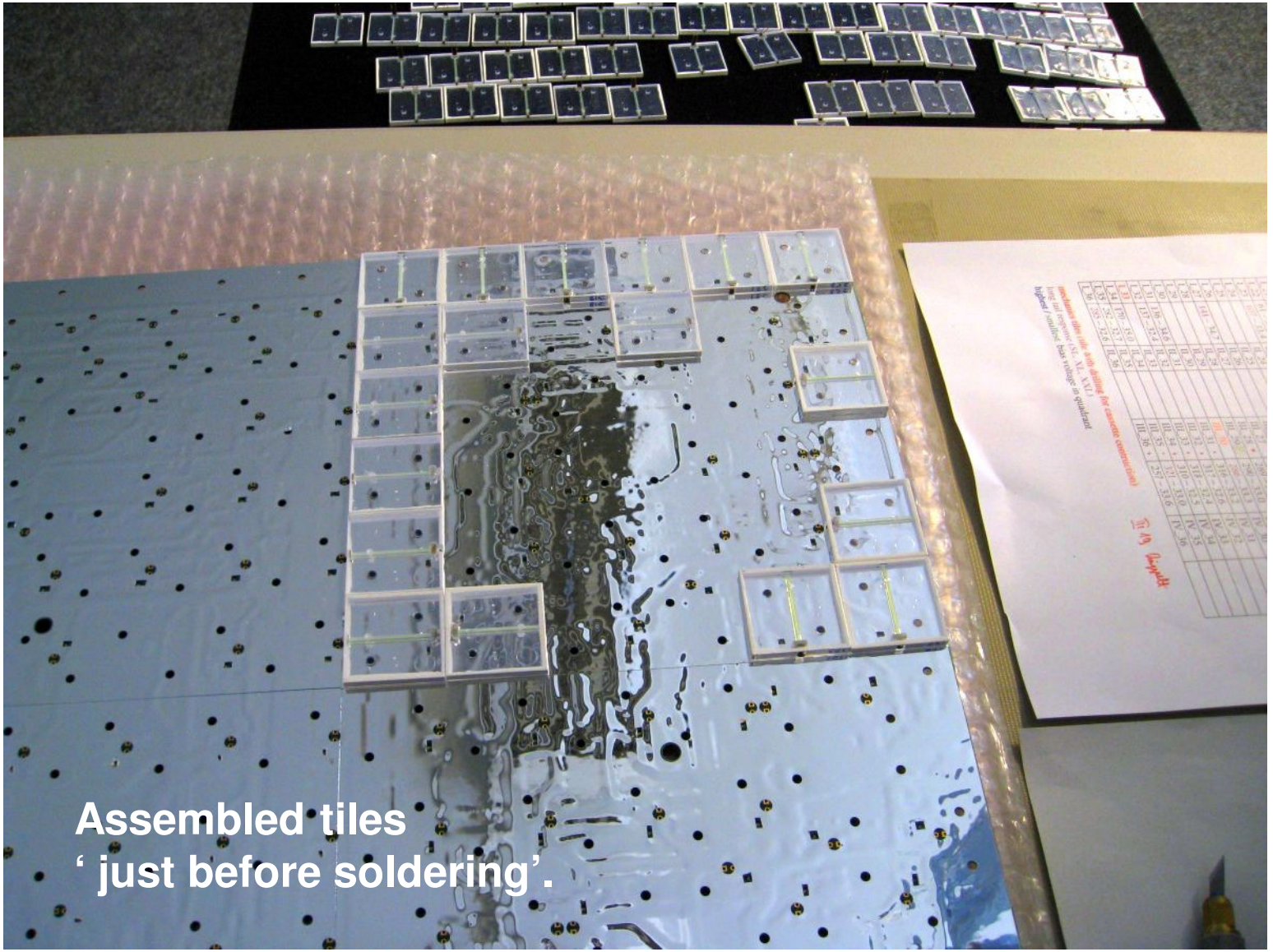
Reflector Foil Assembly



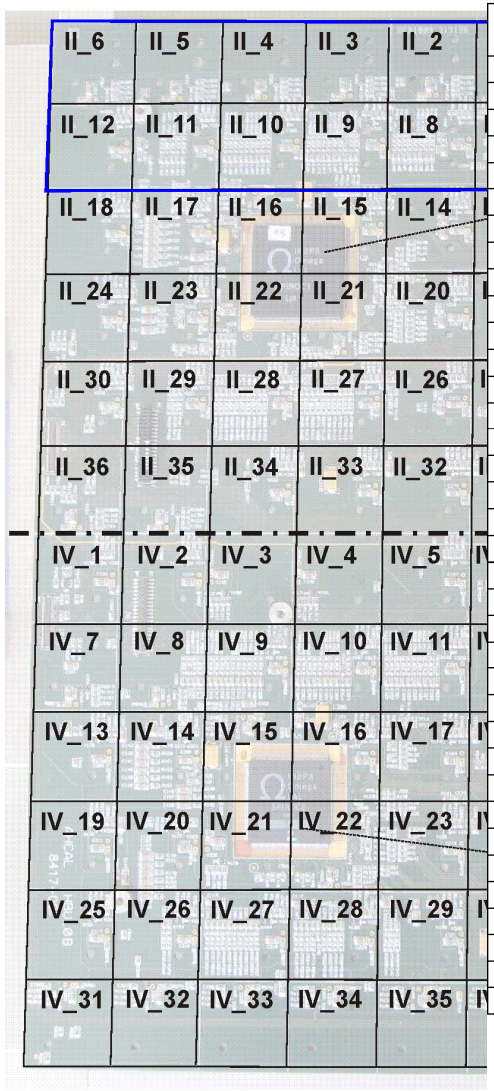
Reflector Foil Assembly



Tile Assembly (the first 18)



Tile Map



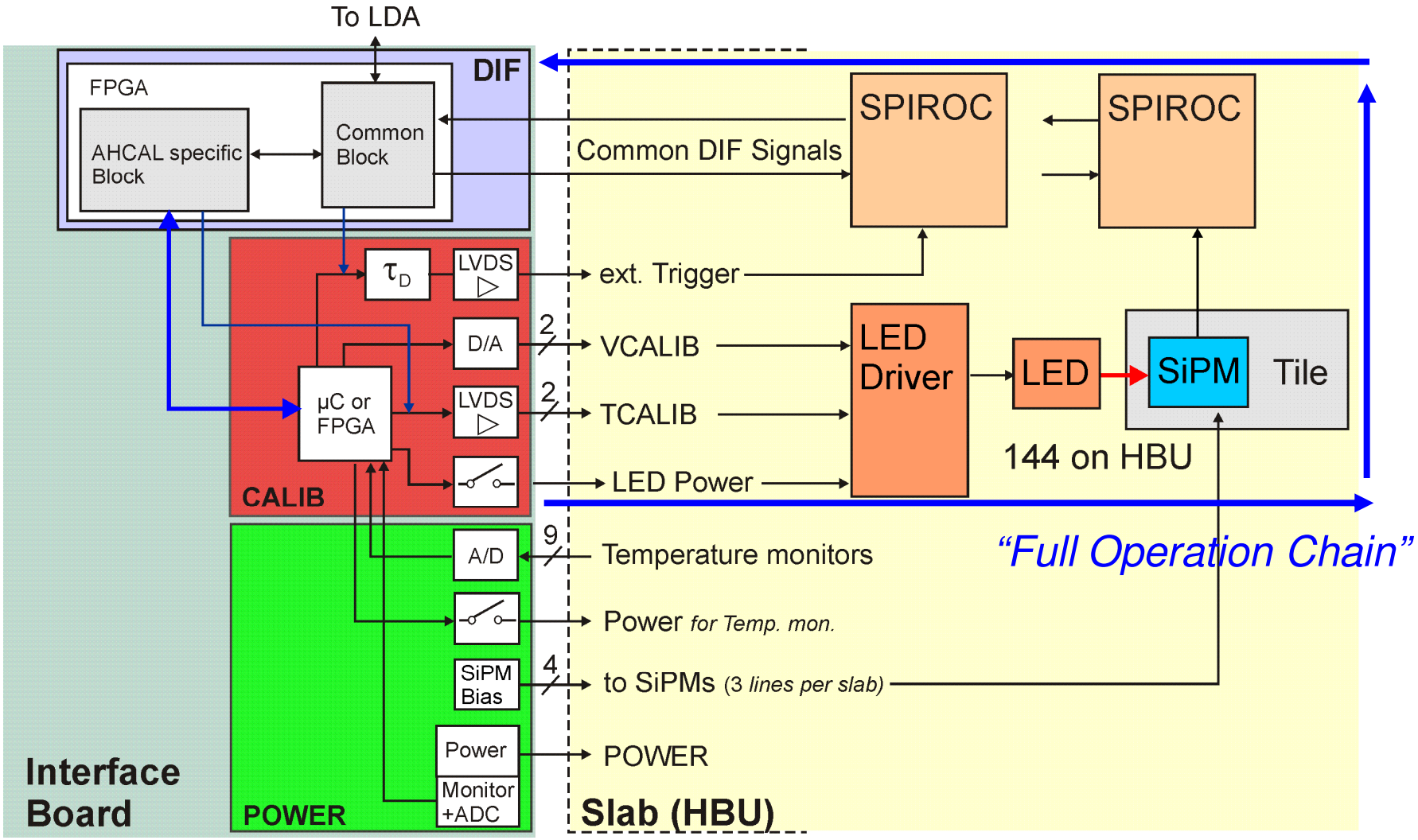
Module HBU0_II

Pos.	Tile – Bias [V]	Pos.	Tile – Bias [V]	Pos.	Tile – Bias [V]	Pos.	Tile – BiasV [V]
I_1		II_1		III_1	26 – 33.5	IV_1	152 – 33.1
I_2		II_2		III_2	33 – 33.3	IV_2	14 – 33.0
I_3		II_3		III_3	41 – 33.3	IV_3	55 – 32.8
I_4		II_4		III_4	43 – 33.6	IV_4	42 – 33.0
I_5		II_5		III_5	50 – 33.4	IV_5	46 – 32.7
I_6		II_6		III_6	81 – 34.0	IV_6	24 – 32.5
I_7		II_7		III_7	90 – 33.9	IV_7	326 – 33.5
I_8		II_8		III_8	95 – 33.5	IV_8	88 – 31.9
I_9		II_9		III_9	98 – 33.9	IV_9	89 – 33.3
I_10		II_10		III_10	272 – 33.5	IV_10	248 – 33.0
I_11		II_11		III_11	133 – 33.8	IV_11	320 – 34.0
I_12		II_12		III_12	138 – 33.3	IV_12	314 – 32.2
I_13		II_13		III_13	147 – 33.8	IV_13	312 – 33.3
I_14		II_14		III_14	157 – 33.7	IV_14	188 – 33.2
I_15		II_15		III_15	166 – 33.5	IV_15	193 – 32.8
I_16		II_16		III_16	167 – 33.5	IV_16	235 – 33.6
I_17		II_17		III_17	168 – 33.9	IV_17	200 – 34.1
I_18		II_18		III_18	173 – 33.6	IV_18	206 – 33.8
I_19		II_19		III_19	178 – 33.7	IV_19	205 – 32.6
I_20		II_20		III_20	184 – 33.8	IV_20	207 – 33.1
I_21		II_21		III_21	249 – 33.8	IV_21	221 – 32.4
I_22		II_22		III_22	186 – 33.5	IV_22	225 – 32.7
I_23		II_23		III_23	252 – 33.7	IV_23	242 – 33.2
I_24		II_24		III_24	264 – 33.6	IV_24	258 – 33.0
I_25		II_25		III_25	241 – 33.6	IV_25	265 – 32.9
I_26		II_26		III_26	213 – 33.6	IV_26	305 – 32.3
I_27		II_27		III_27	227 – 33.7	IV_27	277 – 33.1
I_28		II_28		III_28	185 – 34.0	IV_28	267 – 32.9
I_29		II_29		III_29	240 – 33.4	IV_29	313 – 33.1
I_30		II_30		III_30	208 – 34.0	IV_30	164 – 33.3
I_31		II_31		III_31	196 – 33.2	IV_31	306 – 33.1
I_32		II_32		III_32	201 – 33.2	IV_32	307 – 33.1
I_33		II_33		III_33	194 – 33.3	IV_33	308 – 33.3
I_34		II_34		III_34	87 – 33.3	IV_34	311 – 32.8
I_35		II_35		III_35	125 - 33.3	IV_35	315 – 33.0
I_36		II_36		III_36	181 – 33.3	IV_36	325 – 32.6

mechanics tiles (tile with drilling for cassette contruction)
long tail response (SL, XL, XXL)
highest / smallest bias voltage in quadrant

Each quadrant can choose between 3 SiPM bias voltages

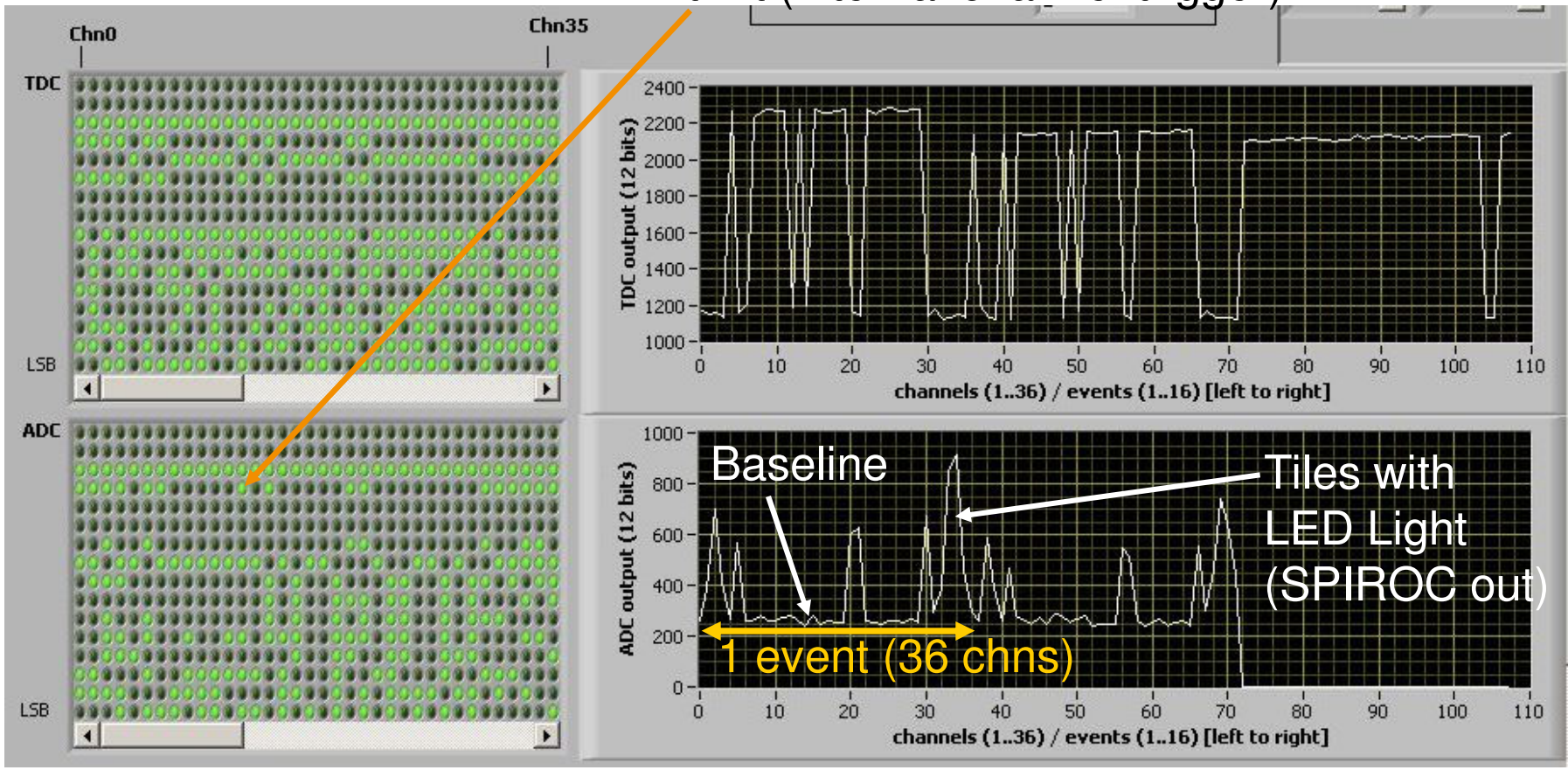
Commissioning – Signal Chain for LED operation



Concept : December 2007

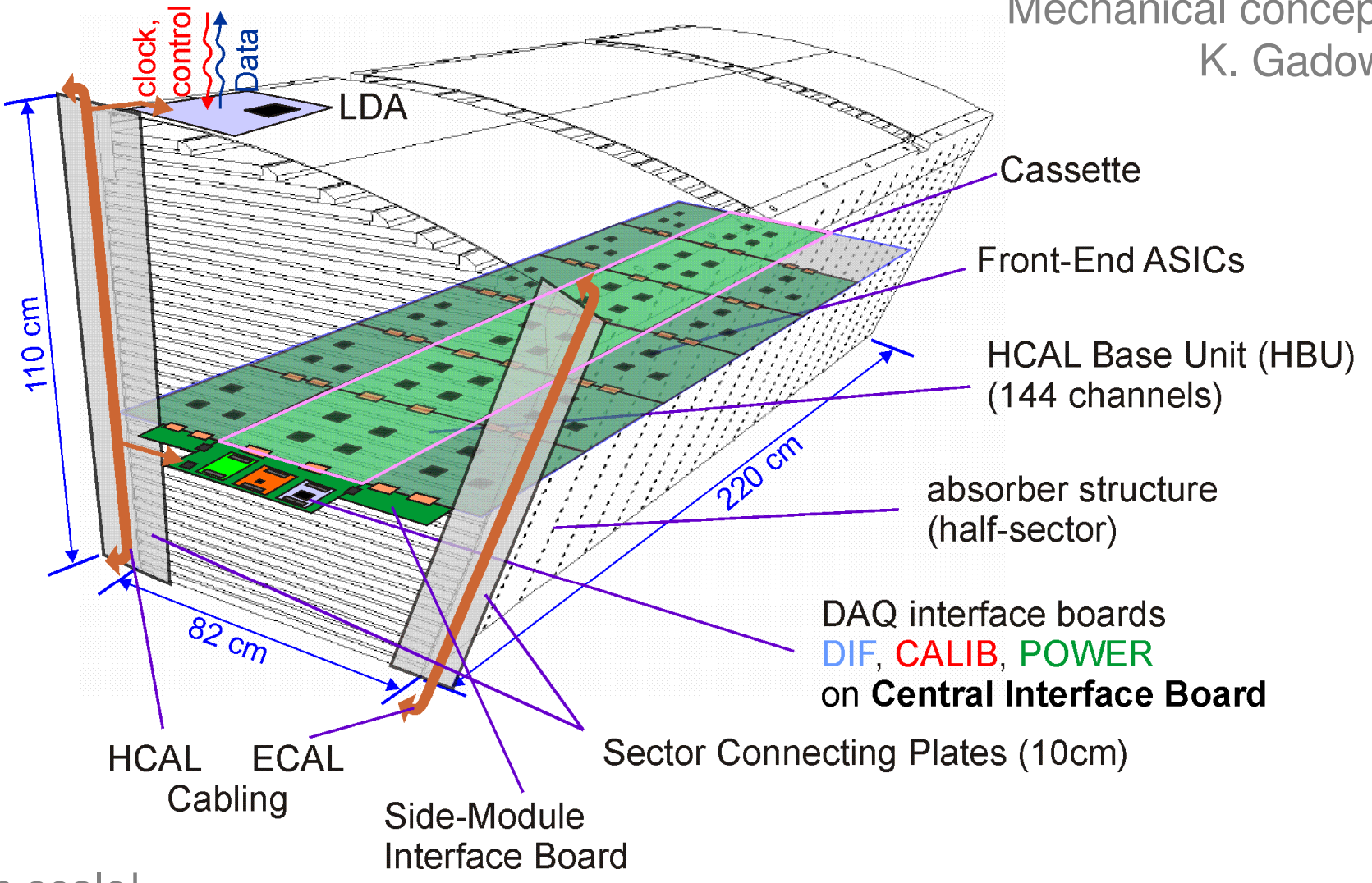
Commissioning (status last Friday)

SPIROC2 output: LEDs firing, 3 events (triggers), 18 tiles assembled



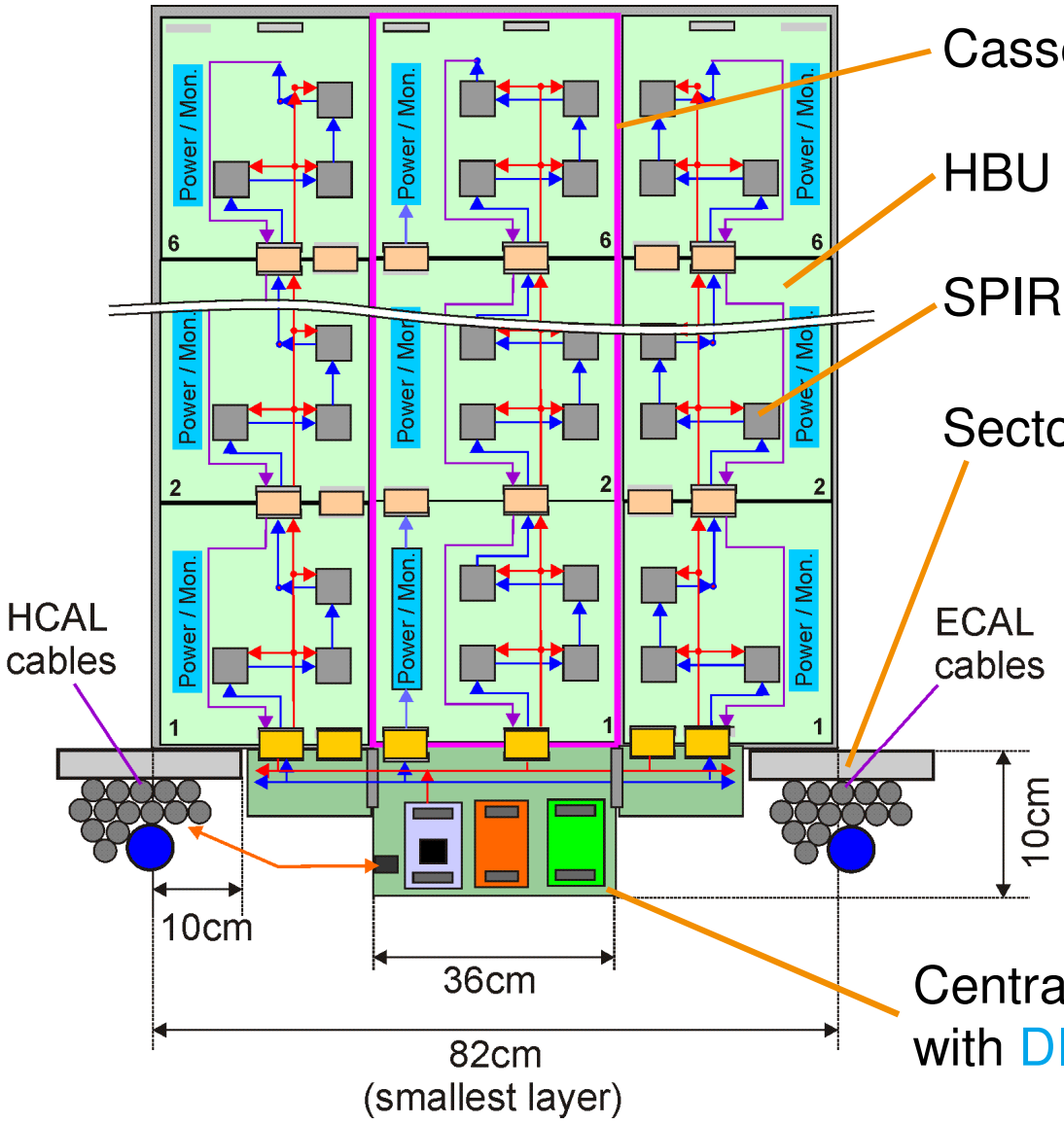
The Next Generation

Mechanical concept:
K. Gadow



Not in scale!

The Next Generation



Cassette (=slab)

HBU

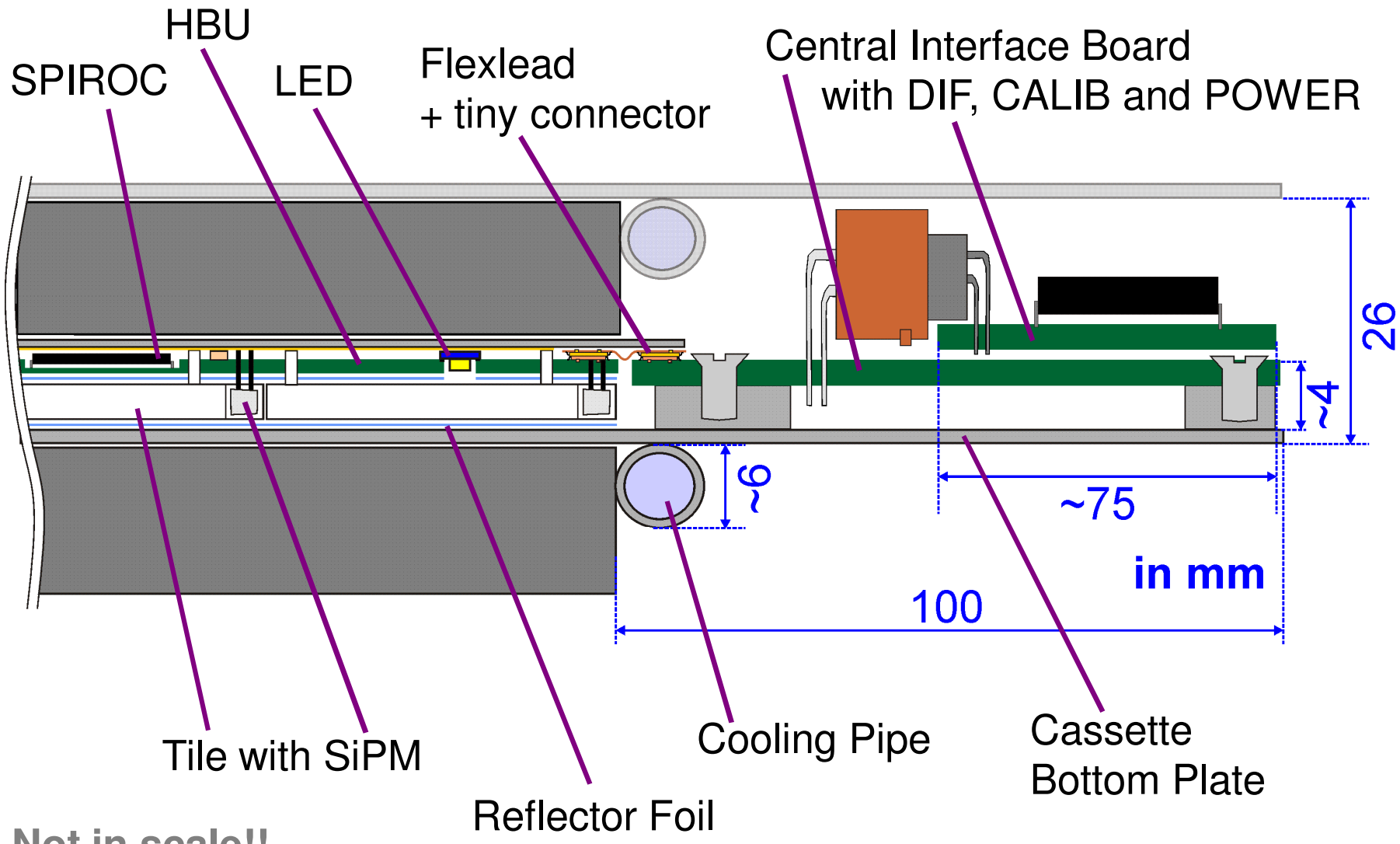
SPIROC

Sector Connecting Plate

Not in scale!!

Central Interface Board with DIF, CALIB and POWER

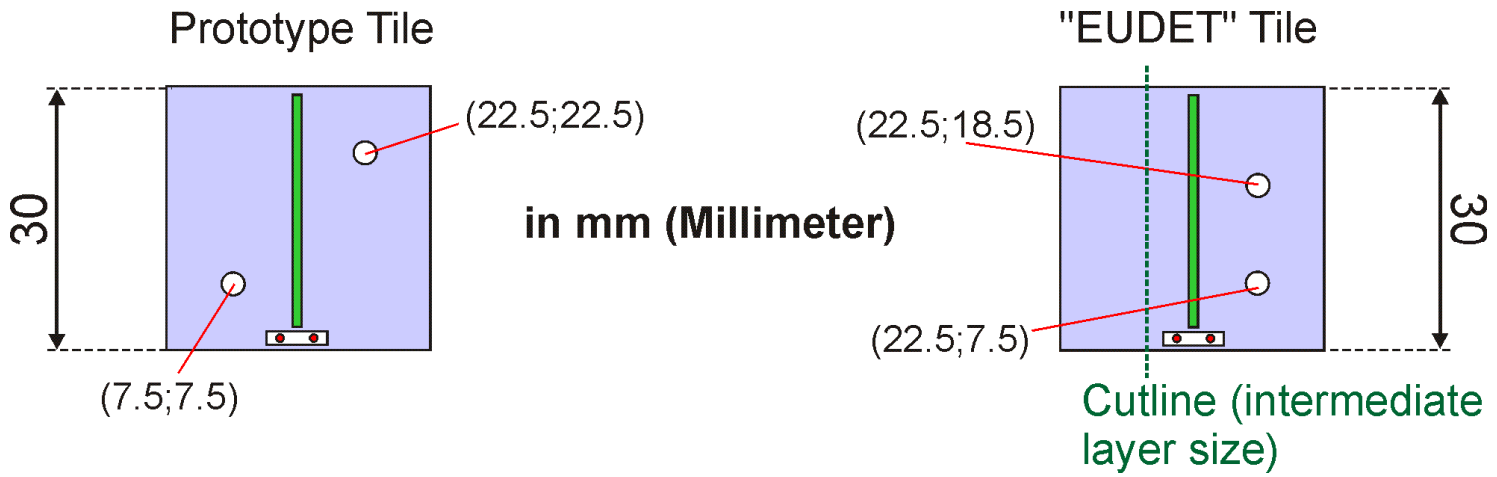
The Next Generation



Not in scale!!

EUDET Tiles

Ideas from November 2008 (ITEP)

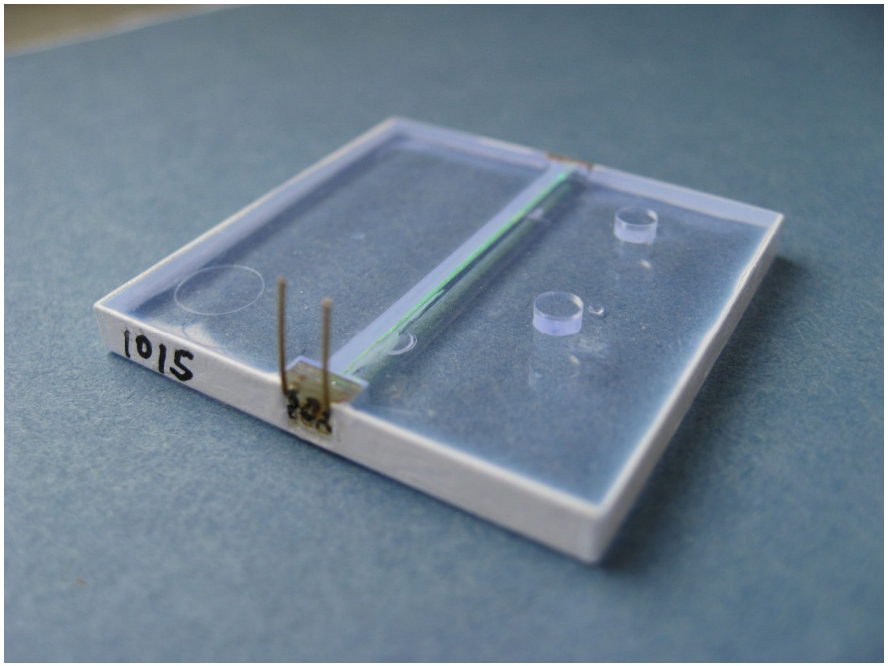


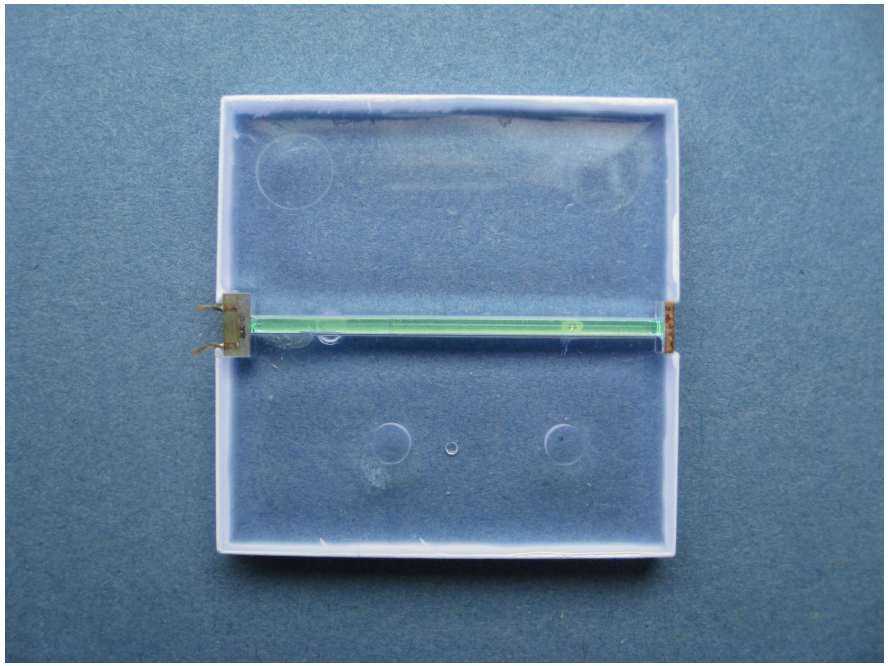
153 delivered

12 samples arrived

EUDET Tiles

12 tiles of new generation arrived from ITEP

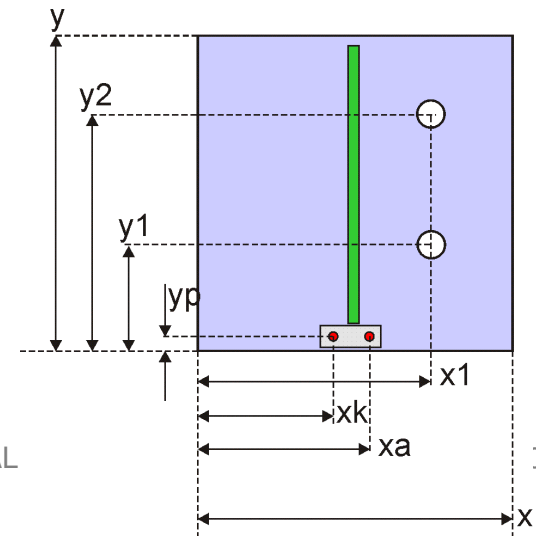




EUDET Tiles

Tile	h	y	x	y2*	y1*	x1	xa	xa-xk	d2	d1
nominal dimension	3.0	30.0	30.0	22.50	11.50	22.50	16.25	2.50	2.50	2.50
1004	3.05	30.043	29.927	22.495	11.492	22.420	16.251	2.554	2.514	2.511
1005	3.0	29.901	29.912	22.399	11.405	22.440	16.339	2.545	2.513	2.506
1006	3.0	29.977	29.971	22.418	11.417	22.449	16.394	2.550	2.519	2.510
1007	3.05	29.980	29.864	22.447	11.446	22.375	16.354	2.581	2.516	2.509
1008	3.0	29.982	30.001	22.479	11.482	22.468	16.500	2.523	2.516	2.504
1009	3.05	30.016	29.914	22.464	11.462	22.446	16.229	2.502	2.518	2.512
1010	3.05	29.965	29.904	22.436	11.437	22.437	16.393	2.563	2.514	2.509
1011	3.10	29.907	29.940	22.423	11.423	22.434	16.373	2.483	2.517	2.512
1012	3.05	29.924	29.993	22.409	11.412	22.452	16.396	2.580	2.518	2.510
1013	3.10	29.879	29.781	22.398	11.400	22.405	16.310	2.539	2.510	2.508
1014	could not be measured, dimensions far off									
1015	3.00	29.898	29.934	22.402	11.402	22.431	16.457	2.546	2.487	2.503

*initial plan was y1=7.5mm, y2=18.5mm



Measured by DESY group ZM31

“quite a lot tiles with larger deviations” => prototypes

EUDET Tiles

UV LED (~10ns pulse width) measurements:

Tile number	Saturation [pixels]
1004	960
1005	997
1006	952
1007	945
1008	900
1009	957
1010	962
1011	1206
1012	892
1013	952
1014	1232
1015	1000

WLS fibre: ~25ns time constant

SiPMs : 756 pixels (CPTA) ?
Size : 1mm² ??
SiPM recovery time < 25ns ?
Quenching resistor, -variations?

Saturation values ok ?
Variations due to fibre alignment?
No. of Pixels ok for physics?

Measured by
Erika Garutti and
Adel Terkulov

Conclusions and Outlook

- AHCAL prototype delivers first test-data from LED system.
- British DAQ (hardware, DIF firmware) still has to be implemented.
- AHCAL prototype is prepared for DESY testbeam (USB based).
- Labview GUI has to be extended for testbeam (=> Sandra Christen).
- Redesign concepts of AHCAL modules are prepared now.
- EUDET Tiles : Status ok (input from ITEP to our comments?)?
- A lot of system's and SPIROC analogue and digital tests ahead.