R&D activity dedicated to the VFE of the Si-W Ecal

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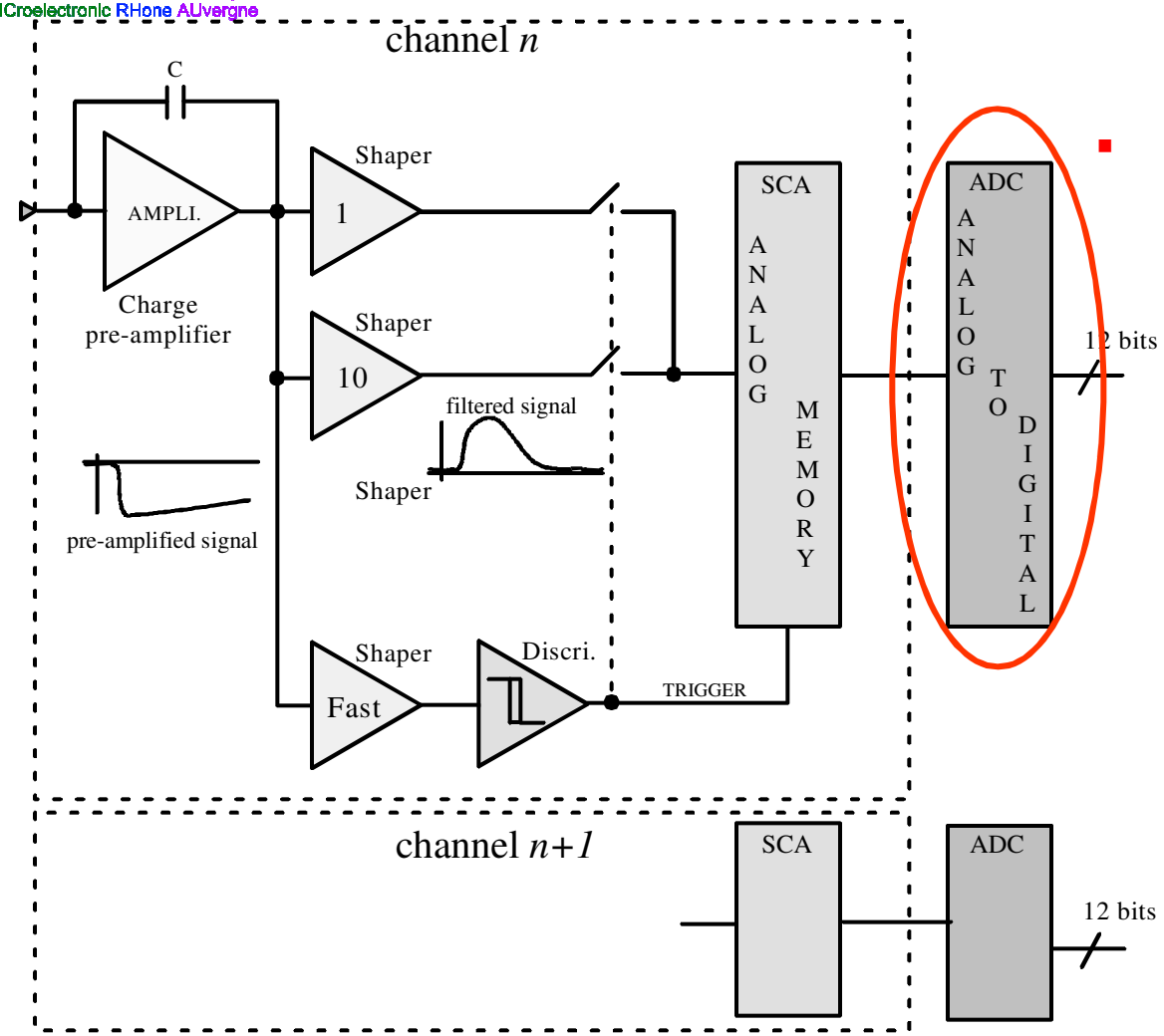
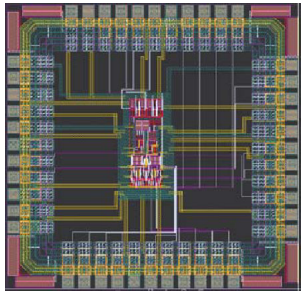
ADC development



- **Main requirements for the ADC:**
  - Resolution:
    - **12 bits with 2-gain shaping**
  - Time of conversion: time budget of 500 µs to convert all data of all triggered channels
  - Ultra low power:
    - **power budget of 2.5 µW/ch** (10% of one VFE channel power budget)
    - Memory depth of 5 → **0.5 µW per conversion**
    - **Power pulsing needed**
  - Die area:
    - **as smal as possible…**

Analog electronics busy	A/D conv.	DAQ	IDLE MODE
1ms (.5%)	.5ms (.25%)	.5ms (.25%)	198ms (99%)

The cyclic ADC designed (03/08)



Die area of the core = 0.12mm2

- ✓ Clock frequency: 1MHz
- ✓ Supply voltage : 3.5V
- ✓ Technology: 0.35 µm CMOS Austriamicrosystems (reliable and cheap !!)
- ✓ ADC designed with the validated building blocks (Amplifier & Comparator) of a 10-bit pipeline ADC (published in IEEE NSS in June 08) but optimized for the 12-bit precision requirement
- ✓ Power pulsing system implemented
- ✓ Digital process of the bits (1.5 bit/stage algorithm) performed by an external FPGA
- ✓ Fully differential ADC: analog signal, reference, clock…

Power pulsing measurement

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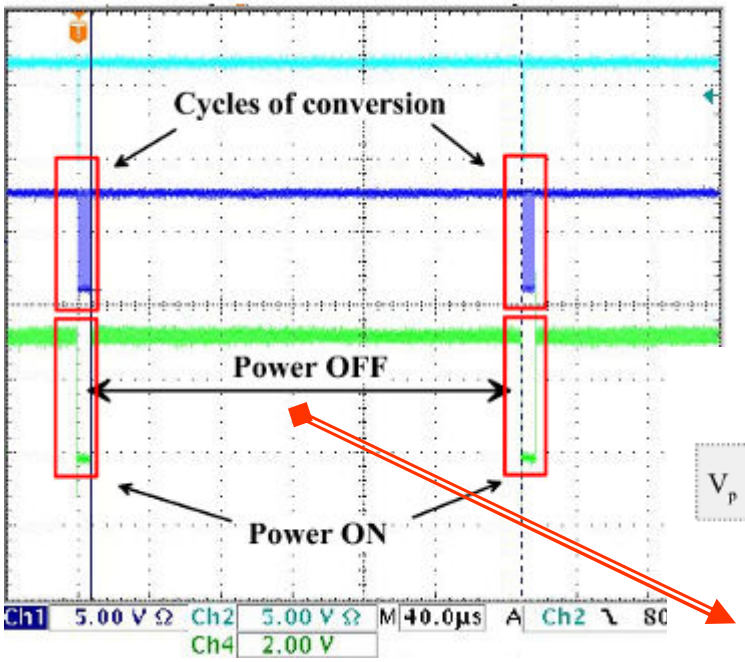
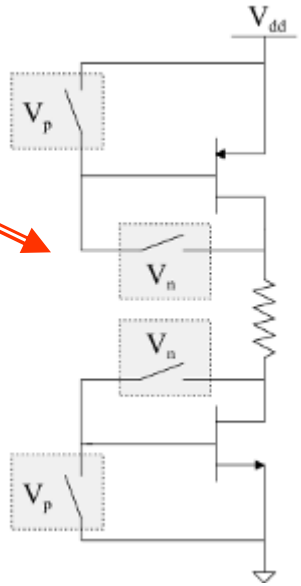
Table 1: Summarized performance of the 10 chips tested.

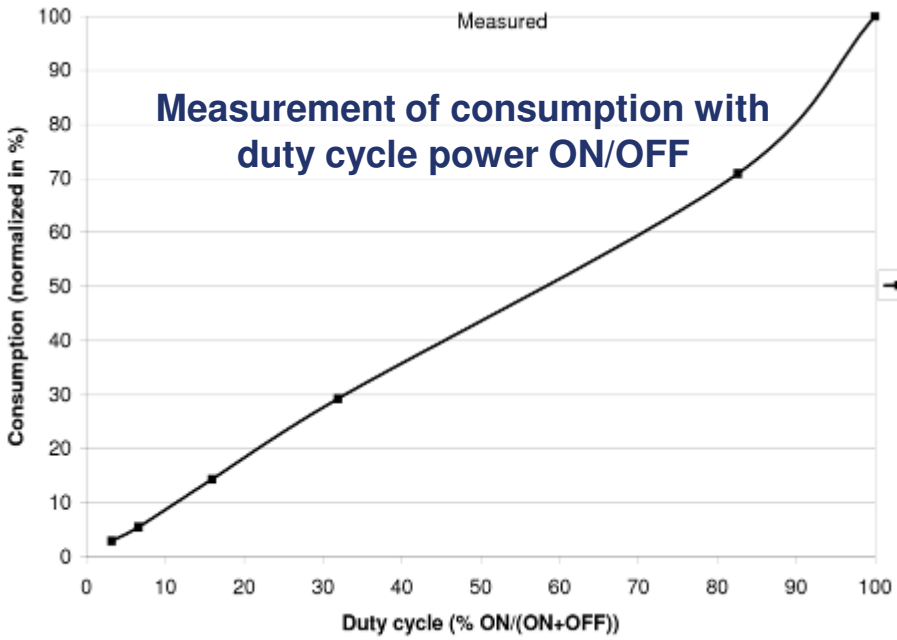
Power supply	3.5 V
Consumption	3.5 mW
Time of conversion	7 μs

1 µs for recovery time included after power ON





Master current sources switched OFF



Integrated consumption with ILC timing : 0.12 µW per conversion

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Summarized performance of the ADC

ADC version	Yield	INL of 6 chips (mean ± σ)	Noise (rms)	Consumption***	Die area*
March 08	6/10	(3.6 ± 1.2) LSB	0.84 LSB	3.5 mW * 0.12 µW w/ PP **	0.12mm^2

* without the digital block

** power pulsing with duty ratio of 1%

*** for one conversion

Improvement of the performance of the ADC

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New cyclic ADC submitted to run in 03/09:

- ✓ Reduction of power supply voltage: 3.5V to 3.0V
- ✓ Optimization (reduction) of BW performance of the amplifier
- ✓ Improvement of the yield: reduction of biasing variation versus process fluctuation → single stage amplifier

ADC version	Yield	INL of 10 chips (mean ± σ)	Noise (rms)	Consumption***	Die area*
March 08	6/10	(3.6 ± 1.2) LSB	0.84 LSB	3.5 mW * 0.12 µW w/ PP **	0.12mm^2
March 09	10/10	(3.0 ± 0.8) LSB	0.3 LSB	**1.5 mW** * 0.05 µW w/ PP **	0.12mm^2

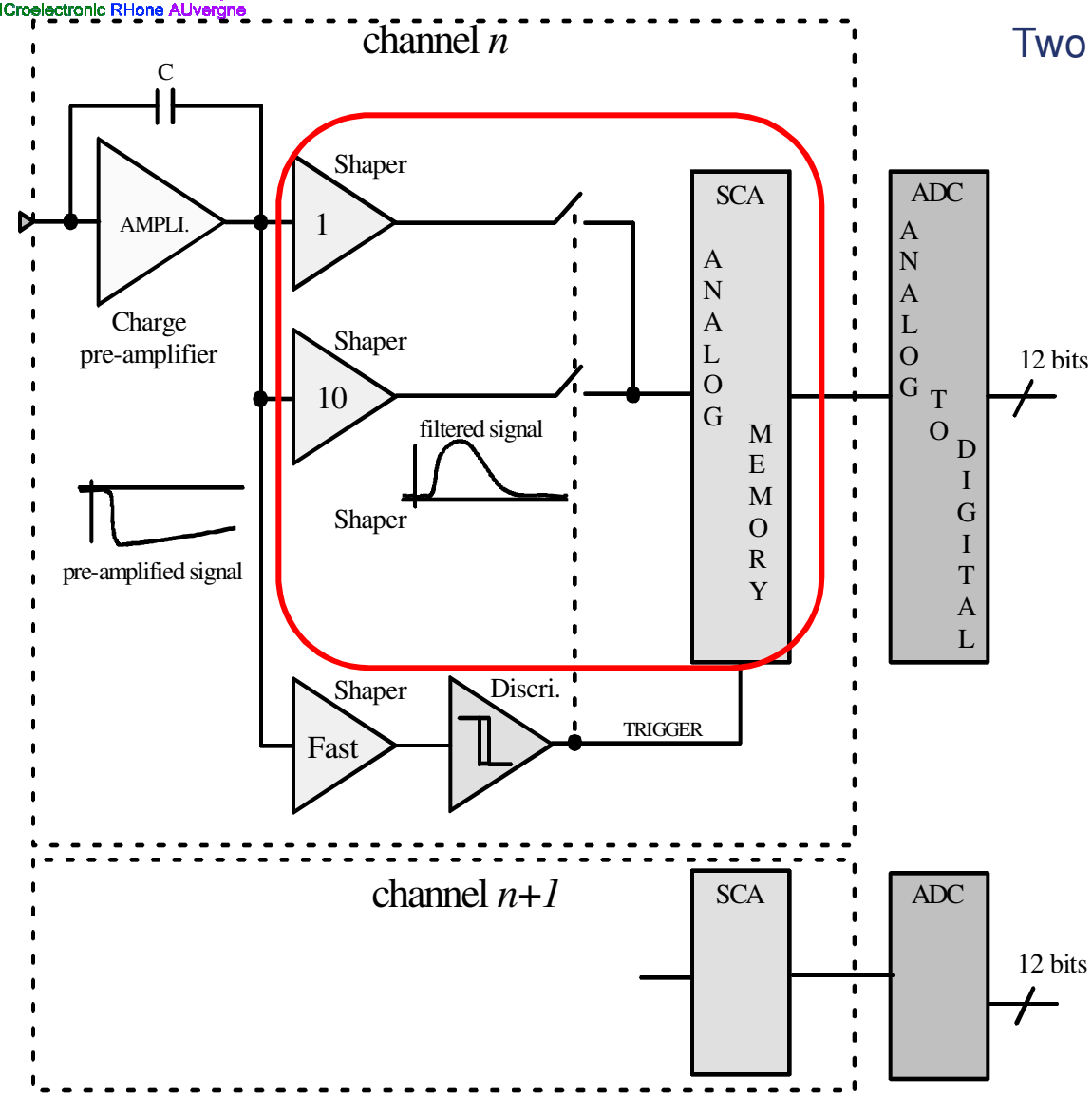
* without the digital block

** power pulsing with duty ratio of 1%

*** for one conversion

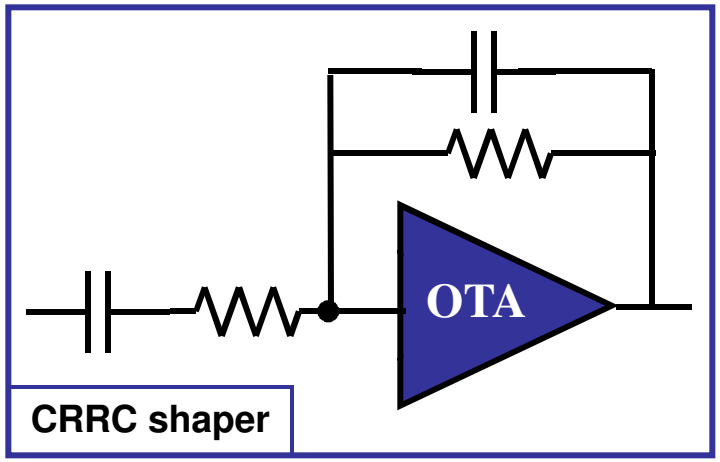
Equivalent to a Capacitance mismatch of about 1 fF !!

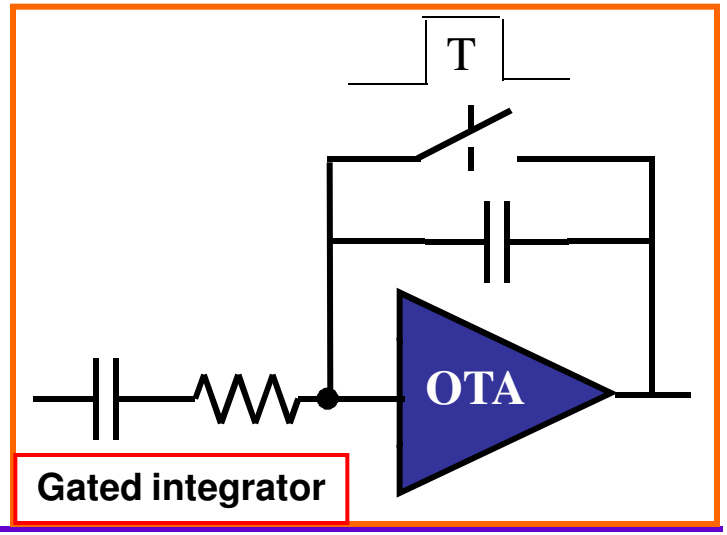
Shaper & analog memory



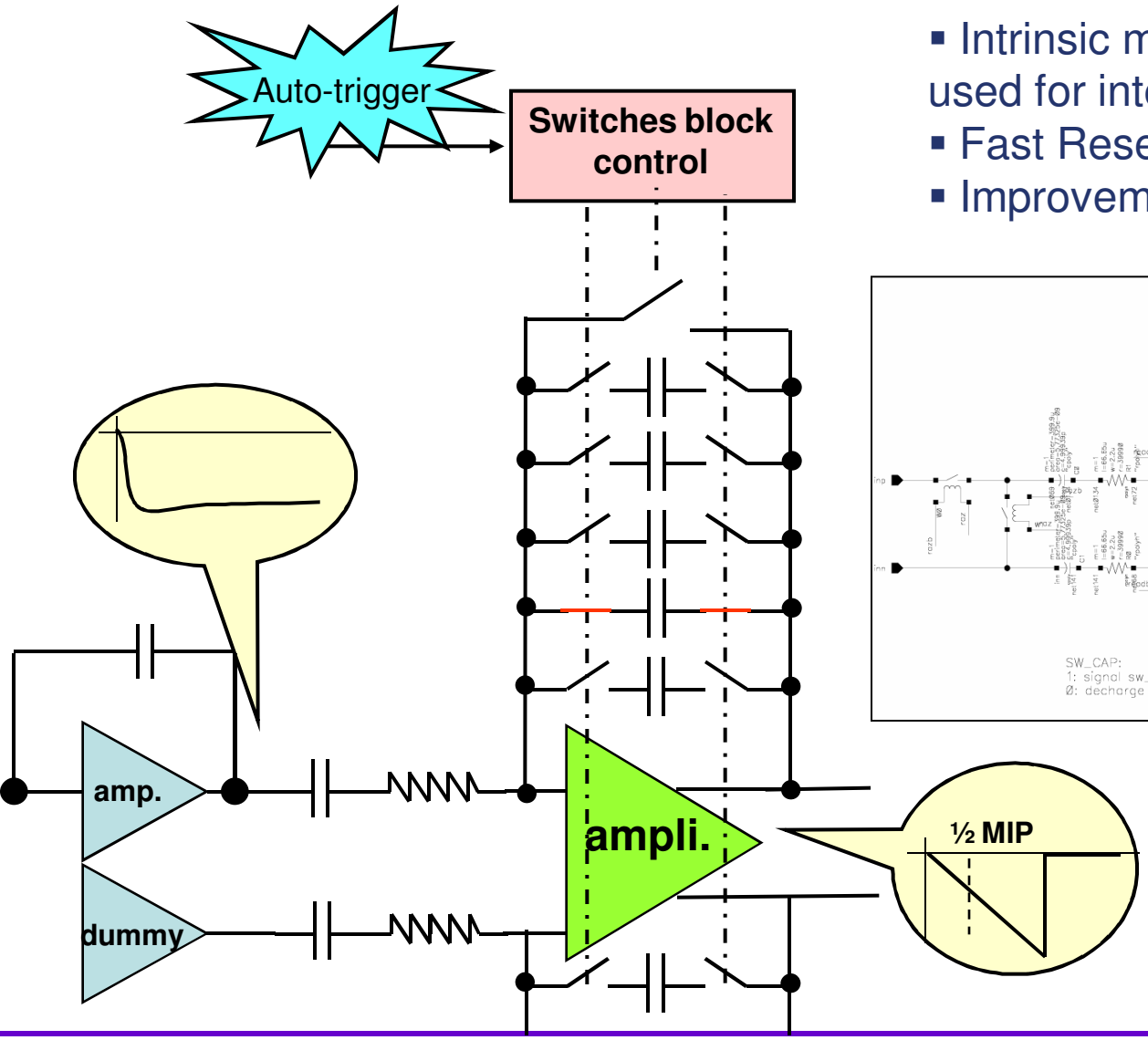
Two types of filtering:

- CRRC shaper → Skiroc chip
- gated integrator → to be evaluated

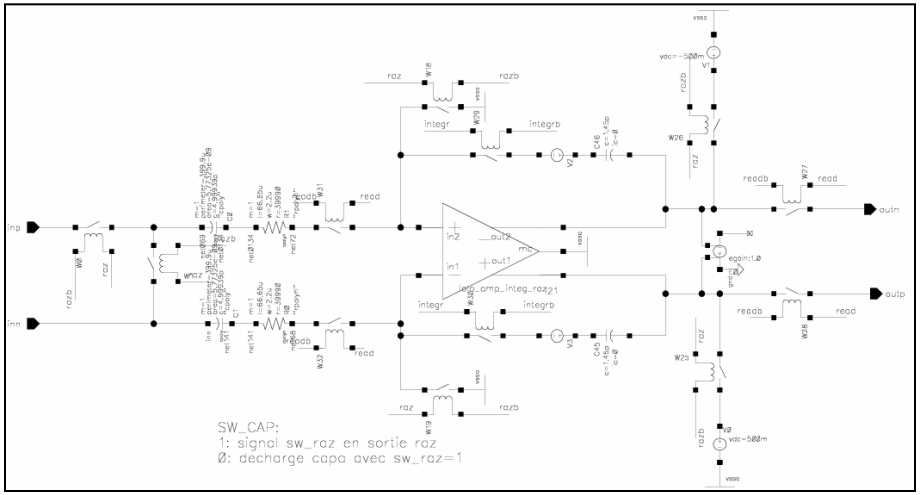




The gated integrator

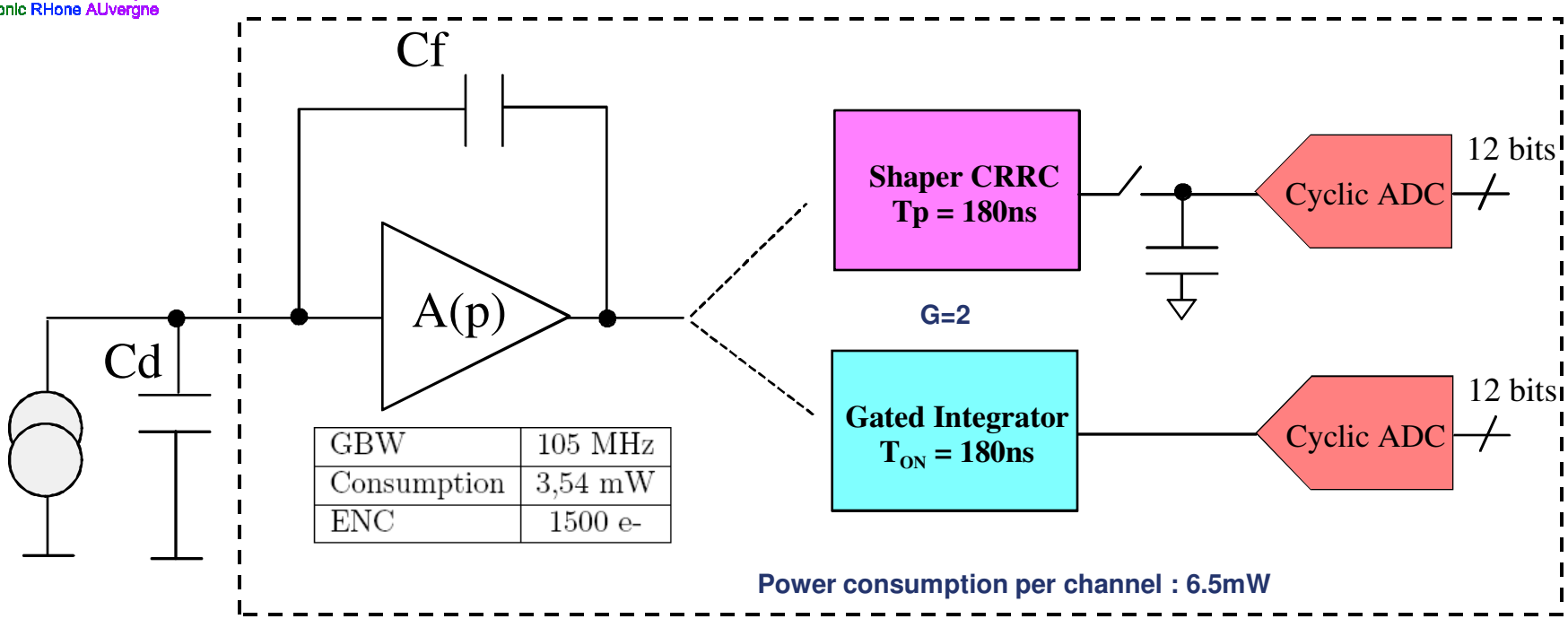


- Intrinsic memory with capacitor used for integration
- Fast Reset → less pile-up
- Improvement of the filtering ?

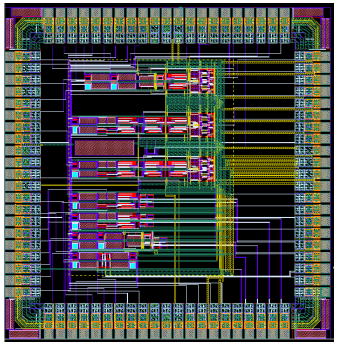


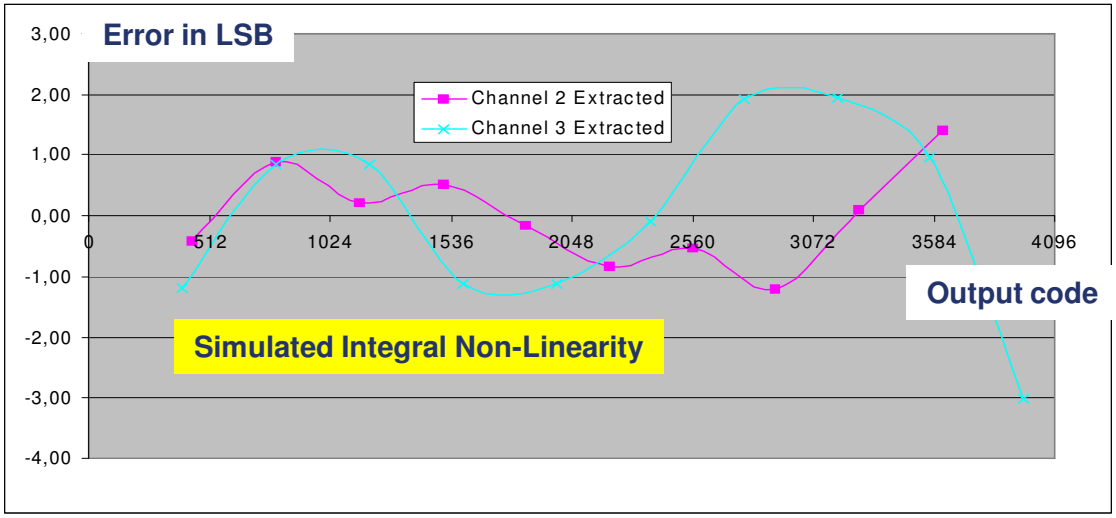
Simulated schematic view

Channel designed for evaluation



Chip submitted to run in July 09





Conclusion

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"Long is the road …"