PCB DEVELOPMENTS AT *IPNL*
(PCB and ASIC)

• PCB for 1m2 of RPC with HR2

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Collaboration with LAL

Calorimeter for ILC

1 m^2 PCB MAIN SPECIFICATIONS

(sane as 1 m2 with HR1)

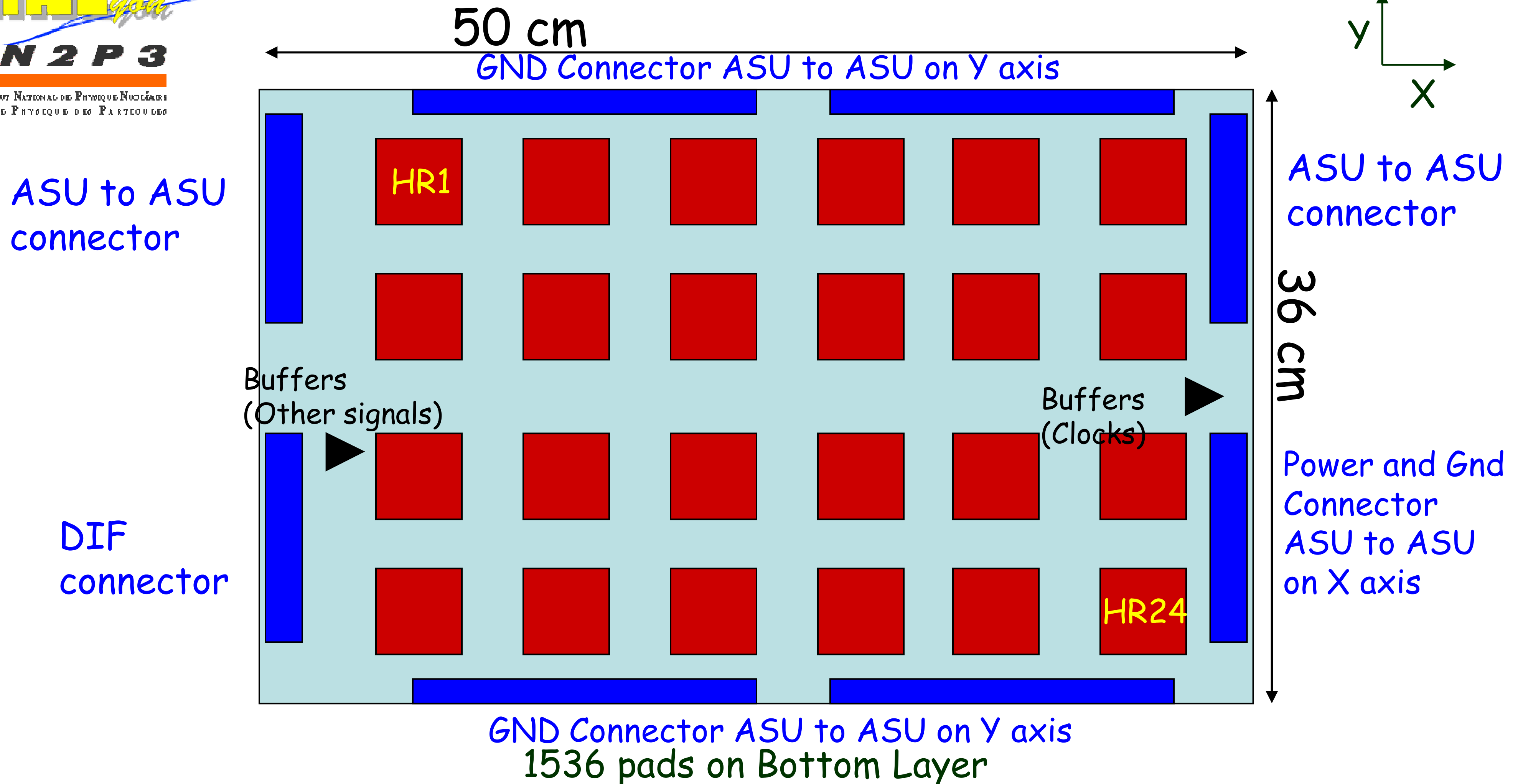
ASU PCB Design
- 24 x 64 1 sq cm pads
- 24 Hardrocs 2 Asics chained in plastic package (very thin 1.2 mm)

1 m2 PCB board :
- 6 ASUs
- 144 Hardroc2 Asics

DIF boards :
- 1 DIF for 2 ASU : 3 DIFs

HR2 :
- ✓ All modifications are implemented
- ✓ SC by pass
- ✓ SC Clocking and so on

ASU PCB DESIGN



- Buried and Blind Vias (Same as the last PCB with HR1 and first PCB with 4 HR)
- *Buffer are implemented but the board must work without buffers*

1 m² PCB DESIGN interconnection

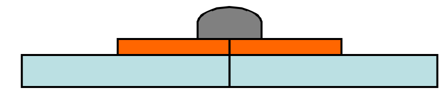
1 DIF for 2 ASUs

DIF Board

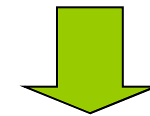
9216 pads on Bottom Layer

ASU to ASU Connection HR1

Solder or 0 ohm resistor



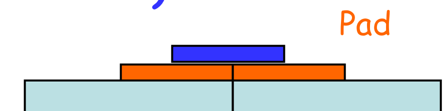
Mechanical Problems



Kapton cable

(return from manufacture next week)

Pad

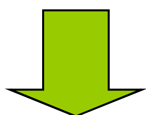


Calorimeter for ILC

1 m2 PCB DESIGN interconnection

1 DIF for 2 ASUs

Problems with 90 pins
Samtek connector :
Pad are teared off after
Several connect/disconnect
DIFF board



Add a ***kapton cable*** between
DIFF board and ASU
To reduce connection problems
(will be design next week)

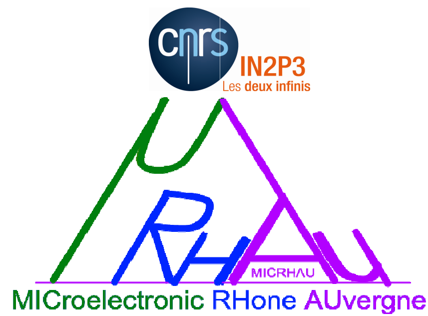
DIF Board

$1\ m^2$ PCB DESIGN (Layers and next steps)

- Layer 1 (TOP) : interconnect
- Layer 2 : GND
- Layer 3 : Digital signal
- Layer 4 : Power
- Layer 5 : GND
- Layer 6 : PADs to Hardroc 2
- Layer 7 : GND
- Layer 8 (BOTTOM) : PADs

Pads to HR2 interconnects are the same for the entire PCB (hierarchical design)

- *Send the first board to Fab last week for components welding*
- *The board will be fully tested at home in a few week*
- Manufacturing the other 5 boards after test results



ASIC DEVELOPMENT
IN
LYON

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(CNRS IN2P3 IPNL)

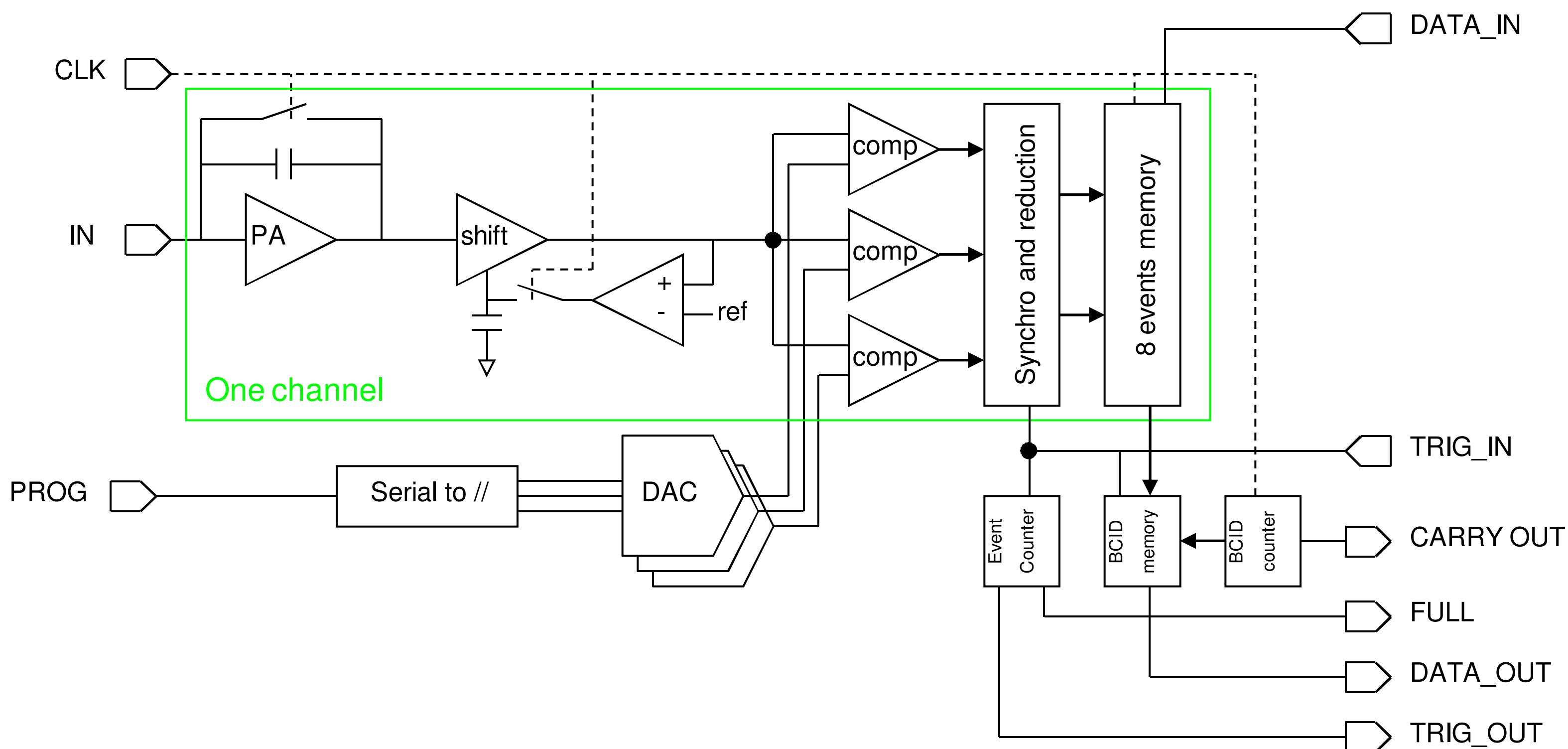
Collaboration with LAL/LAPP

Université Claude Bernard Lyon 1

Université Blaise Pascal

DIRAC synoptic

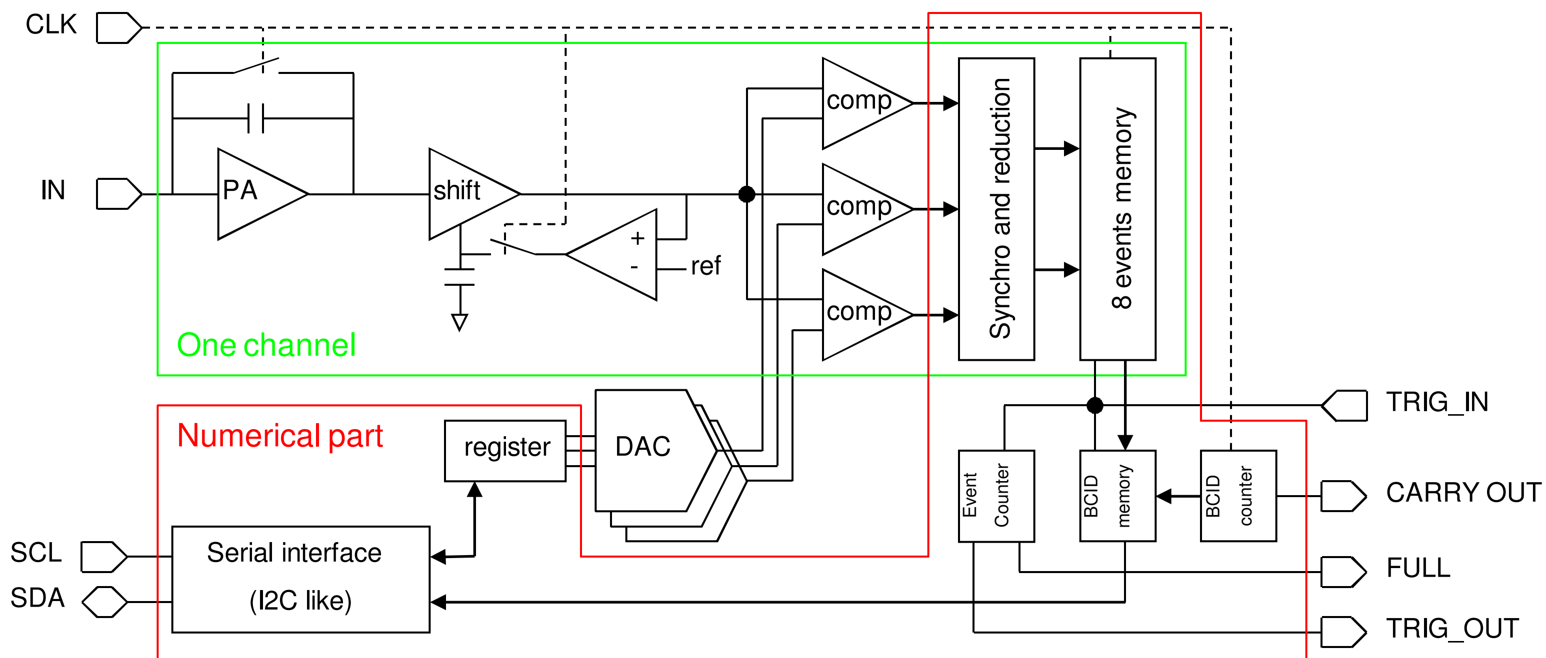
Compare input charge to 3 thresholds (set by 3 DACs) and store the 2 bits energy information



Configuration and read-out by shift register …

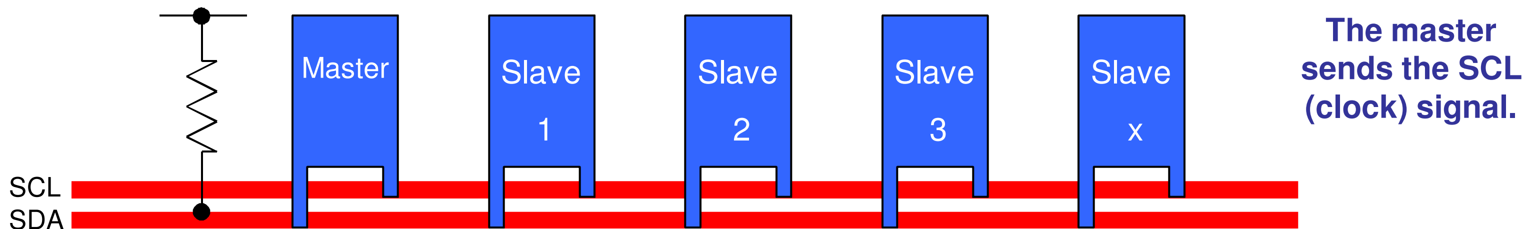
DIRAC synoptic

Proposal for the next DIRAC version :



A new read out and configuration interface based on an “I2C like” link

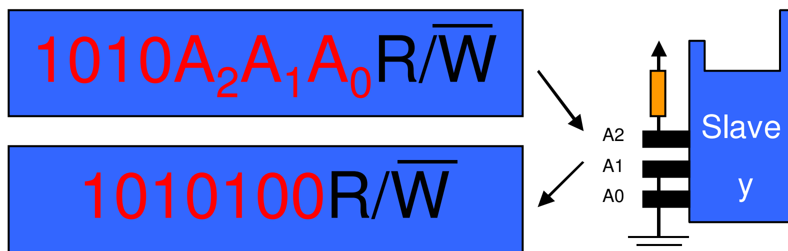
How does the serial interface work ?



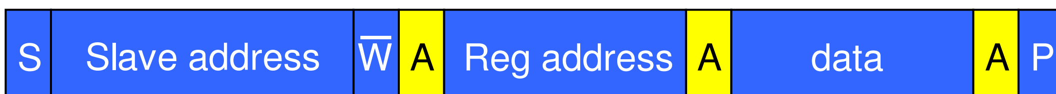
The master sends the SCL (clock) signal.

Each device is addressed individually by software with a unique address that can be modified by hardware pins.

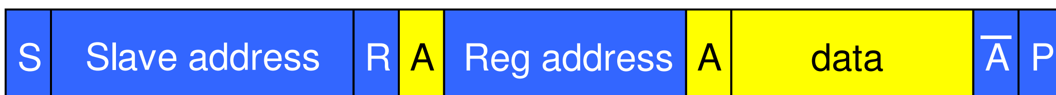
The open drain/collector outputs provide a "wired AND" connection that allows devices to be added or removed without impact.

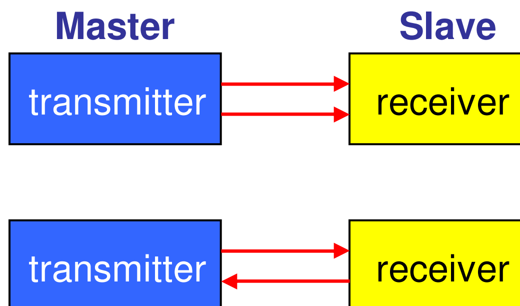


Write data



Read data





S = START CONDITION

A = ACKNOWLEDGE

P = STOP CONDITION

$R/\overline{W}$ = READ / WRITE not

$\overline{A}$ = not ACKNOWLEDGE

Advantages of the serial interface vs a shift register

- Individually addressed read out and slow control.
  - More flexible for the user
  - easier for the pilot firmware design (DIF board)

- The reading of sending parameters without rewriting them is possible.

- Board routing easier (without chips chaining).

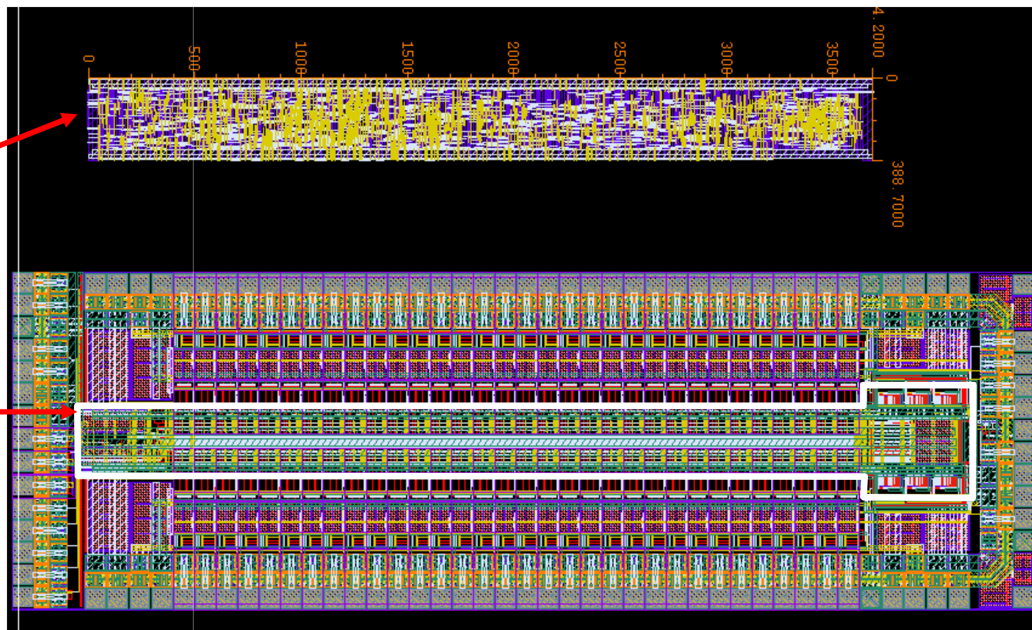
- Less sensitive to the risk of failure propagation.

All of these advantages for a small increase of the layout surface and for a similar power consumption (still to be measured).

Layout result

“new version” with serial interface : 1.432mm2

“old version” with shift register : 1.334mm2



- AMS 0.35 µm in CMOS process
- Design in VHDL.
- Synthesis with RTL compiler.
- Floorplanning and place and route with first Encounter (CADENCE tools).
- Return from fab on October

MICroelectronic RHone AUvergne

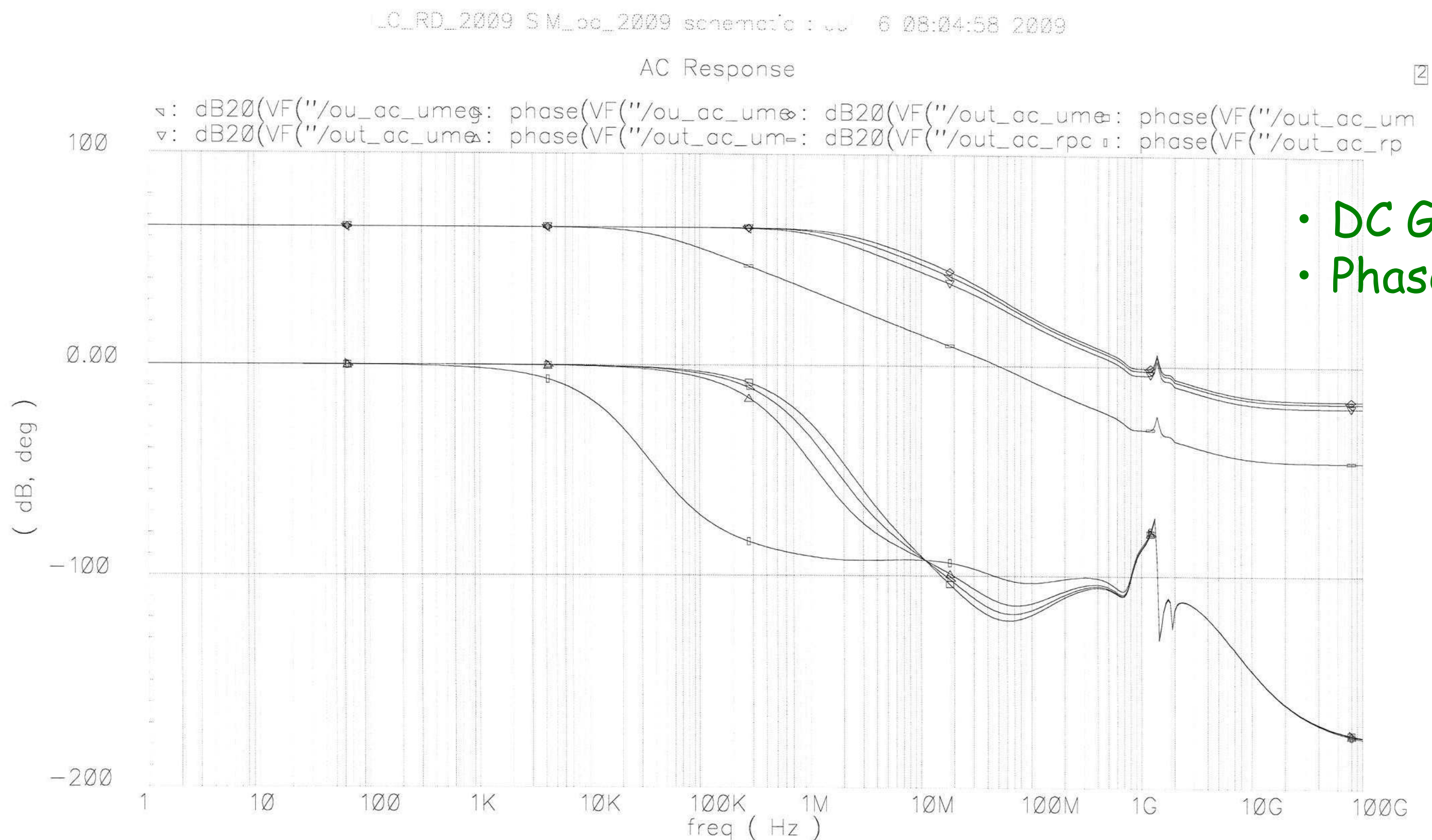
CSA for RPC/μMEGAS

- AMS 0.35 μm in CMOS process
- Switch integrator
- Folded cascode with feed forward compensation technique
- 4 gains (10pF 200fF 100fF 50fF)
  - 100 mV/pC, 4 mV/fC, 7 mV/fC, 10 mV/fC
- Main goal is to detect pulses as low as <u>2fC</u>
- Return from fab in October
  - Tests will be performed with standard comparator

MICroelectronic RHone AUvergne

Simulation results

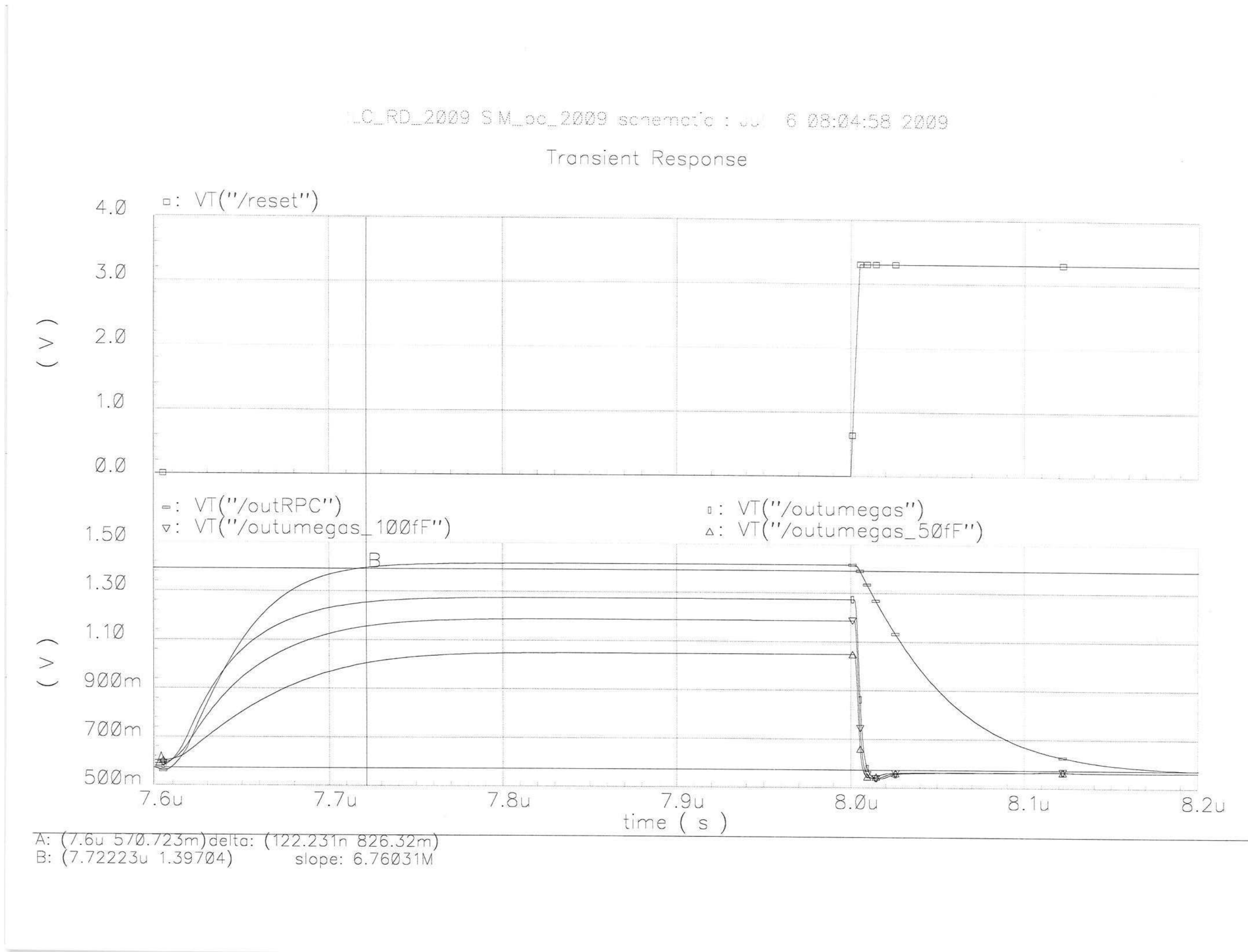
AC response for the 4 integrator capacitor



- DC Gain : 70dB
- Phase margin 70 deg

MICroelectronic RHone AUvergne

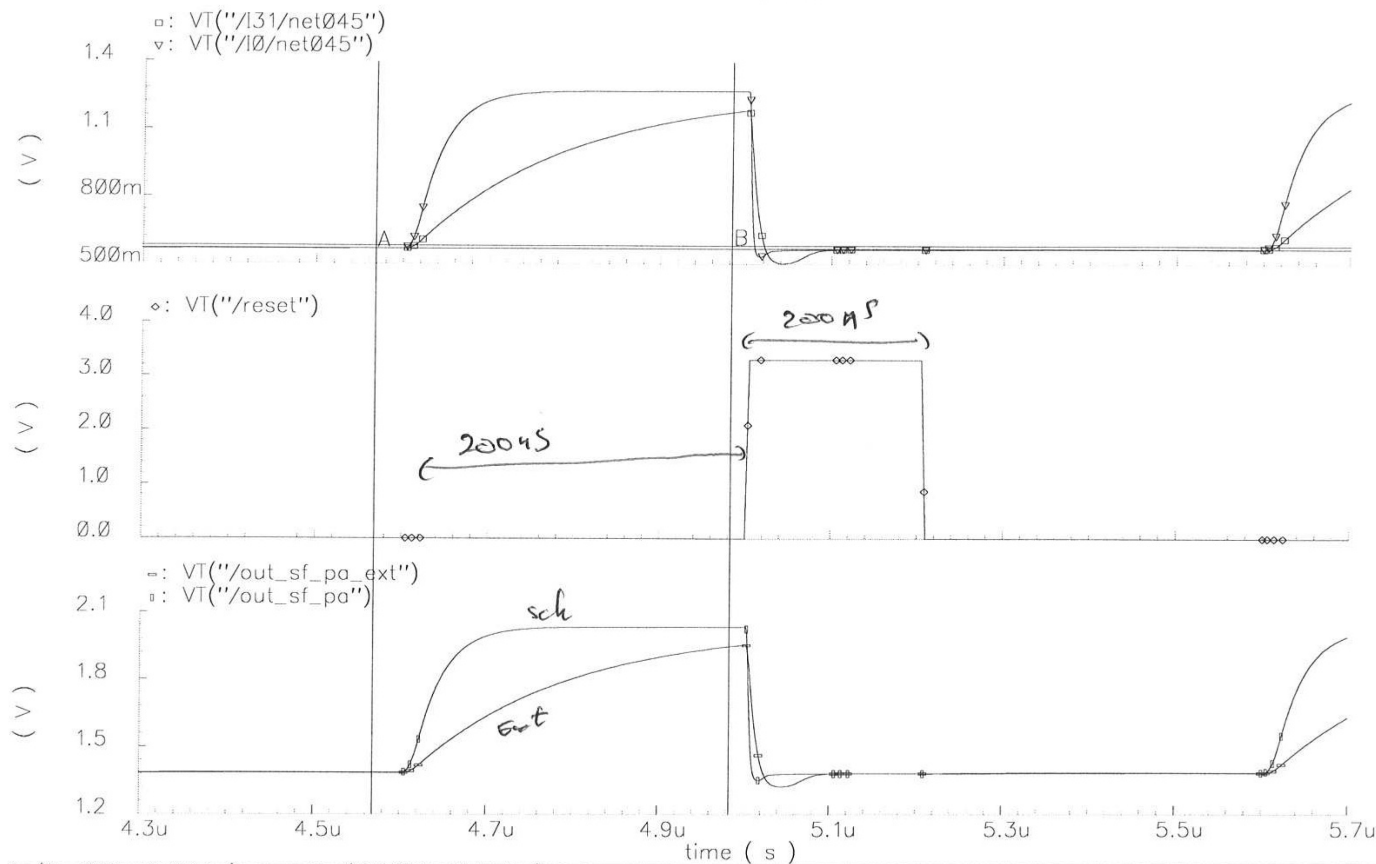
Simulation results



Qin

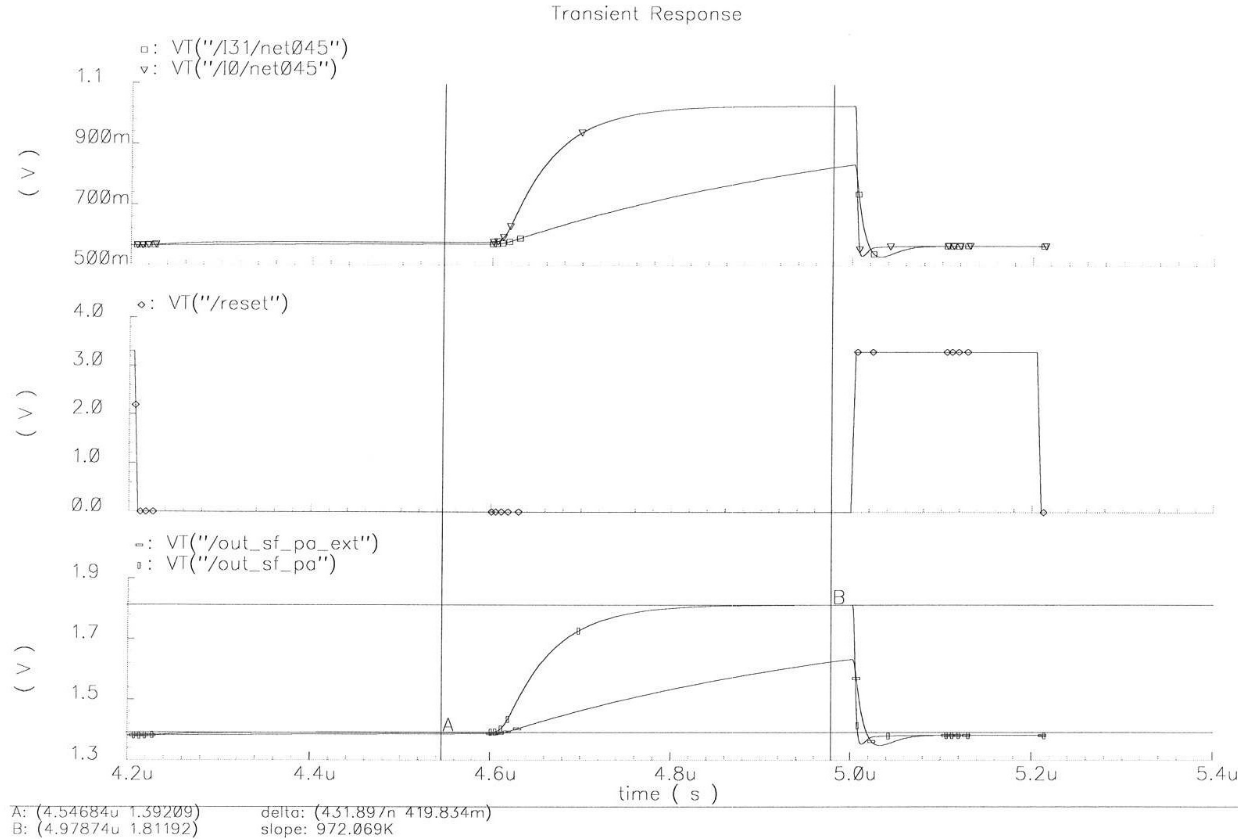
- 8.5 pC
- 170 fC
- 85 fC
- 42 fC

Simulation results



Qin = 170 fC
Cf = 200 fF

Simulation results



Qin = 42 fC
Cf = 50 fF

Conclusion

ASIC :

- Return from fab : October
- Tested before the end of this year
  - Digital part
  - Analog part
  - Mixed analog and digital

- Next step
  - Digital part can be implemented in DIRACx/HARDROCx