

Analog Channel for SiPM charge readout

Wei Shen

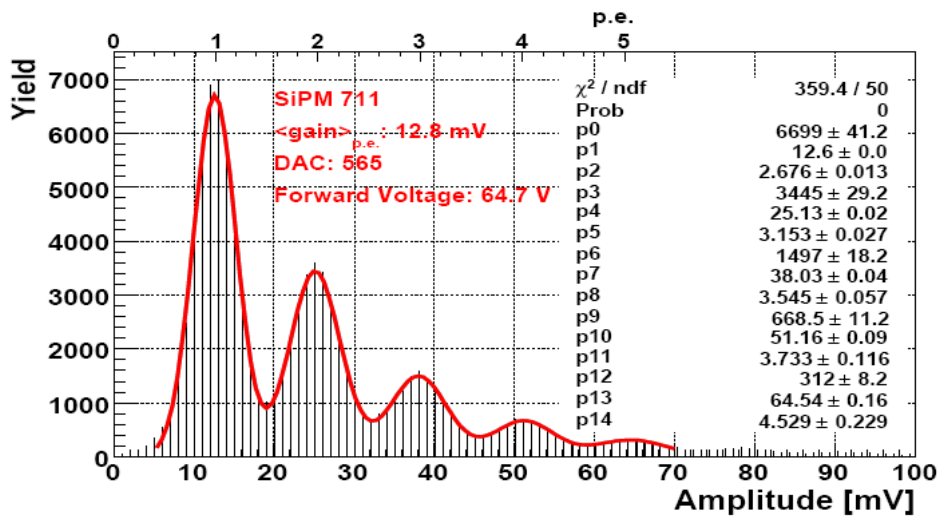
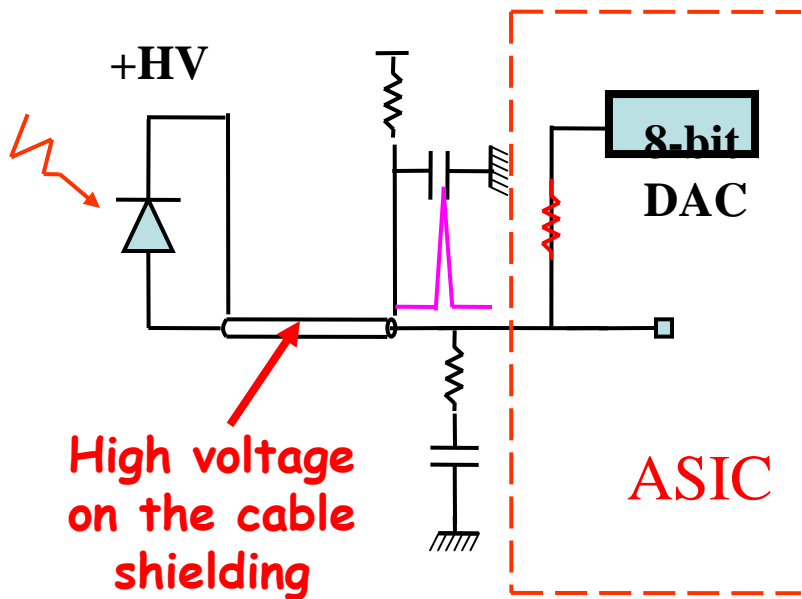


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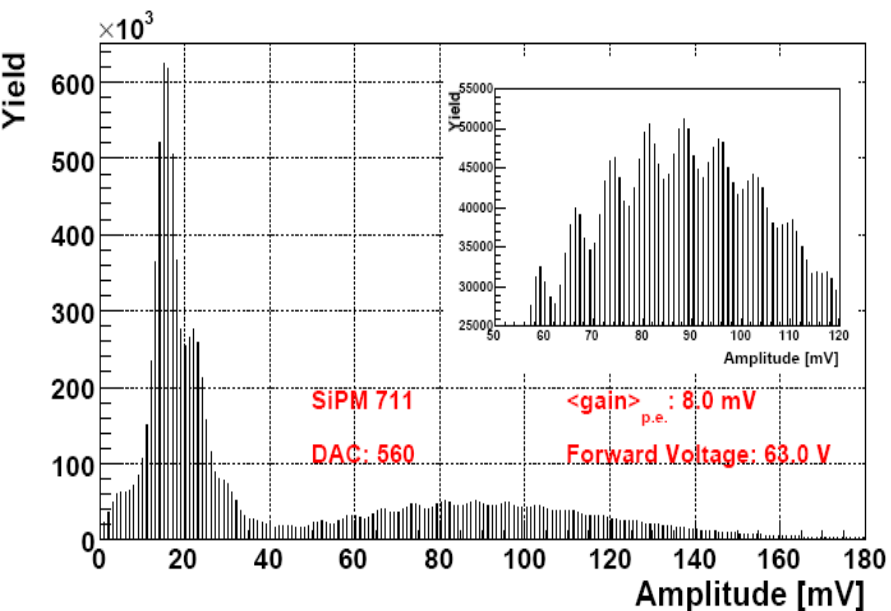


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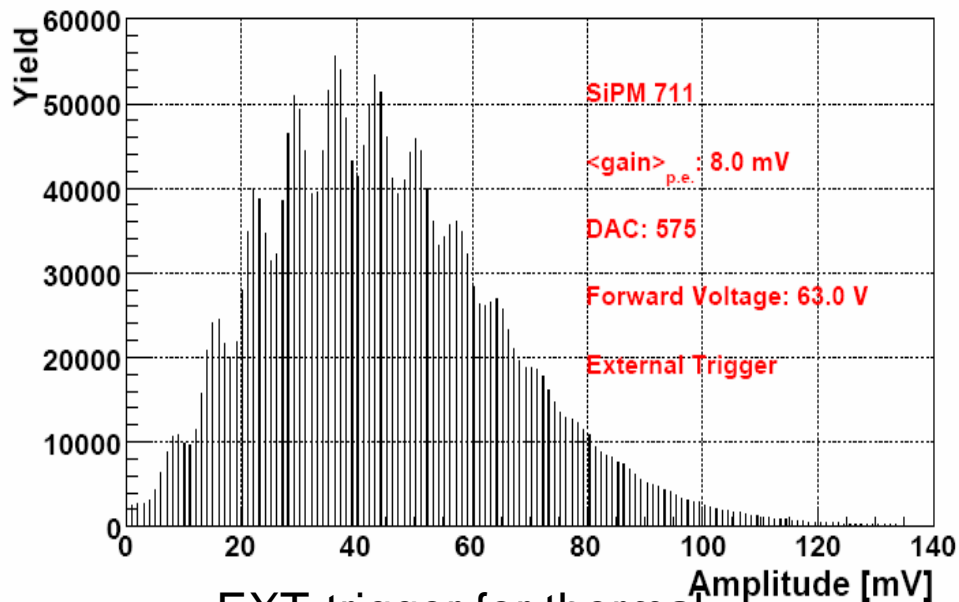


Auto-trigger for thermal noise, gain $\sim O(10^6)$



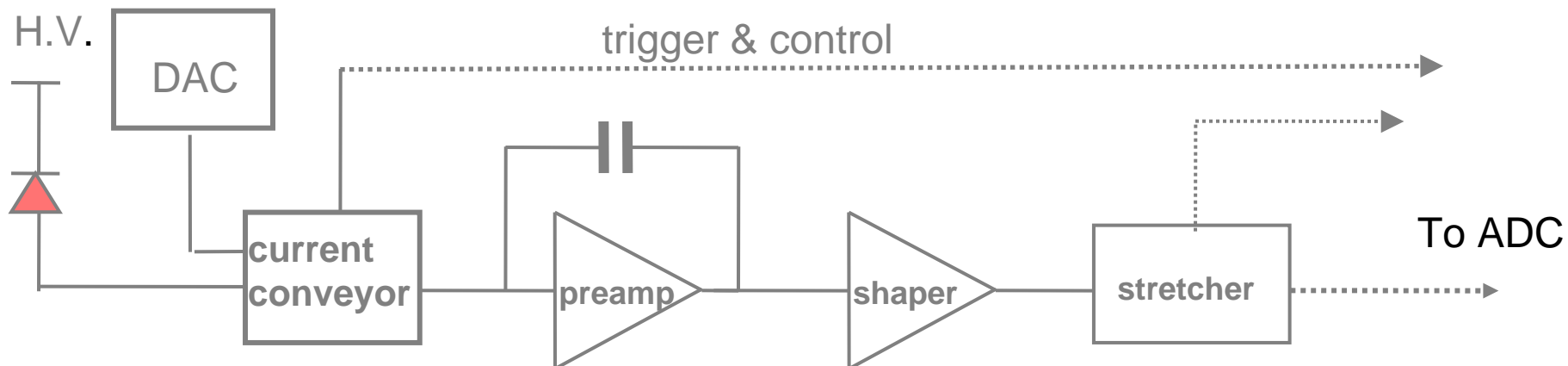
Sep. Auto-trigger for thermal noise, gain $\sim O(0.5 \cdot 10^6)$

Calice Lyon week 09



EXT-trigger for thermal noise, gain $\sim O(0.5 \cdot 10^6)$

single channel architecture



input DAC : gain tuning

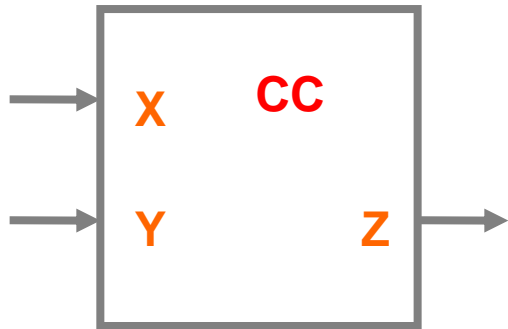
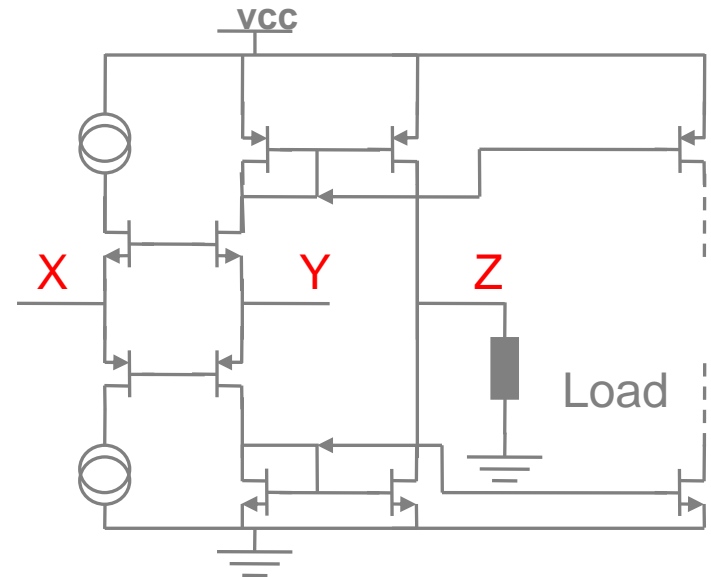
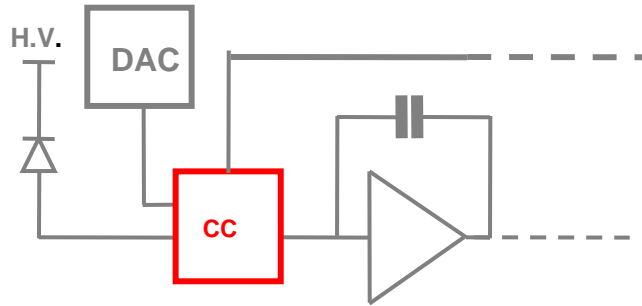
current conveyor : fast rising edge and large dynamic range

CSA : high signal to noise ratio

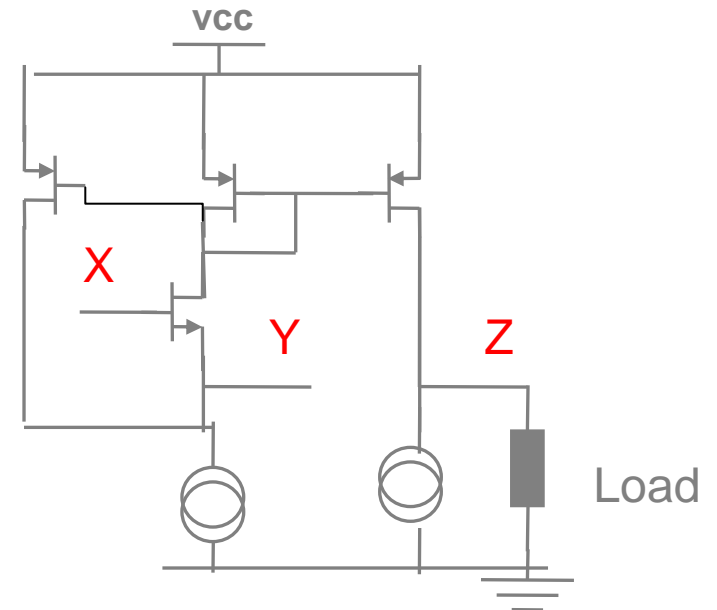
different shaping time : avoid pile up

AMS 0.35um CMOS technology

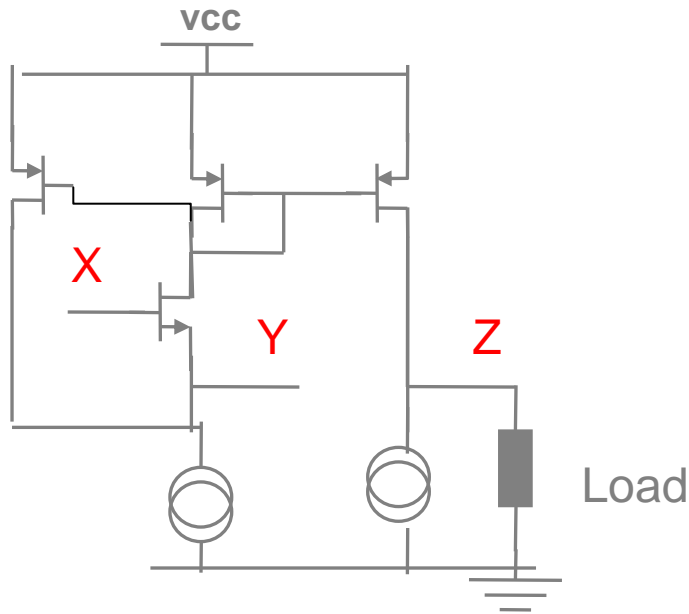
current conveyor



$$V_Y = V_X \quad I_Z = I_Y \quad I_X = 0$$



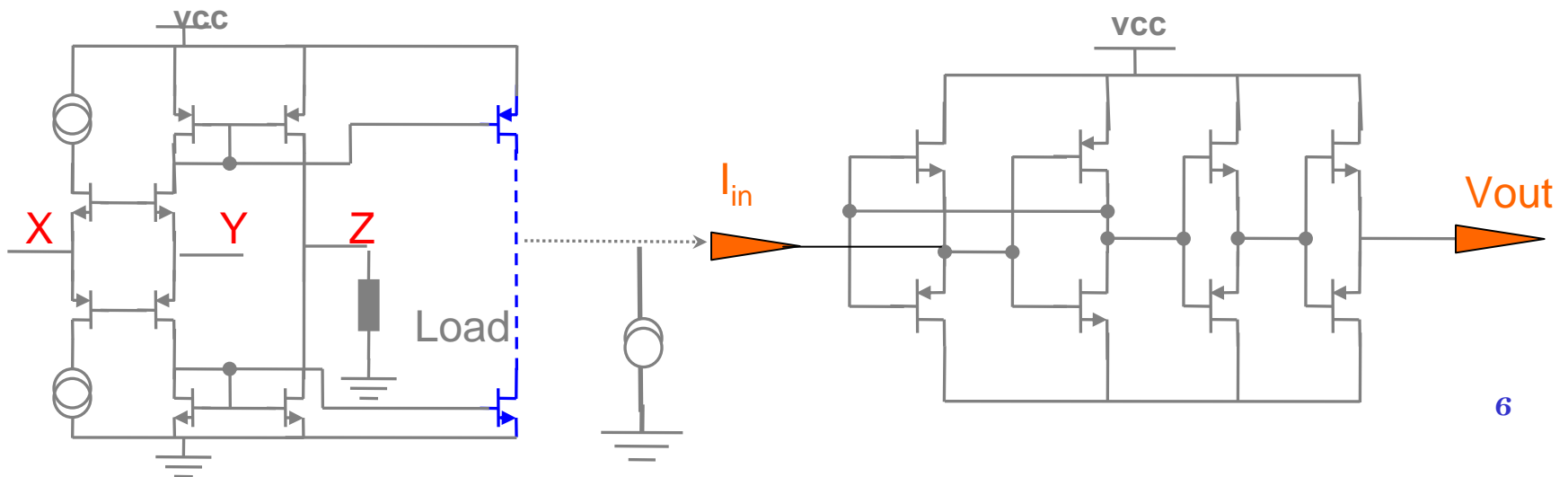
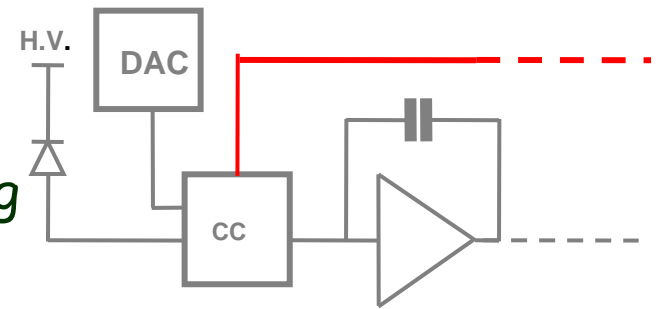
current conveyor : detail



1. Input impedance
2. Oscillation, due to output impedance of conveyor
3. undershoot

current comparator

- class B output stage & 3 inverter
- Latched output , low dc offset,
- low power consumption
- ~2 ns delay with leading edge triggering
- TTL logic output
- different threshold can be set for triggering (standby current)

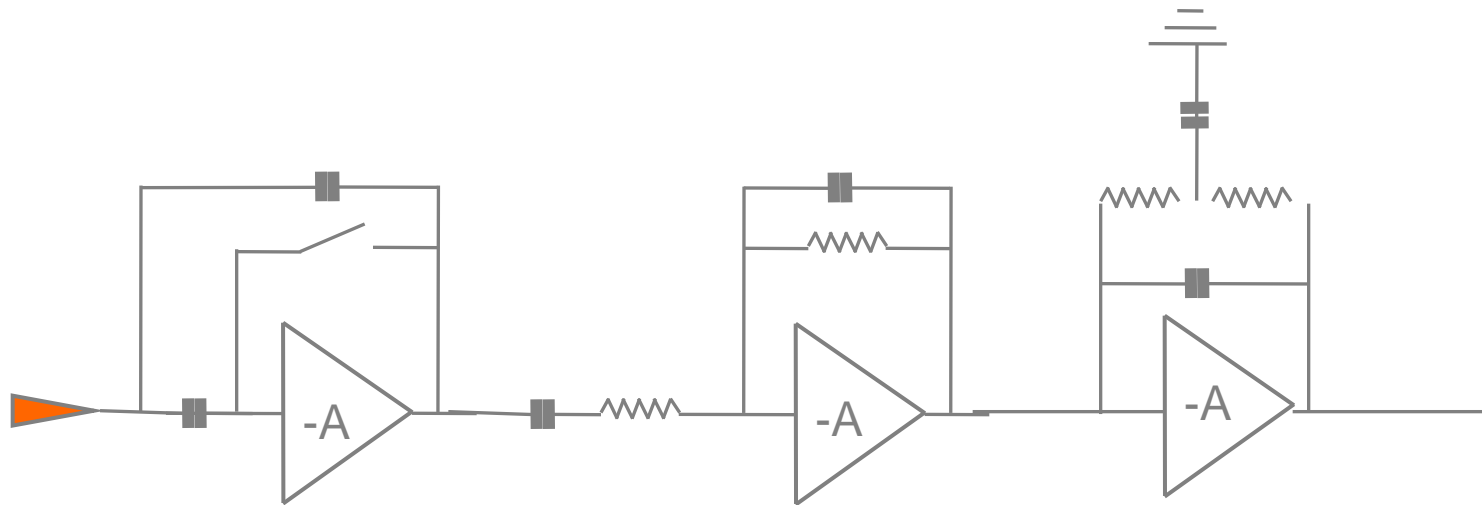


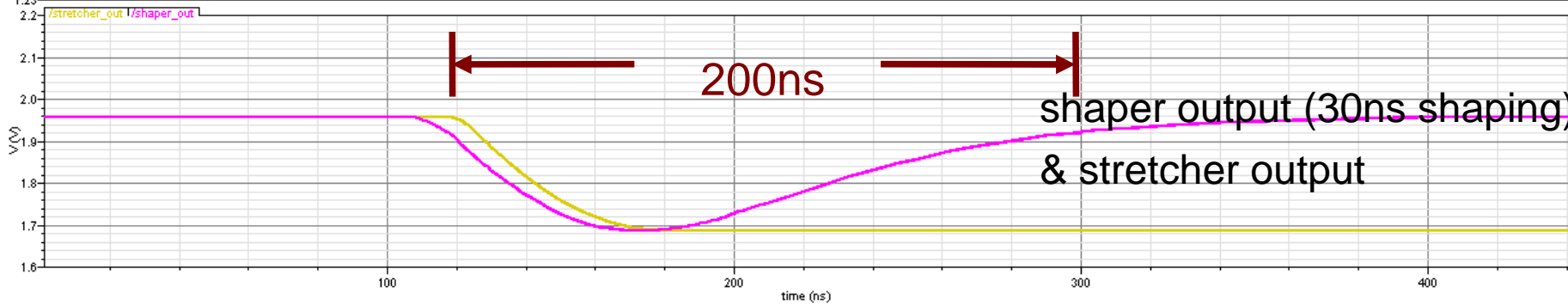
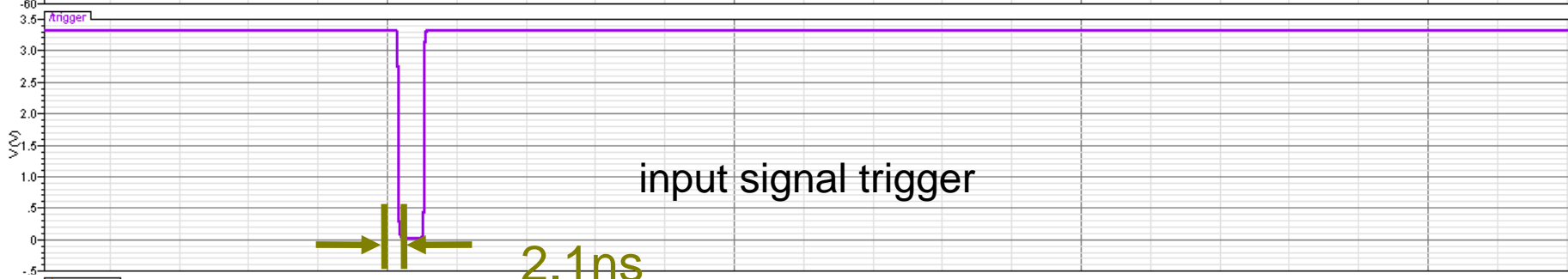
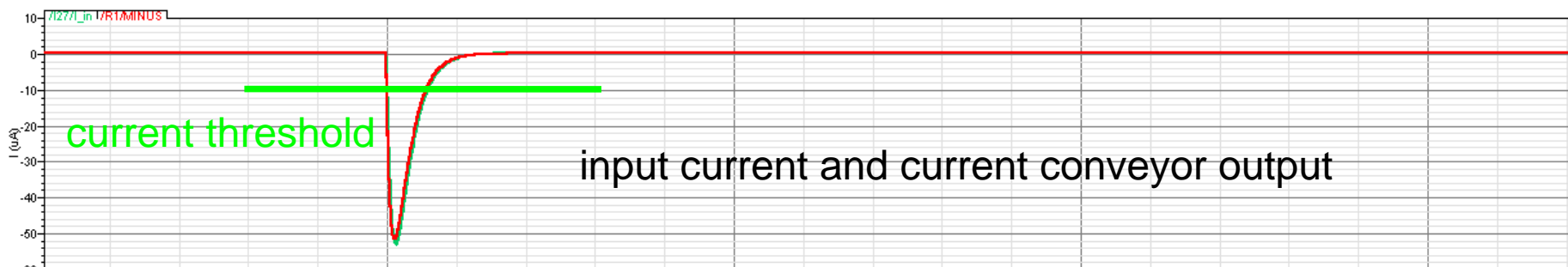
pre-amplifier + shaper

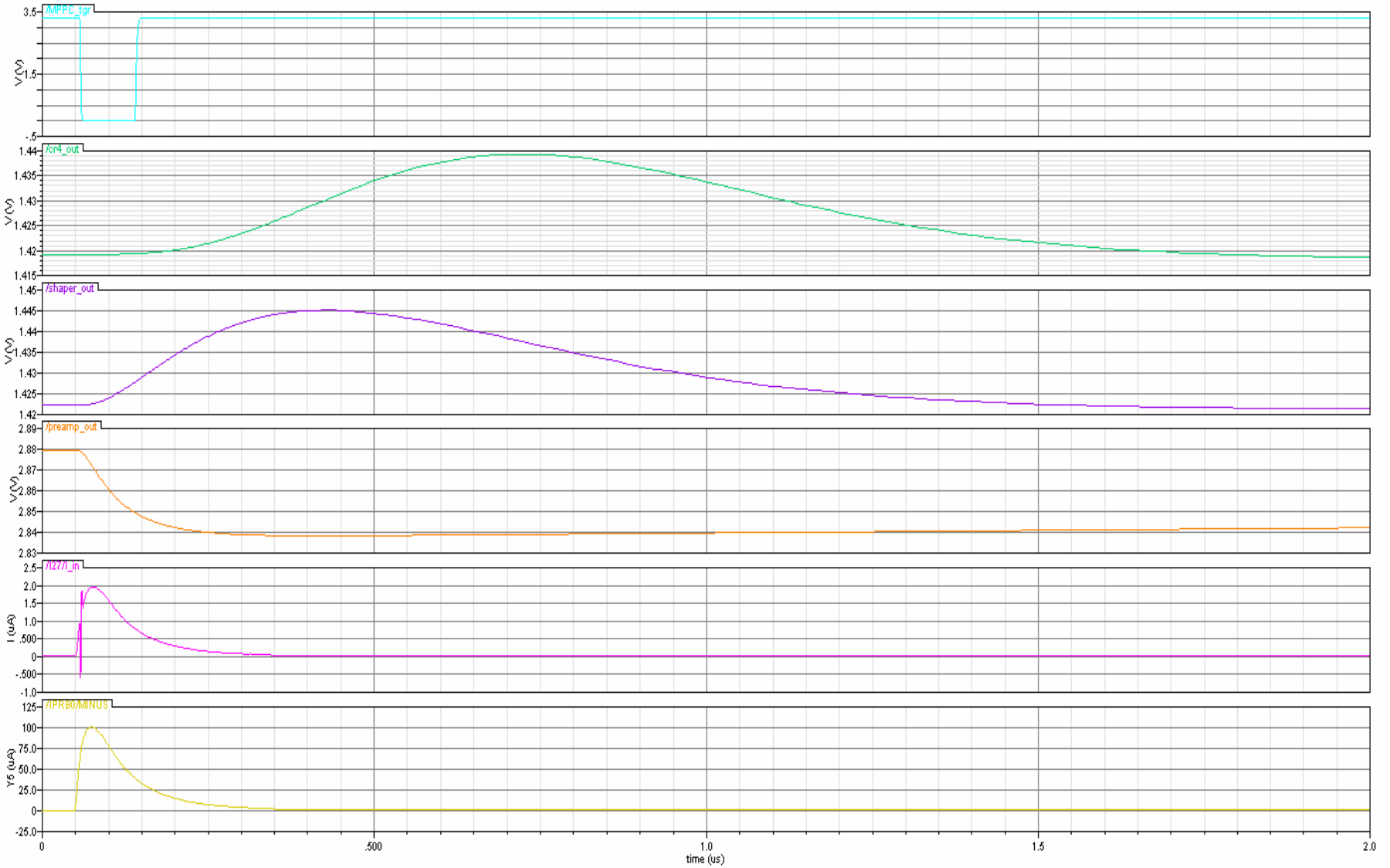
folded cascode structure

CR- (RC)4 shaper , shaping time (20ns - 200ns)

ballistic deficits







SUMMARY

- Analog channel designed for silicon photomultiplier
- High S/N ratio (>10 for single pixel w.r.t. $40fC$ charge)
- Narrow output to avoid pile up (20ns - 200ns)
- Fast trigger information (2ns delay for input current triggering)
- dynamic range : $\sim 200pC$

STATUS

- Layout : Preamp , shaper , discriminator
- Miniasic run in Oct.