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CALICE Calorimeter for ILC

Digital HCAL Electronics
Status of Electronics Production

Gary Drake

Argonne National Laboratory

CALICE Collaboration Meeting

Lyon, France

Sept. 16-18, 2009

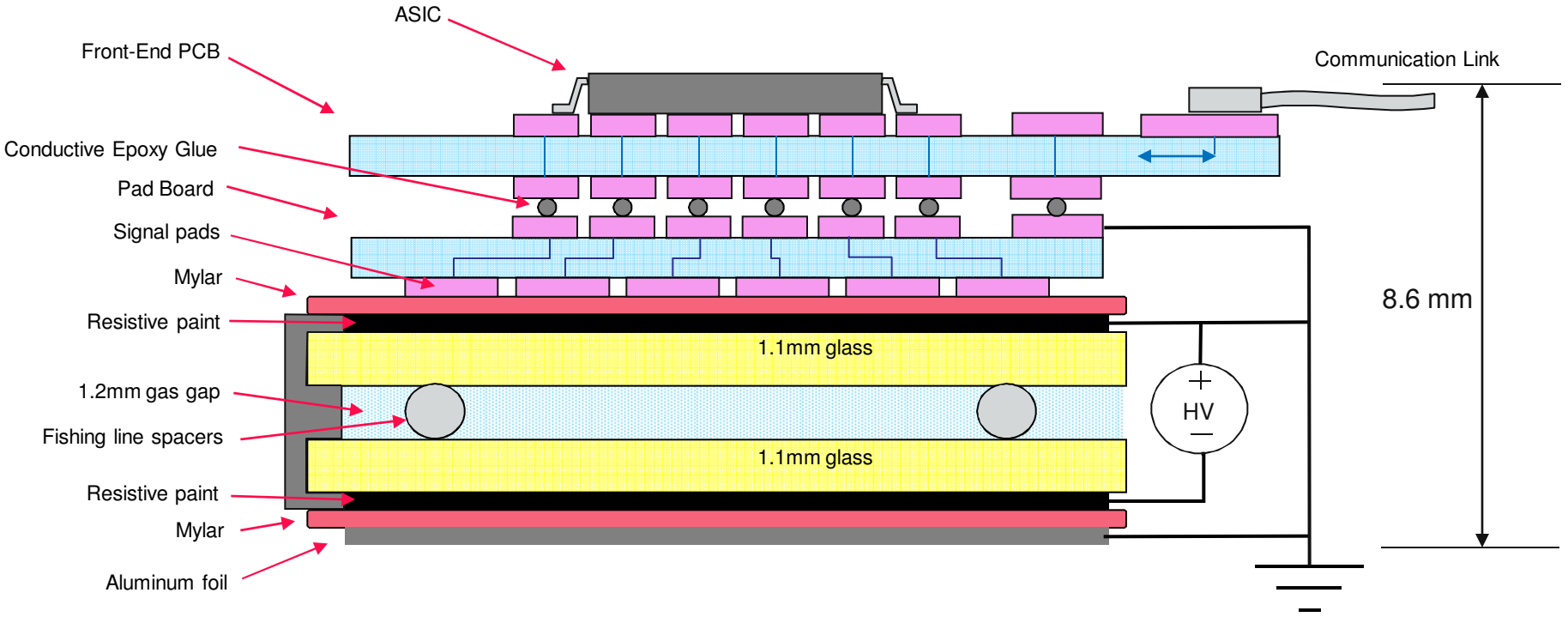
Representing the Work of Our DHCAL Group:

Burak Bilki, Iowa
John Butler, BU
Tim Cundiff, ANL
Vic Guarino, ANL
Bill Haberichter, ANL
Eric Hazen, BU
Jim Hoff, FNAL
Scott Holm, FNAL
Andrew Kreps, ANL
Ed May, ANL
G. Mavromanolakis, FNAL
Ed Norbeck, Iowa
David Northacker, Iowa
Yasar Onel, Iowa
José Repond, ANL
Jim Schlereth, ANL
Shouxiang Wu, BU
Jacob Smith, ANL/UTA
Lei Xia, ANL
Dave Underwood, ANL
Andy White, UTA
Ken Wood, FNAL
Jae Yu, UTA
Qingmin Zhang, Beijing

BOLD = Electronics Design Contributions

Detector Configuration

Current Construction:



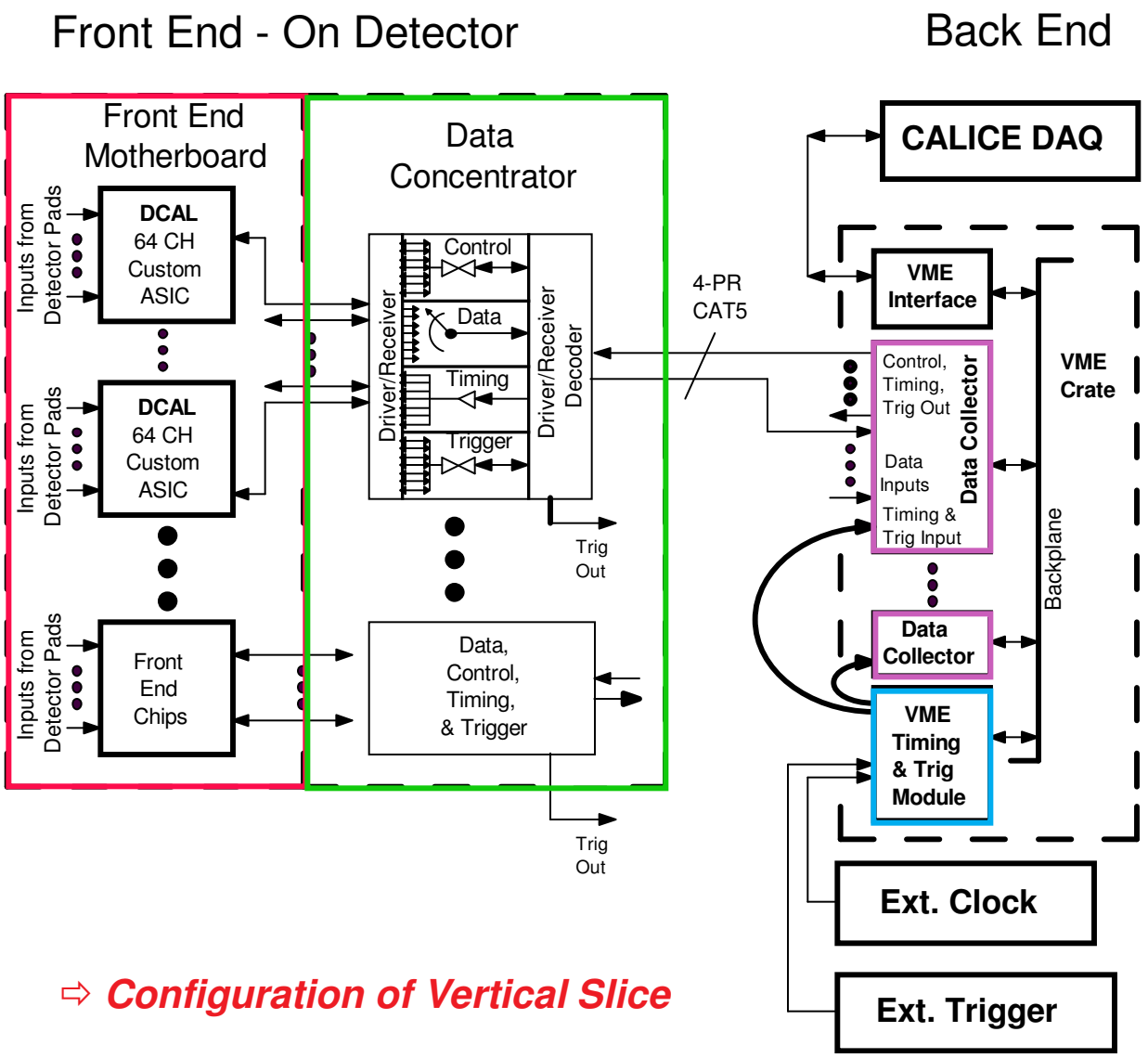
General System Specifications & Design Decisions

- Front-end instrumentation to use 64-channel custom ASIC
  - 1 cm^2 pads, 1 $meter^2$ planes, 40 planes, → ***400,000 channels***
- Front-end channel consists of amplifier/shaper/discriminator
- ***Single programmable threshold*** → 1 bit dynamic range
  - Threshold DAC has 8-bit range
  - Common threshold for all 64 channels per ASIC
- ***2 gain ranges***
  - High gain for GEMs (10 fC - ~200 fC signals)
  - Low gain for RPCs (100 fC - ~10 pC signals)
- 100 nSec time resolution
- ***Timestamp each hit***
  - 1 second dynamic range → 24 bits @ 100 nSec
  - Synchronize timestamps over system
- ***Data from FE consists of hit pattern in ASIC + timestamp***
  - 24 bit timestamp + 64 hit bits = 88 bits (+ address, error bits, etc.)
  - Readout format: 16 bytes per ASIC

General System Specifications & Design Decisions (Continued)

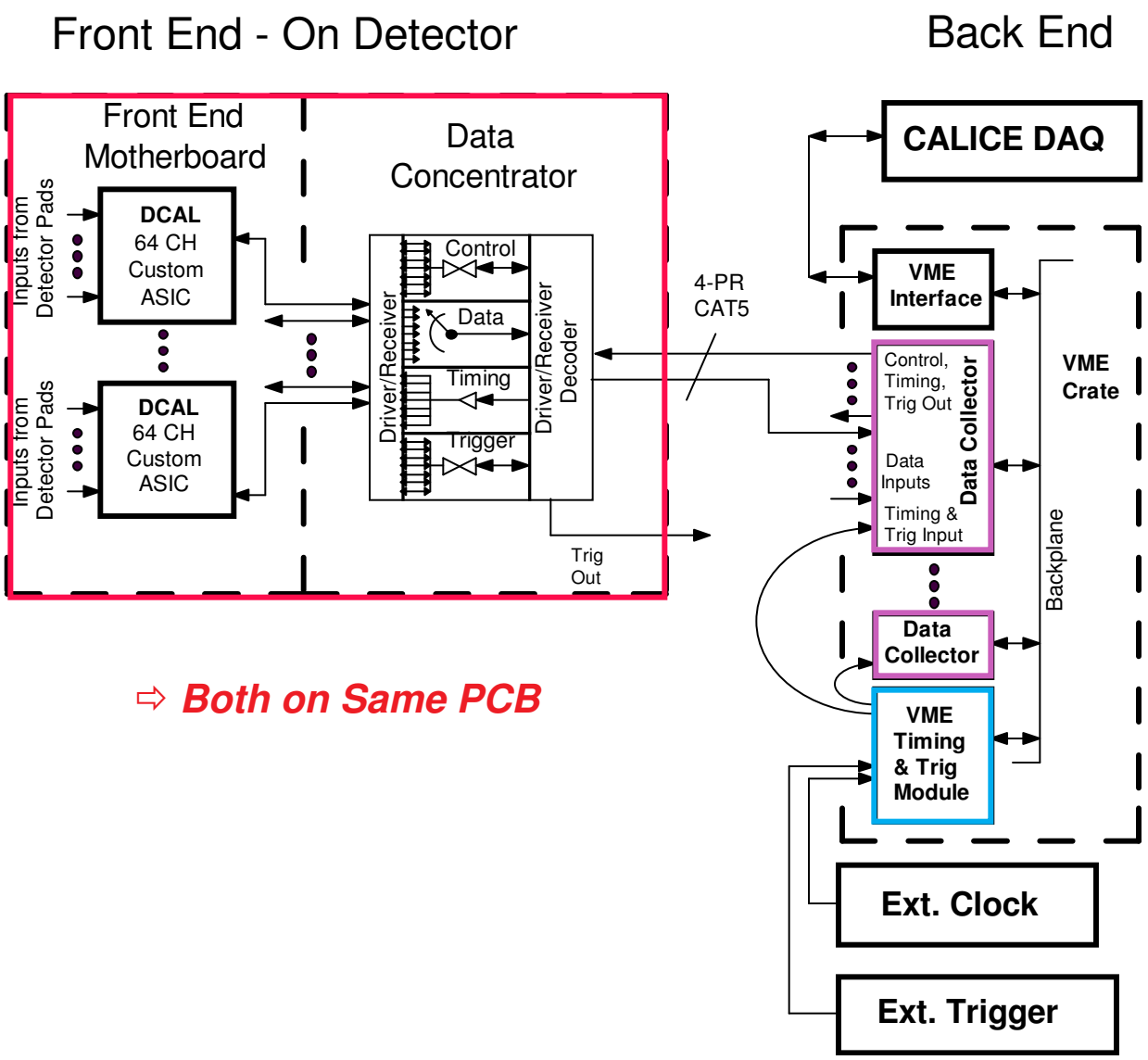
- Capability for ***Self Triggering*** → Noise, Cosmic rays
- Capability for **External Triggering** → Primary method for beam events
  - 20-stage pipeline → 2 μSec latency @ 100 nSec
- Capability of FE to source prompt Trigger Bit (simple OR of all disc.)
- Capability to store up to 7 triggers in ASIC output buffer (FIFO)
- Design for 100 Hz (Ext. Trig) nominal rate
- ***Deadtimeless Readout***
- Zero-suppression implemented in front-end
- On-board charge injection with programmable DAC
- Design for 10% occupancy
- Concatenate data in front-ends
- Use serial communication protocols
- Slow controls separate from data output stream
- Compatibility with CALICE DAQ

Original System Block Diagram – Sept. 2007



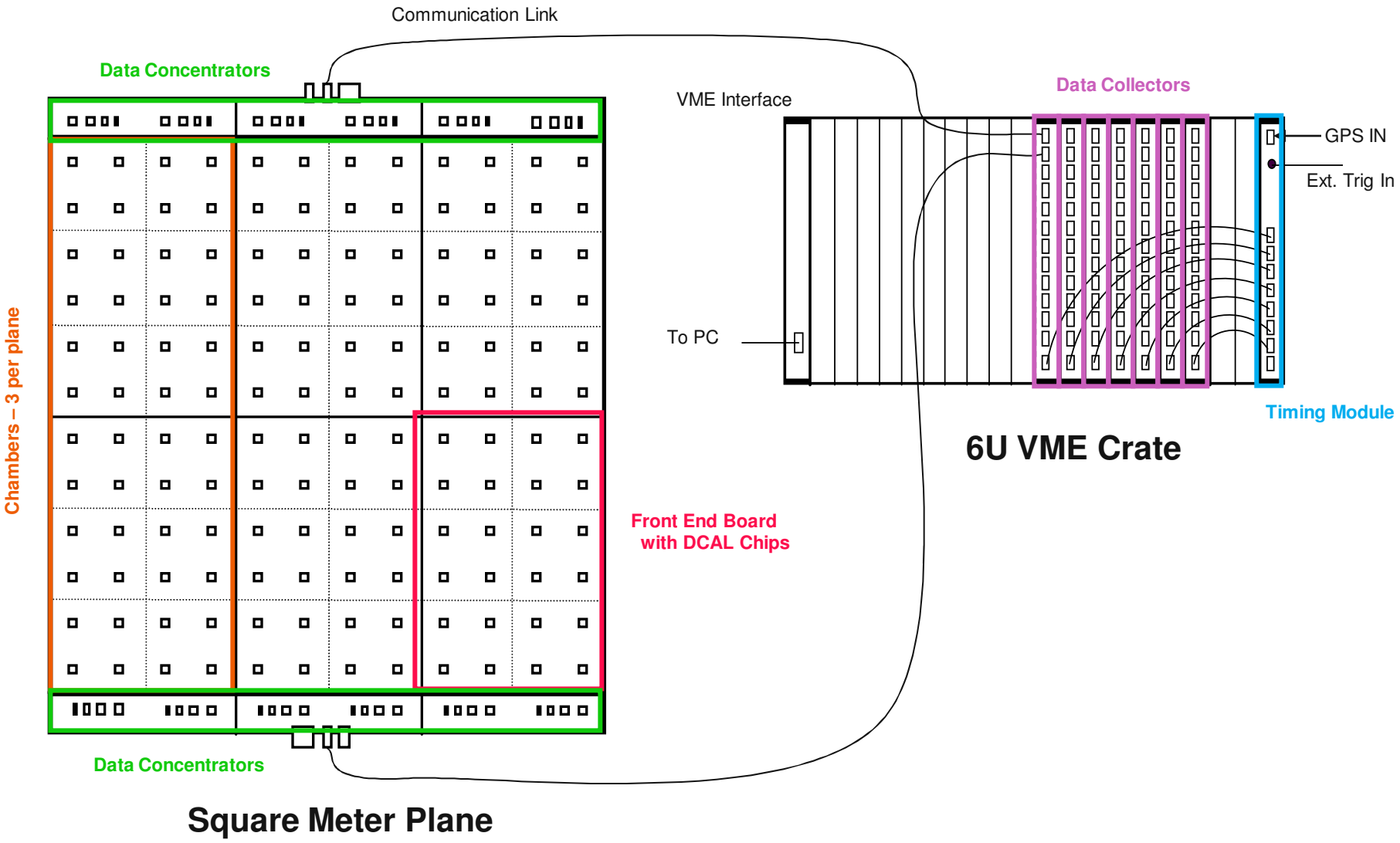
⇨ ***Configuration of Vertical Slice***

Final System Block Diagram

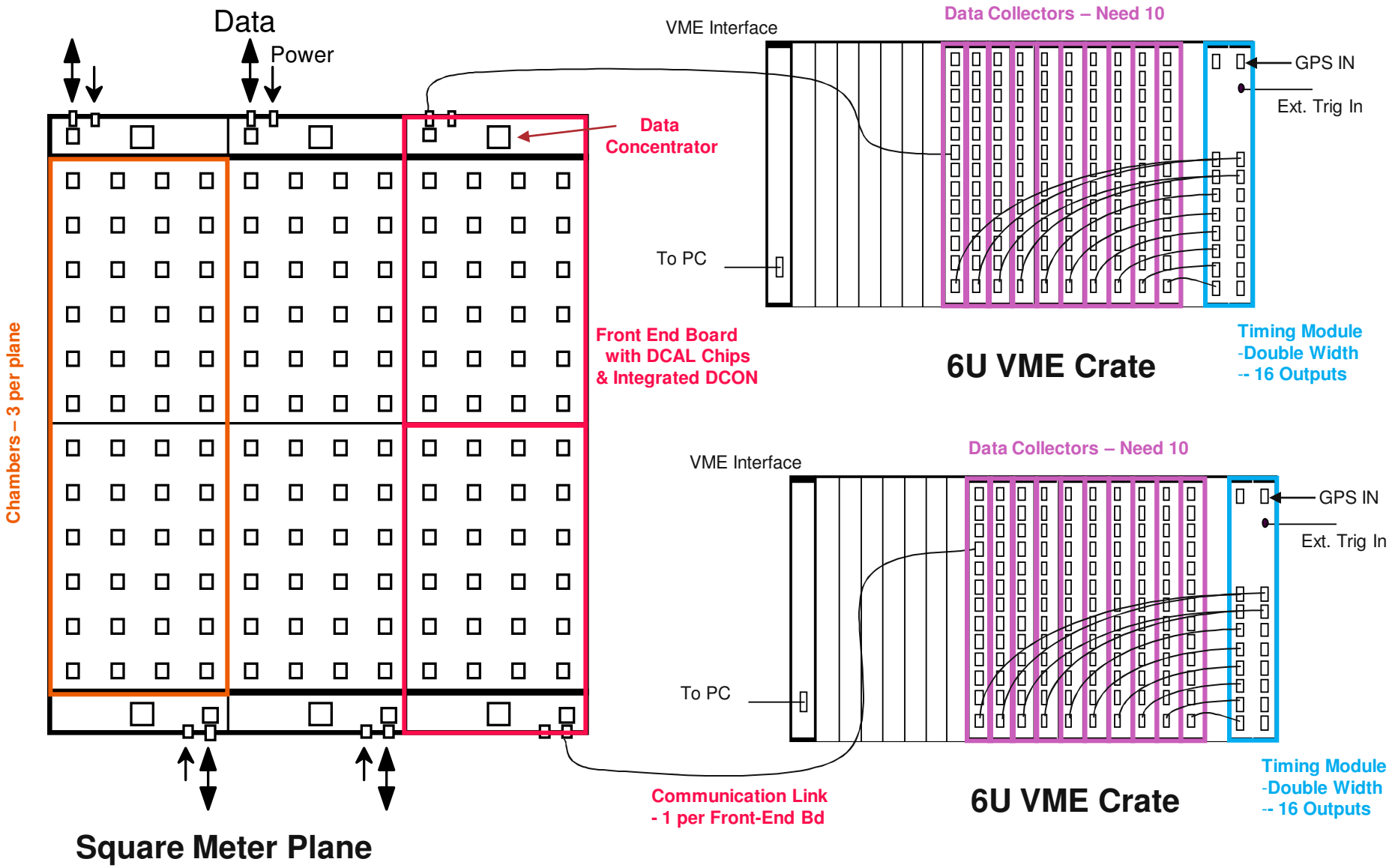


⇨ ***Both on Same PCB***

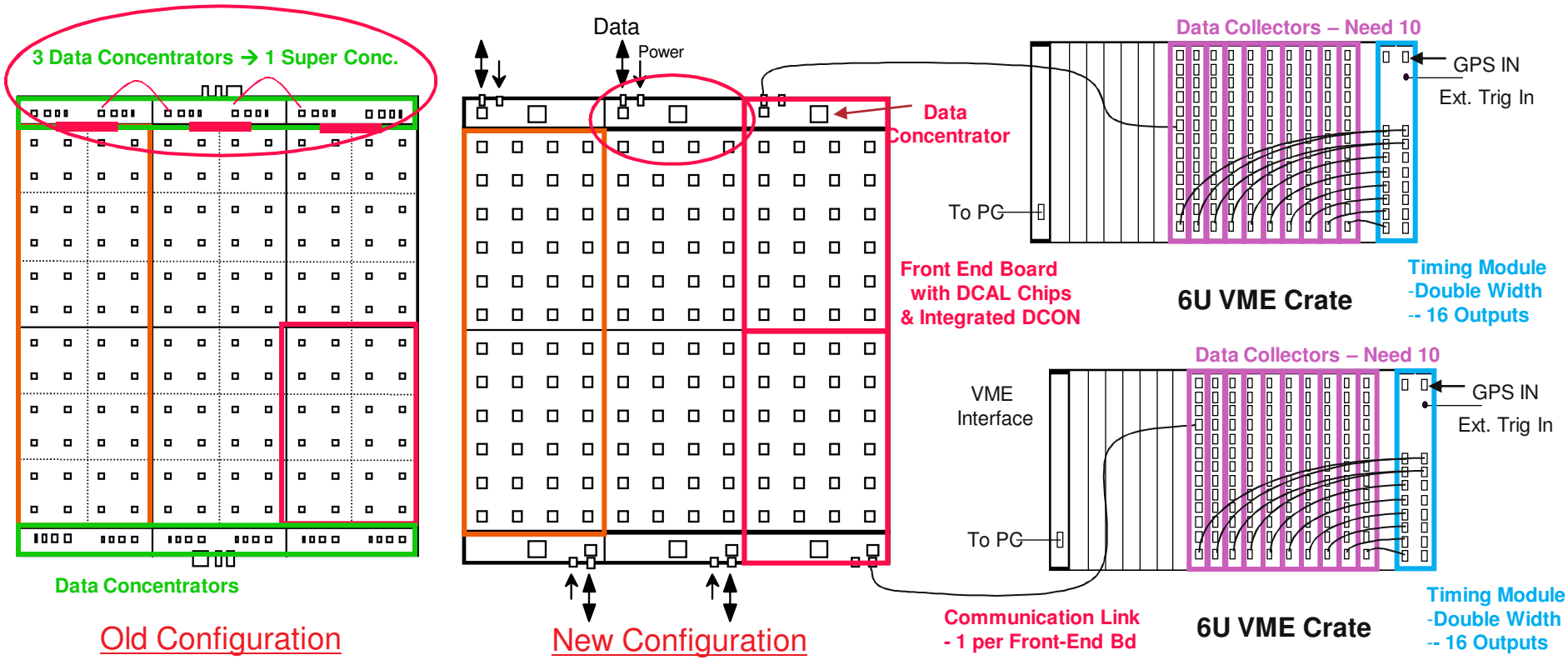
Original System Physical Implementation – Sept. 2007



Final System Physical Implementation

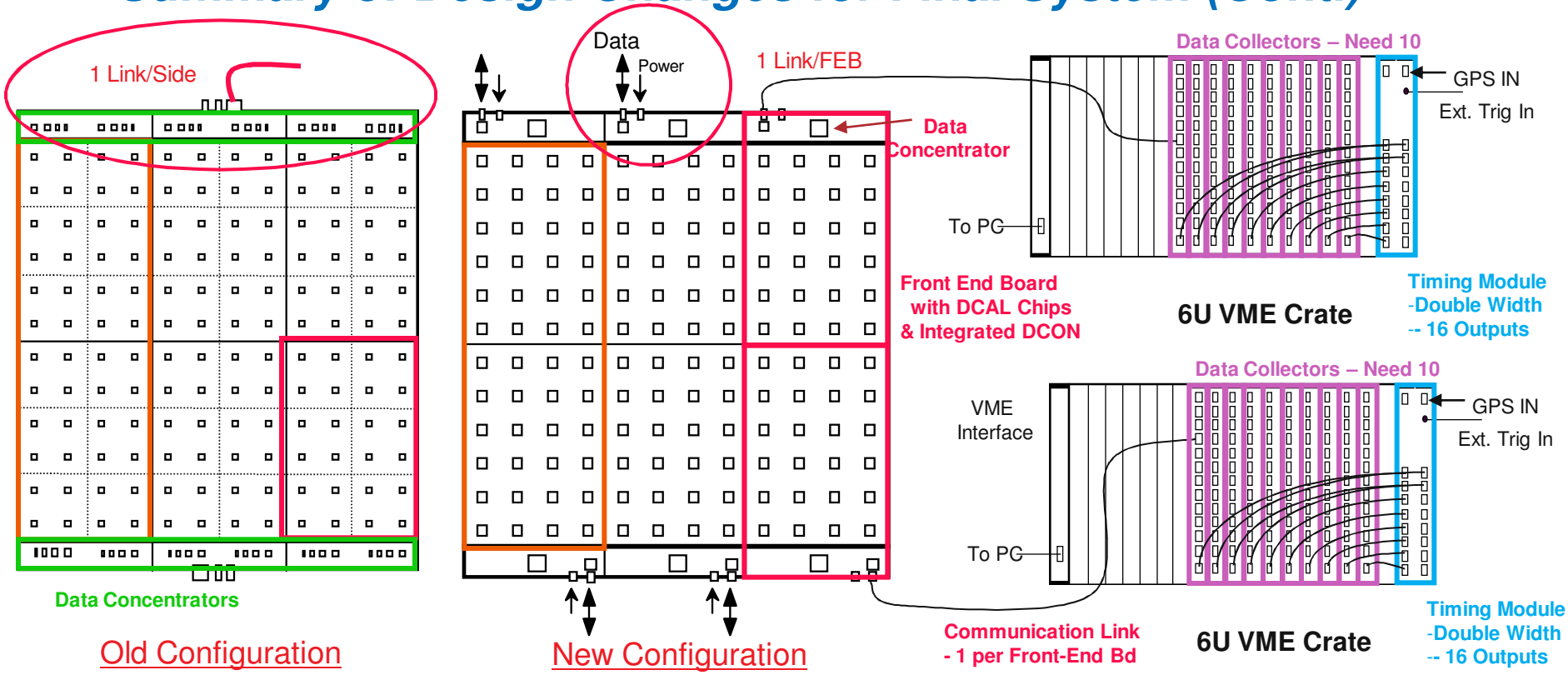


Summary of Design Changes for Final System



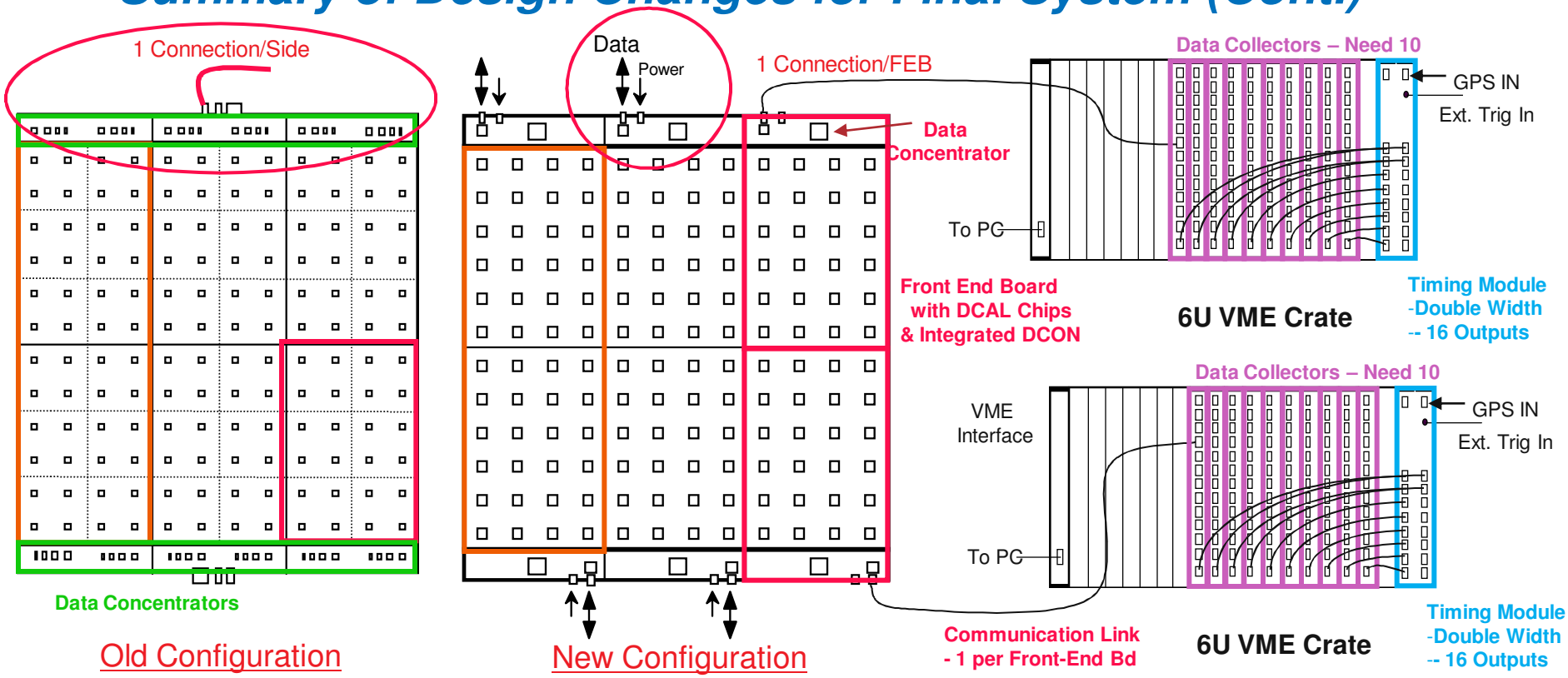
- Eliminate Super Concentrators (Mux 3 DCONs into 1 output)
- Eliminate connection between Data Concentrators & Super Concentrators
- Eliminate connector between FEB and DCON
  - ⇨ ***Simplifies system design, construction, mechanical…***
  - ⇨ ***Reduces costs (~$2K/plane)***
  - ⇨ ***Eliminating connectors is always a good thing… → Reliability***

Summary of Design Changes for Final System (Cont.)



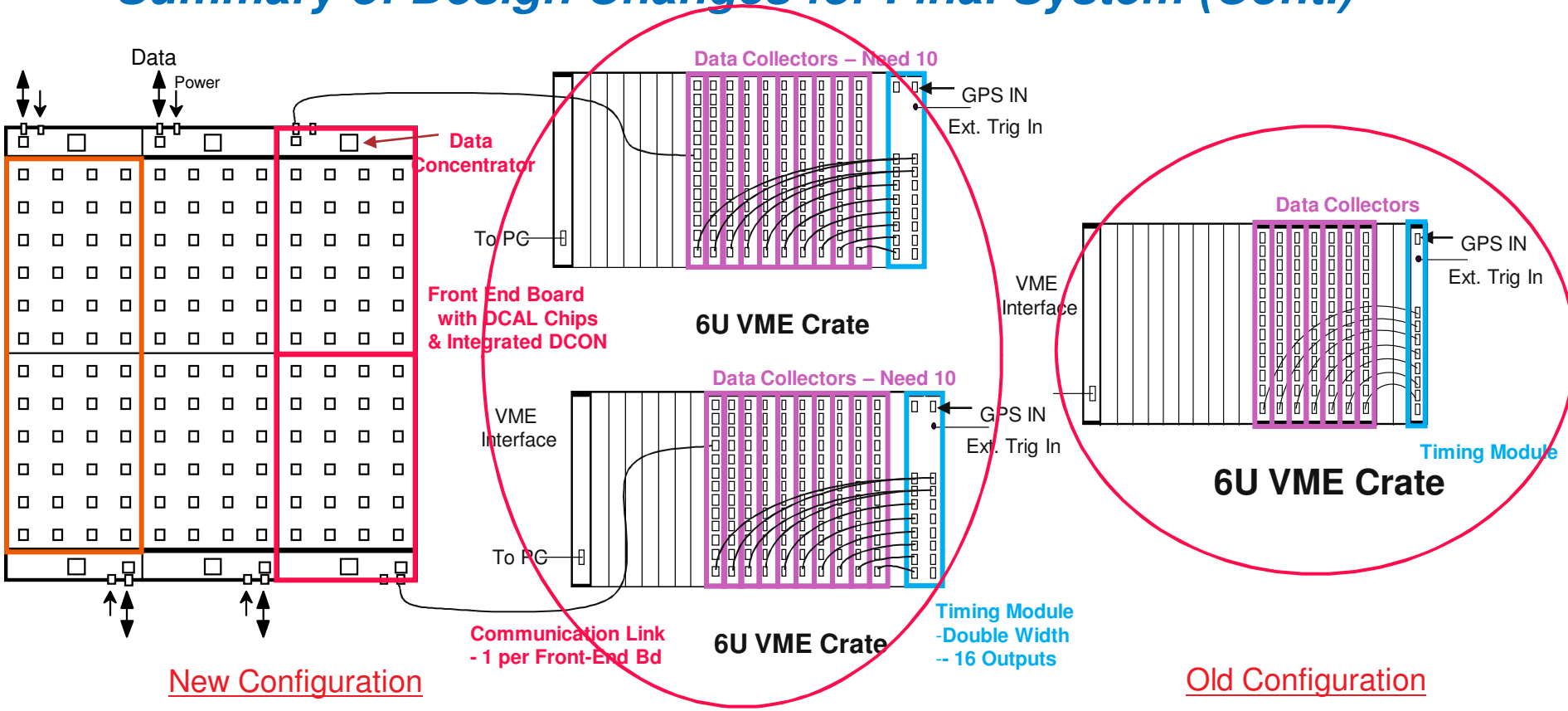
- One com link per front-end board, instead of one per half plane
  - ⇨ ***More cables from front-end to back end - X3 → OK***
  - ⇨ ***Higher bandwidths for data readout possible***
  - ⇨ ***Shorter configuration time for slow controls***

Summary of Design Changes for Final System (Cont.)



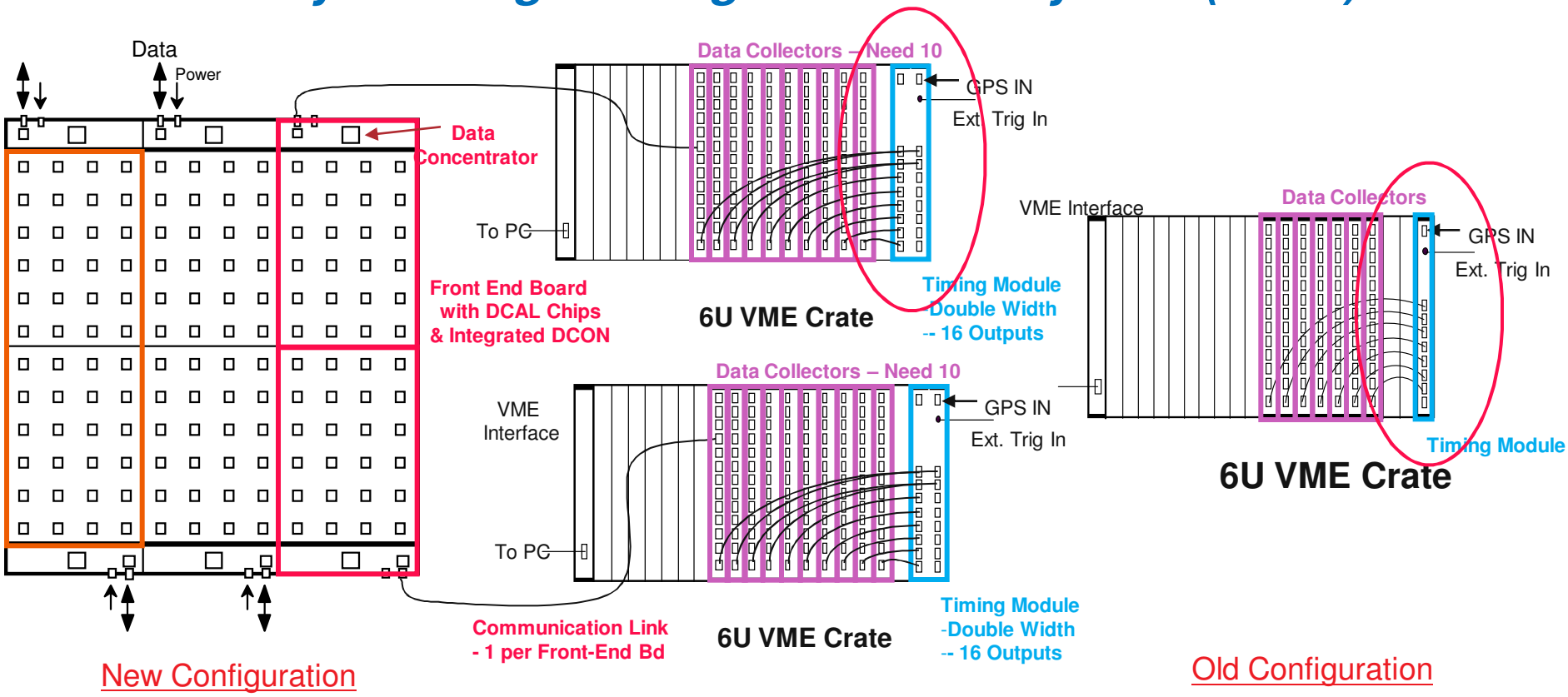
- One power connection per front-end board, instead of one per half plane
  - ⇨ ***More cables from front-end to back end - X3 → OK***
  - ⇨ ***More power connections***
  - ⇨ ***Lower current per connector → smaller cables, smaller IR drop***
  - ⇨ ***Makes power distribution & safety issues easier***

Summary of Design Changes for Final System (Cont.)



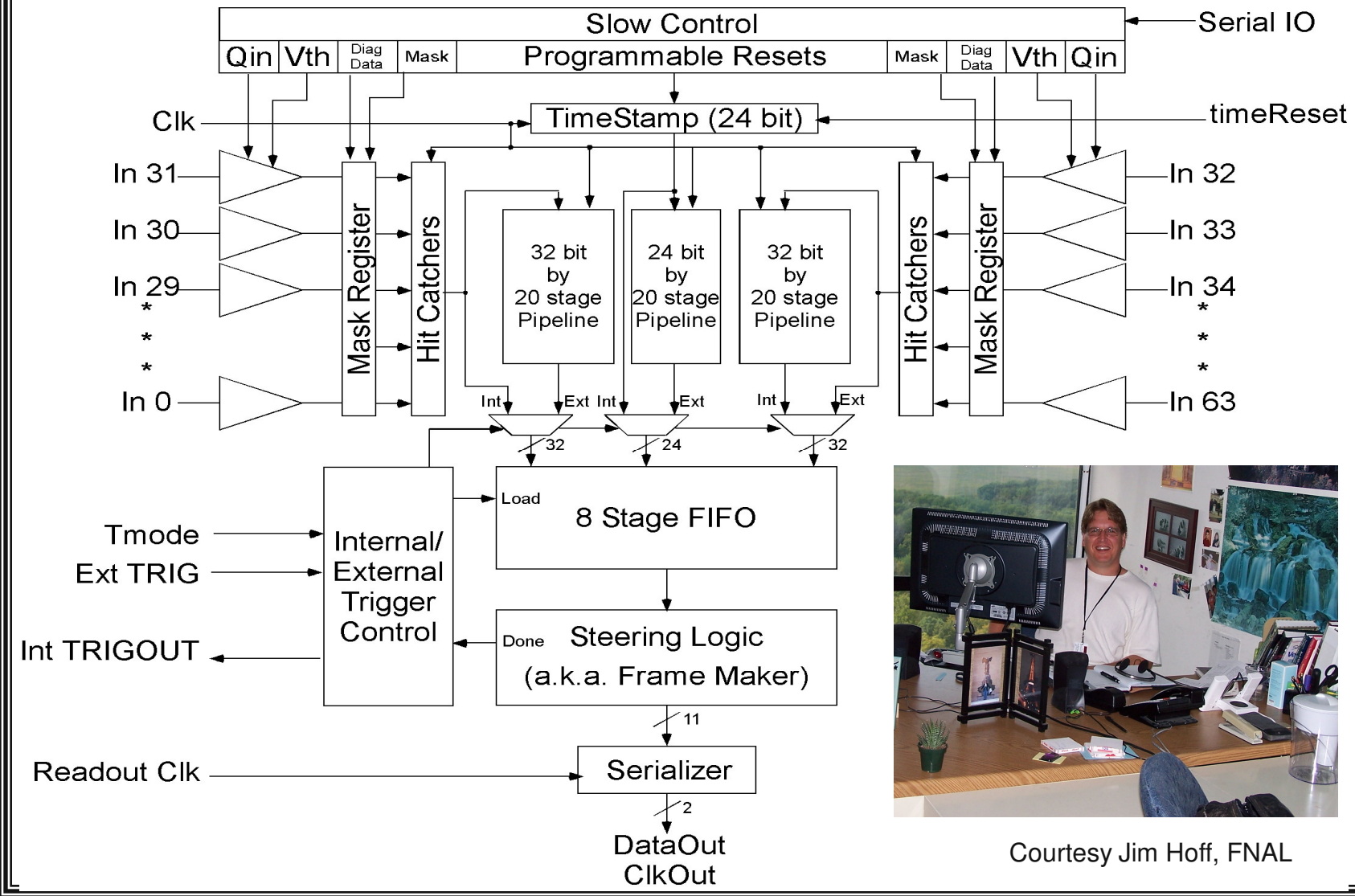
- Increase number of VME crates from 1 to 2 (one per side)
- Increase number of Data Collectors from 7 to 20
  - ⇨ ***Small increase in cost (~$2K/DCOL, ~$4K/Crate, ~$3K for VME Interface)***
  - ⇨ ***Must work out synchronization → OK***
  - ⇨ ***System is now scalable***

Summary of Design Changes for Final System (Cont.)



- Change Timing Module, from 8-output, single width, to 16-output, dual width
  - ⇨ ***Small additional in complexity → OK***
  - ⇨ ***Need additional prototype phase for this module→ in progress;***
  - ⇨ ***Can use old design for now, same protocol***

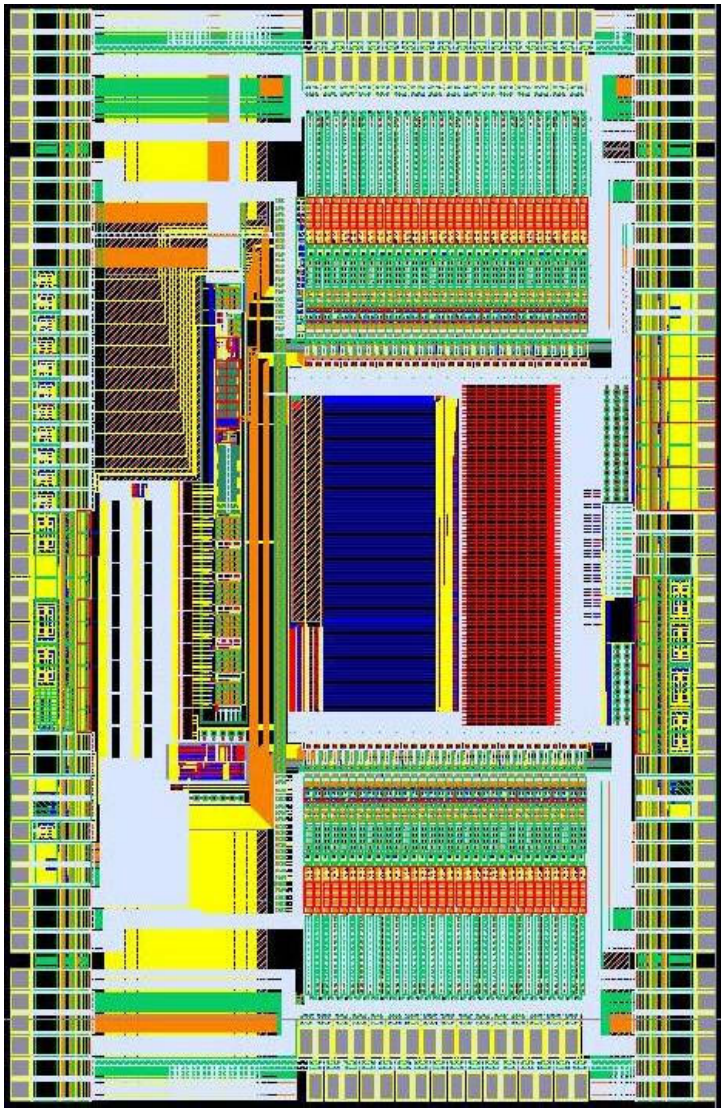
Block Diagram of the DCAL3 ASIC



Courtesy Jim Hoff, FNAL

DCAL3 Production

- Summary of Changes to Chip:
  - A few minor bugs fixed:
    - *output buffer state machine*
    - *slow control read not tristated*
    - *MASK & QINJ registers not readable*
    - *MASK & QINJ regs sensitive to noise*
    - ⇨ ***None affected Vert. Slice operation***
    - ⇨ ***Needed fixing before production***
    - ⇨ ***All changes successful***
  - Change of package needed
    - *DCAL2 package no longer available*
    - *160 pin → 174 pin → added grounds*
    - *Pkg still TQFP, 1.4 mm*



DCAL3 Layout

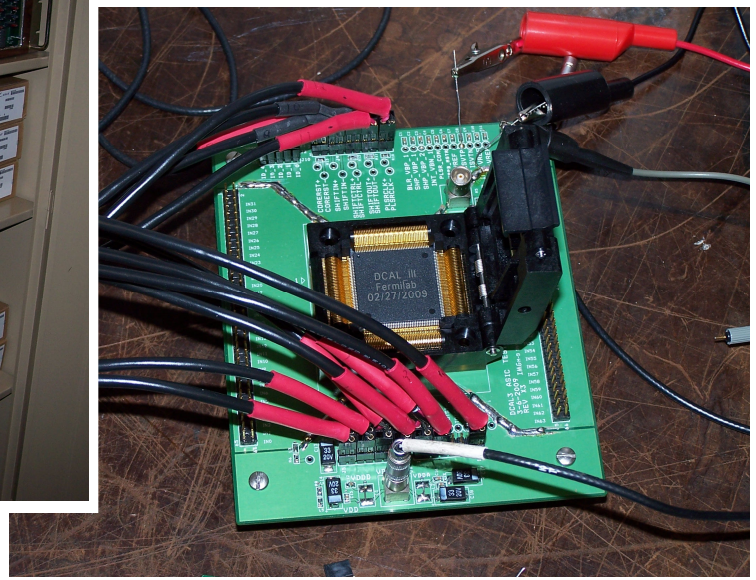
Fermilab

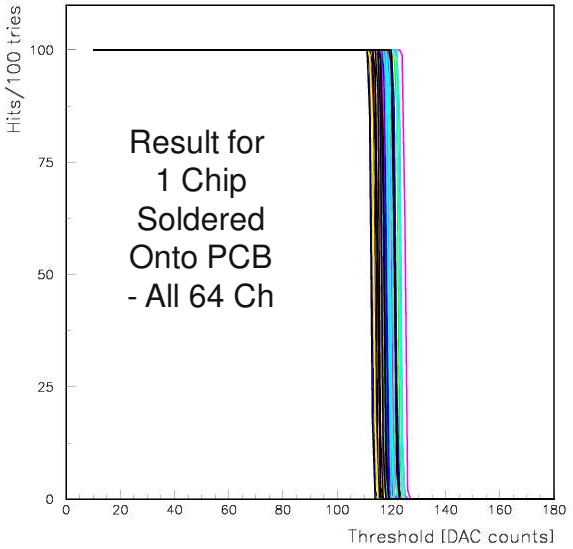
DCAL3 Production (Cont.)

- Status of Production:
  - 11 wafers, 10,300 chips, fabricated, packaged, in-hand
  - Bench tests at Argonne
    - ⇨ ***Basic performance is the same***
    - ⇨ ***Only problem: performance in socket not as good as when soldered onto PCB → OK for most tests***

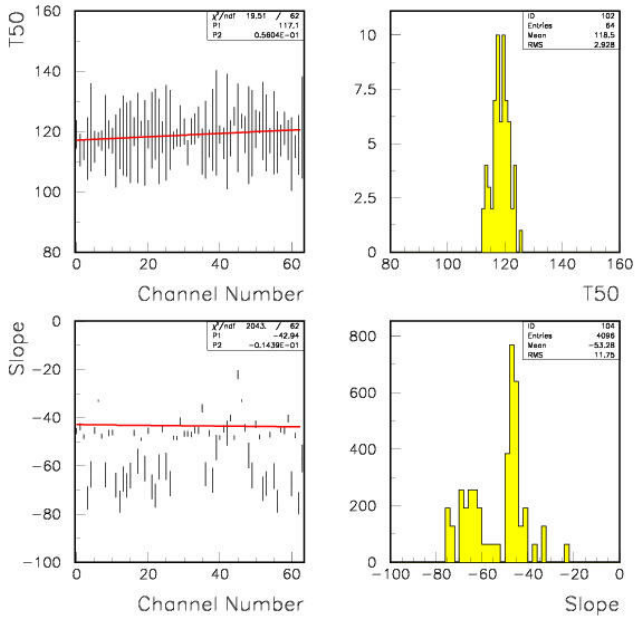
Chips in Storage at FNAL
(About half of total)

Test Fixture at Argonne

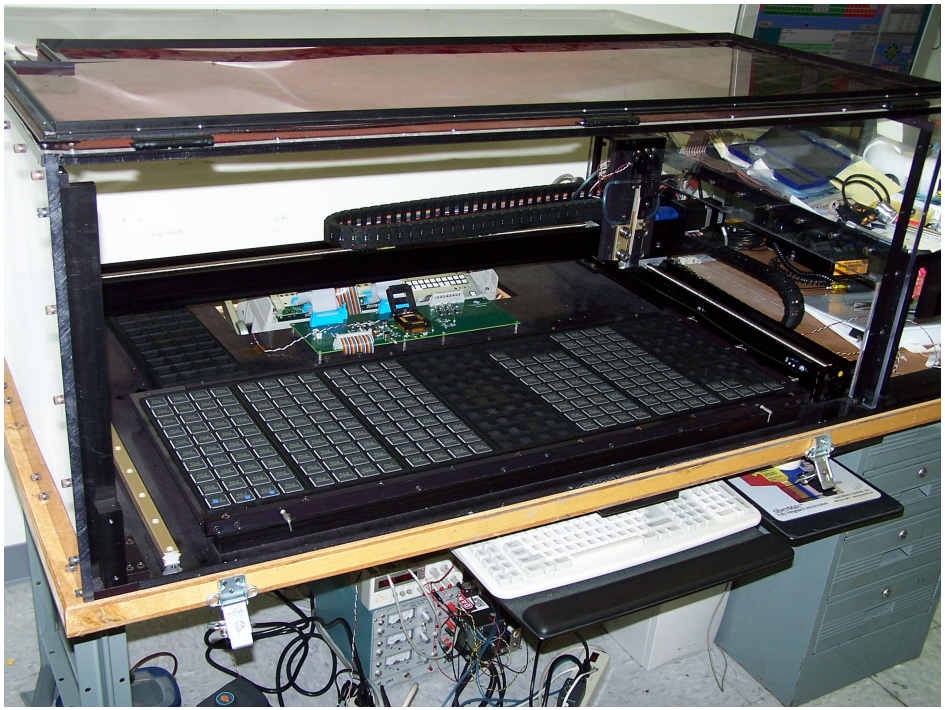




DCAL 3.1 - Threshold Scans



DCAL Chip Testing at Fermilab



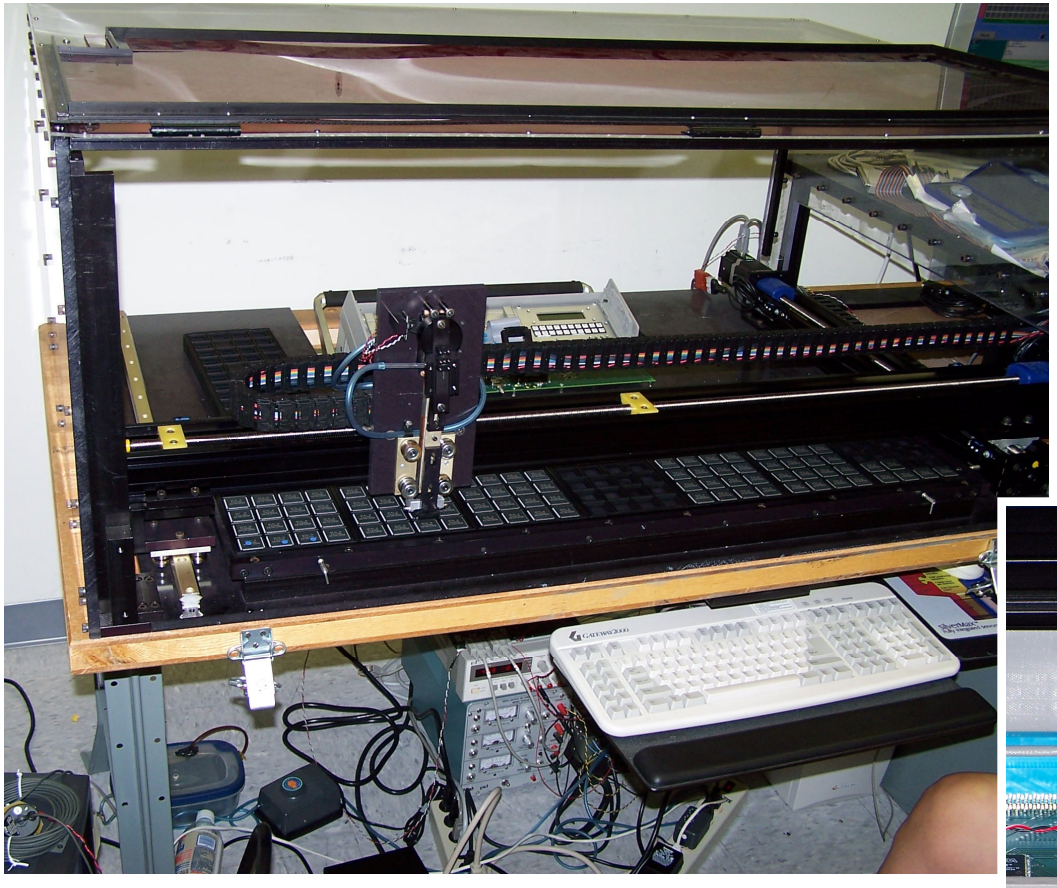
Lou Dalmonte Al Baumbaugh

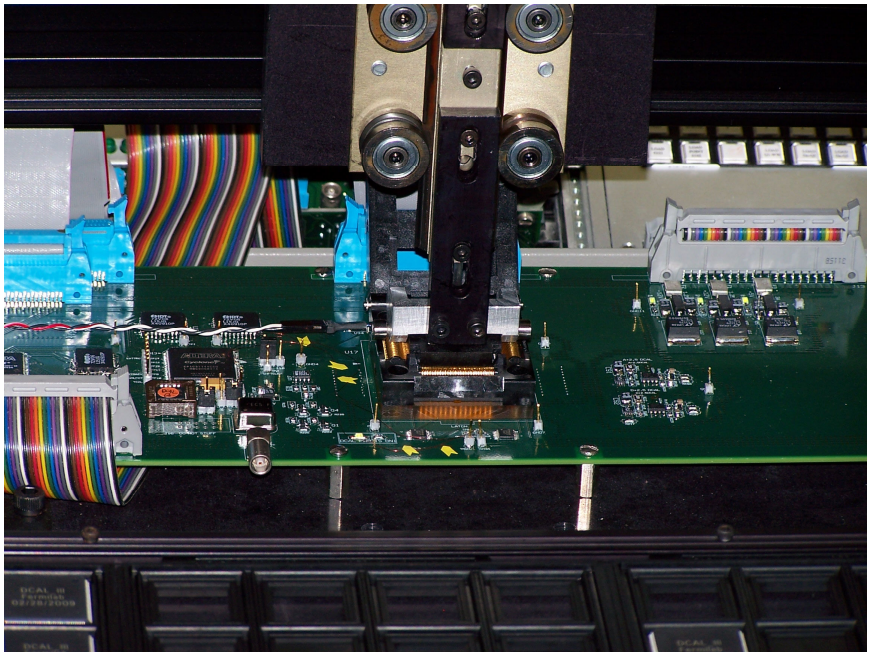
- Fermilab Chip-Testing Robot
  - Designed, built, & programmed by Al Baumbaugh, FNAL
  - Used for previous chip production projects
  - For DCAL, needed “personality module” + test software

    ⇨ ***Complete and operational***

Fermilab

DCAL Chip Testing at Fermilab (Cont.)

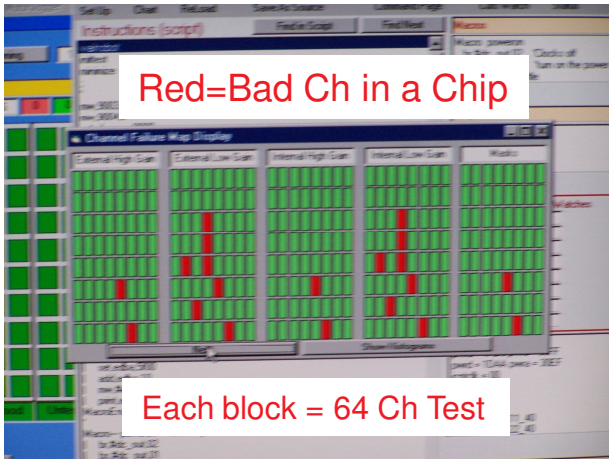


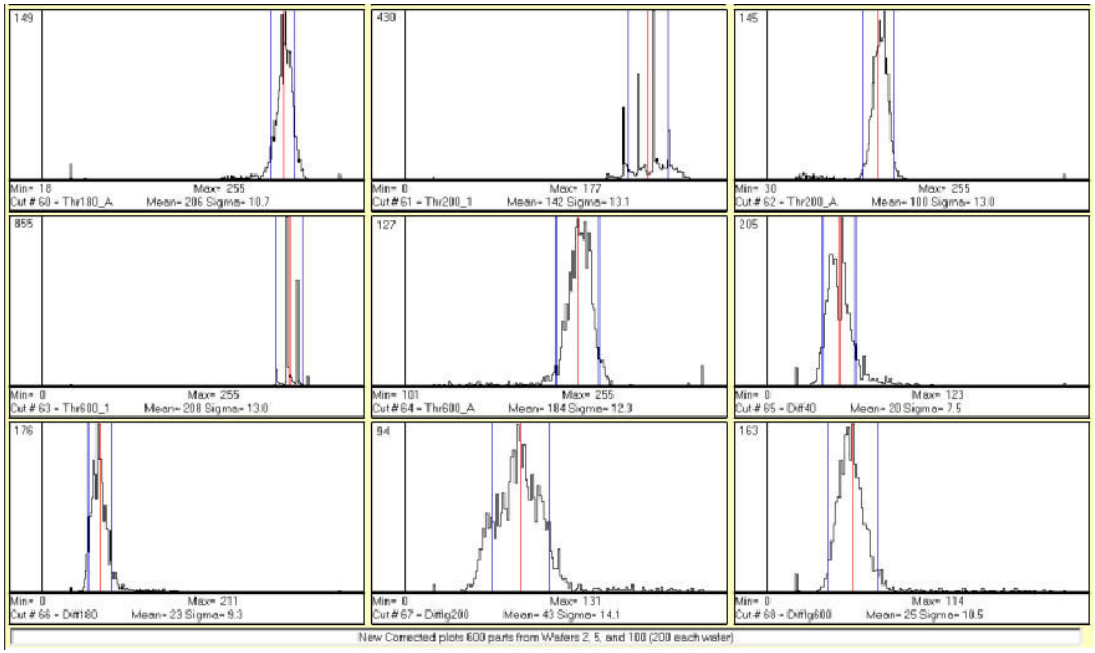


Fermilab

DCAL Chip Testing at Fermilab (Cont.)

- Fermilab Chip-Testing Robot (Cont.)
  - 78 parameters measured per chip
    - *Currents & voltages (analog & digital)*
    - *Slow Control Reg R/W (20)*
    - *Linearity of 8 DACs*
    - *Internal QINJ*
    - *External QINJ*
  - Test mode:
    - *No cuts applied*
    - *Measure parameters*
    - *Calc mean & σ*
    - *Decide nσ cuts*
  - Checkout mode
    - *Apply cuts*
    - *Robot sorts*



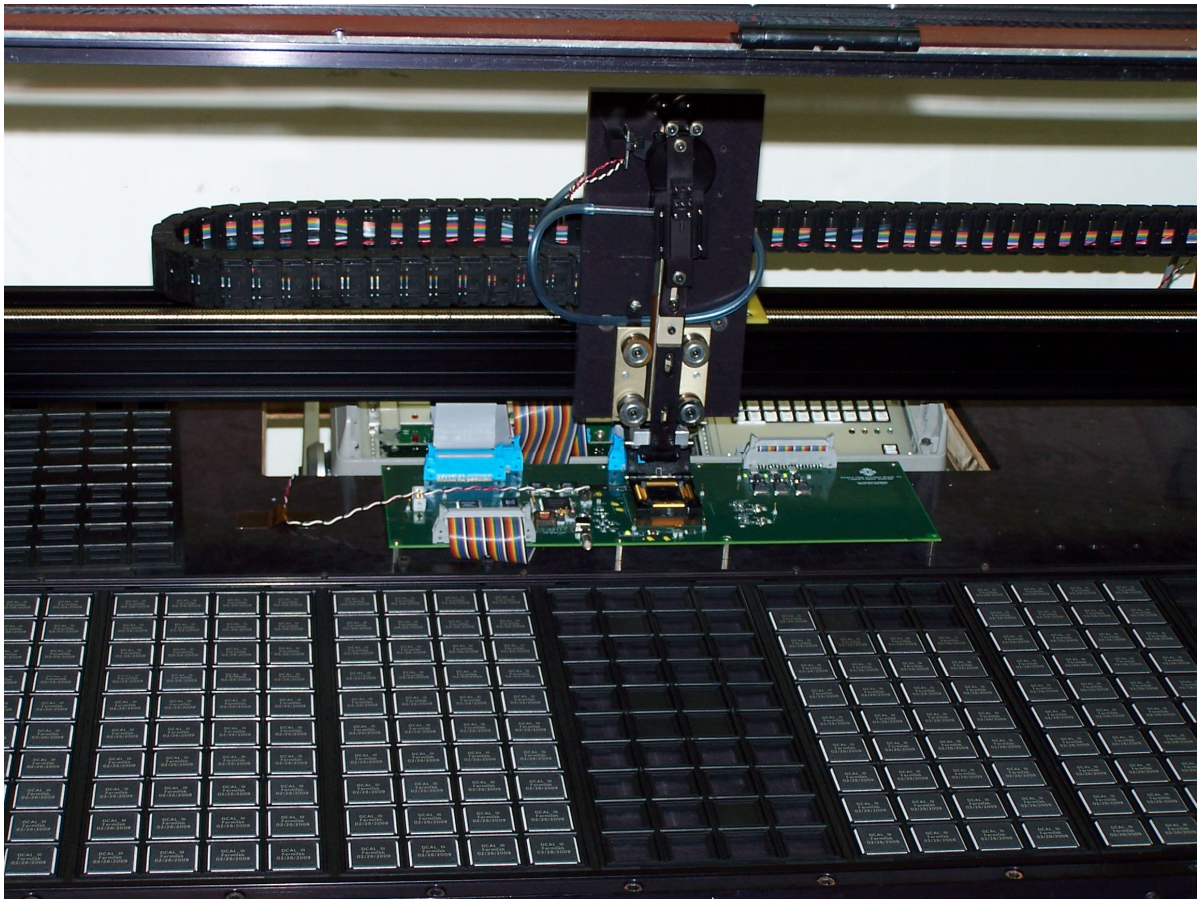


DCAL Chip Testing at Fermilab (Cont.)

- Fermilab Chip-Testing Robot (Cont.)
  - Robots sorts good chips & bad chips into trays
  - ~1 minute per chip
- Results so Far:
  - Checked 800 chips
  - One bad wafer (of 11)
  - Yield 68% (→ 80%)
  - Check 400 chips/day

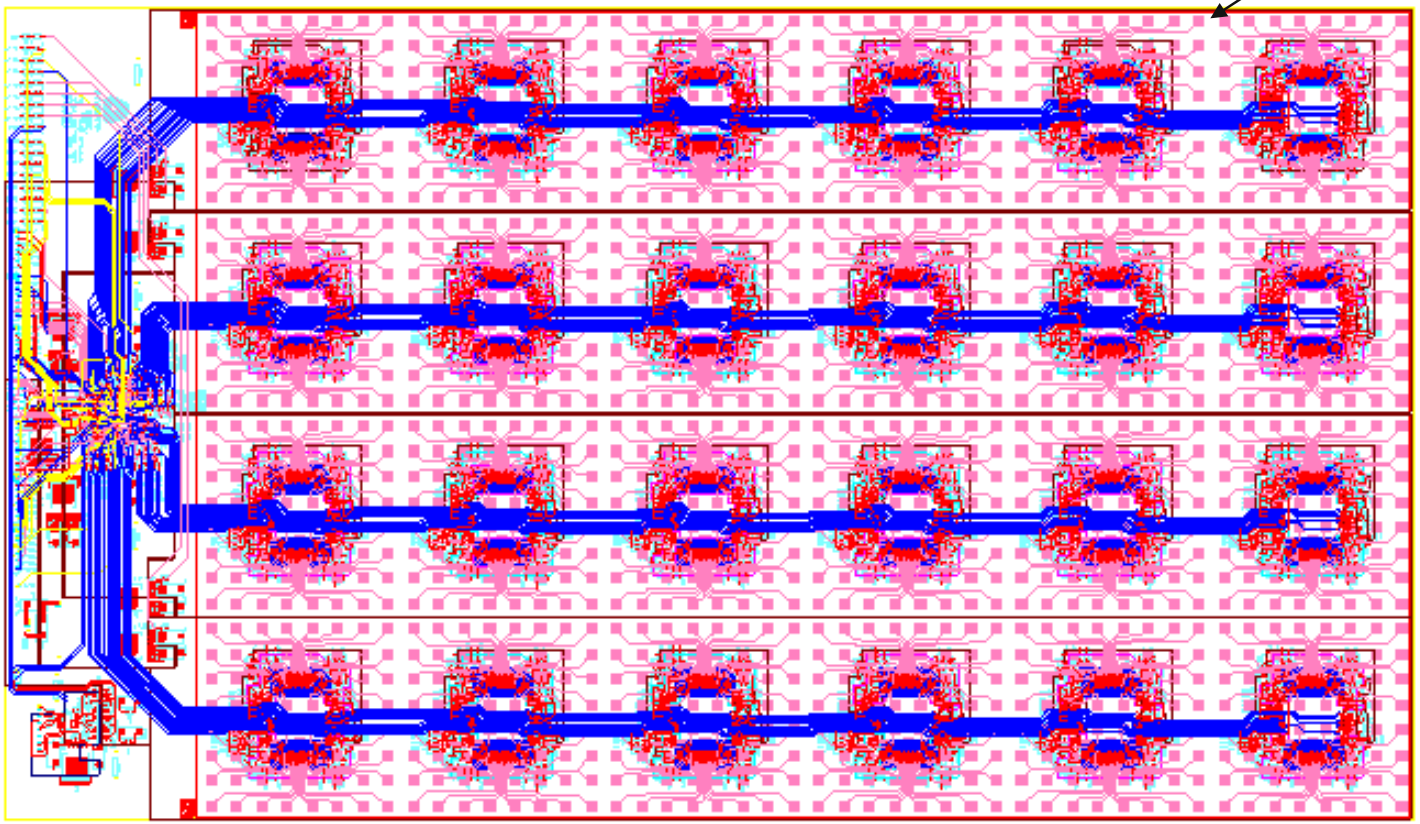
⇨ ***Checkout Beginning Now***

Display after Checkout Run



Front End Board Design

- 32 cm X 48 cm (54 cm) → ½ Chamber → 1/6 of a sq. meter Plane
- 24 chips per board → 1536 channels per board



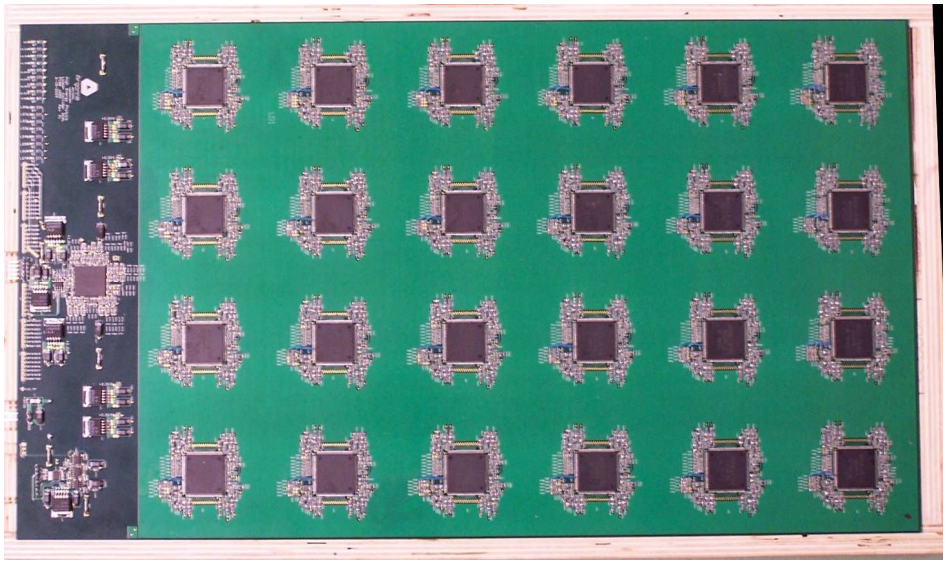
8-layer FE-board (3 layers shown)

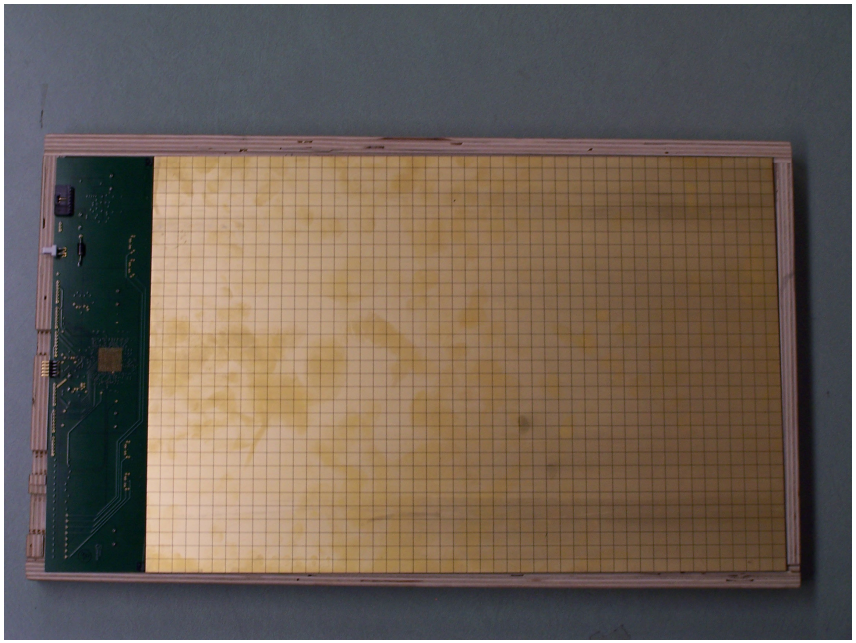
⇨ ***DCON on Same PCB***

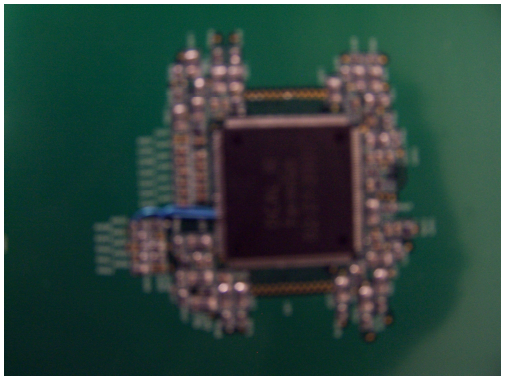
⇨ ***Design has Eliminated Blind Vias!***

⇨ ***Fab Cost ~$200/Bd → Meet Target***

Front End Board Construction & Testing







- Have built & checked out 2 boards.
- Have glued 1 pad board
- Testing in progress
- Cosmic ray tests have begun

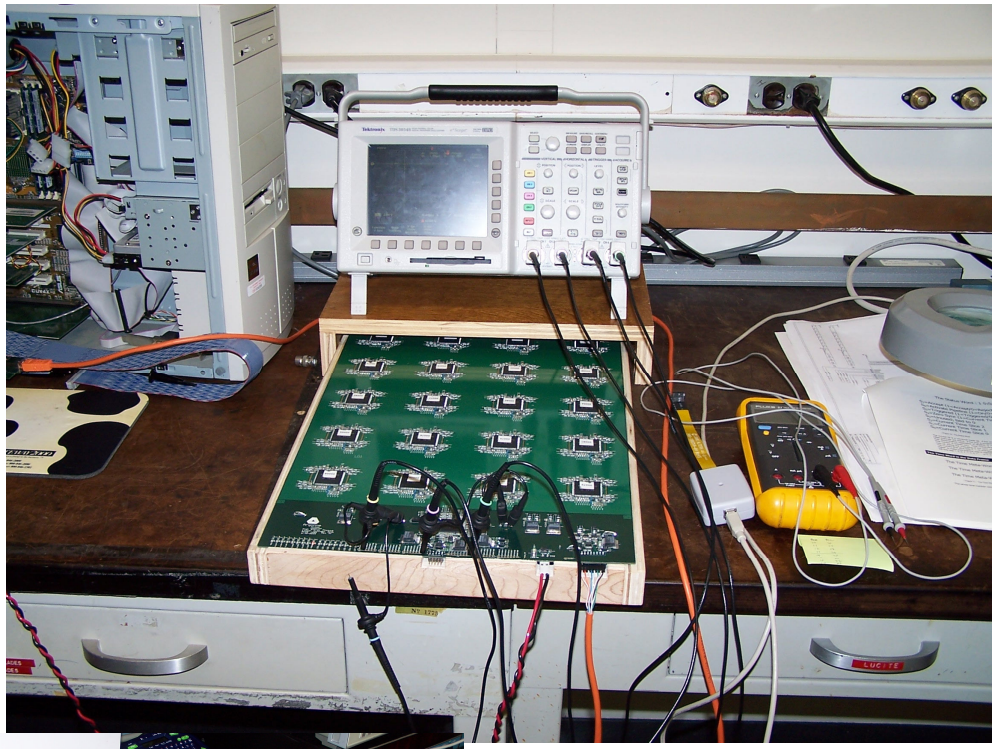
⇨ ***One small PCB artwork error per chip***
⇨ ***Have fixed with wire kludge on board***
⇨ ***Will fix artwork for production***

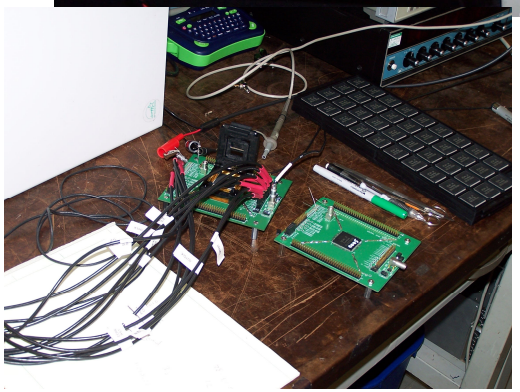
Front End Board Construction & Testing (Cont.)

- Status
  - 2 checkout programs complete
  - 2 more in progress
  - Noise tests to begin

  ⇨ ***Results so far look very good***
- Plan
  - Complete tests ~Nov.
  - Begin fab 300 bds ~Nov
  - Begin assembly ~Dec
  - Begin to have finished boards ~Jan, 2010
  - Testing begins ~Jan., 2010
  - Then begin gluing…

⇨ ***This is now the critical path in the project…***

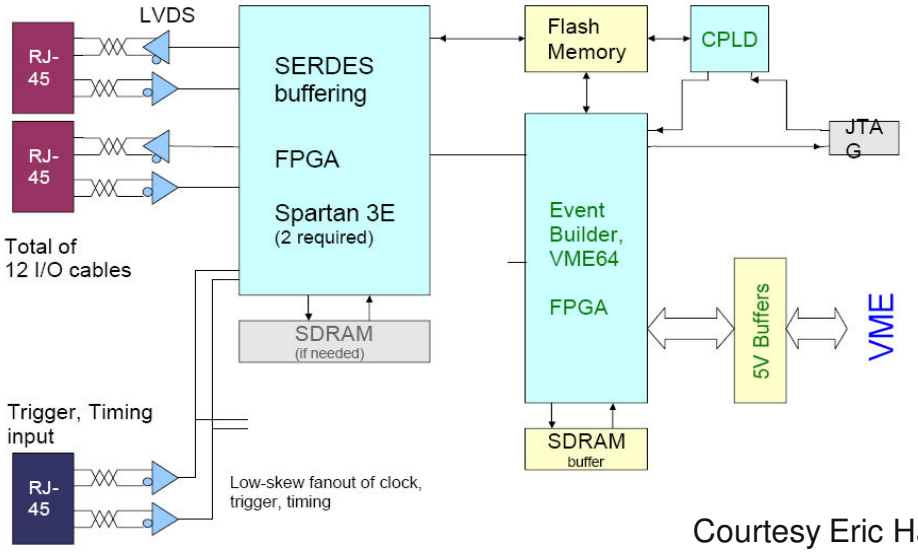


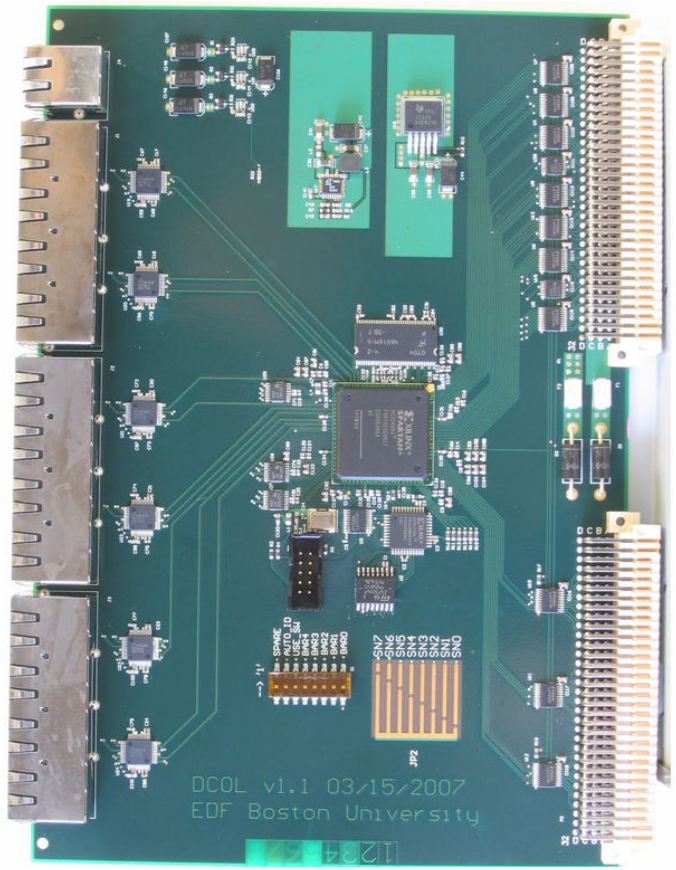


Data Collector

- Status
  - No hardware changes from Vertical Slice
  - Minor firmware changes only
  - 30 boards fabricated & assembled
  - Testing in progress

⇨ ***Will be ready when needed***



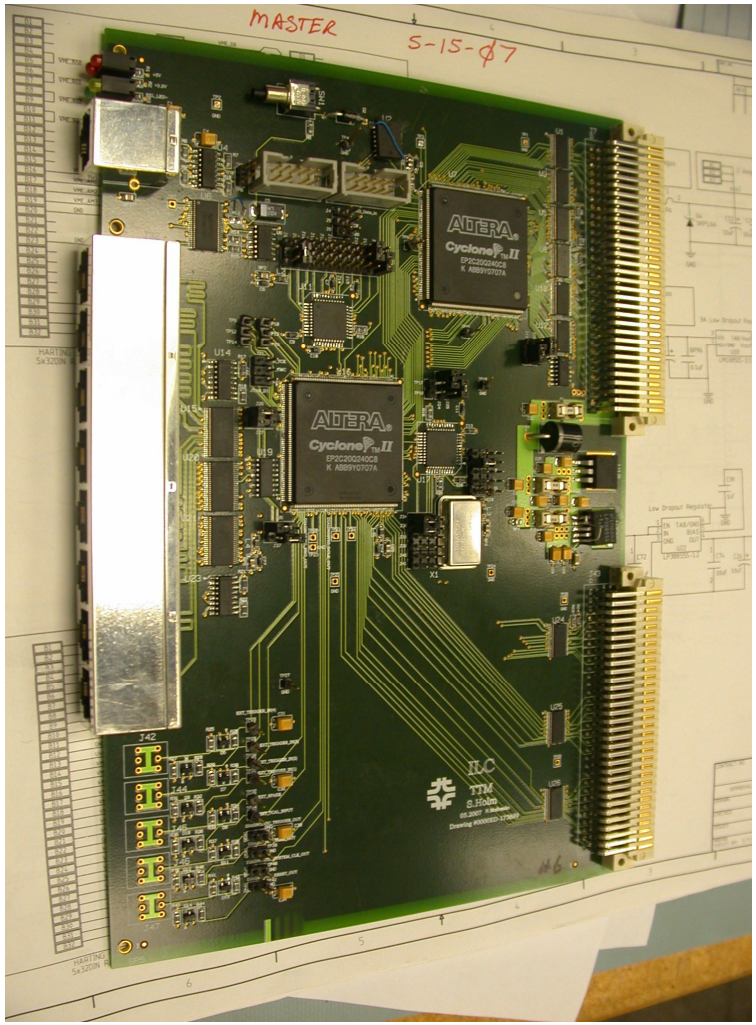


Courtesy Eric Hazen, BU

Timing & Trigger Module (TTM)

- Status
  - Redesign in progress
    - *Add outputs: 8 → 16*
    - *Makes double-width*
    - *Add capability to use as fan-out to other TTMs → multi-crate operation, one GPS unit*
  - Plan
    - *Fabricate ~Nov.*
    - *Assemble ~ Dec.*
    - *Ready ~Jan., 2010*

⇨ ***Project on-track to be ready when needed, despite redesign…***



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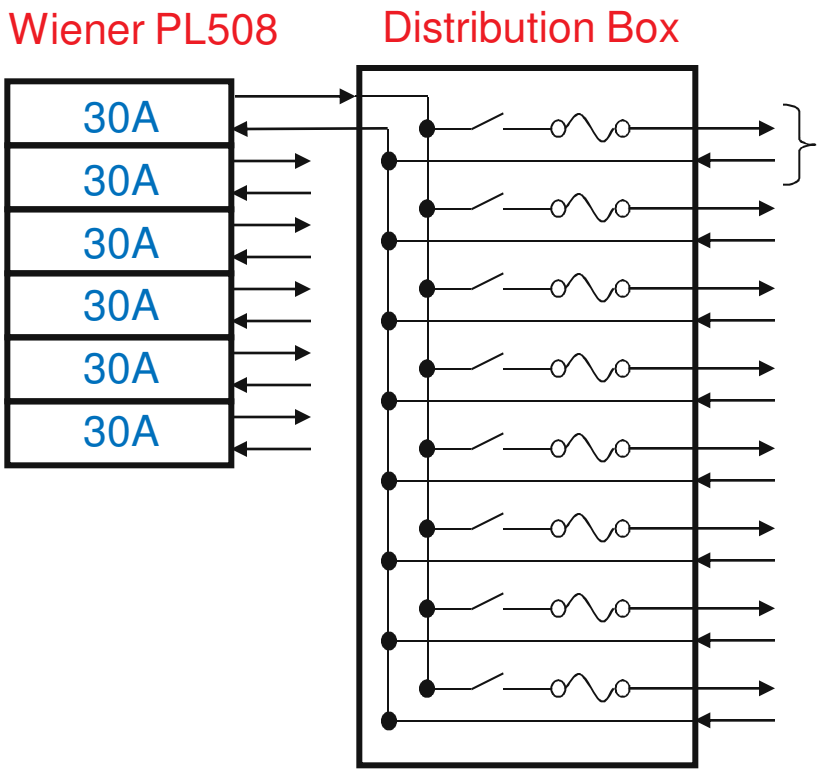
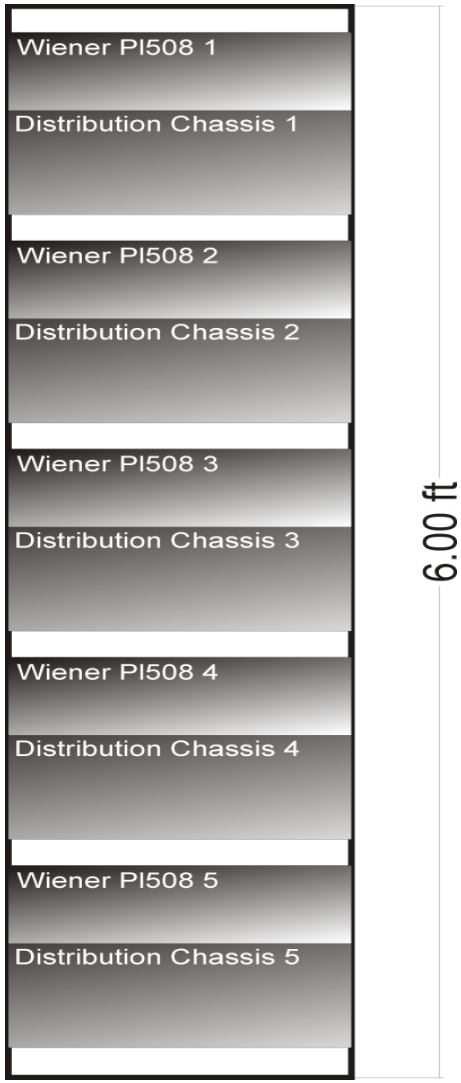
Power Distribution System

- Cubic meter detector power requirements:
  - 40 planes * 6 FEBs/plane * 3.0 amps/FEB = 720 amps at 5V
- Solution:
  - 5 Wiener PL508 chassis
  - Each PL508 has six independent 5V at 30 amp supplies
  - 5 PL508 * 6 PS/PL508 * 30 amps/PS = 900 amps total ampacity
  - Operate at ~80% of capacity (Wiener: 100% OK!)

Power Distribution System (Cont.)

- Rack Configuration
  - Power supplies will fit into one rack
- Power Distribution
  - Custom distribution boxes, with fuses, safe wiring, etc.





Summary

- **Production preparations in progress**
  - **DCAL ASIC**
    - *10,300 chips in hand, fabricated & packaged*
    - *Testing in progress*
    - *Expected completion: ~November, 2009*
  - **Front-end Board & Pad Board**
    - *Prototypes in hand*
    - *Testing in progress*
    - *Expect to begin fabrication of 300 boards ~ November, 2009*
  - **Data Concentrator**
    - *Now part of front-end board*
    - *Firmware is working; Debugging last few problems*
  - **Super Concentrator**
    - *Eliminated from system architecture*
  - **Data Collectors**
    - *Fabrication and assembly of 30 boards complete*
    - *Checkout in progress*
  - **Timing & Trigger Module**
    - *Redesign in progress*
    - *Expect fabrication ~November, 2009*
  - **Power System**
    - *Procurement and fabrication of components in progress*

⇨ ***Expect to begin having electronics ready for system checkout ~Jan, 2010***