DIRAC 2 Tests Status
&
Mini-Stack of MICROMEGAS chambers

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Plan

DIRAC 2 ASIC

ASIC Tests

MICROMEGAS detector

ASIC improvements

Conclusions

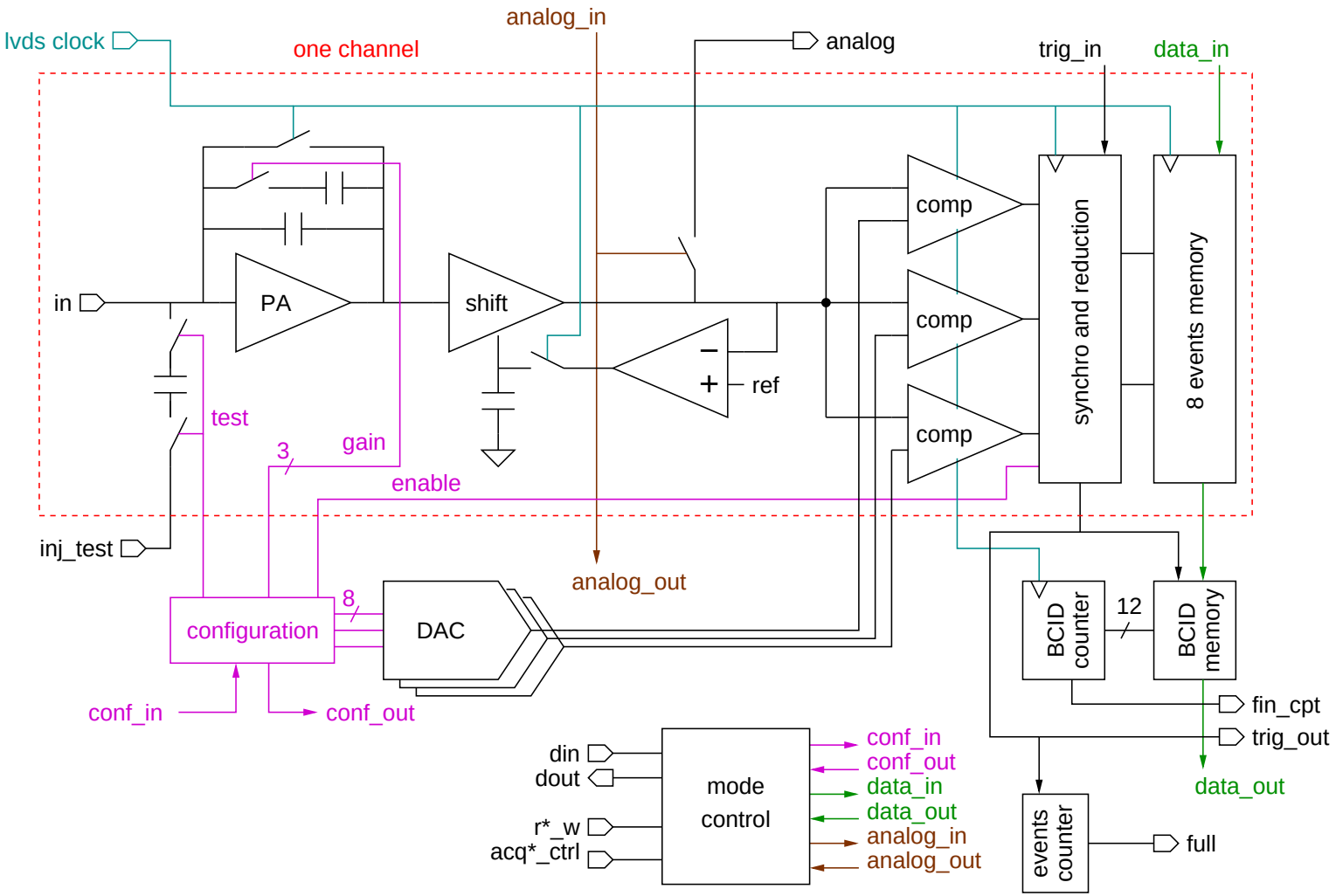
DIRAC 2 ASIC reminder

Version 1 was originally designed at IPNL/IN2P3, version 2 in collaboration with LAPP/IN2P3.

- CMOS 0.35 µm;
- 64 channels (CPA+BLR+discriminator+memory);
- C_{det}=80 pF;
- 3 thresholds programmable on 8 bits;
- Dynamic range: 50, 100, 200 fC or 10 pC;
- 12-bit event identifier;
- 10 µW per channel in pulsed mode.

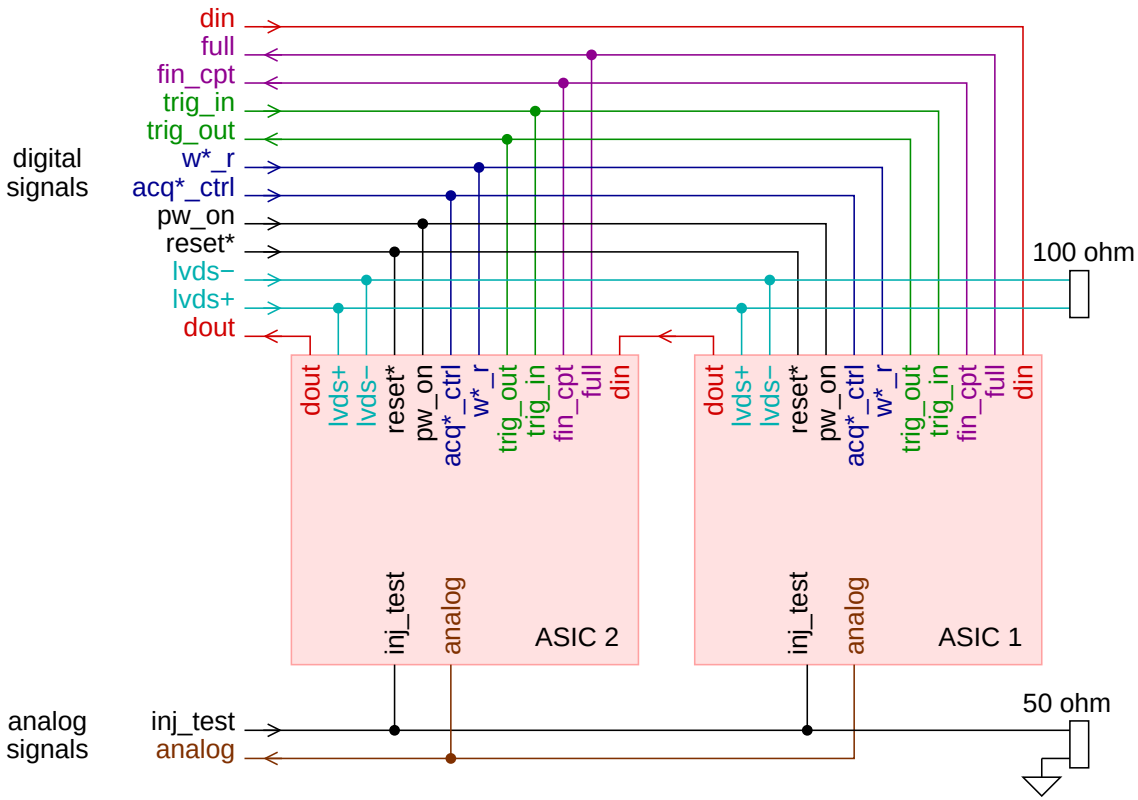
Chip architecture

Functional block diagram:



Chip interconnexion

- Digital interconnexion;
- Serial readout $\longrightarrow$ daisy chainning of many chips;
- Analog input are on both side of the die $\longrightarrow$ minimize Xtalk and simplify PCB design.



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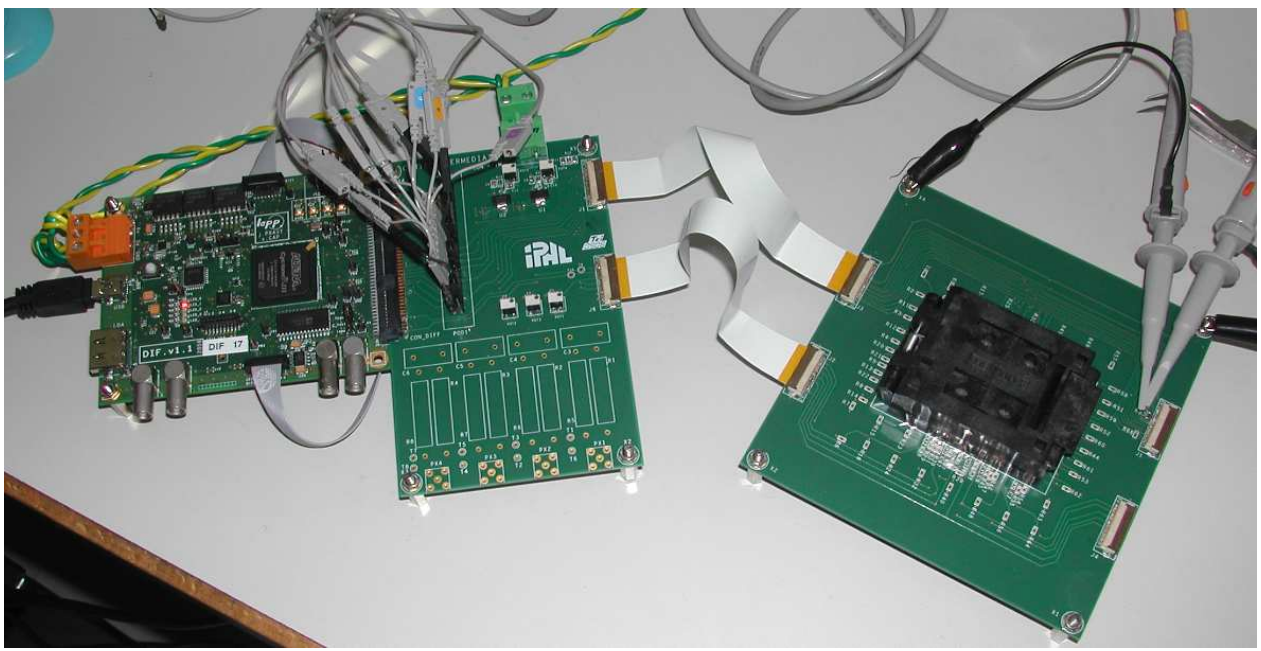
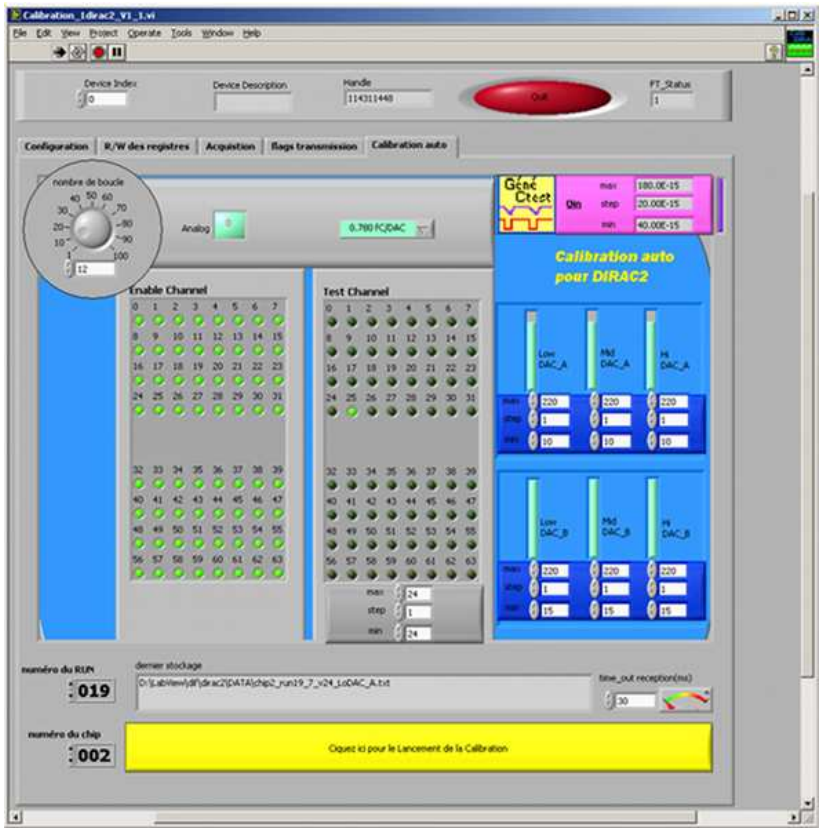
Test bench

- One DHCAL DIF (J. Prast, S. Cap) with DIRAC VHDL firmware (G. Vouters);
- One Intermediate Board (IPNL);
- One ASU-like testboard with IC support on top side and 64×1 cm^2 pads on the other side (IPNL);
- 5 prototypes of DIRAC 2 ASIC (designed at IPNL).



Acquisition software

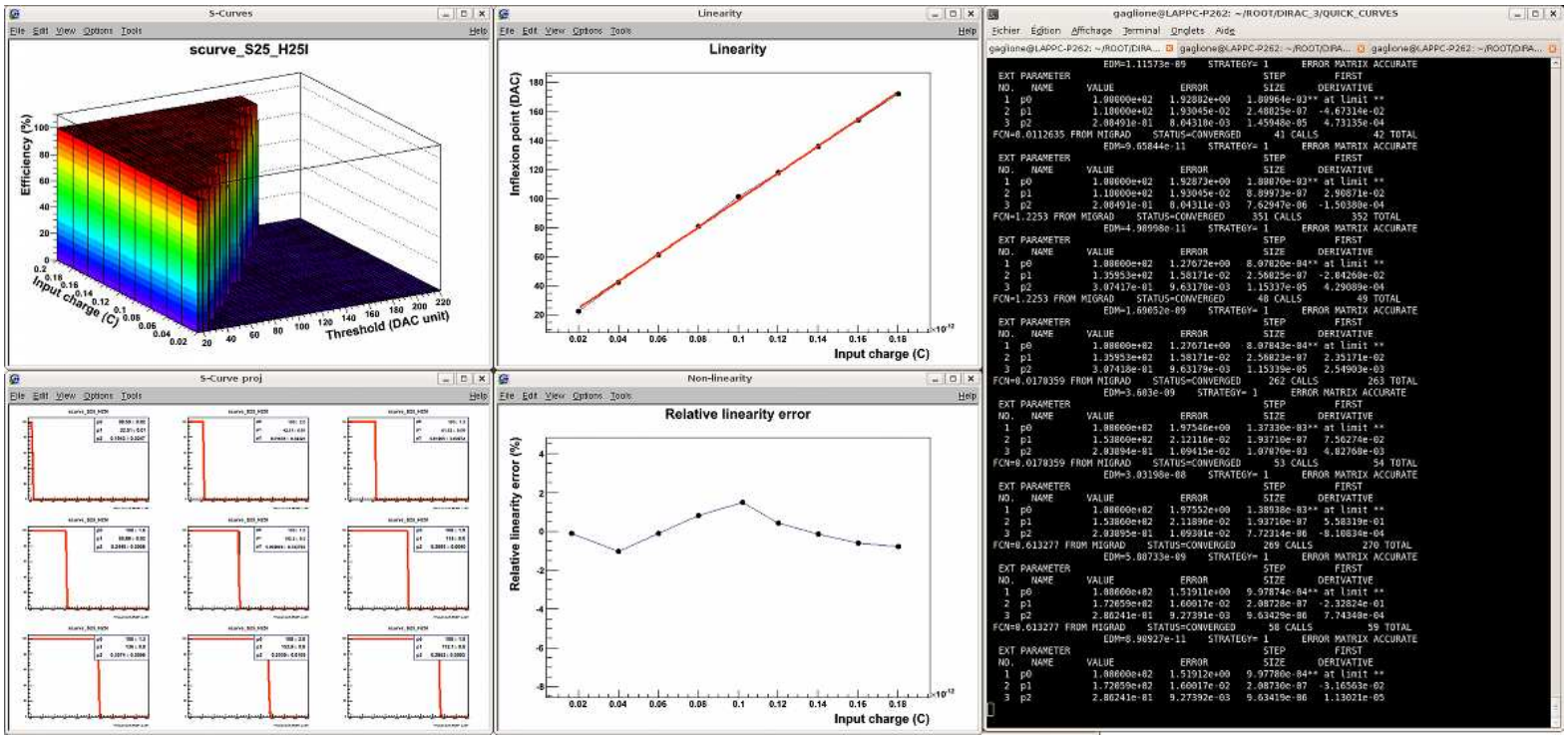
Labview on a PC to control DIF and store data to disk (C. Drancourt).



Automatically inject patterns to test ASIC.

Analysis software

Automated software for data extraction (C++/root), compatible with LAPP MICROMEGAS framework.



Automatically extract chip parameters, and some plugins will be writen for testbeam analysis.

Test overview

Methodology:

- Measure trigger efficiency *vs* thresholds *vs* input charge;
- *S-Curves*: fit with a Fermi-Dirac distribution for each input charge:

$$S(x) = \frac{max}{1 + e^{\frac{x-\mu}{w}}}$$

max : maximum efficiency
μ : inflexion point abcisse
w : inflexion slope

Next:

- μ *vs* input charge for each channel;
- Linear fit:

$$F(x) = 1/g \cdot x + b$$

g : gain
b : pedestal

- Non-linearity: difference between fit and measures normalized to the input charge.

Test results: performances

- Linearity: $\Delta F/F = \pm 2\%$ on 20–200 fC range.
- Minimum threshold: $<$10 fC (0.5 MIP-MPV)
- Noise: less than 5 fC@5σ ;
- Dispersions:

Example for 1 gain setting (64 channel per chip, gaussian distribution, mean/sigma)

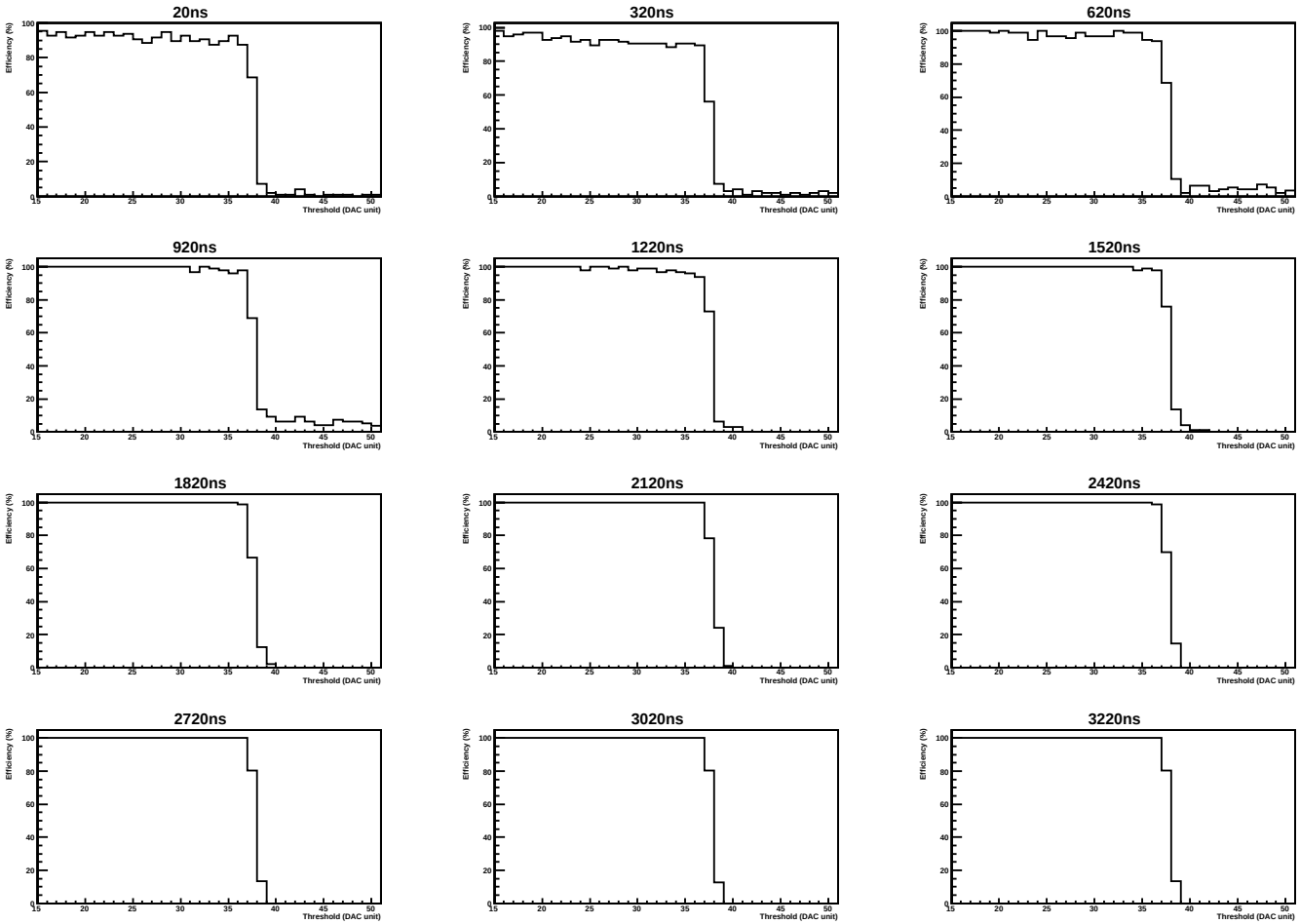
	chip1	chip2	chip3	chip4	chip5
gain (fC/DACU)	1.1/0.03	1.0/0.03	1.1/0.02	1.0/0.02	1.1/0.02
pedestal (fC)	6.2/2.0	4.0/1.6	6.7/1.8	6.9/1.6	5.6/1.7

No calibration needed for a DHCAL !

Overall performances meet the present requirements for a MICROMEGAS/GEM DHCAL.

Test results: power pulsing

SCurve *vs* power-on time:



Stable after 2.7 µs: compliant with ILC power pulsing !

Test summary

No bug in ASIC, some non-critical mistake in test PCB.

- New features: channel masking, LVDS clock ✓
- Power pulsing ✓
- Overall performances ✓
- VHDL Firmware ✓
- Acquisition software: Labview ✓ – Still no X-DAQ available
- Analysis software ✓
- Analog output: to be characterized, but seems OK with scope.

Now, let's test this chip on a real detector !

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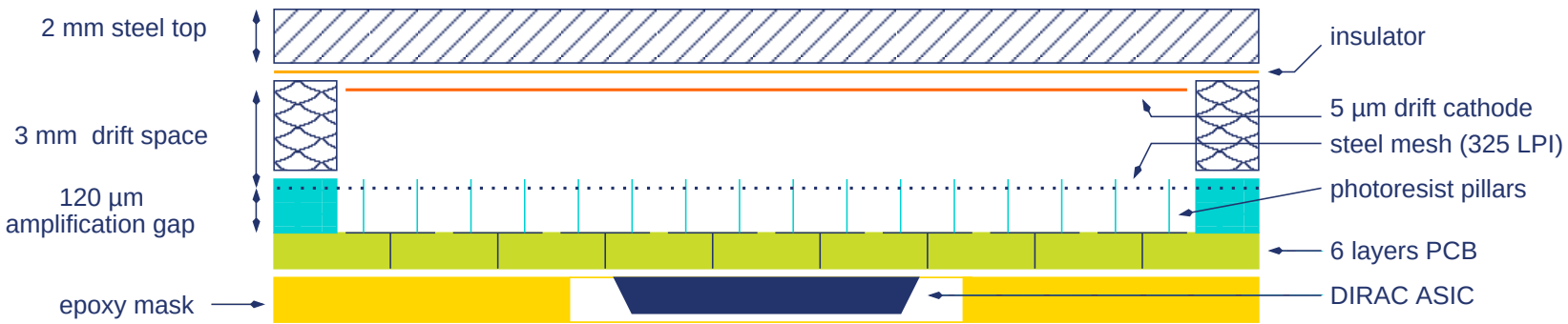
Bulk MICROMEGAS with embedded DIRAC

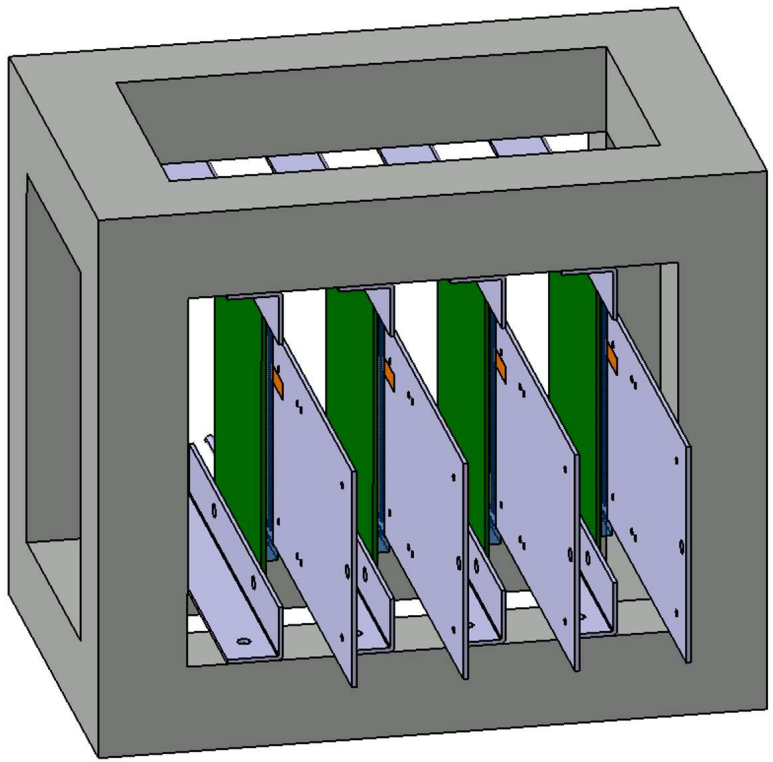
PCB designed at LAPP (A. Dalmaz), then PCB manufacturing, cabling and mesh lamination are made by CERN TS/DEM (R. De Oliveira) and chamber design and construction are performed at LAPP (N. Geffroy and F. Peltier).



Major parts of detector manufacturing can be made in a PCB workshop: advantageous for large area detector!

Mini-stack

After 2008 testbeam with DIRAC 1, four 8×8 cm^2 chambers with DIRAC 2 ASIC are currently build.
Mechanical structure is ready:



The mini-stack should be ready at the end of october.

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New preamplifier

With our bulk MICROMEGAS, a 97% efficiency involves a minimum threshold of 1.5 fC.
We need to improve the preamplifier, challenge: not increase power consumption too much! A new design has began at LAPP:

- Improved gain with "gain boost "and cascoded current source;
- Improved stability;
- Improved gain and bandwidth (@ same power consumption);
- Additional programmable biasing current to reduce noise.

But is it really needed for physics ? (see J. Blaha and H. Mathez talks)

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We are waiting for the detector PCB for this autumn test beam.

- Micromegas chamber with DIRAC v1 has been succesfully tested in beam in 2008;
- Prototypes of version 2 have been received succesfully characterized on bench;
- Four 8×8 cm^2 chambers are under construction;
- Next step: 32×48 cm^2 MICROMEGAS PCB to builds a 1 m^2 + tracking chambers.