High speed pipelined ADC + Multiplexer for CALICE

Why this high speed (25MS/s)

- Because pipeline is not power efficient below 10MHz.
- For a good FOM, the converter must be used at high frequency affordable by the process.

10 bits Pipelined ADC performance trends

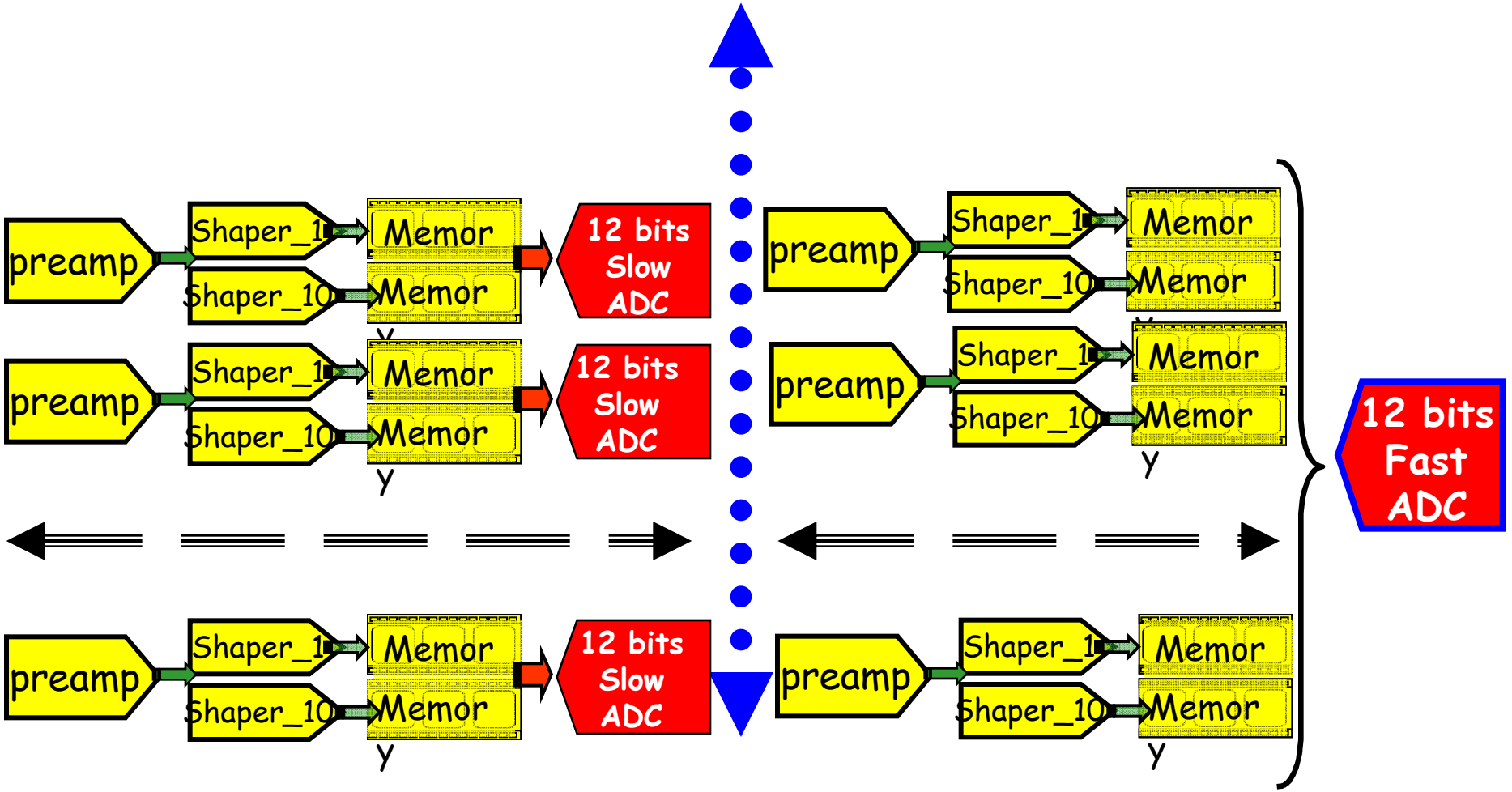
Process matching is basically limiting

The **faster** design is the more **power efficient**

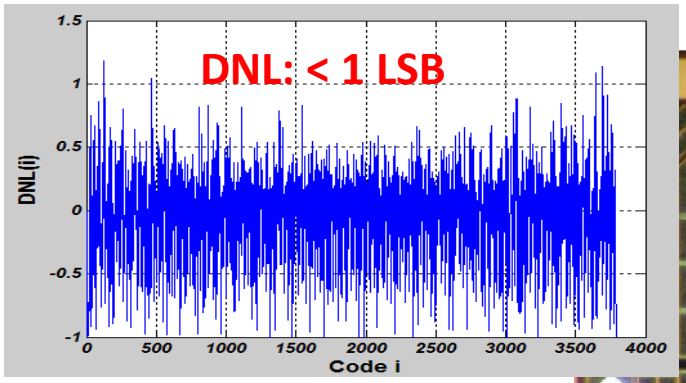
Feature Size [µm]	Year	Speed [MS/s]	Power [mW]	Supply [V]	*FOM3*=Power/Speed [mW/MS/s]
0.8	1995	40	85	2.7	2.1
0.8	1999	40	119	3.3	3
0.8	1998	20	28	2.4	1.4
0.6	1998	14.3	36	1.5	2.5
0.6	1996	40	28	5	0.7
0.5	2001	200	280	3	1.4
0.35	2000	40	55	3	1.4
0.35	2000	100	105	3	1.1
0.35	1999	100	93	3	0.9
0.35	2000	10	15	3.3	1.5
0.3	2002	30	16	2	0.5
0.25	2000	20	43	1.4	2.2
0.25	1999	45	25	1.5	0.6
0.18	2001	80	80	1.8	1.0
0.18	2003	100	69	1.8	0.7
0.18	2003	150	100	1.8	0.7
0.12	2002	100	120	1.2	1.2

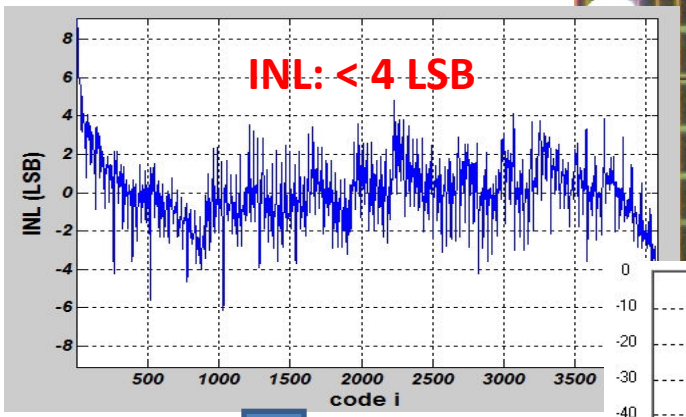
Slow versus fast digitizer for CALICE

Which one will optimize better: Power / Clock noise / cross talk

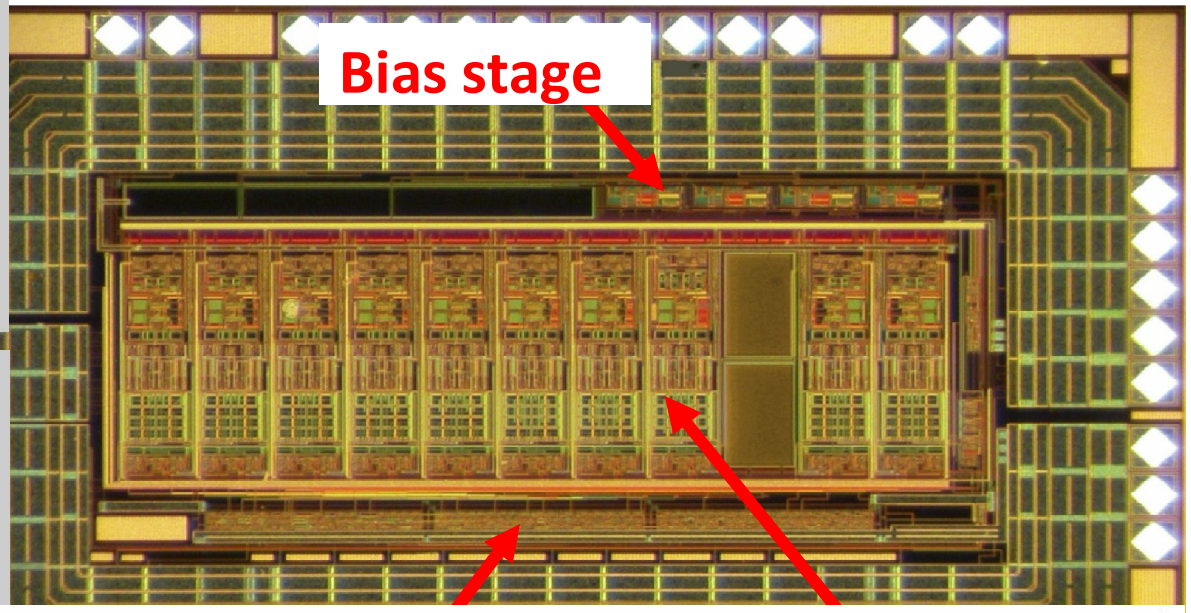


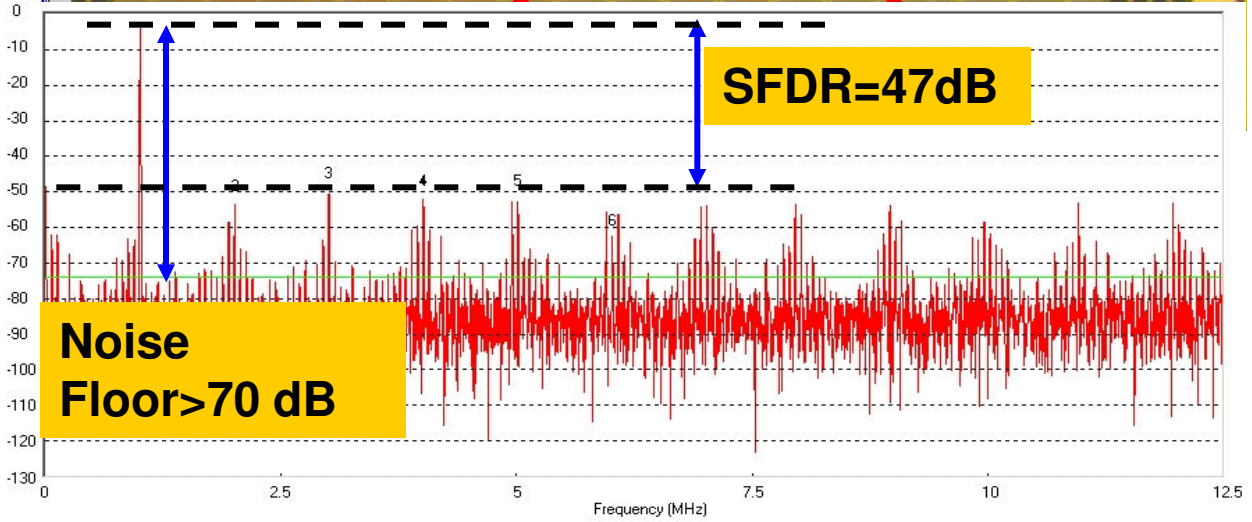
12 bits ADC; 25 MS/s; 35mW; and 2VPP range in 3.5V supply



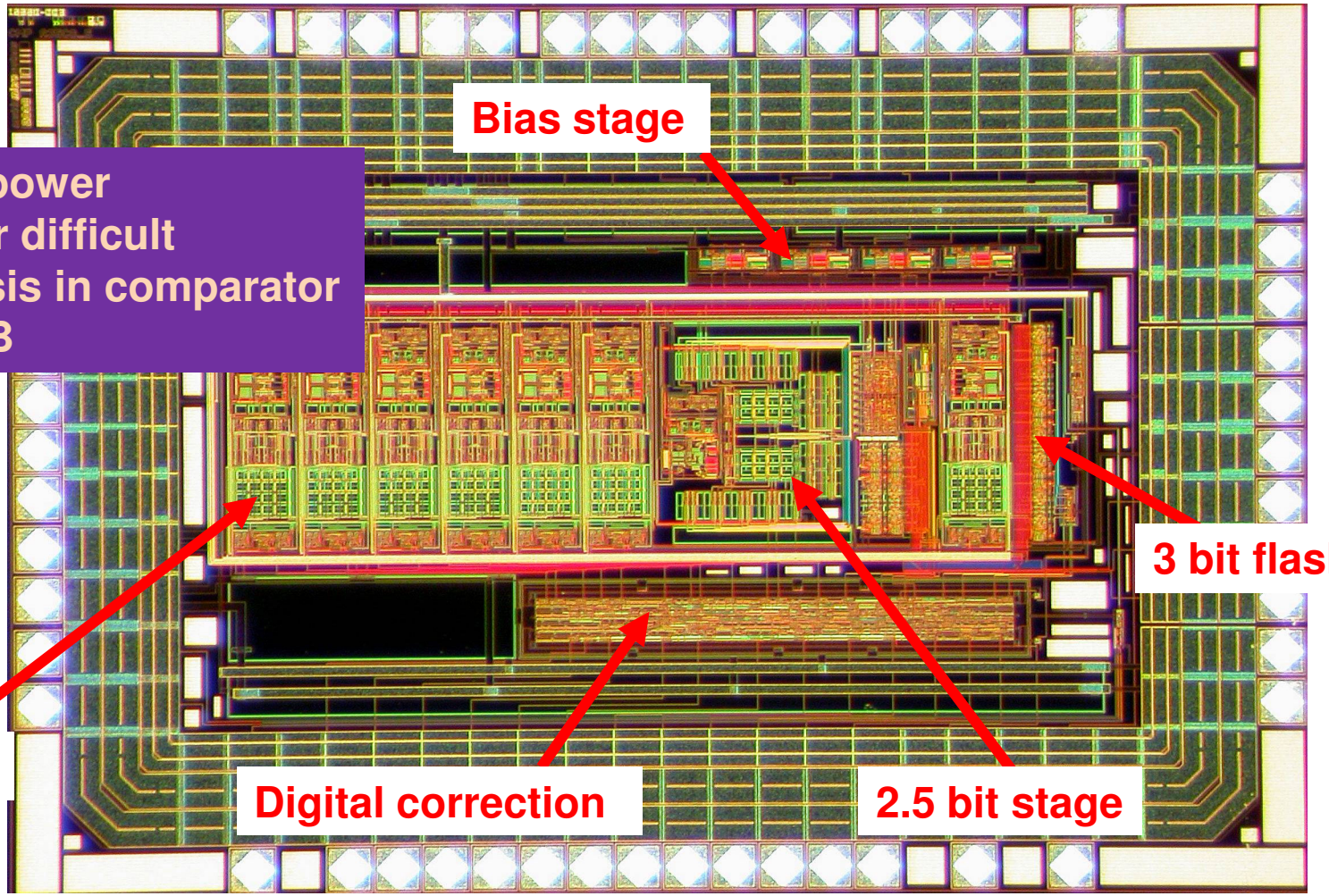


Process limiting (10 bits)



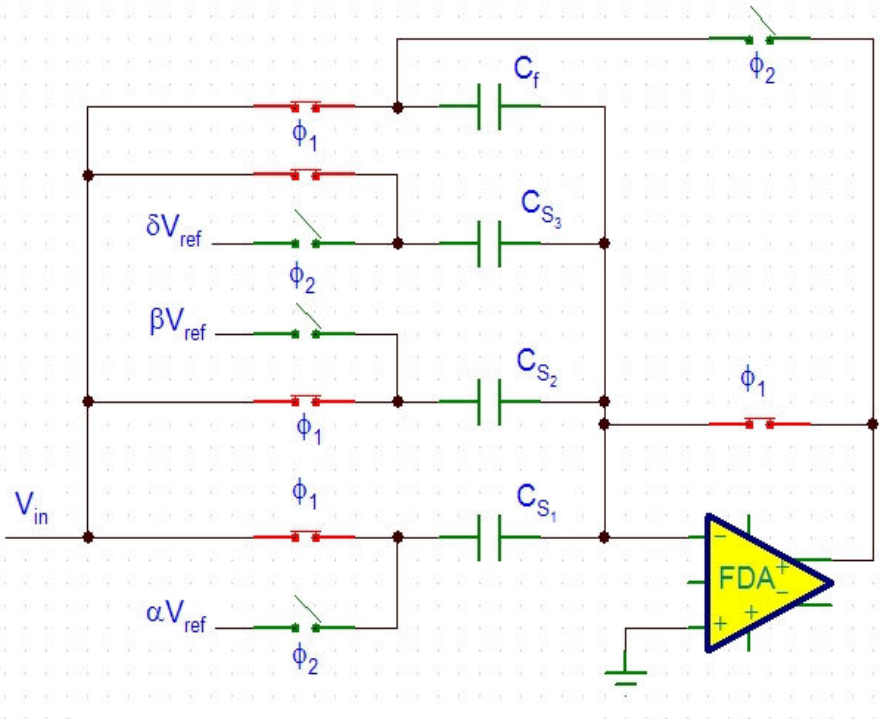


12bits ADC=2.5 bits + 1.5 bits +….+ 1.5 bits + 3 bits

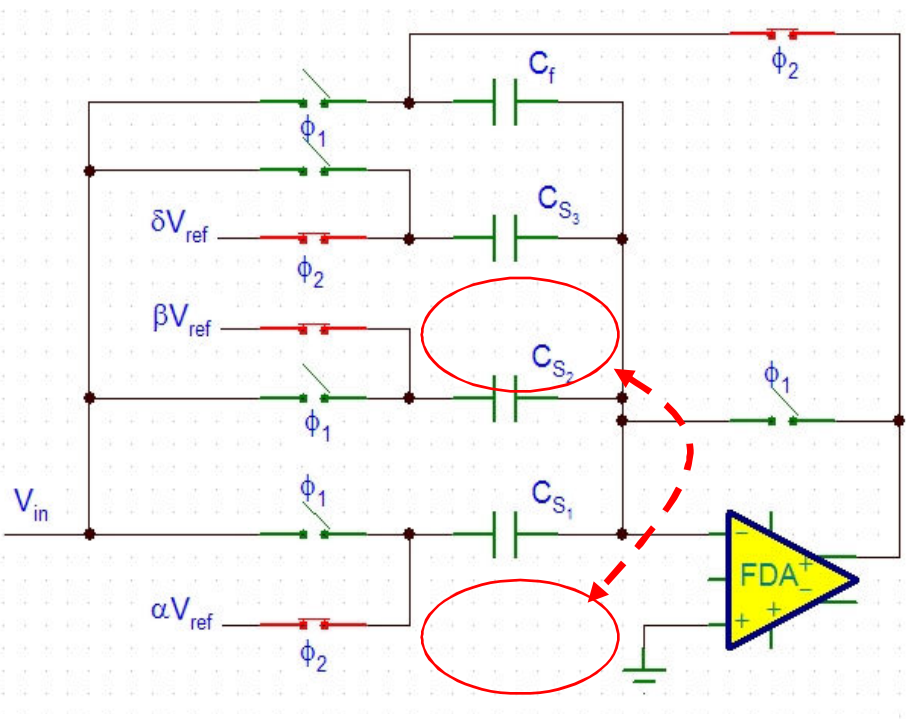


A little less power
But amplifier difficult
And histeresis in comparator
⇒INL ±6 LSB

MDAC 2.5 bit + DEM: Architecture



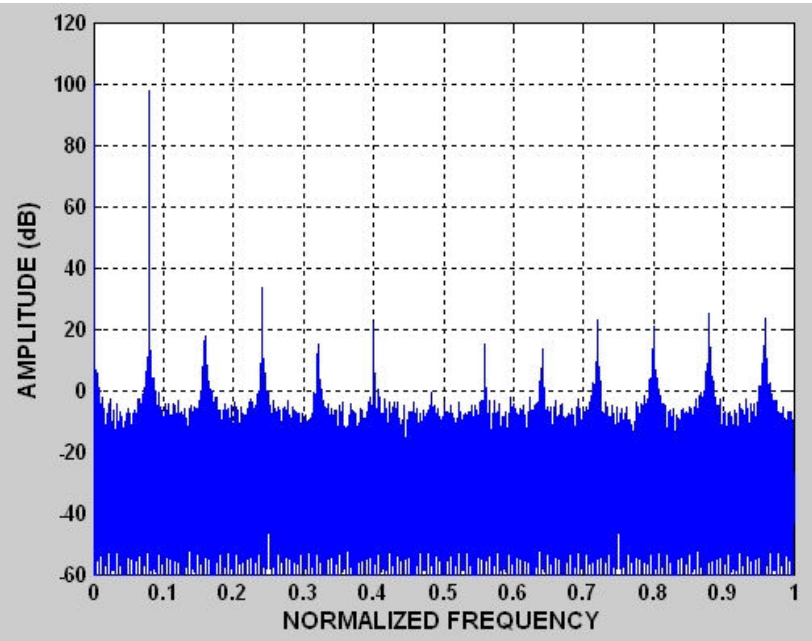
Sampling phase

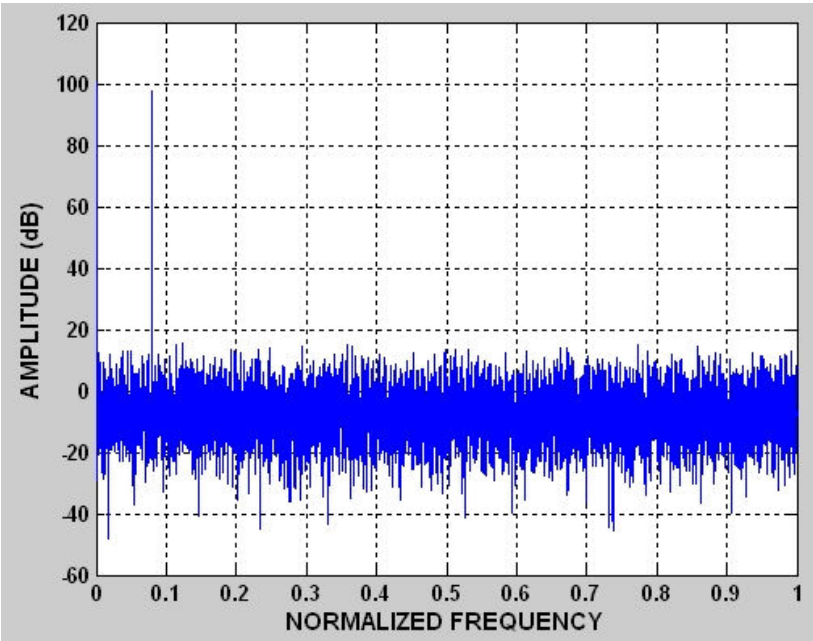


Hold phase + **DEM=> Cf is randomly chosen**

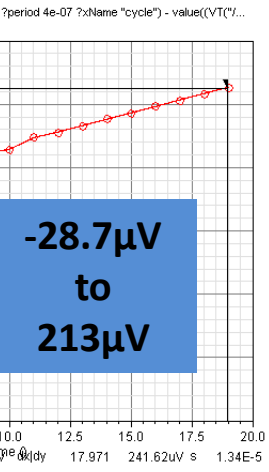
$$V_s = 4 \times V_{in} - 3 \times \mu V_{ref}$$

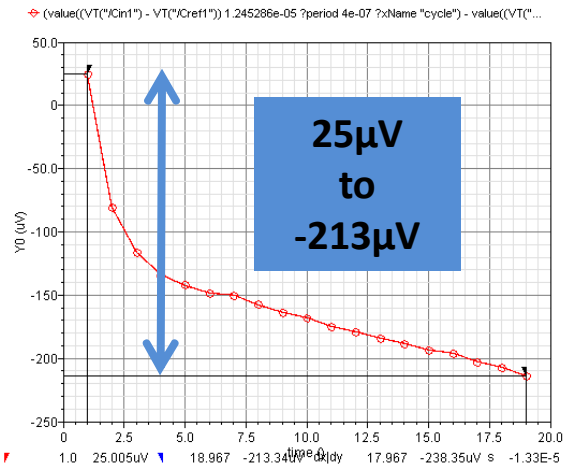
DEM impact on distortion
= harmonics transfert into noise



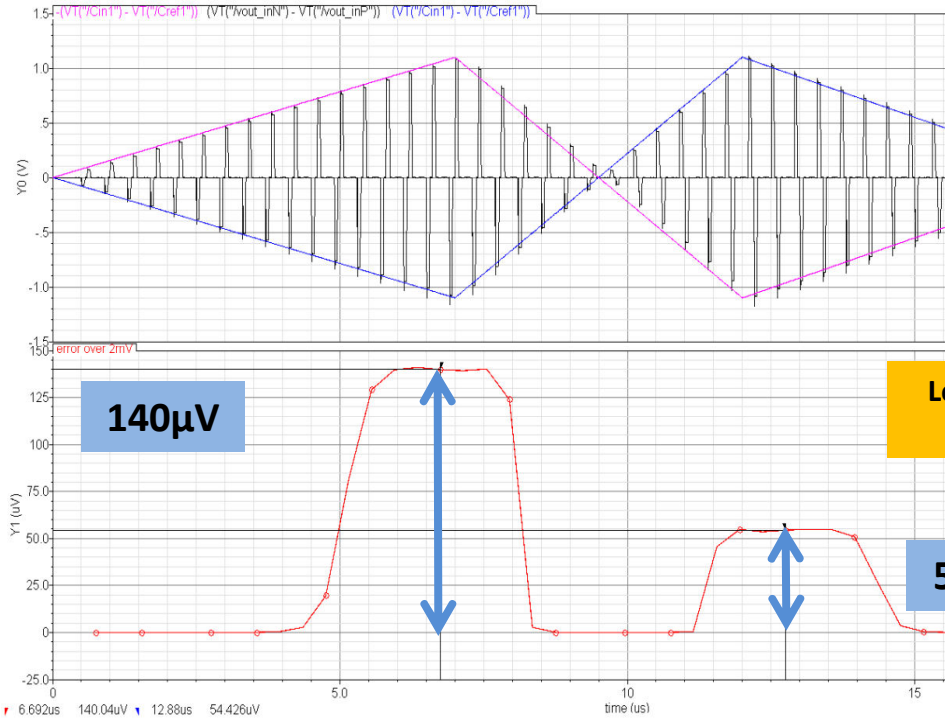


Multiplexer simulation results



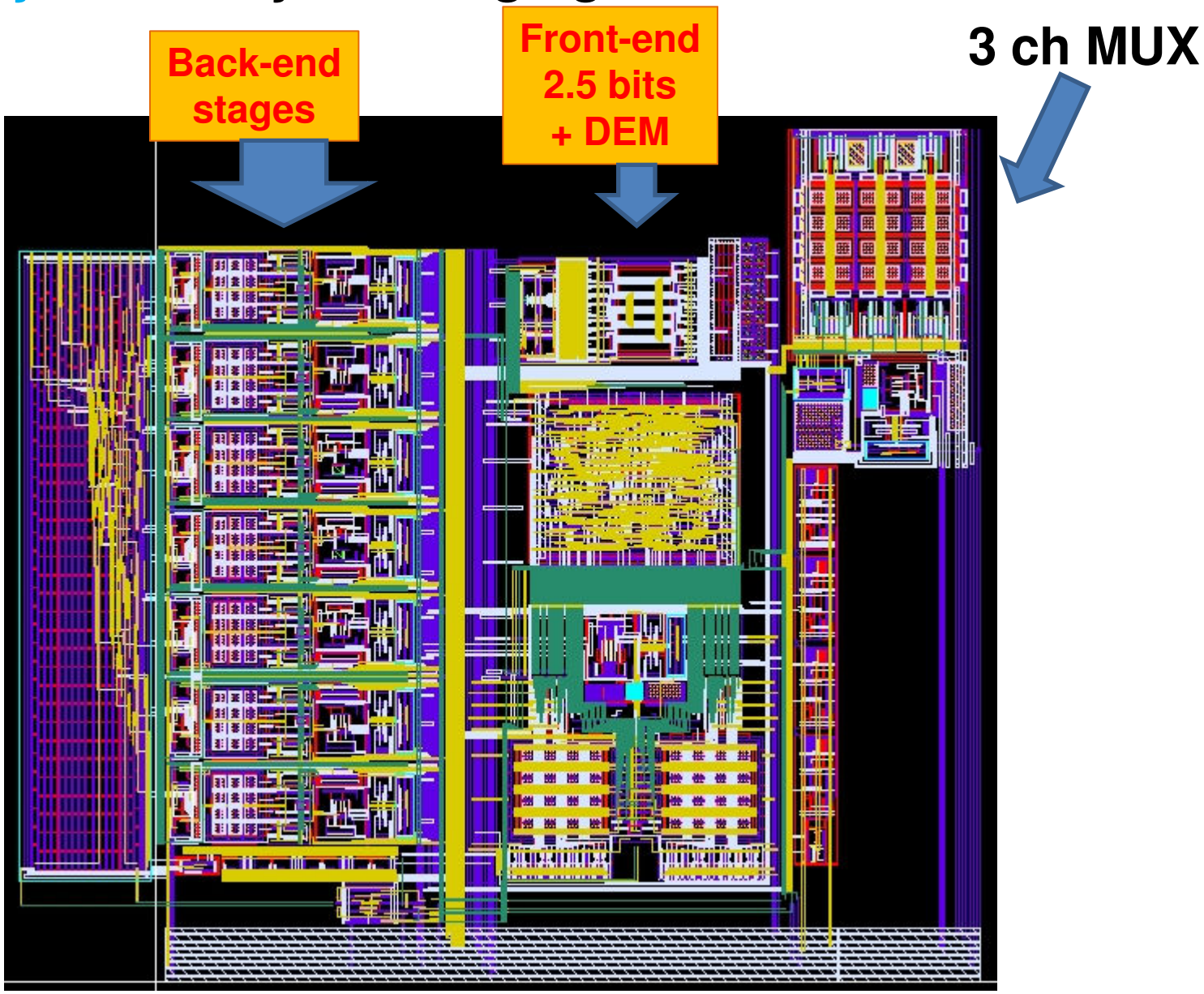


utput multiplexer signal linearity

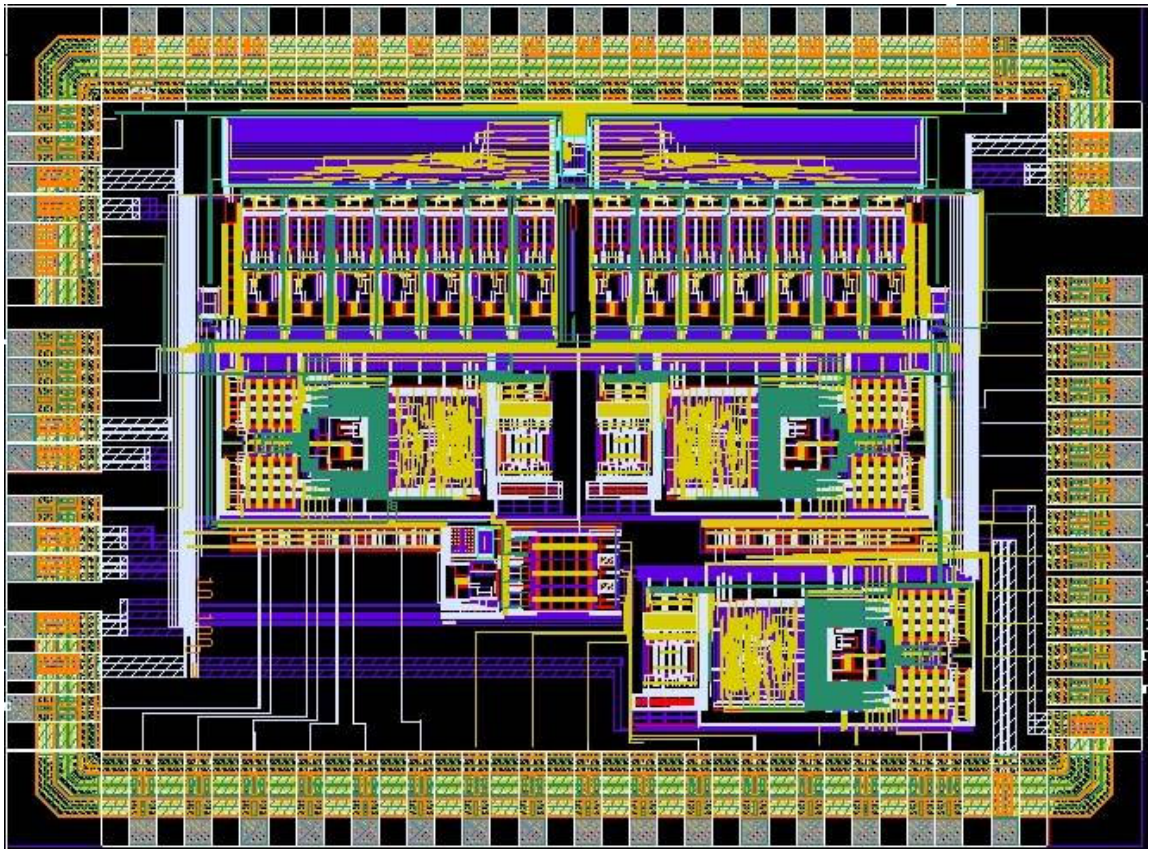


Output multiplexer low signal line

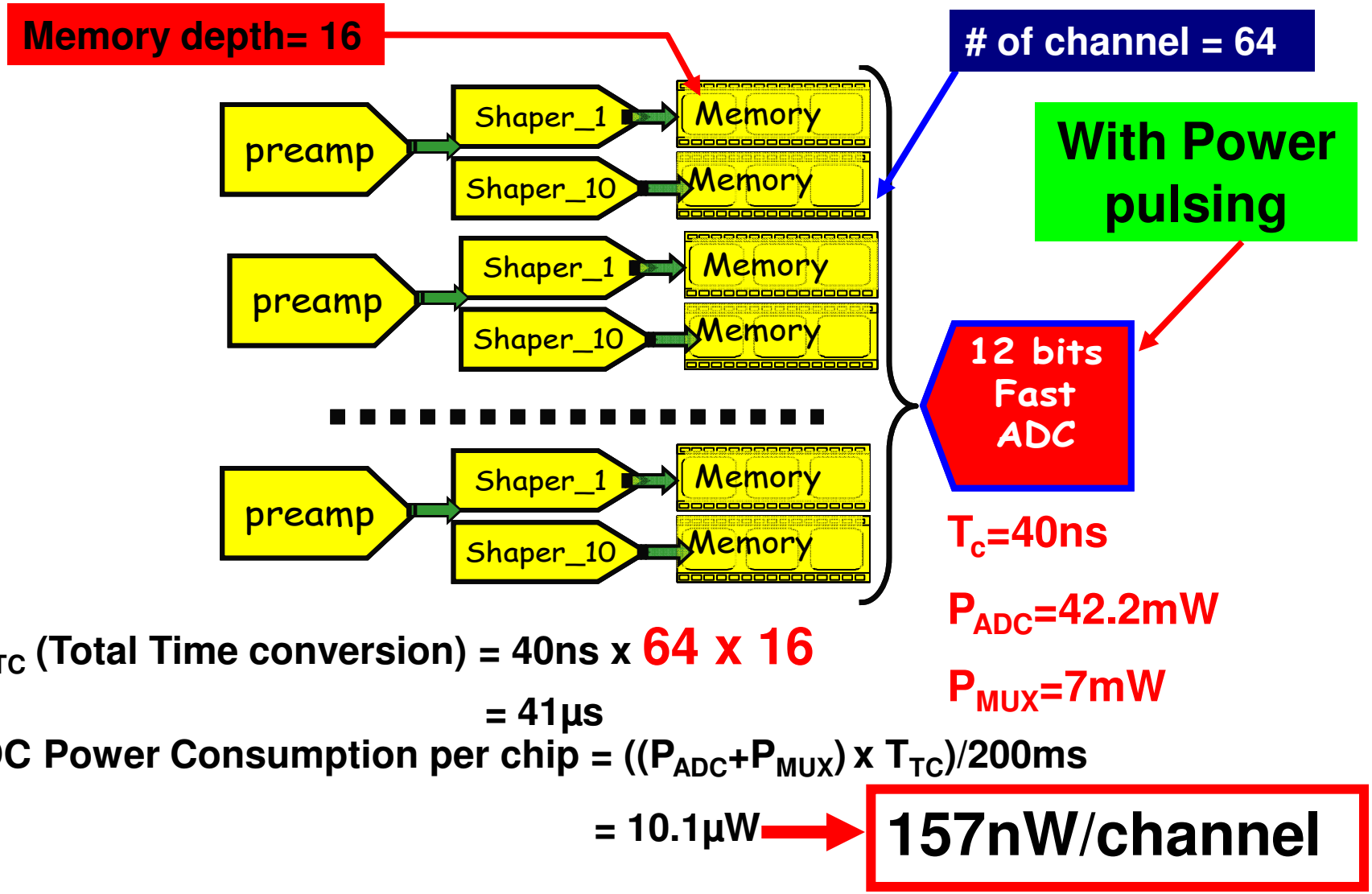
The layout is very challenging for the DEM



Ultimate prototype of our ADC,
including: the DEM stage and the Multiplexer



Conclusion 1: power efficiency



T_{TC} (Total Time conversion) = 40ns x 64 x 16

= 41µs

ADC Power Consumption per chip = ((P_{ADC}+P_{MUX}) x T_{TC})/200ms

= 10.1µW → **157nW/channel**

Conclusion 2

1. A DEM archictecture is design to improve the SFDR and INL
2. A digital correction algorithm was successfully tested, and will be published
3. A critical point is the MUX => simulations for 16 channels but testing will be a more strong argument.

1. DO WE REALLY NEED A 12 BITS CONVERTER ?? WATCH THE SNR IN THE FRONT-END STAGES ……