SPIROC ADC measurements

http://omega.in2p3.fr/

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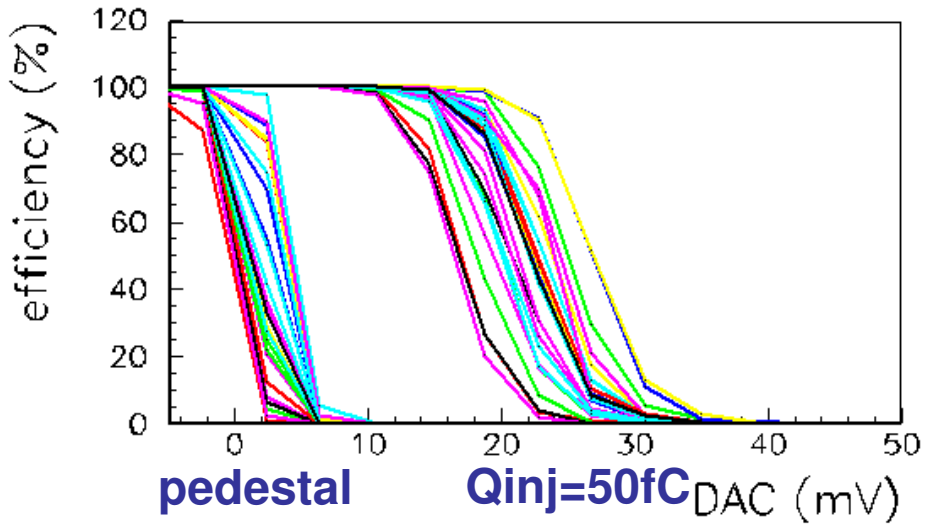
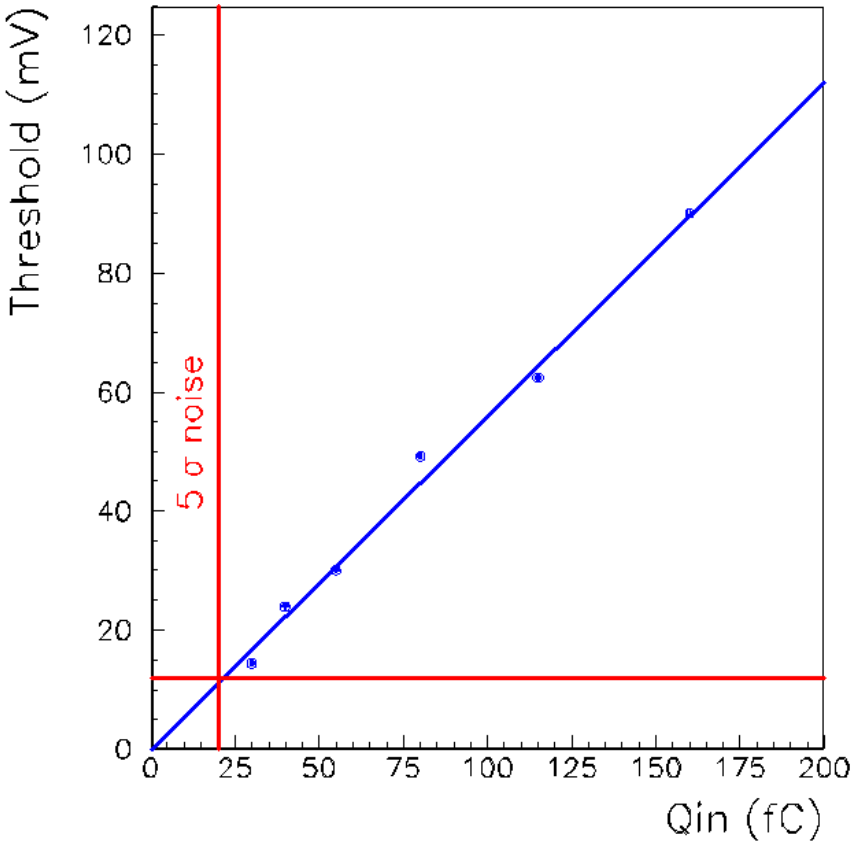
Orsay MicroElectronic Group Associated

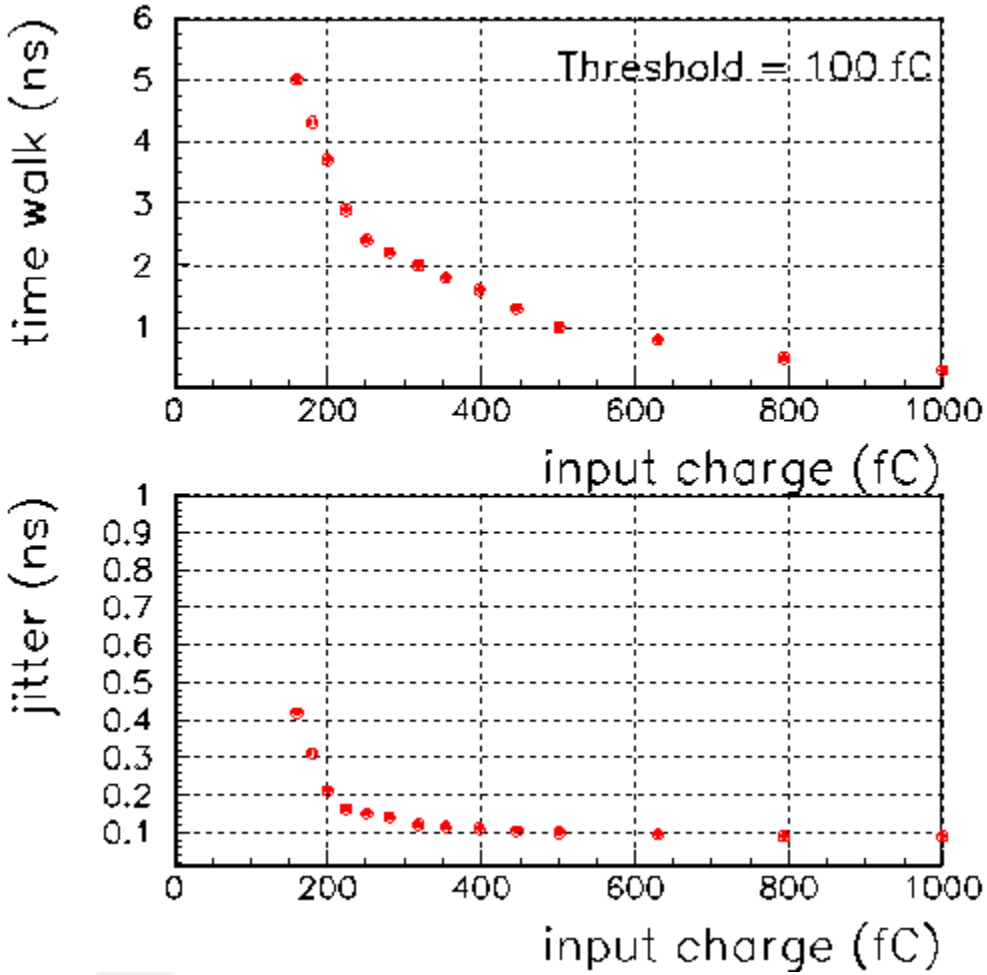
S-curves on fast shaper

- Trigger efficiency versus Threshold (1UDAC=2mV)
- Qinj=50 fC (1/3 pe-)





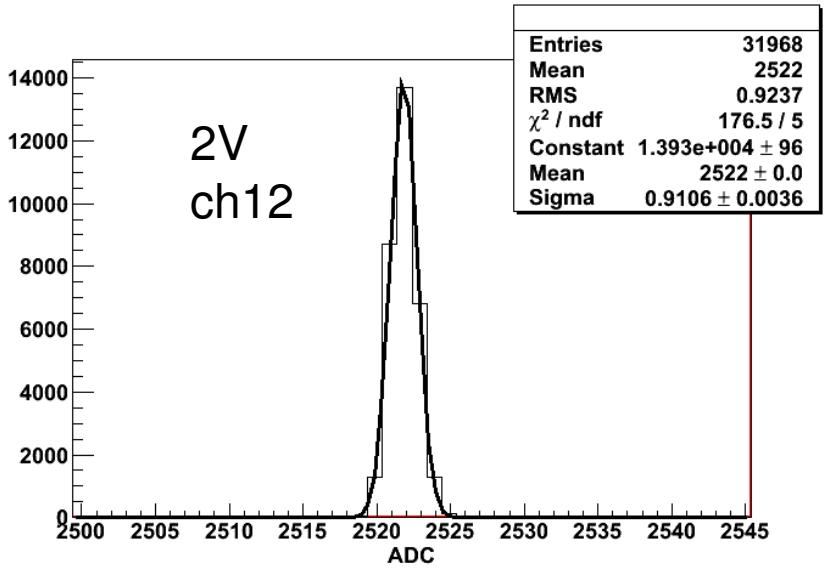
Time measurement

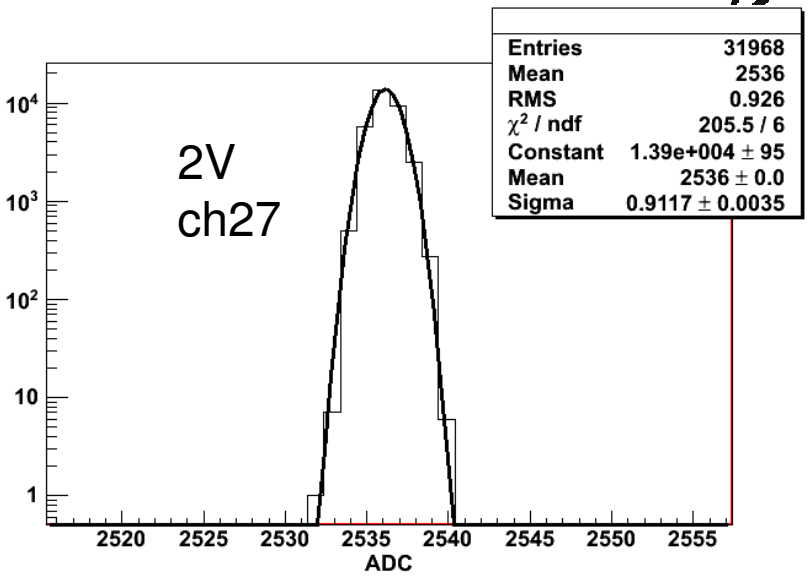


ADC measurements

- ADC alone on SPIROC2
- External DC input
- « Gaussianness »
- noise
- Linearity
  - Steps of 250µV between 1.2 and 2.5 V input
- Stability
  - Measurements during 48h

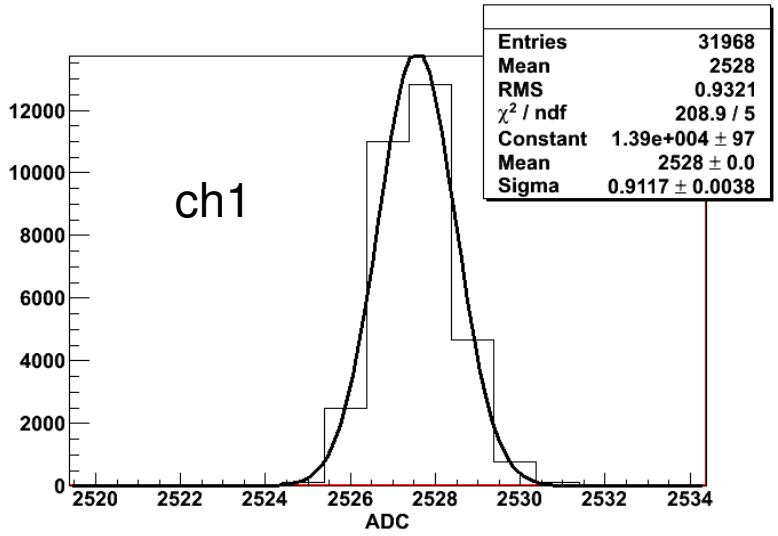
Gaussienne – Forme typique

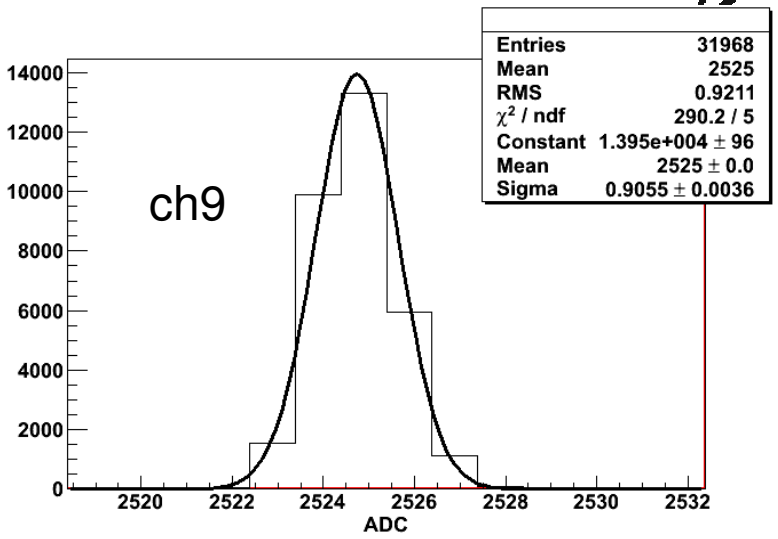


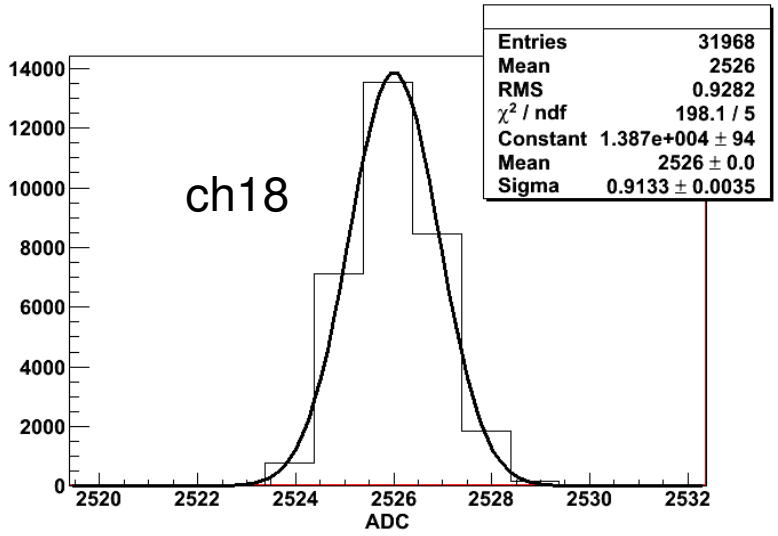


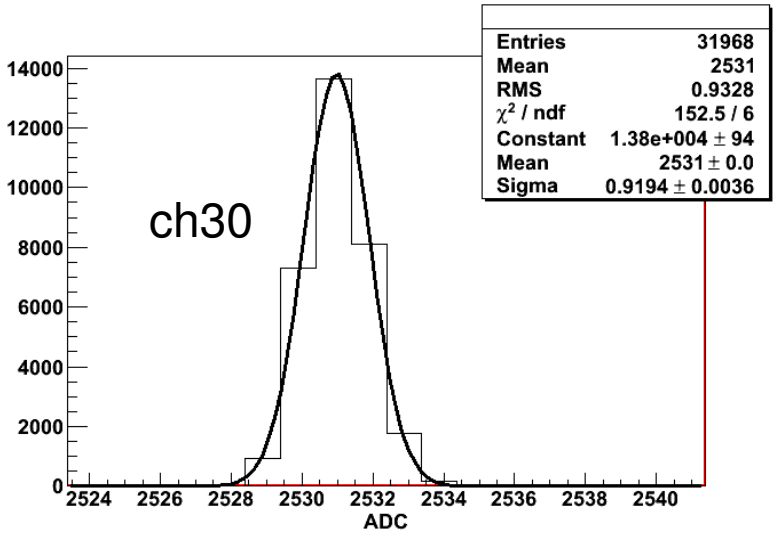
- No tails,
- good uniformity between channels

Gaussiennes – 2 Volt

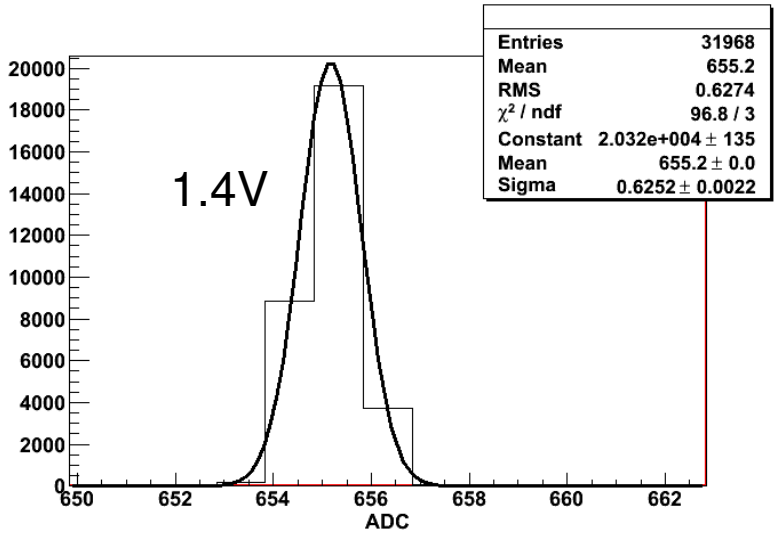


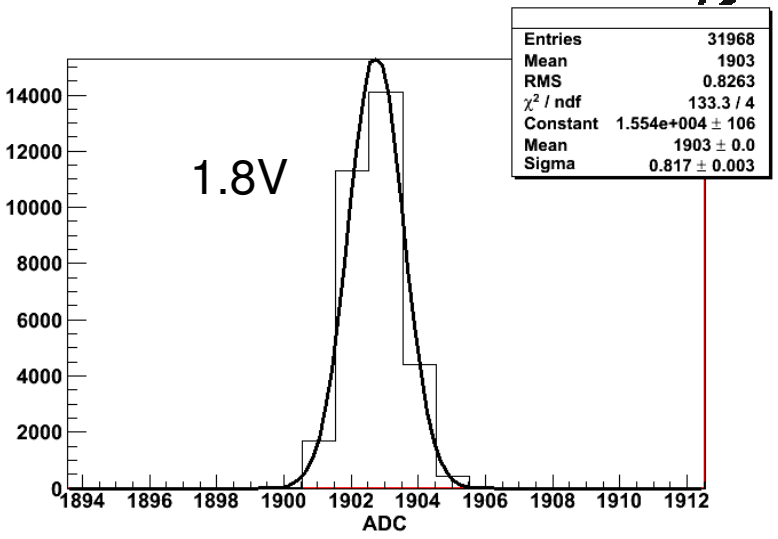


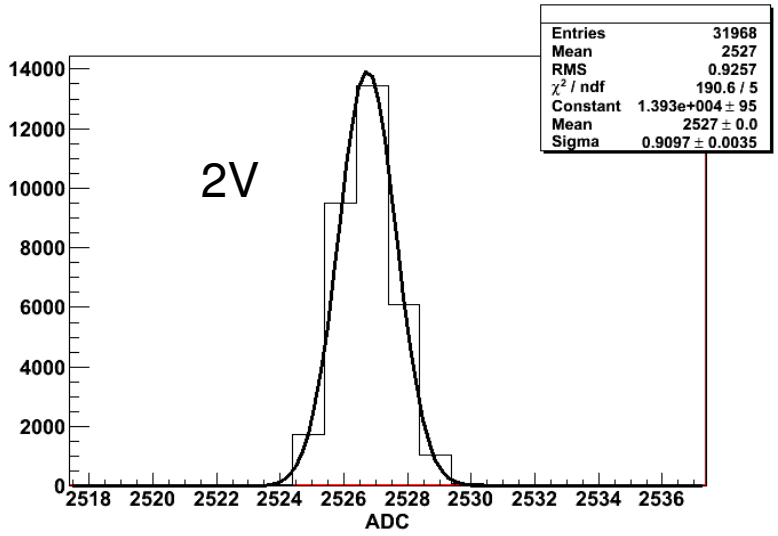


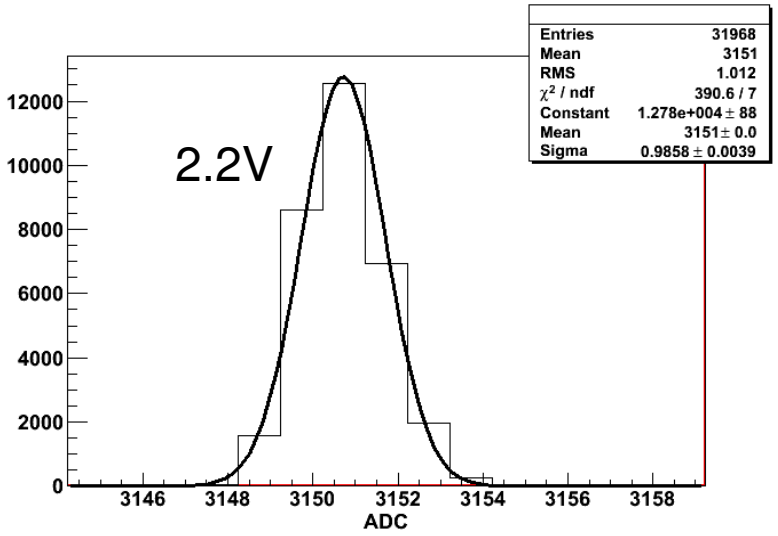


Gaussiennes – Channel 16

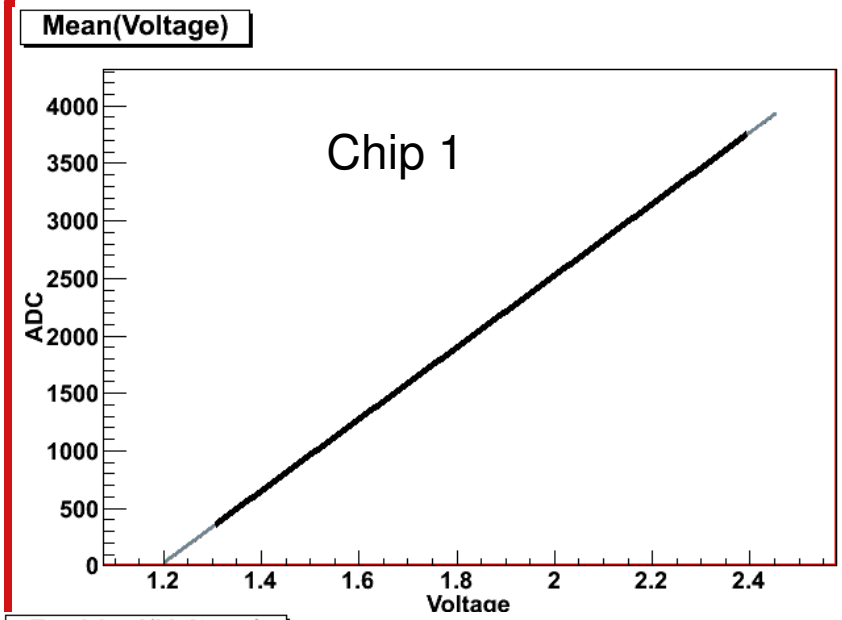


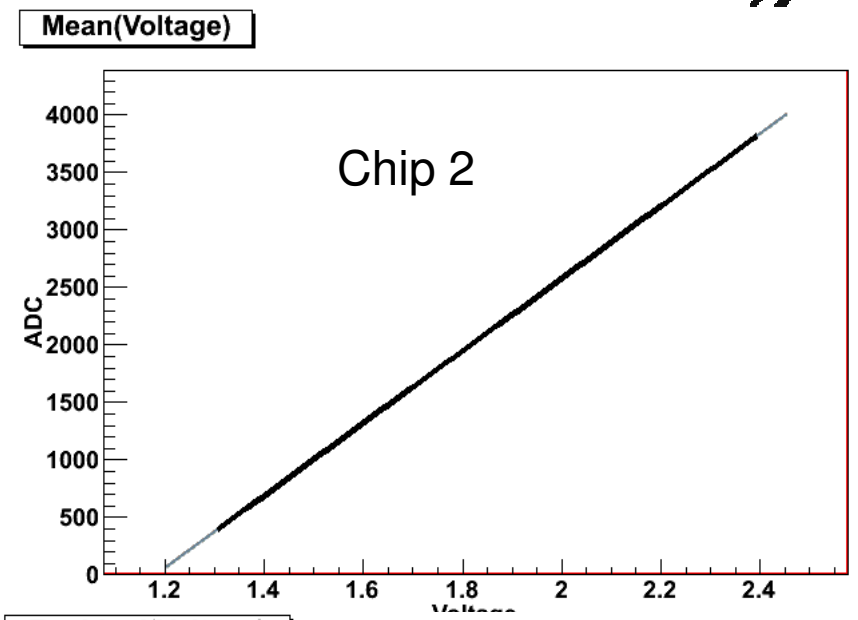


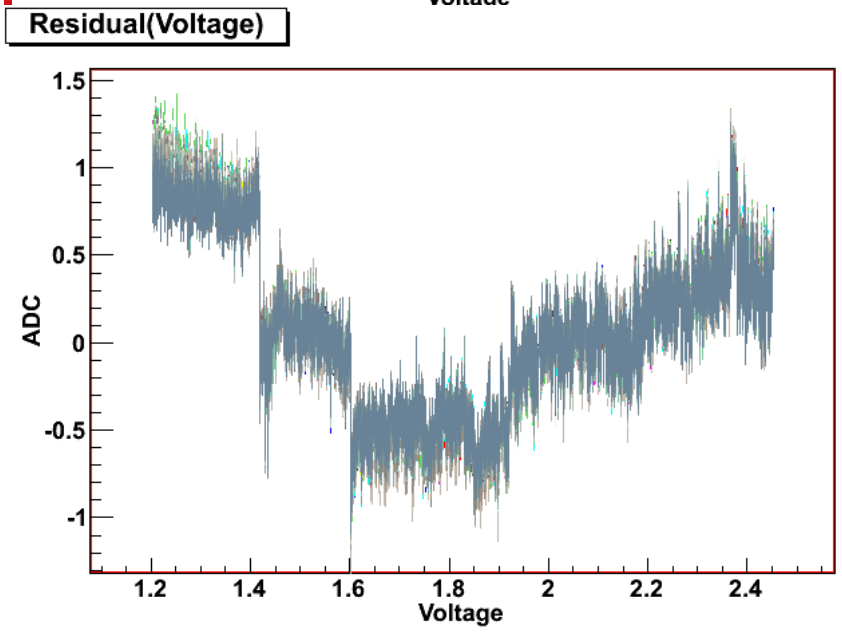


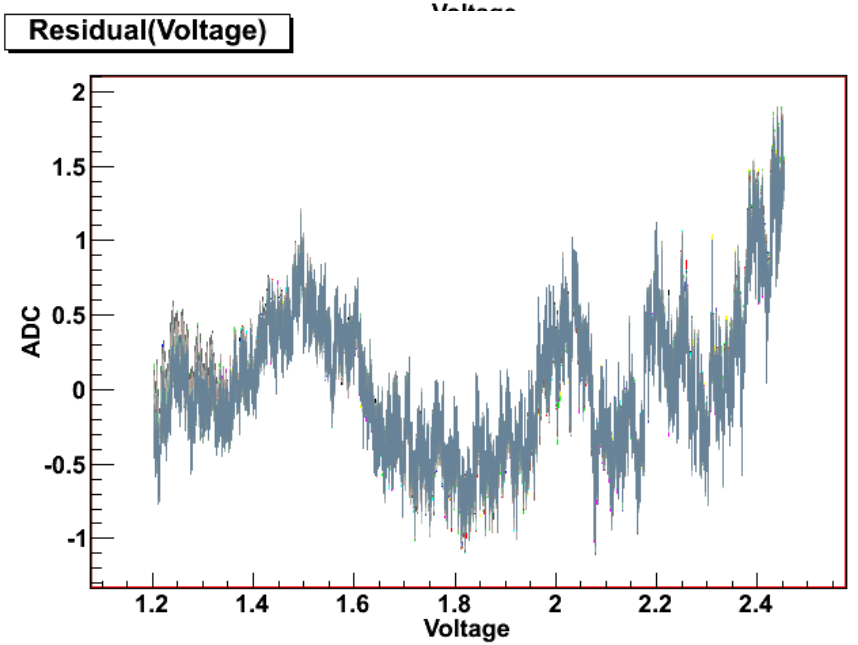


Linéarity

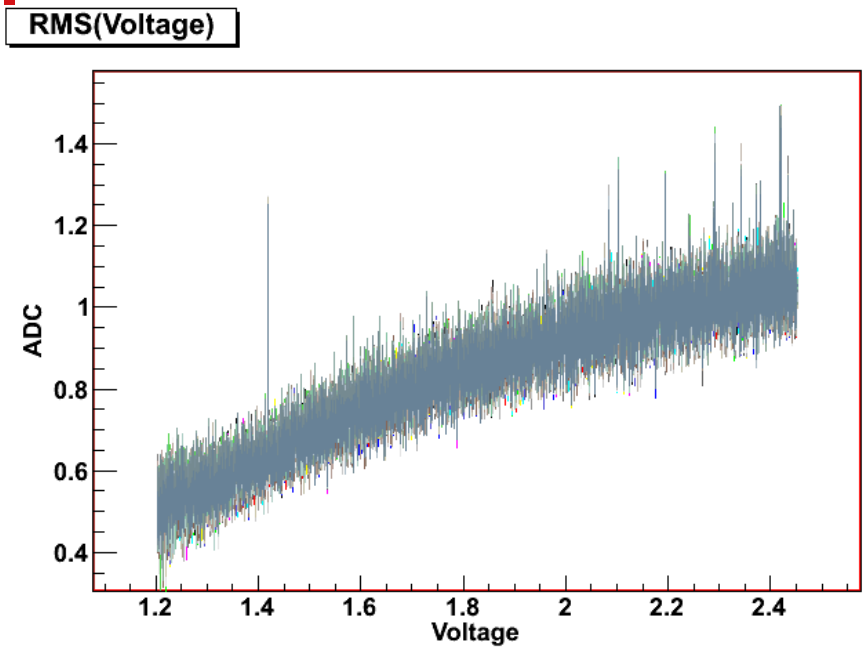

Mean(Voltage)
Chip 1
ADC
Voltage

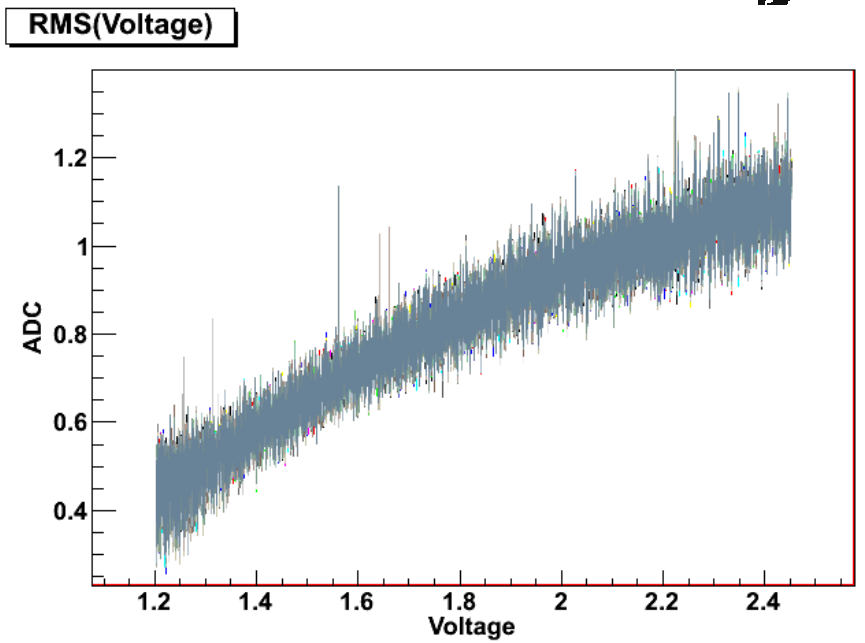

Mean(Voltage)
Chip 2
ADC


Residual(Voltage)
ADC
Voltage


Residual(Voltage)
ADC
Voltage

Linearity : noise



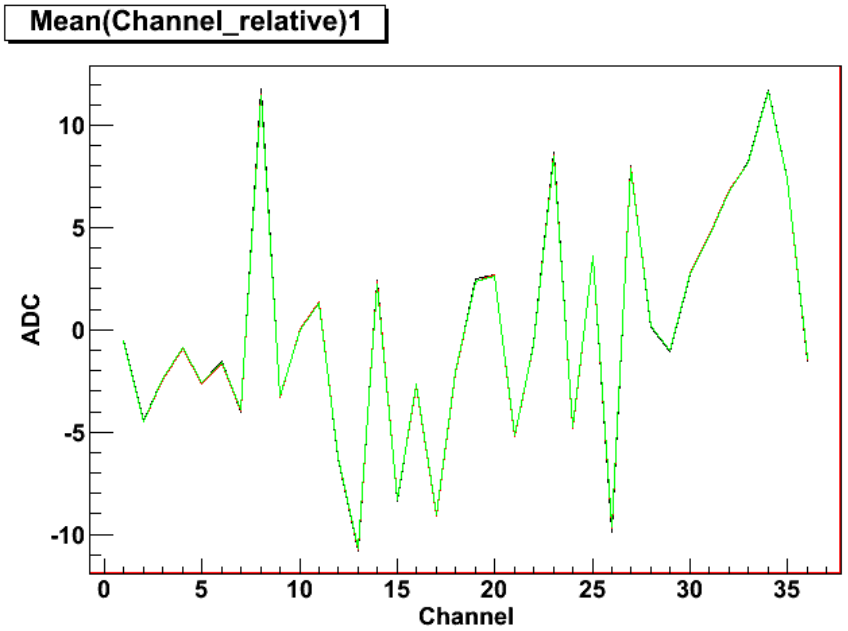


Chip 1

Chip 2

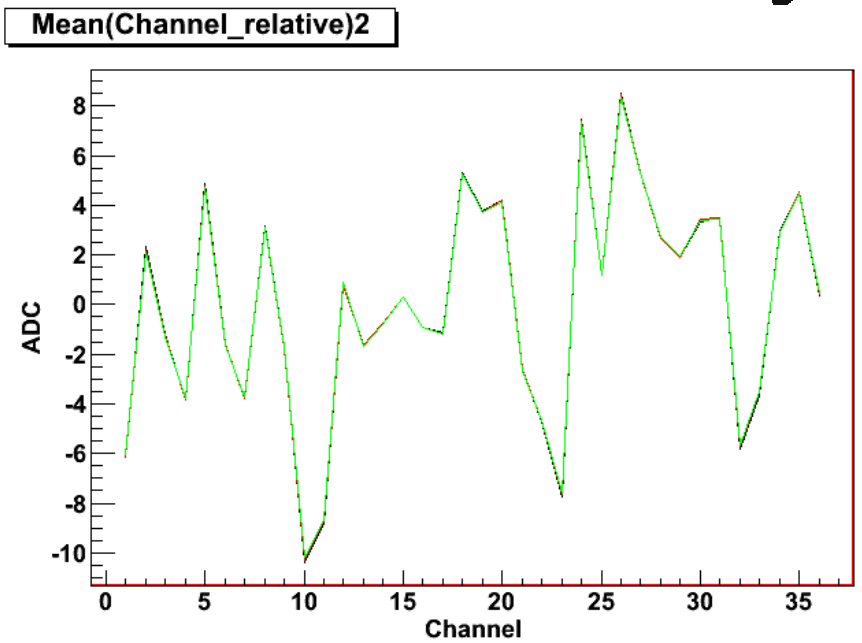
- RMS increasing as a function of amplitude (in sqrt)
- Expected from noise on ramp increasing with time (parallel noise)

Channel - Mean



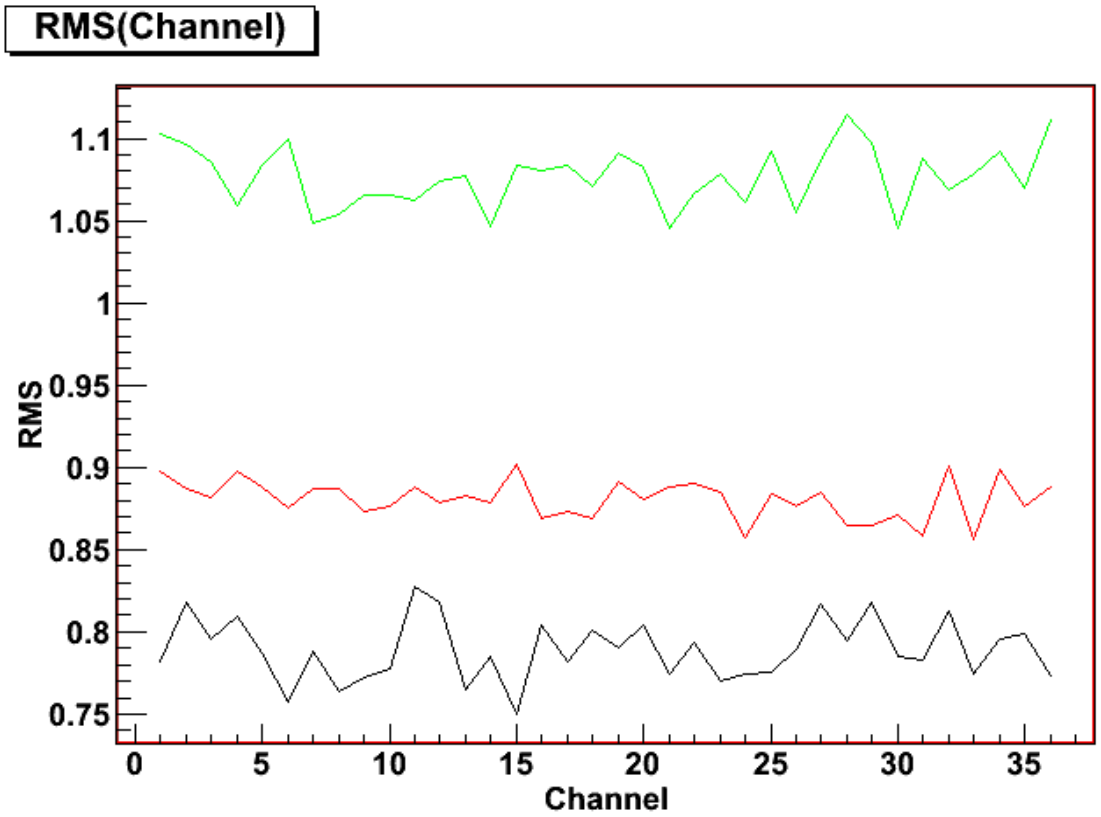
Chip 1

1.6V
2V
2.4V



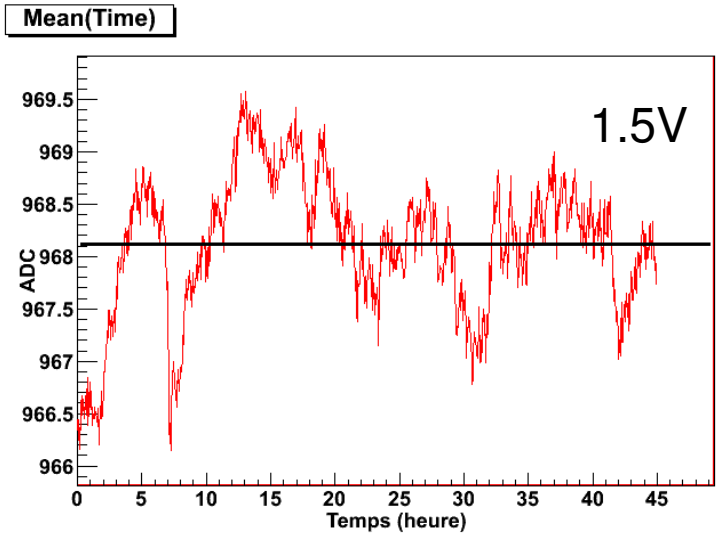
Chip 2

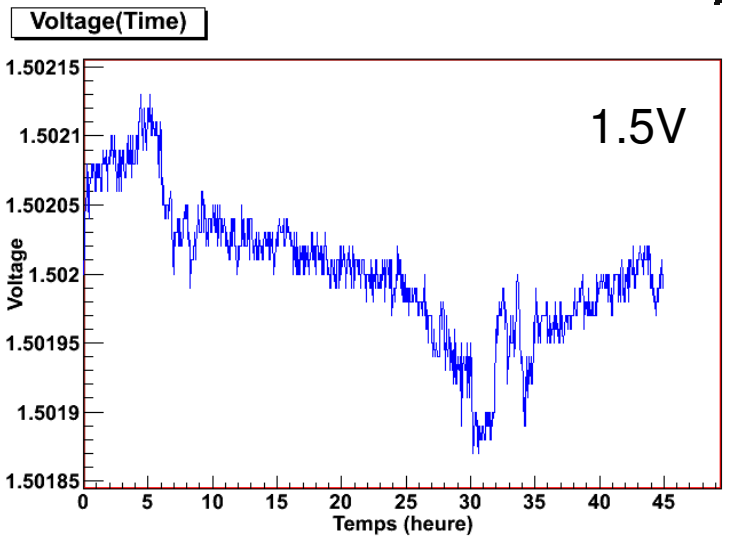
Channel - Chip n °2

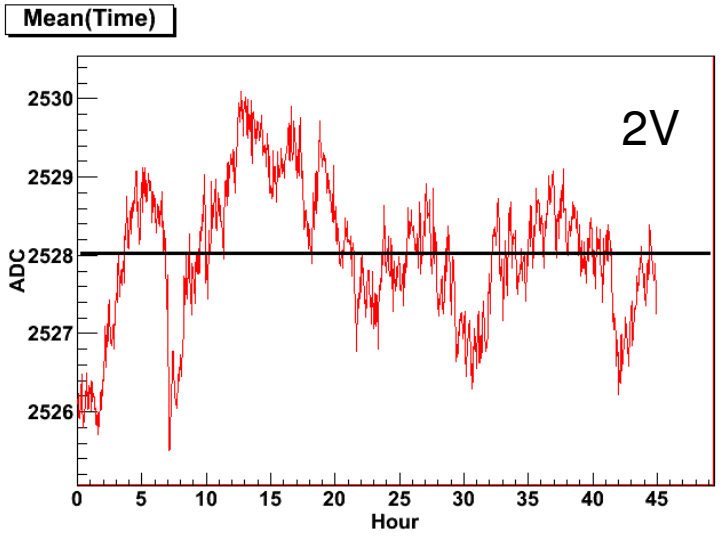


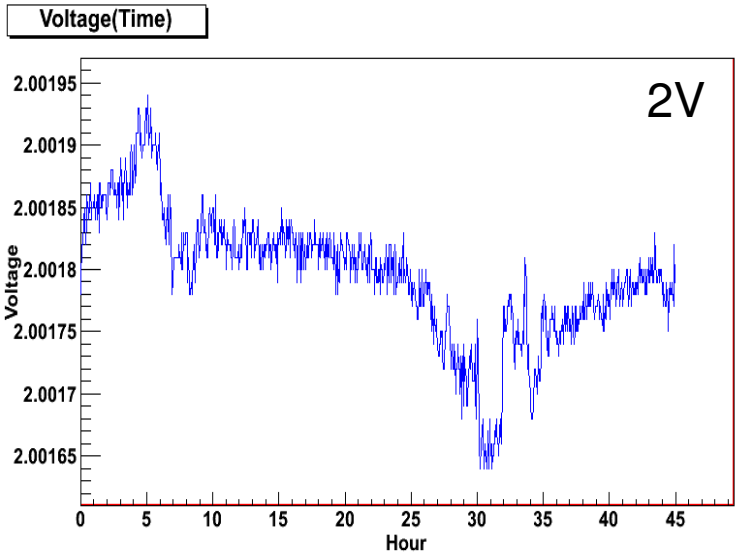
1.70V
1.95V
2.45V

Time stability

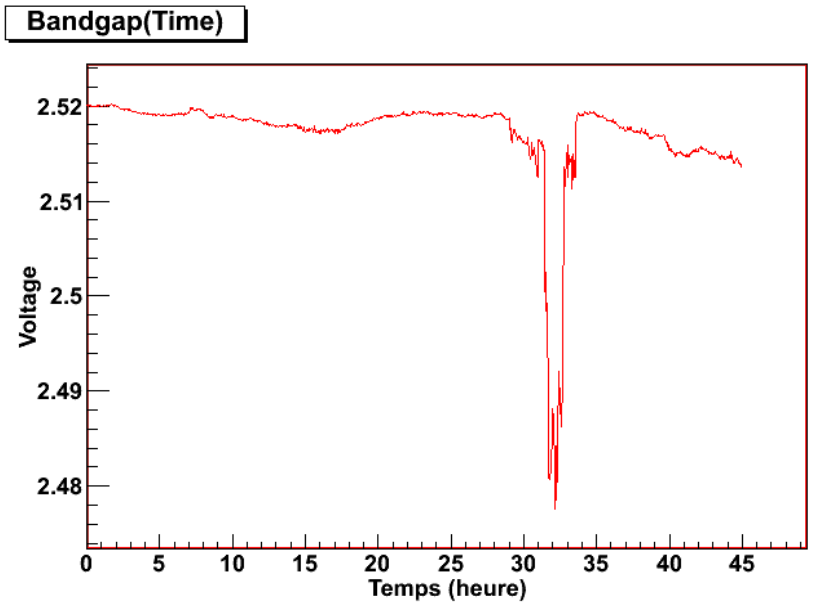


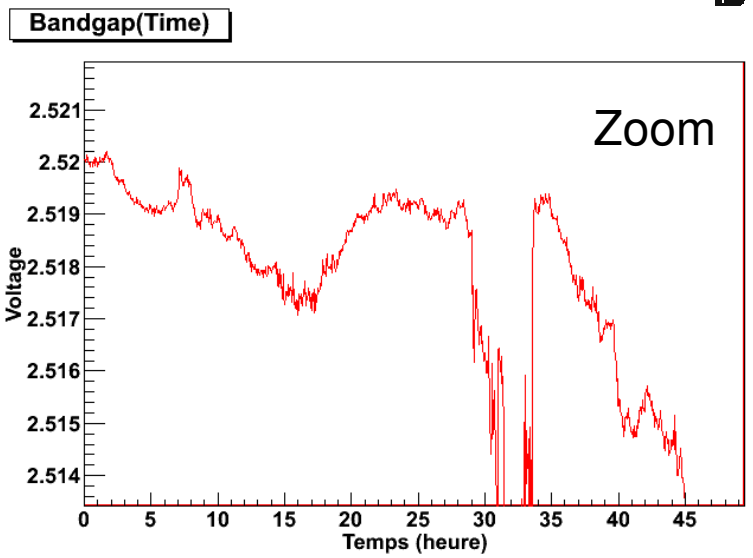


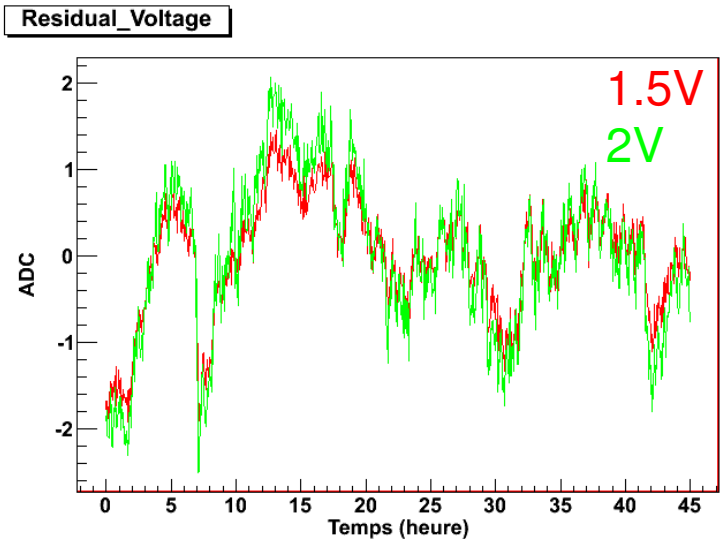




Bandgap







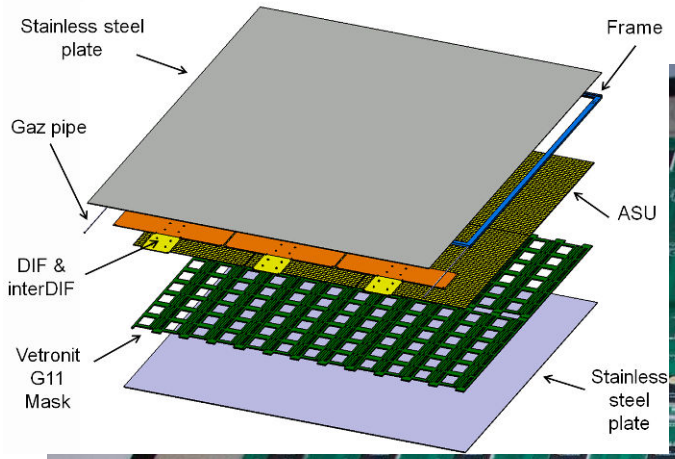
Pas de corrélation évidente entre le bandgap et la stabilité de l'ADC.

Summary and next steps

- ADC performance OK in 12 bits
  - ADC range : 1.2 V, LSB=300 µV
  - Linearity : ± 1 UADC/4096
  - Noise : 0.5-1 UADC but possibly coherent…
  - Stability : ± 2 UADC @ 48 h

- Next steps
  - More stability measurements
  - Full chain measurement
  - Power pulsing operation

DHCAL 1m2 RPC [I. Laktineh et al.]



GRPC

Slab #1 DIF #1

Slab #2 DIF #2

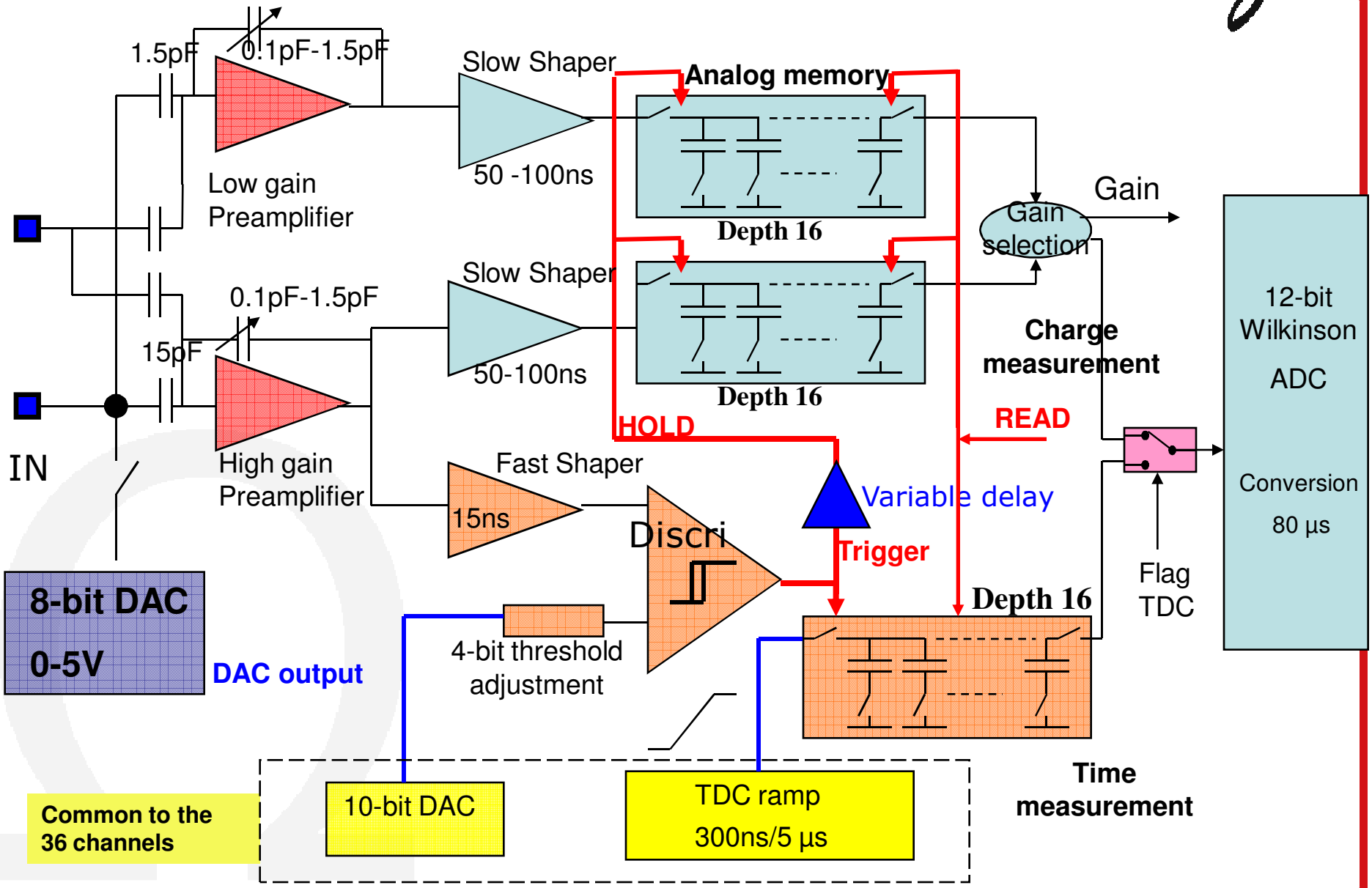
Slab #3 DIF #3

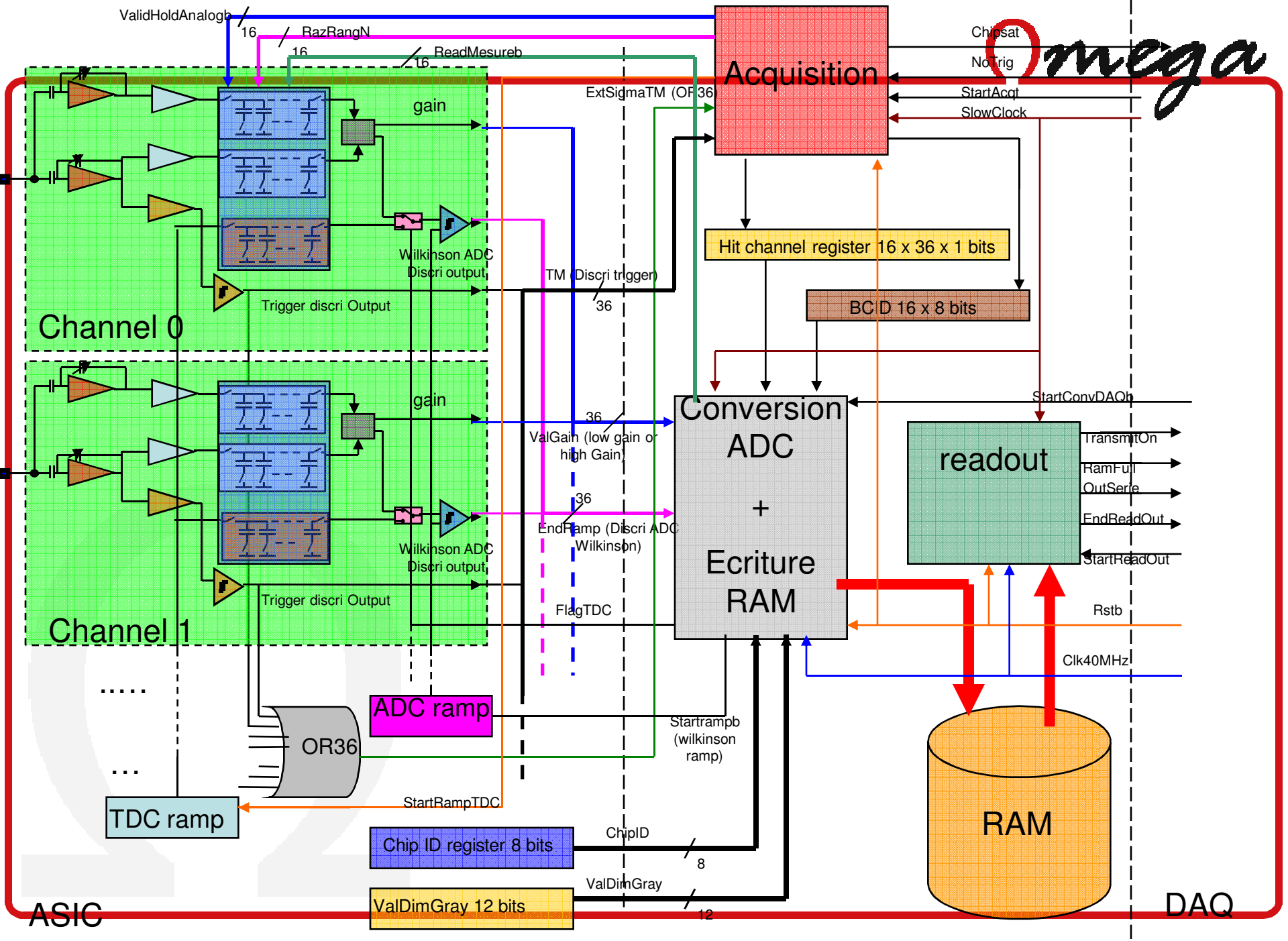
Fully equipped large scalable detector to be soon tested in cosmic rays bench and in test beam at cern in **summer 09**

µMEGAS DHCAL [C. Adloff et al.]

- 2 boards with 24 HaRDROC2
- Validation of readout on long bus lines
- Preliminary power pulsing looks clean.
  - Expect 10 mA for full slab !

SPIROC : One channel schematic




ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BC ID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
RAM
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
ASIC
DAQ