AHCAL Electronics.

Status of Integration

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for the DESY AHCAL developers
AHCAL main and analysis meeting
Hamburg, July 16th and 17th, 2009

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

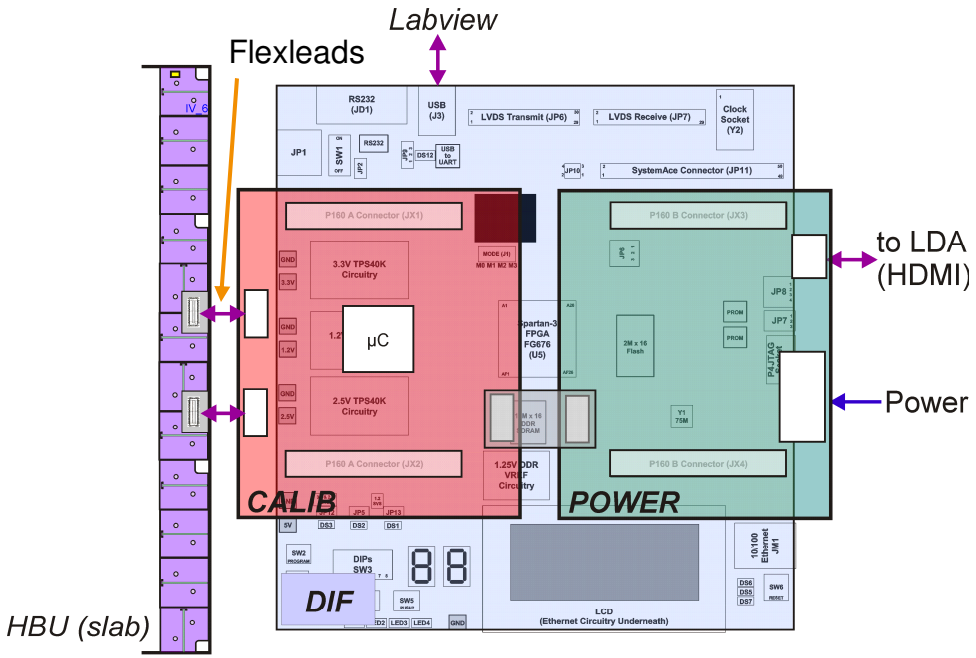
EUDET

DESY

Outline

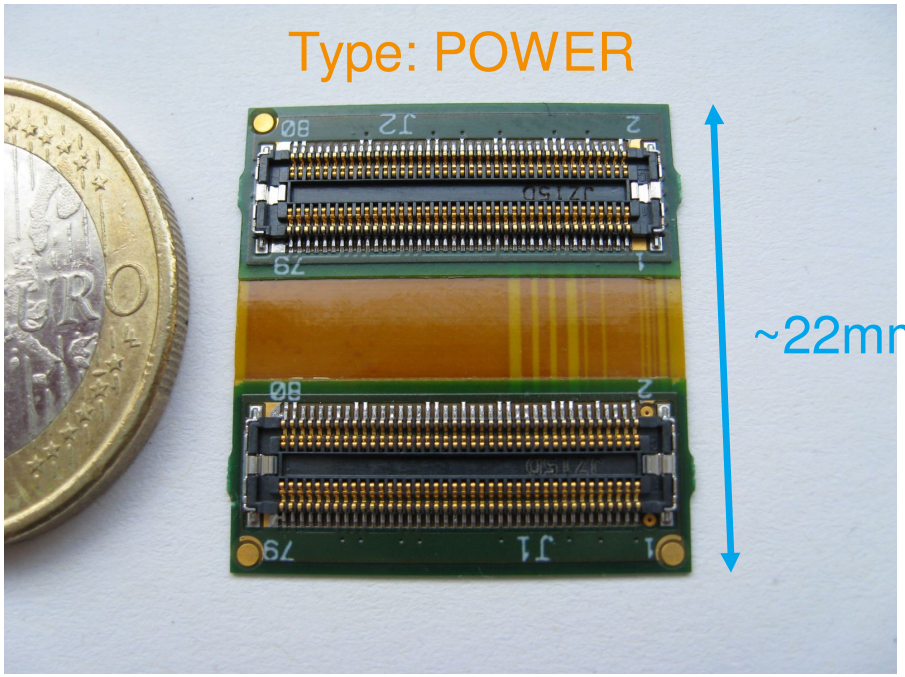
- Hardware Developments at DESY
  - CALIB, POWER, Flexleads
  - HBU0
  - Tiles integration
- System Commissioning
- DIF status
- Conclusions and Outlook

'old-fashioned overview'

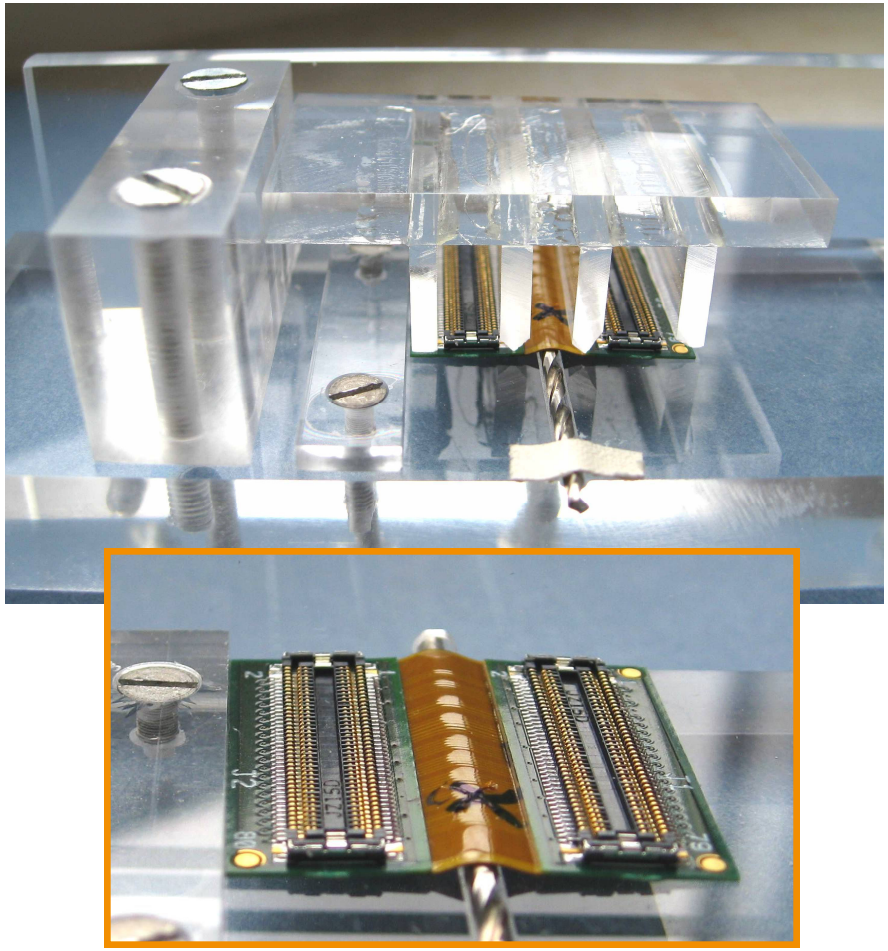


Flexleads (SIGNAL and POWER)

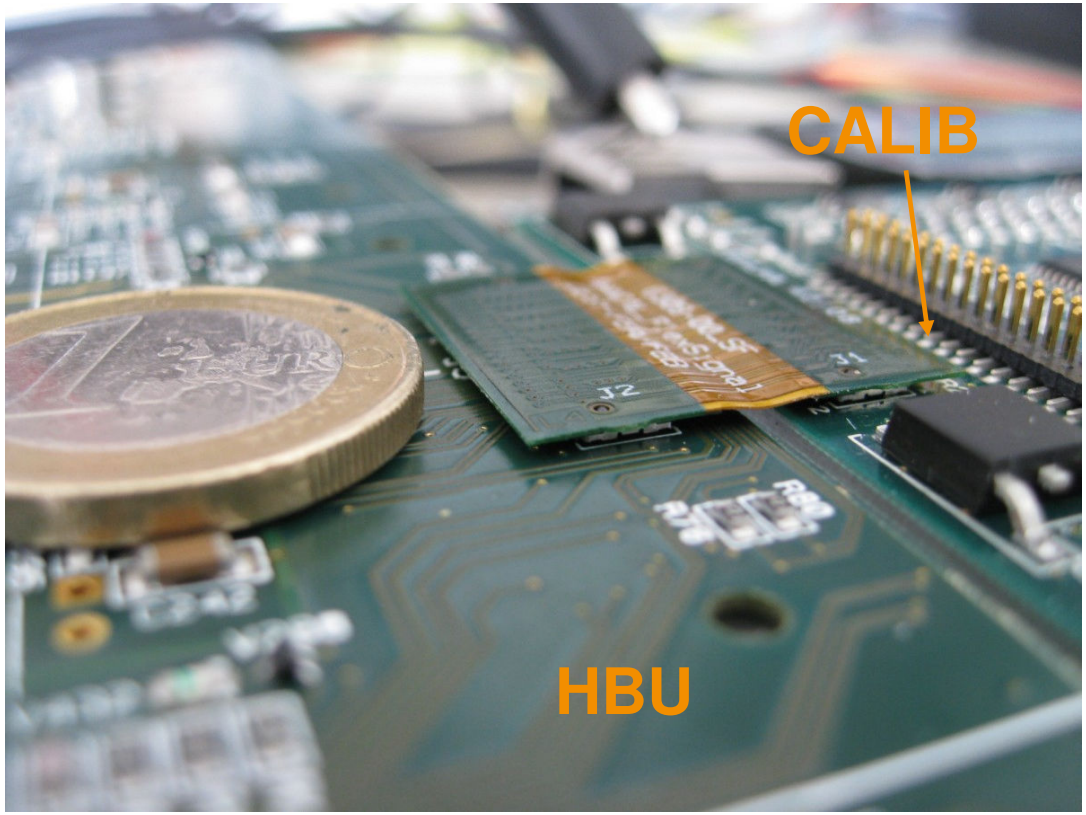
- 20 pieces of each type finished.
- Pre-bending procedure ok.



Flexlead Pre-Bending:



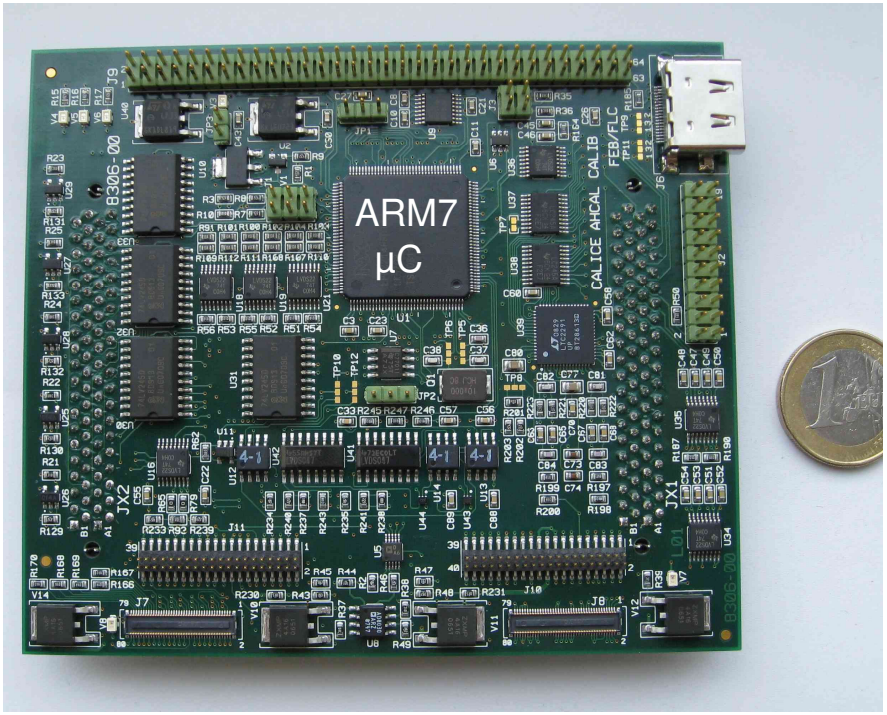
Flexleads (SIGNAL and POWER)



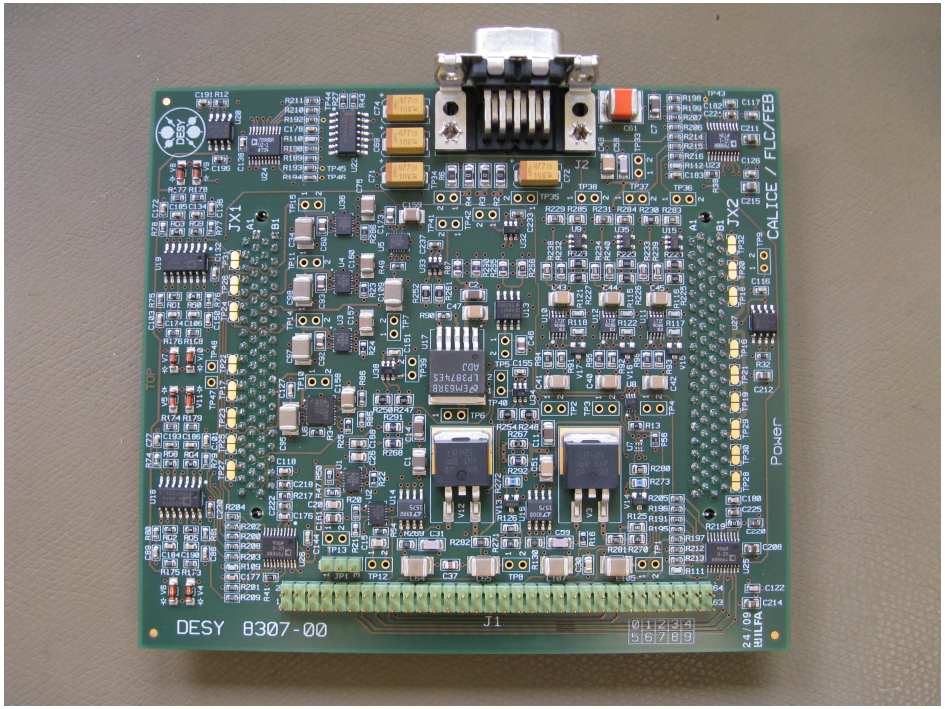
- About 40 connection cycles up to now - still ok.
- Compensate HBU misalignments in distance.
- Fulfill AHCAL height requirements.
- Tests ok concerning:
  - Signal allocation
  - Signal quality
  - Resistance for power

CALIB and POWER modules

CALIB module: 11 x 10 cm²



POWER module: 12.5 x 11 cm²

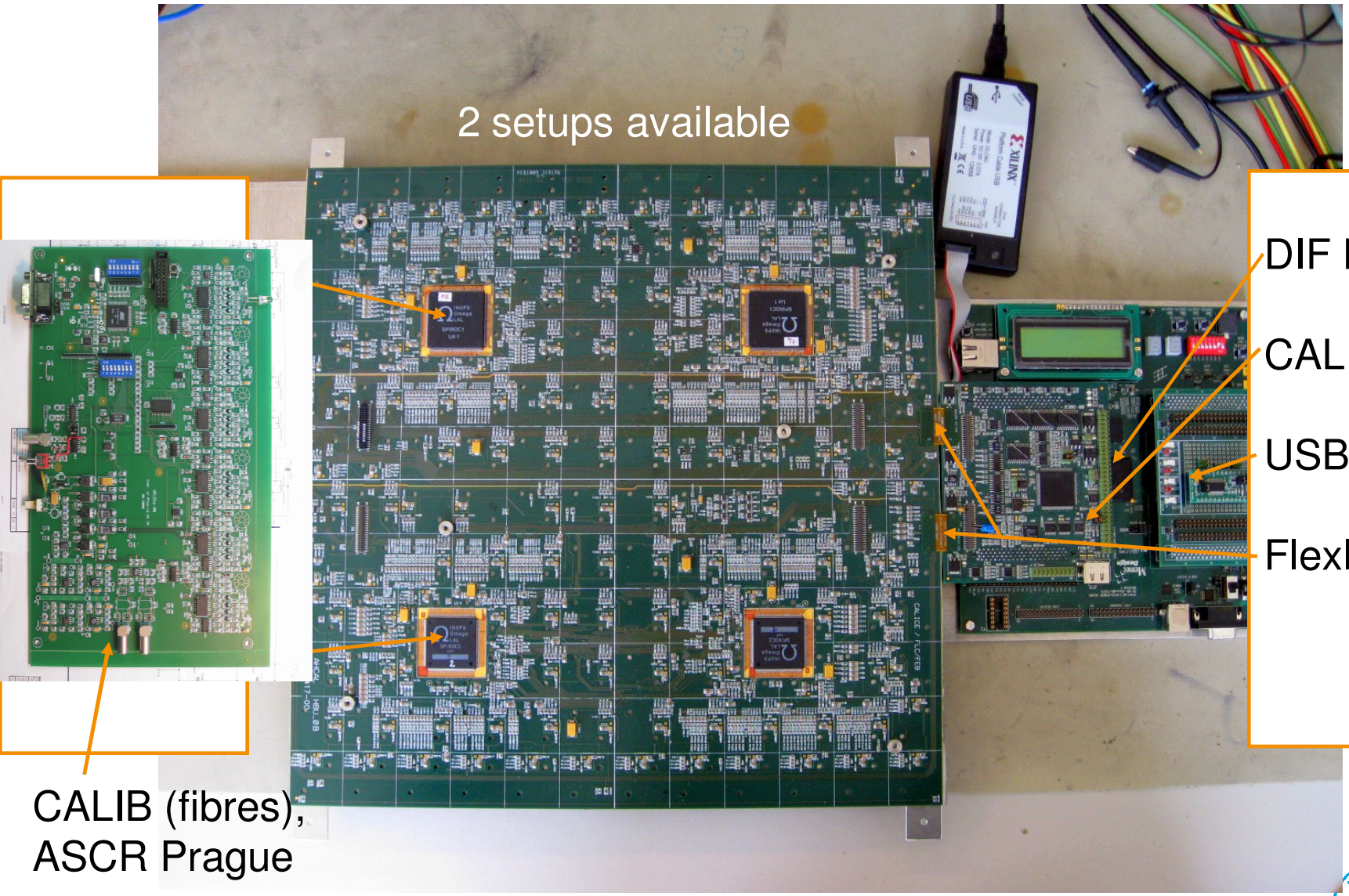


- 4 Modules finished, in operation.
- First tests successful.

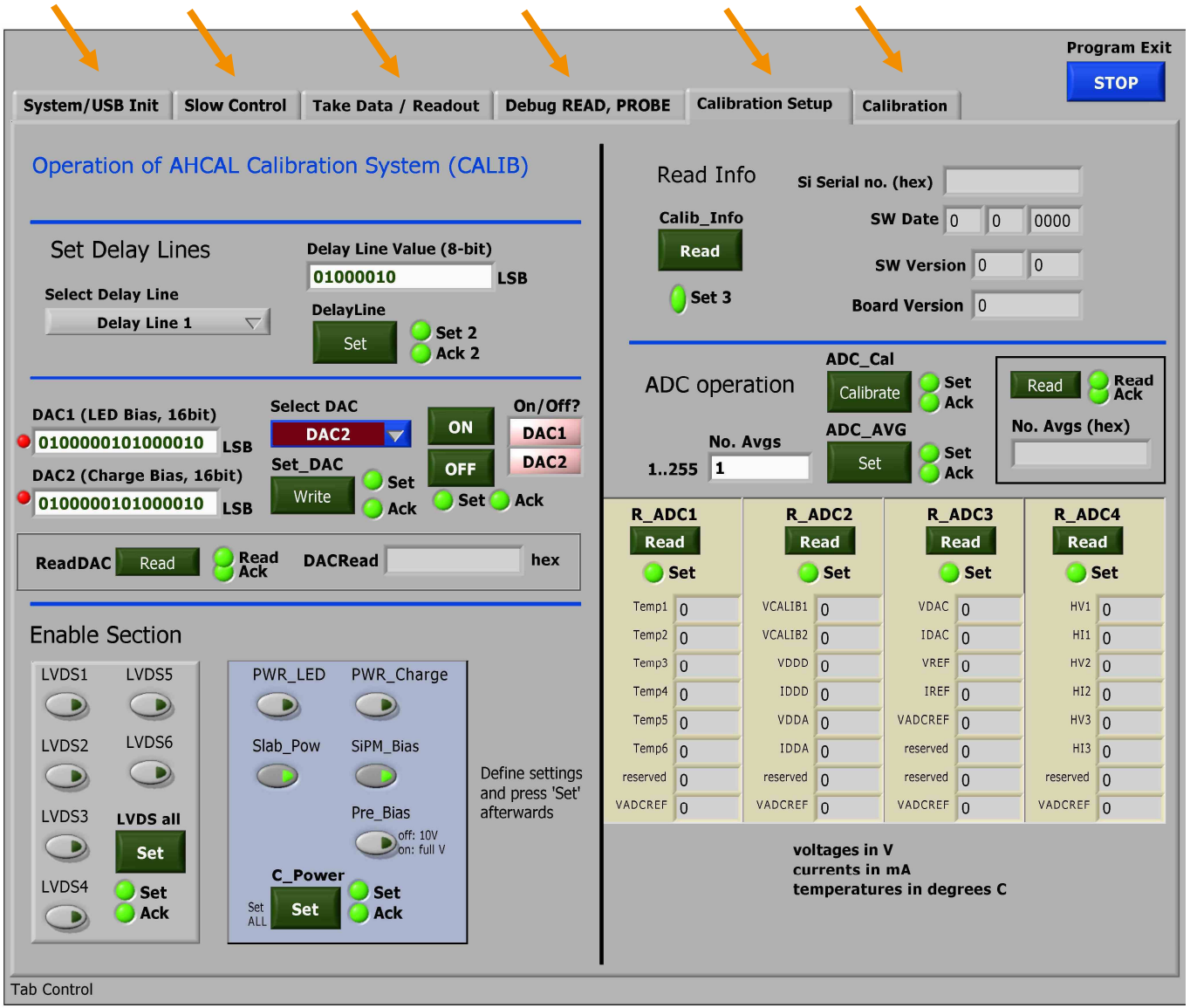
- 4 Modules arrived at DESY.
- Tests will start now.

Sizes and heights: To be adapted to ILC mechanics later.

HBU0 status


2 setups available
DIF FPGA
CALIB
USB / DAQ
Flexleads
CALIB (fibres),
ASCR Prague

Labview Control of the Prototype System

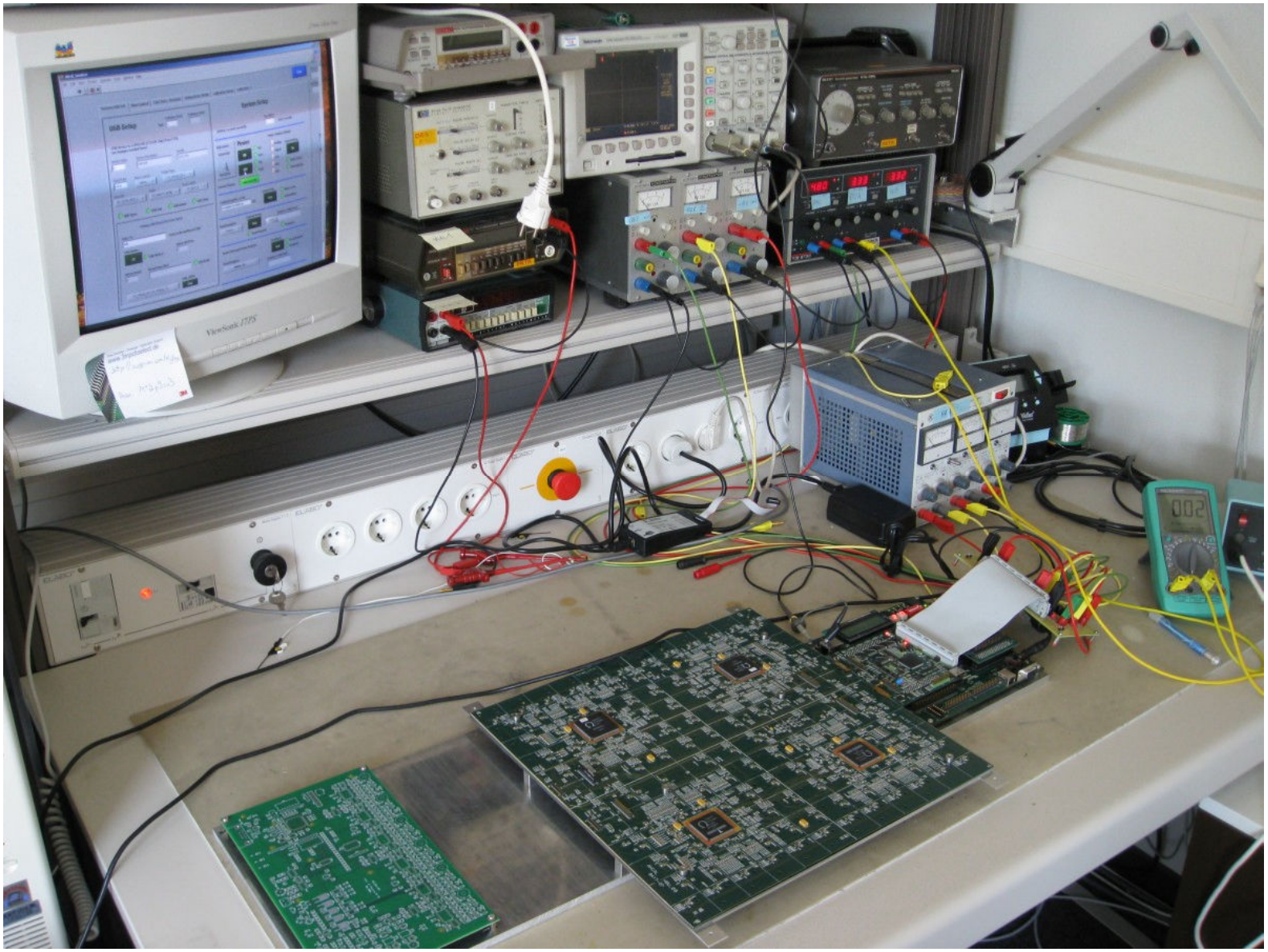


AHCAL: Focus on:

- > USB Interface
- > Slow-Control
- > Take Data
- > Readout

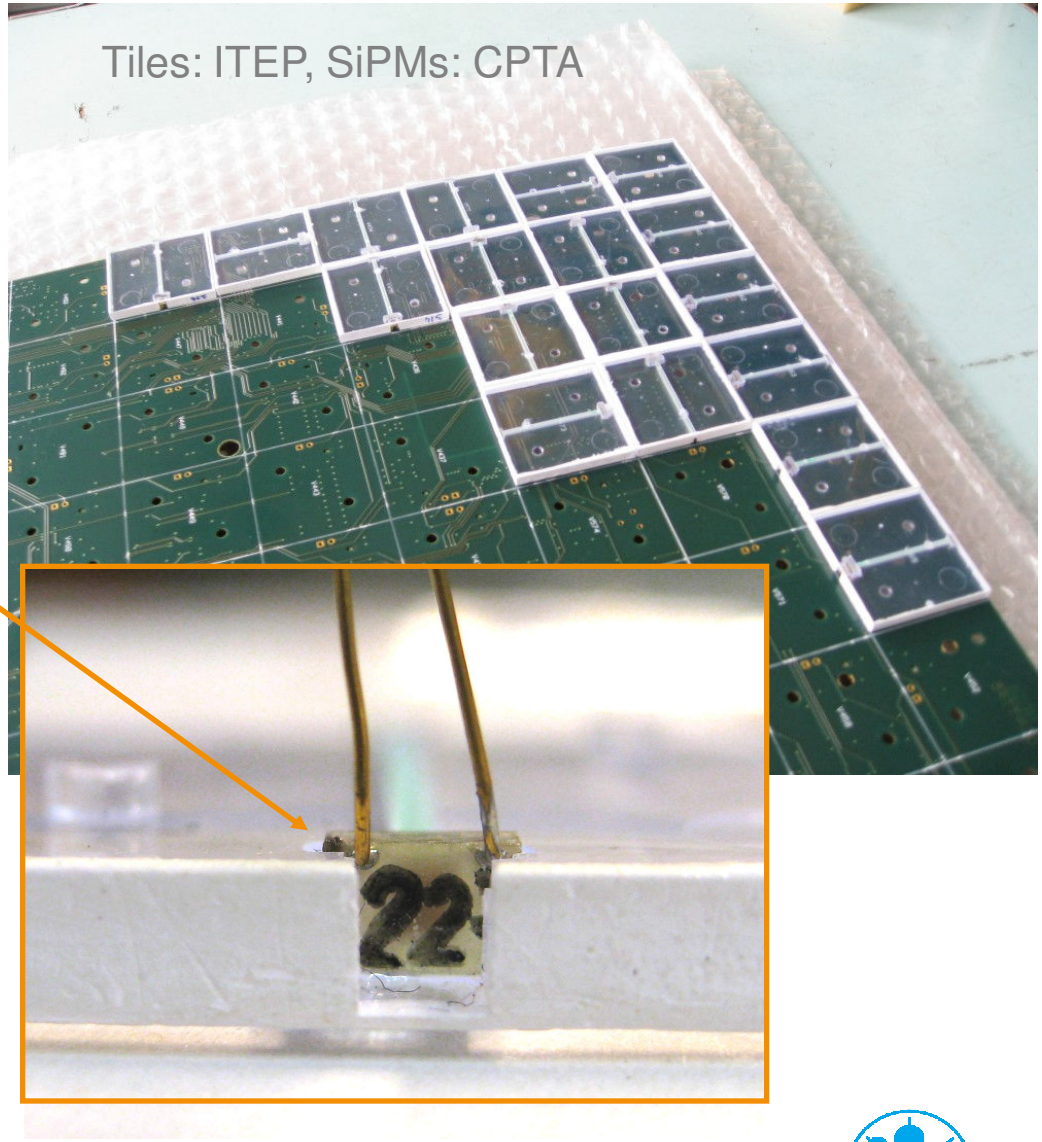
>Current Version: 20

Prototype System Commissioning



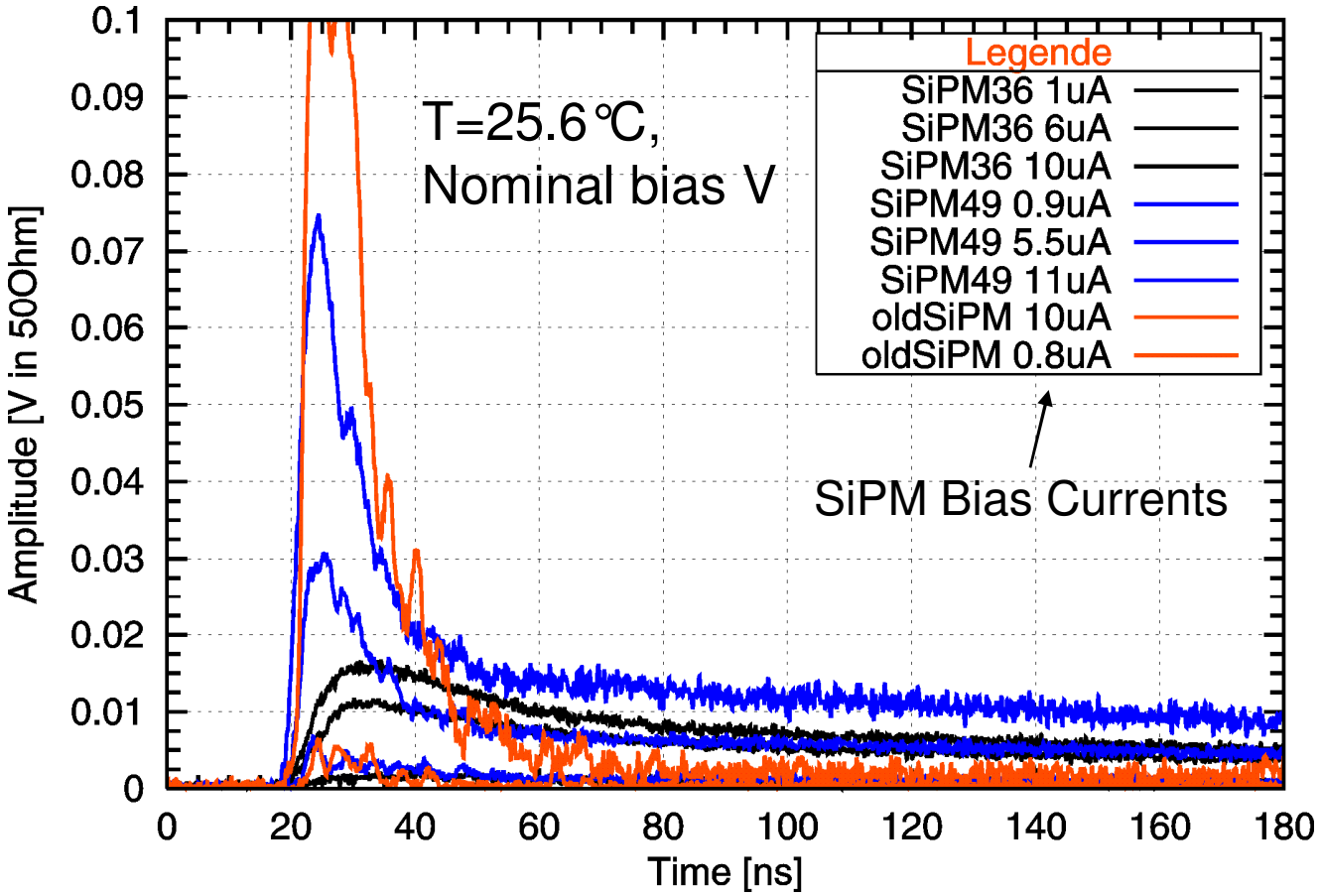
Tiles Interconnection Test

- Tiles not connected yet (HBU electrical test first).
- Test assembly shows:
  - Strong force to SiPM pins during assembly.
  - A few SiPMs cases are too large (only a few!).
  - Mirrors are too large, but can be cut.
  - Alignment concept (-pins) works!!



SiPM long tails - LED Test (3 light intensities)

19% of SiPMs show pulse responses wider than 50ns.

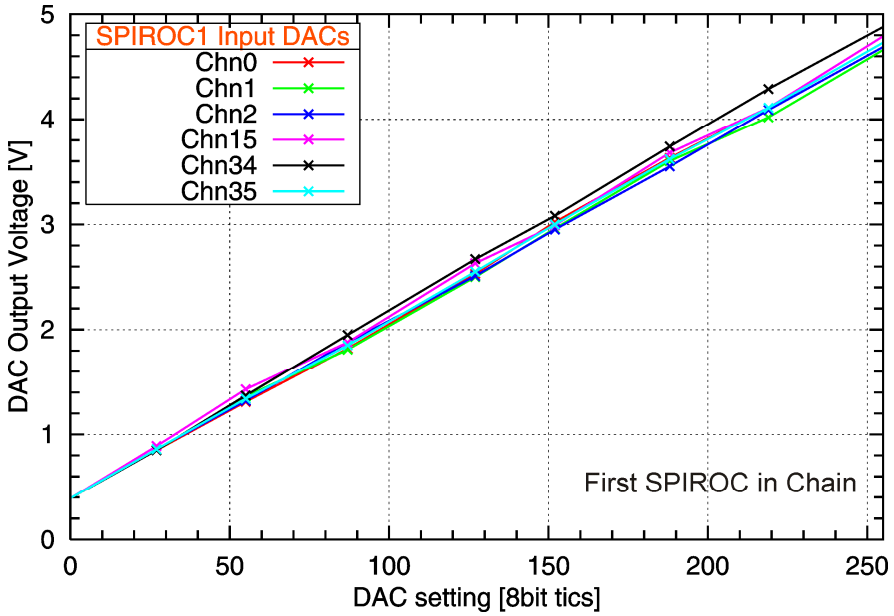


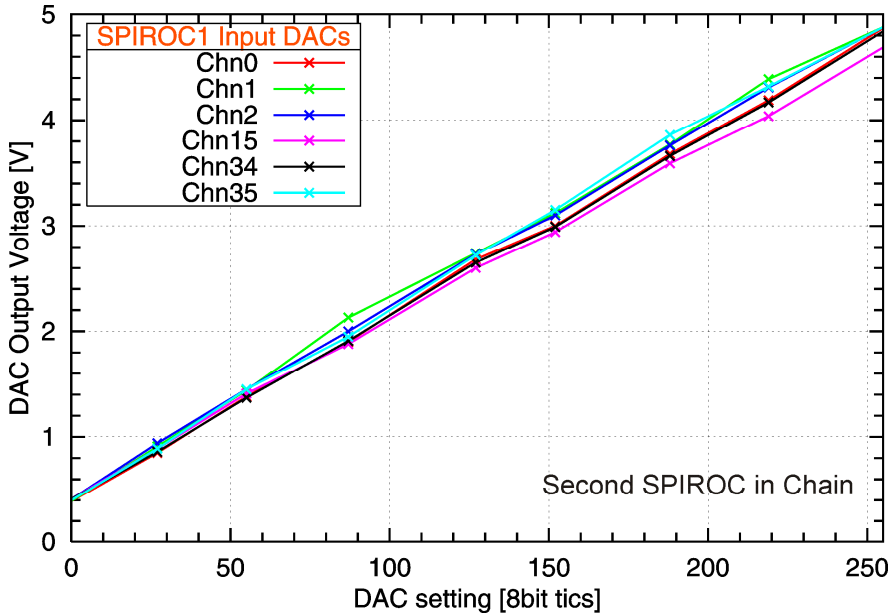
SiPM36: long tail
SiPM49: good

oldSiPM: 6x6 tile with SiPM 538

System Commissioning – Slow Control (SC)

Input DAC Outputs (8-bit, 5 of 36 channels):





Both SPIROC1s show the same results.
Output voltage **measured against +5V.**

System Commissioning – Slow Control (SC)

SC programming conclusions

- SC works stable for both SPIROC1s.
- SC Register Length is 701 bits in our case (not 703).
- Rise Time of SC Clock (clk_sc) has to be <12ns.
  How to realize for 2.20m long slabs?? Should be addressed in next ROC generation.
- Power Supply voltages : adjustable <3.25V (except for one pin).
- **Still under test for SPIROC2** (@VDD around 1.5V):
  - Operation is not stable.
  - First SPIROC2 does not deliver correct SC data at output. Replace chip?

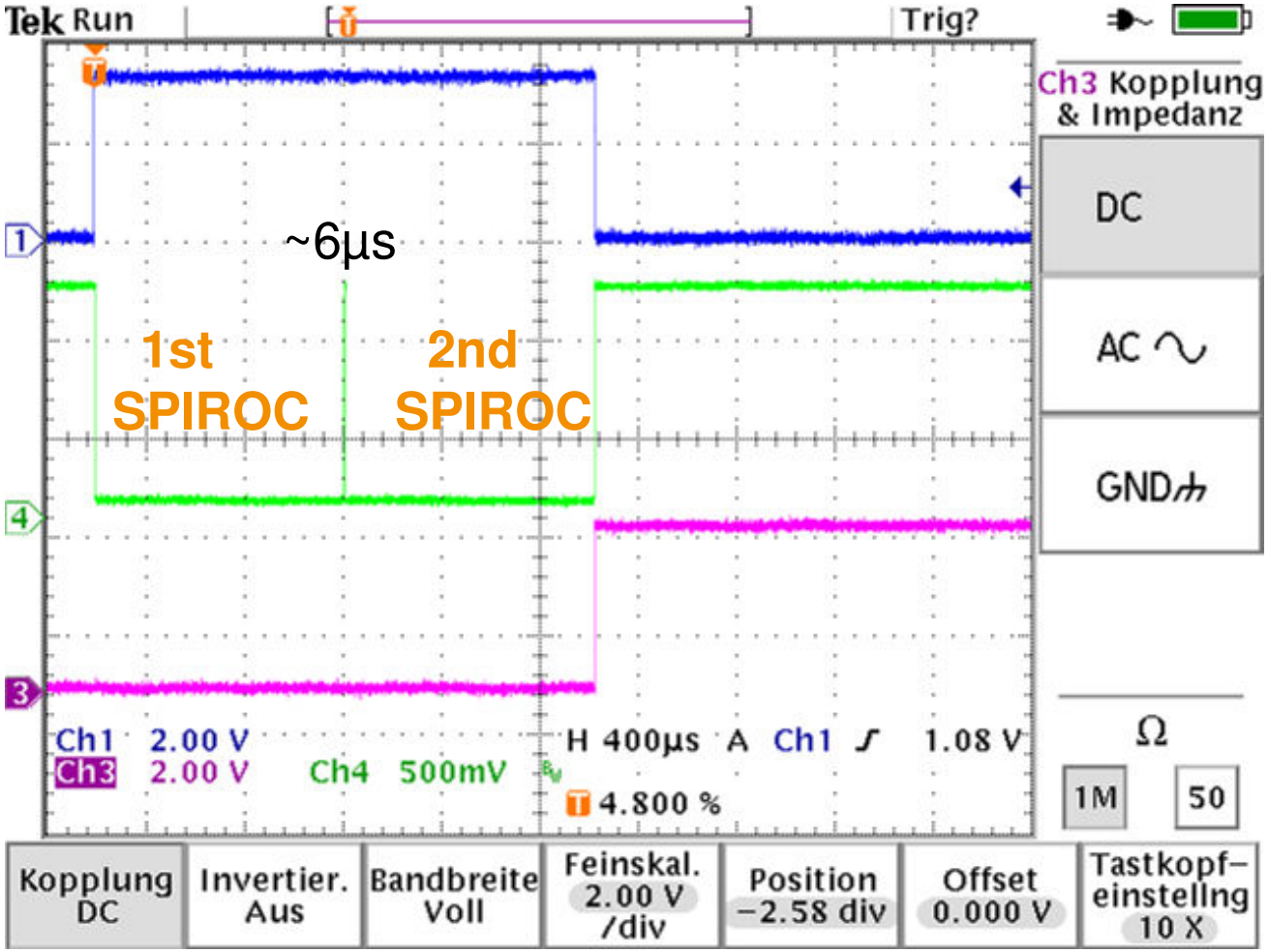
System Commissioning – Readout

First time READOUT of two SPIROC1s in a chain!!

start_readout

TransmitOn
(open collector)

end_readout
(2nd SPIROC outp.)



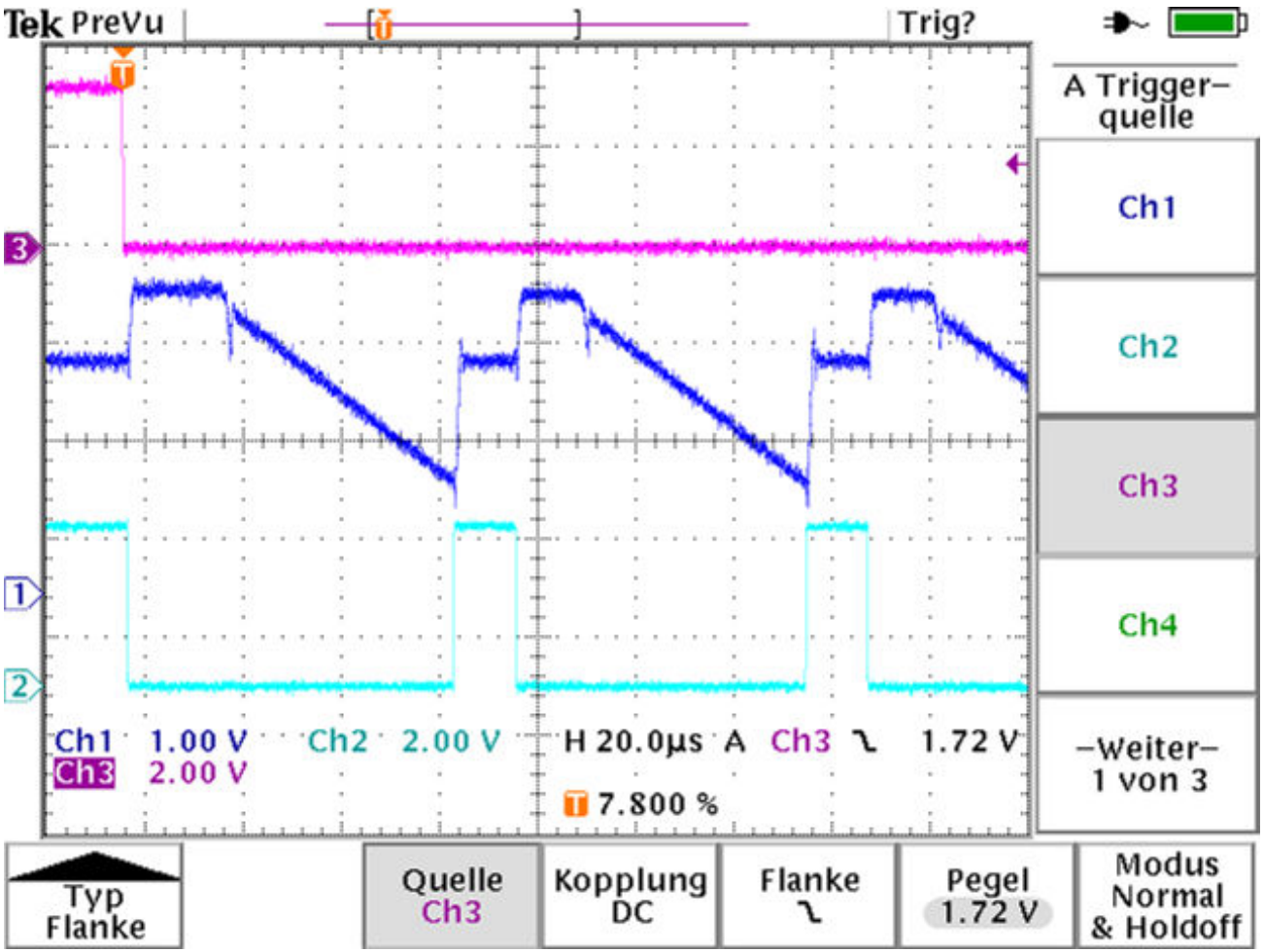
System Commissioning – Probe Register

Probe Register controls external ADC ramp (now working):

start_convDAQb

Ext. ADC ramp on HBU

Digital_probe2: Start_ramp_ADC



Many thanks to Christophe and Stephane !!

DIF Status

Reference Documents (the DIF Task Force):

'Format of the Readout Data of the DIF'
Version 1.1.0

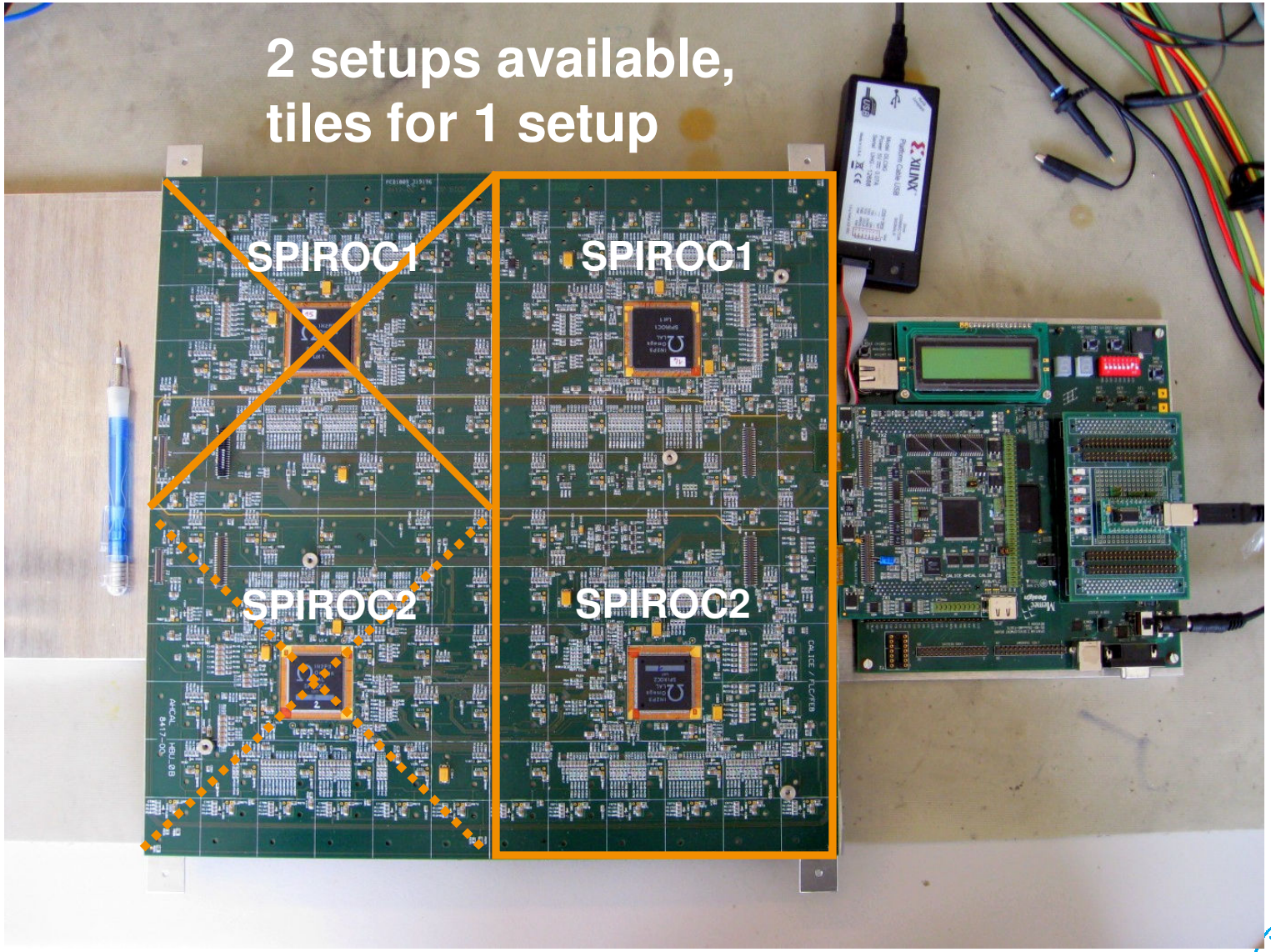
DIF – Operating Manual (May 18th, 2009):
http://adweb.desy.de/~reinecke/DIF_Firmware_vers1_13.pdf

'All' necessary command- and address-definitions for DOOCS development.

DIF USB interface

- Purposes of the USB-to-DIF interface
  - Debugging interface in ‘final environment’: error in CALICE DAQ communication
  - Commissioning of the Prototype Detectors.
  - New: Spy interface (in parallel to CALICE DAQ).
  - Not: Synchronous operation of full detector.
- USB interface emulates CALICE DAQ interface as much as possible.
- AHCAL: Started with USB (not CALICE DAQ), but switch to CALICE DAQ is straightforward.
- DIF Task Force work enables efficient DOOCS development (Consistent DIF firmwares for ECAL, DHCAL and AHCAL).

HBU0 : Discussion about tile assembly of 1st HBU0



Conclusions and Outlook

- None of the modules shows severe errors up to now.
- Minor errors in operating software (DIF-USB-Labview chain), to be solved now (SPIROC1 first data (pedestals): expected within two weeks).
- Probe register only works for first SPIROC1 in chain. => Only first SPIROC1 on HBU0 can be used.
- Next steps:
  - Commissioning of Calibration Systems as last basic HBU test (already started with integrated LEDs, TCALIB distribution promising)
  - **Set SPIROC2 to life (!!!) – foreseen for EUDET module!!**
  - DESY testbeam
  - Switch to CALICE DAQ (early autumn) and use POWER module
  - Redesign HBU (one type of SPIROCs) and DIF (replacement of commercial module)