



In2p3

LLR

FEV7/DIF testbench at LLR

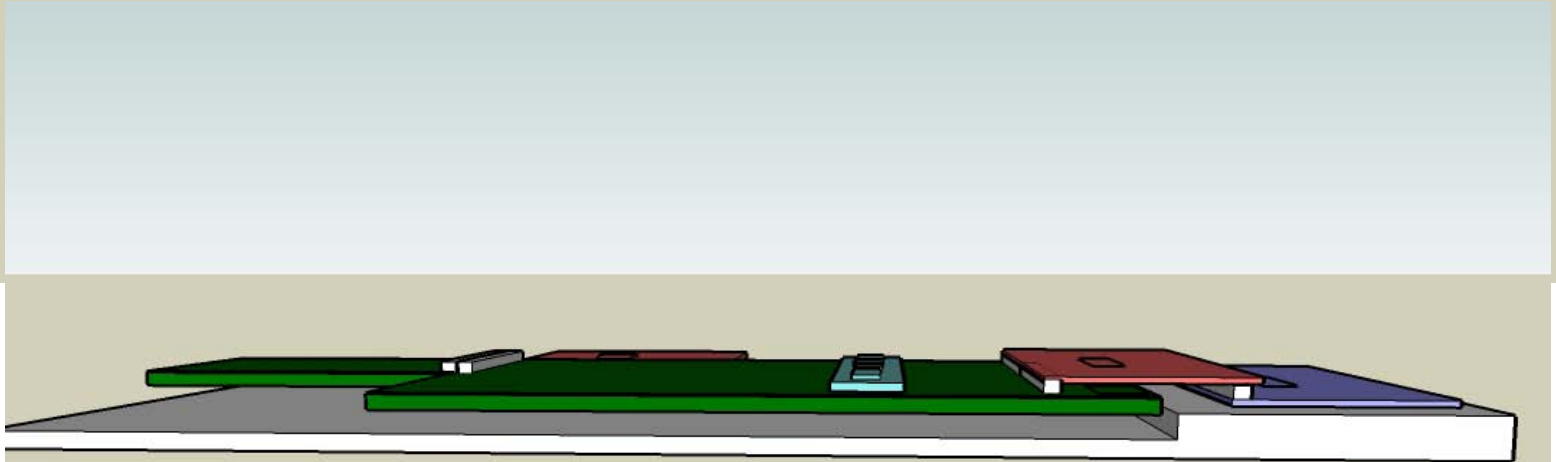
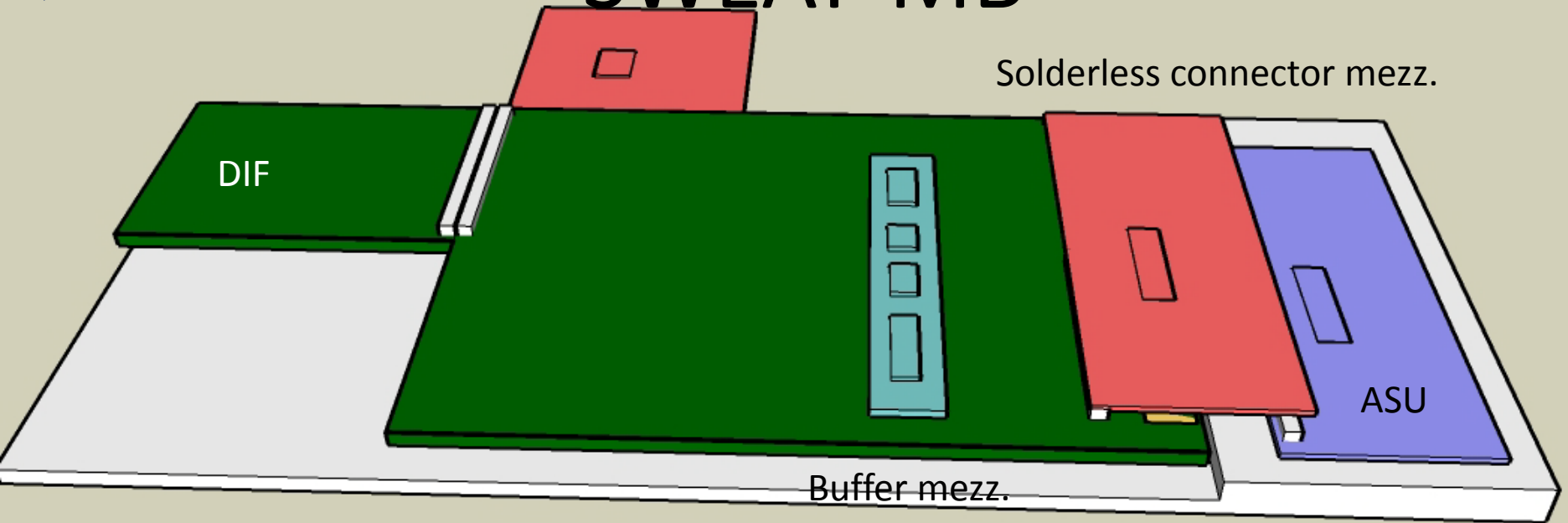
adapter

- SWEAT-MB (Si-W Ecal AdapTer-MainBoard)
 - Main board To be received tomorrow
 - Mezzanine for Power, tx/rx buffers, connector development Cabled at LAL (thanks for supporting)
 - Expected end of June (no mezzanines)
 - Also for Cosmic test bench
- SWEAT-BUFFER (TX/RX mezzanine)
 - Ordered last week together with SWEAT-MB

Not to scale

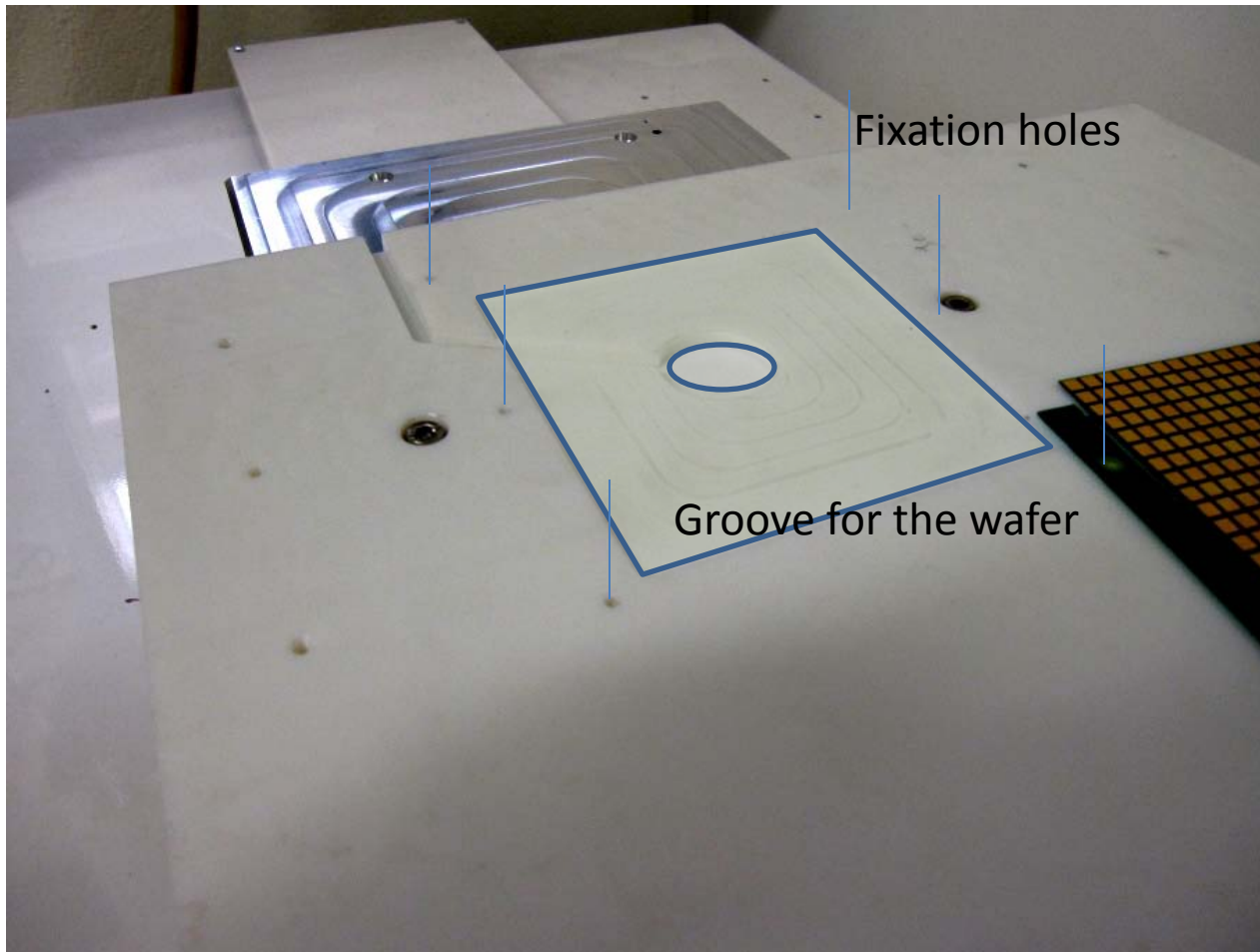
SWEAT-MB

Solderless connector mezz.



Can be used as a support
to glue the wafer
Scalable in order to build a
slab (same edge as FEV7)

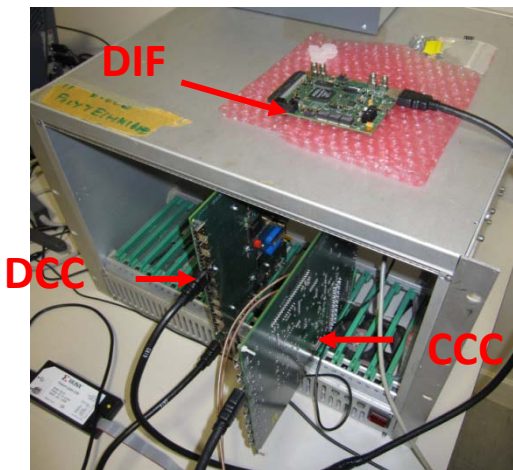
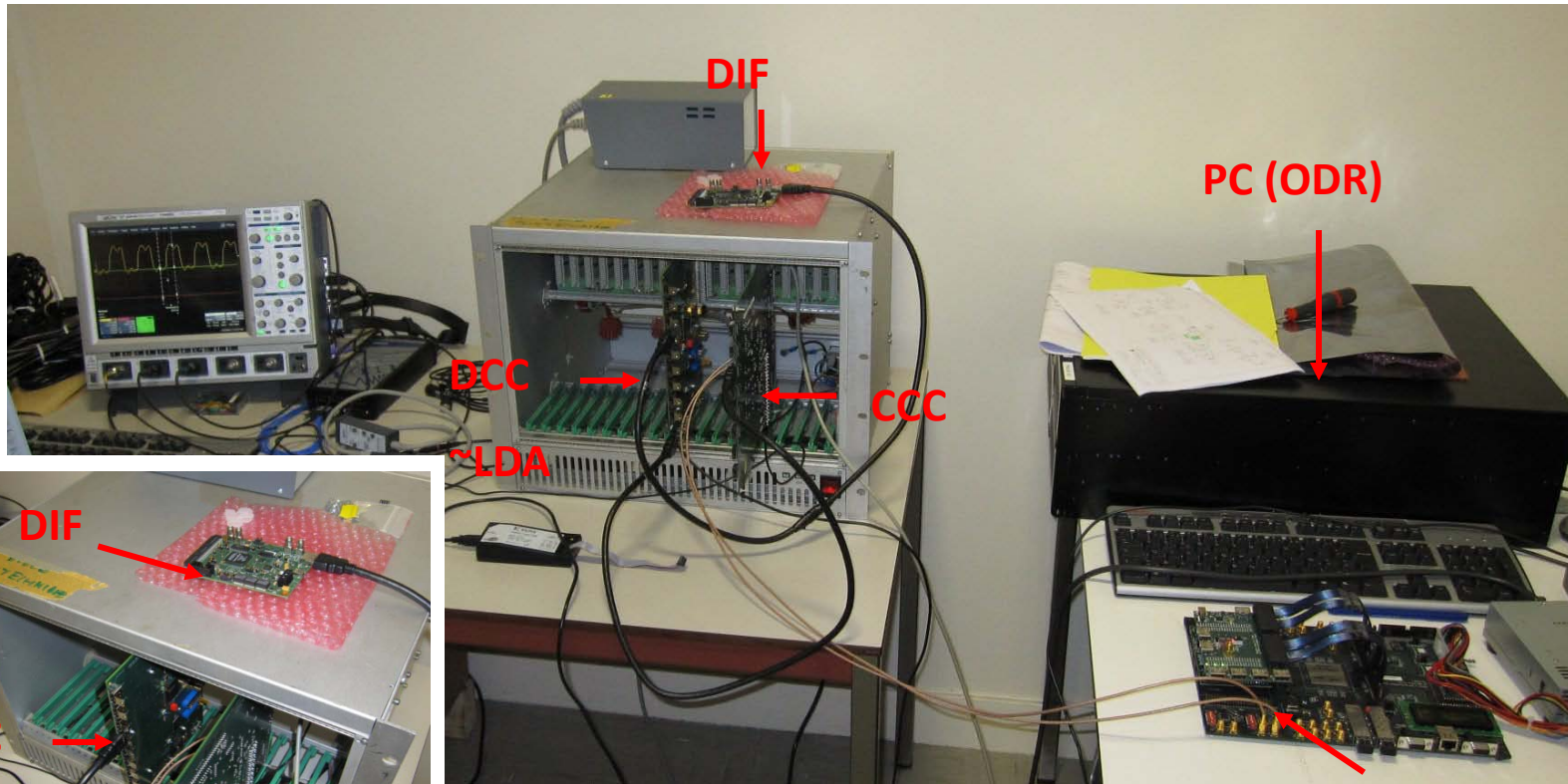
Support



DIF & FEV

- We have now 2 ECAL DIFs (old prototype)
- Loaded with a test firmware for USB
- Firmware in good progress
 - Slow control
 - Read-out
 - No other functions for the 1st version
- We have 1 FEV7_CIP (1 chip)
- Solder-less connector under investigation
 - Nothing available yet

Test Bench



PC (ODR)

DIF

DCC

CCC

~LDA

CLK_Gen

(50-150 MHz)

DAQ & DCC

- Developments for DCC lead us to understand well the serial link
- Data transfer between a virtual LDA and a virtual DIF is enabled
 - Firmware into the DCC fpga Leimeng
 - Pattern generation from USB
 - Upscale to 9 link in simulation (DCC) Franck

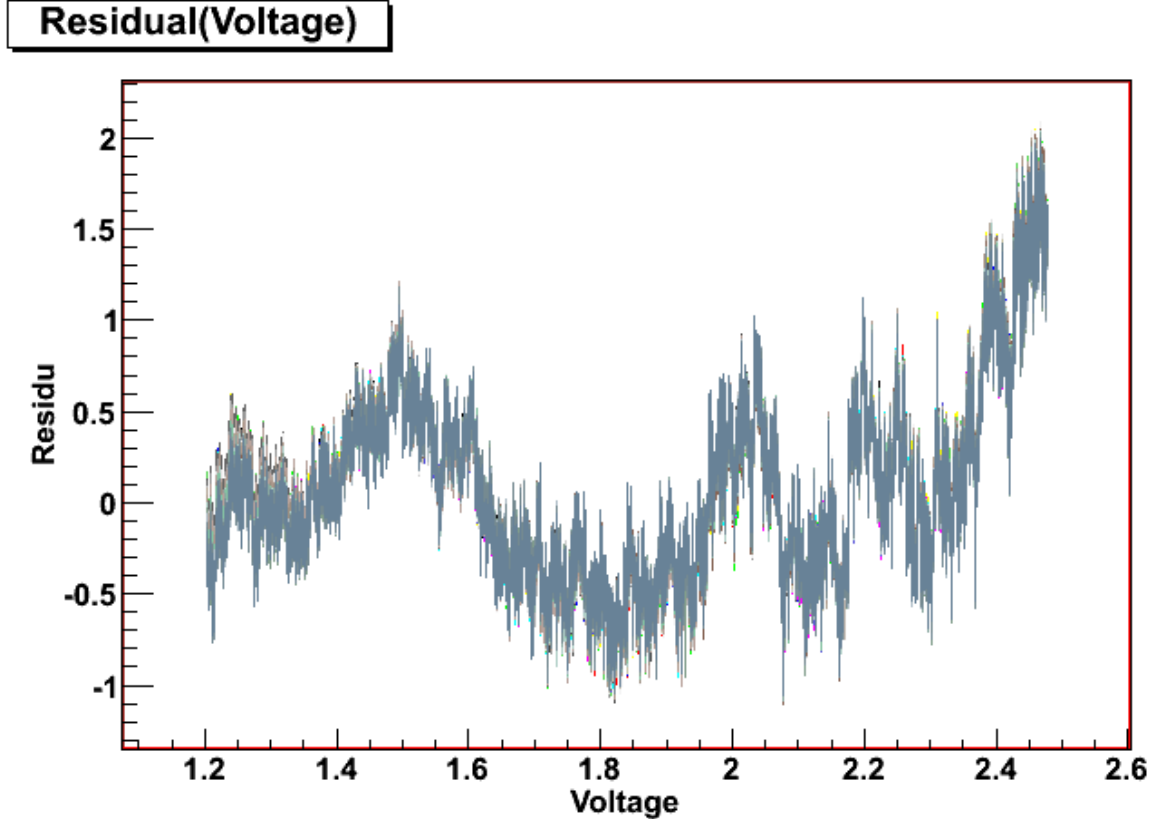
Plans

- Glue a wafer on FEV7_CIP This week
- Connect to the adapter board once available Uncertainty!
This week or in
one month...
- Plug the DIF
- Start playing...
 - Fast/BT commands from USB or LDA
 - Clock from CCC
 - Generate few signals... Prior the CALICE week at LYON
- Takes time as we will try to enable the whole DAQ chain
 - Functionalities added “on the go”

SPIROC2: ADC

- On a caractérisé l'ADC
- Comportement gaussien pour les deux chips
 - Tous les channels et tous les voltages.
 - Pas de “tails”.
- Les deux chips sont bien linéaires entre 1.2V et 2.4V.
 - Résidus compris entre -1 et 2.
- Pour les channels la réponse relative est constante avec le voltage, mais différentes pour les deux chips.
- Certains channels ont des problèmes dans l'acquisition des données.

Linéarité - Chip n°2



- Résidu compris entre -1 et 2 ADC
- Augmentation du résidu à haut voltage