Linear Collider Beam Test Workshop 2009

SiLC test beam activities

Alexandre Charpy – LPNHE/UPMC/CNRS/IN2P3

On behalf of the SiLC R&D collaboration

LPNHE
Laboratoire de physique nucléaire et des hautes énergies

Overview of SiLC test beams

I. Standalone multi-purpose tests system

II. Combined test beams

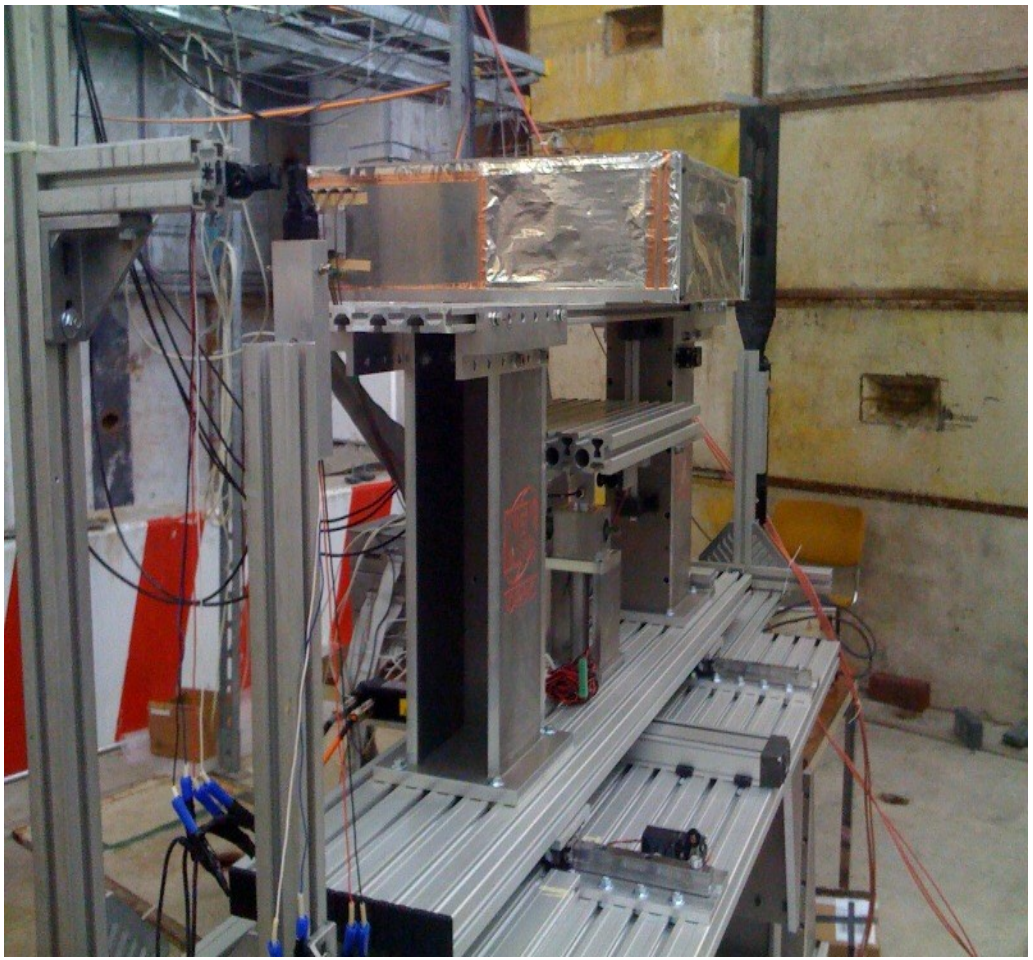
III. Preparation of the combined test beam with calorimetry

IV. Next years prospects

Standalone multipurpose test beams system
LPNHE

Goals:

- Tests of new sensors technology
- Tests of new Front-End Electronics (FEE)
- Include a reference FEE system (VA1 based)
- Adaptable to various combined tests
- DAQ – read both FEE systems (new SiTr130-128 chips & VA1)
- Locate up to five silicon modules



New sensor developments under studies

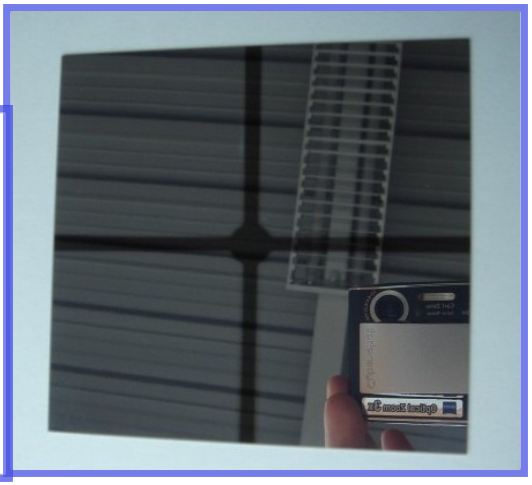
Conducted by LPNHE:

- Research baseline: wafer 6”-8”, 200µm of thickness, pitch of 50 µm, transparency ~70%, active edge

•Classical design named HPK:

- 50µm pitch, 320µm of thickness
- Hammamatsu manufacturing

Surface treatment of silicon wafers:
→ ~ 20% transmittance
→ Alignment System (IFCA) using an infra-red laser in labs & tests beam
→ Santander – I.Villa, M.Fernandez



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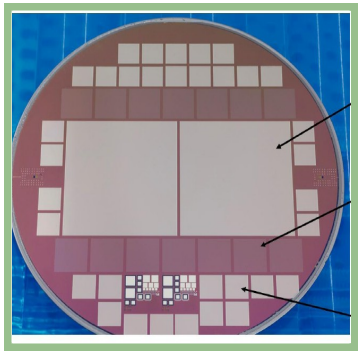
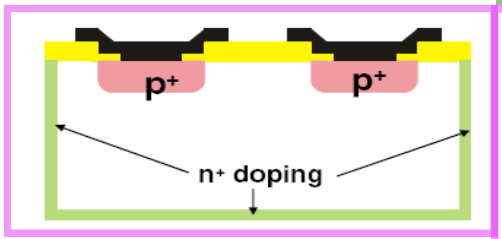


Edgless with Silicon On Insulator (SOI) technology

VTT- Juha Kalliopuska

Manufacturing achievement:

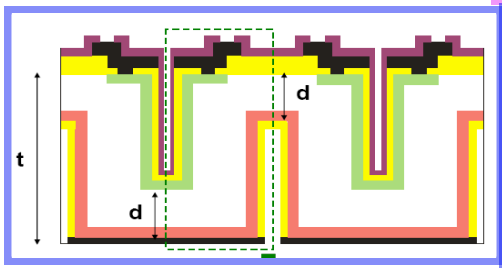
- edgeless strips & pixels sensors
- 6” SOI wafer, 50 µm pitch



Edgeless planar strips

FBK-irst-U. Trento/INFN - Gian Franco Dalla Betta

- Prototyped sensors 2.5x5cm^2 (Trento & LPNHE)
- full characterization at Lab followed by beam test & HPK comparison



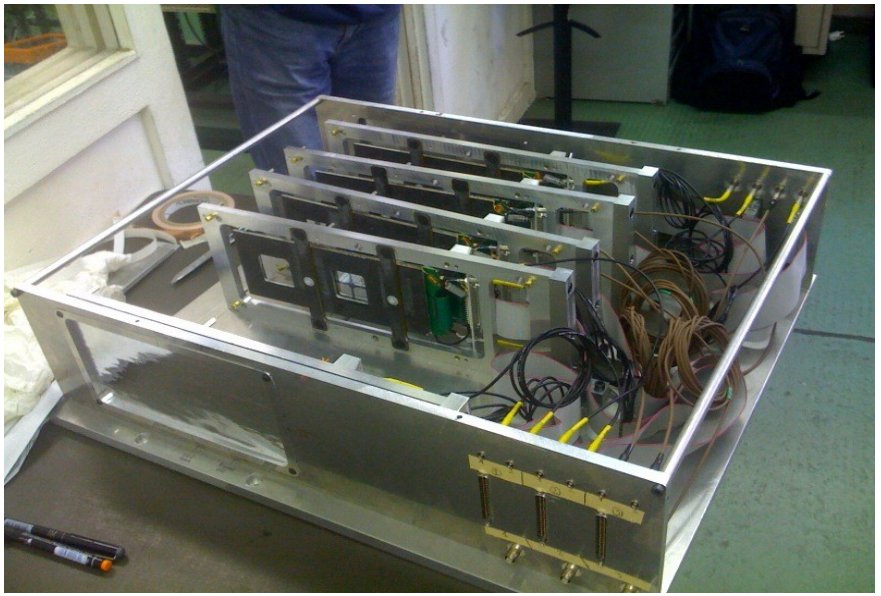
3D technology (short strips)

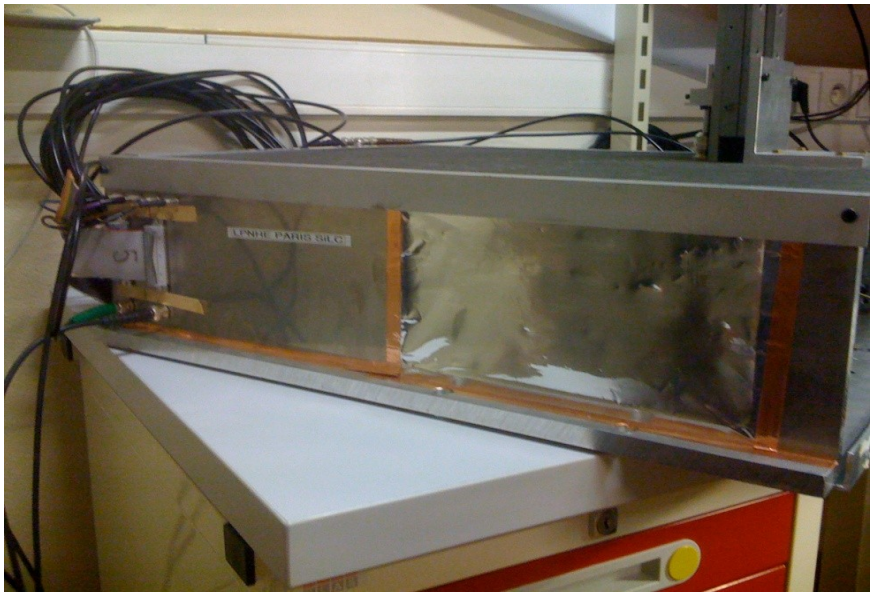
FBK-irst-U. Trento/INFN - Gian Franco Dalla Betta

•250 µm thick substrate, full 3D detectors and passing-through columns

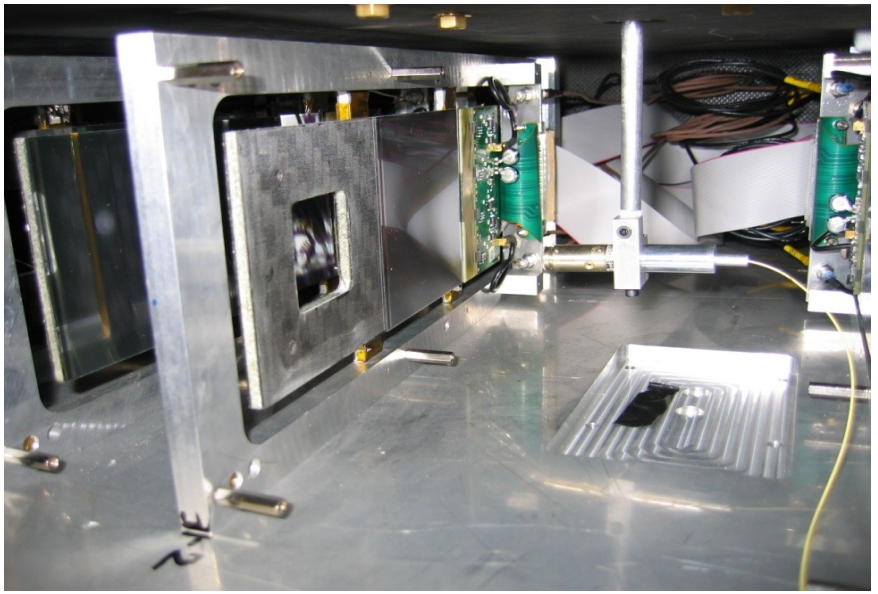
•New double-sided process defined, no need for support structure, allow dual read-out

Standalone Test Beam System
LPNHE





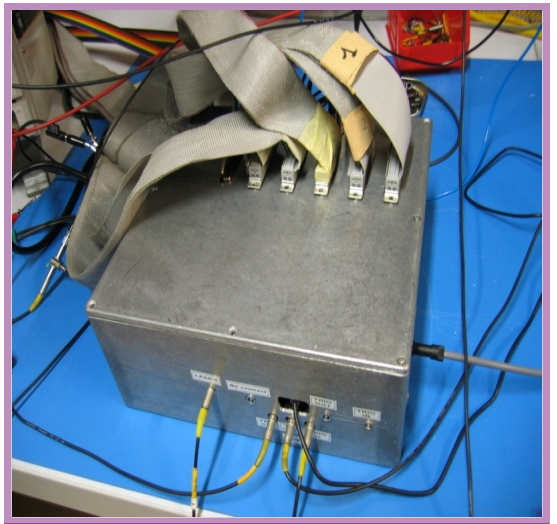
- Tests of the friendly aligned HPK sensors with a laser beam embedded
- Tests of other sensors types (new strip technology, new pixel devices)
- Tests of new Front-End Electronics (FEE) → SiTr130-128
- Combined tests with other sub-detector prototypes => new such infrastructure are developed and adapted to those tests

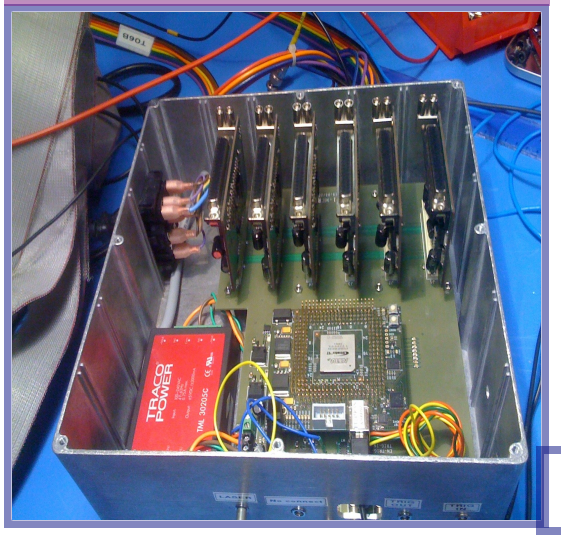


Standalone Test Beam System

LPNHE - DAQ - Hardware

- Increase of the number of channel to read:
  - Alignment tests=> 2560 voies
  - EUDET and transnational tests (mi-2010) => 15000 à 20000 voies
  - 2011-2012 -> much more !!!
- Evolutive DAQ Hardware ToolKit (EUDET deliverable)
  - Adapted to both: VA1 (référence) prototypes SiTr-130 and next, mix mode (VA1+SiTr chips)
  - Altera/Usb → Altera/Ethernet under way
  - FPGA/(USBx, Light Peak)? for the future





VA1

Standalone Test Beam System

LPNHE - DAQ - Software

Acquisition needs:

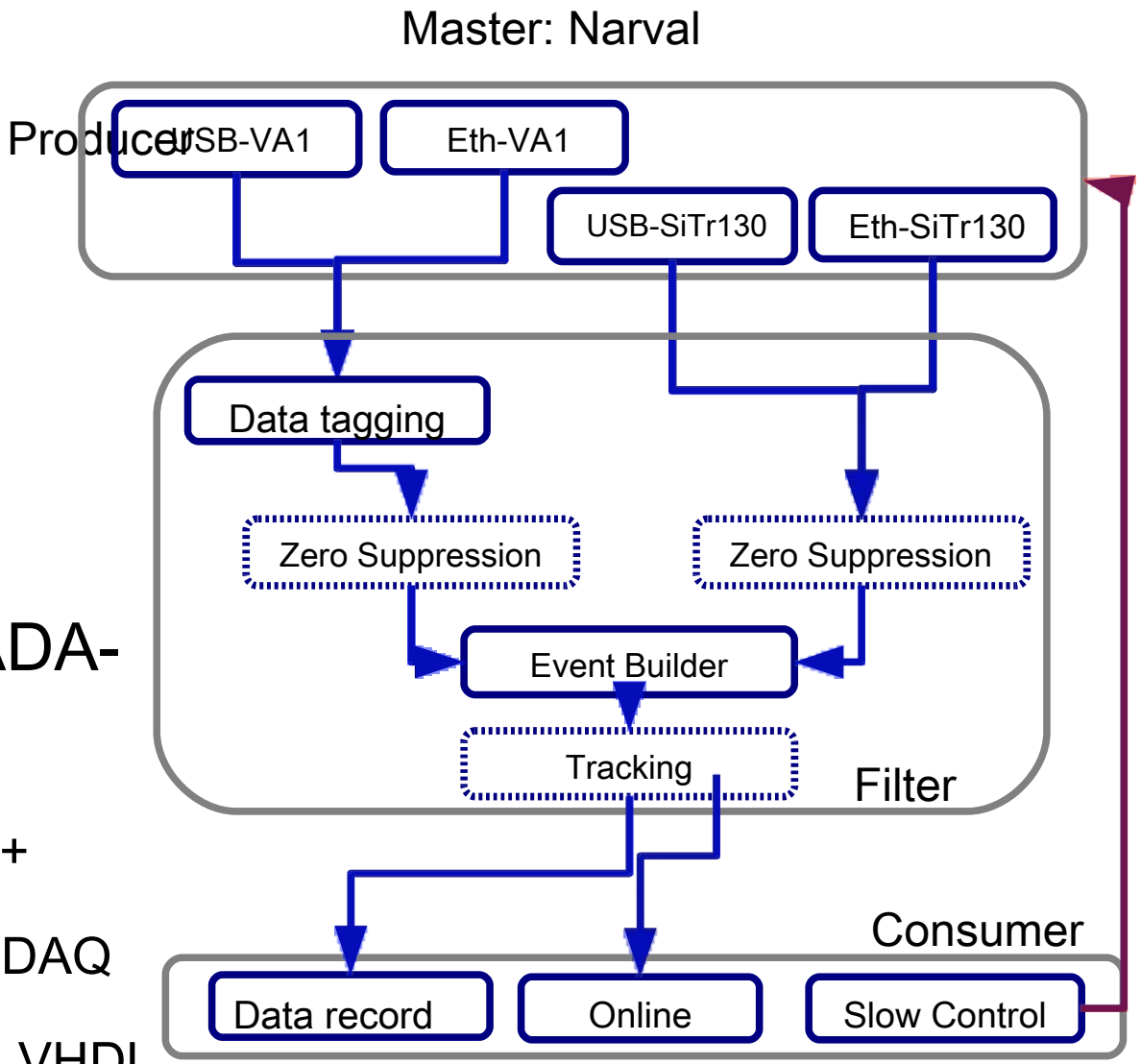
- Increasing of the Data size management
- Addressing of the data
- On-line control
- Flexibility

Narval is the main frame (ADA-oriented)

→ module programming: ADA/C/C++

→ Can be interfaced with any other DAQ

→ FPGA system is handled by a full VHDL software package.



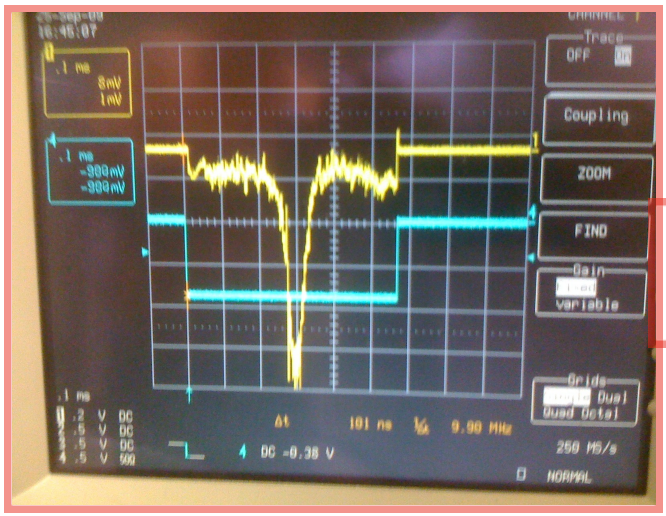
Standalone Test Beam System

LPNHE - test beam & alignment

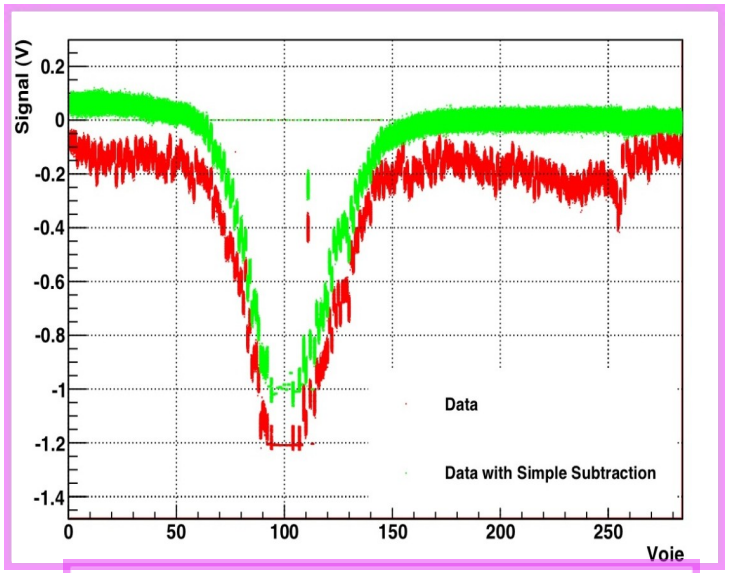
Next Tests Beam preparation

- VA1'® chip
512 channels per module, => total of 230 cm² active area

- 3 transparency sensors surrounded with two HPK sensors



- Analogic response of VA1 chip with a laser pulse

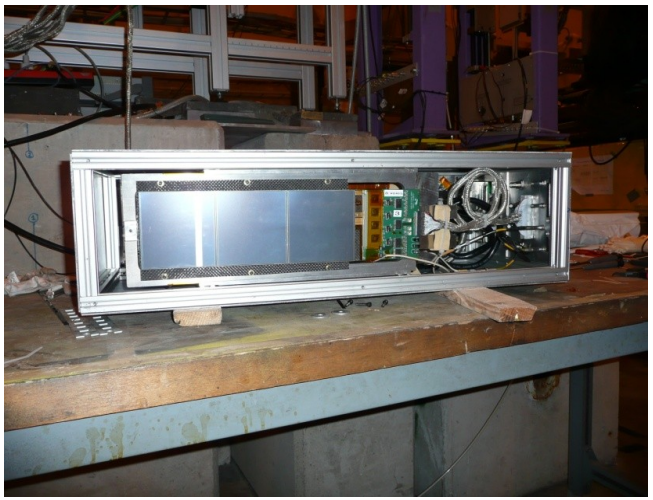


Offline reconstruction of the laser pulse w/wo simple pedestal subtraction

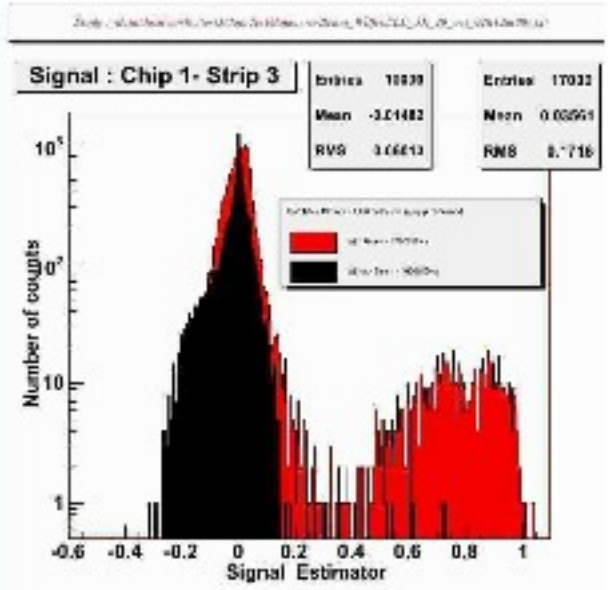
November and december 2009:
tests beam @ CERN & laser tests @ Santander

Combined test beams with EUDET telescope since 2007

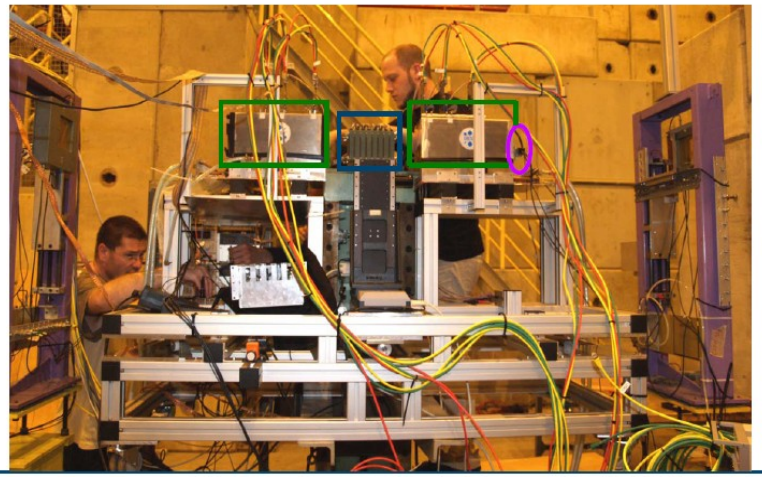
Tests of SiTr130-4 chip with HPK sensors



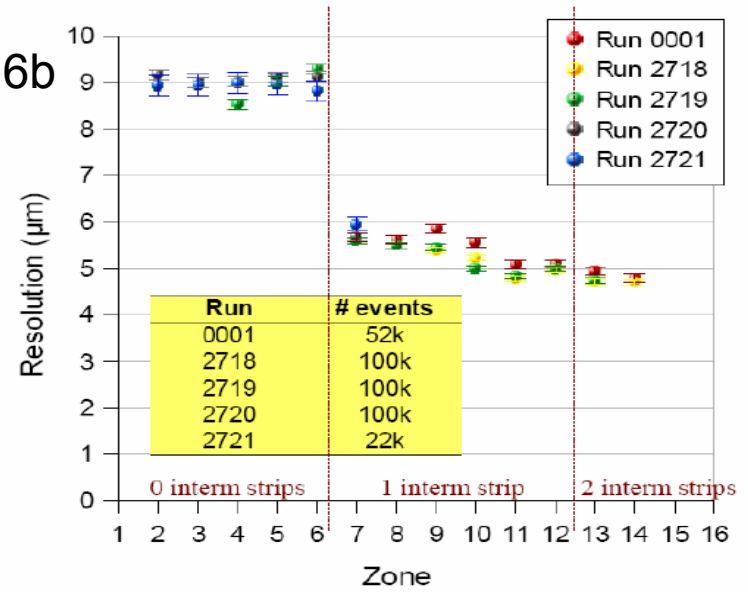
SPS West area
10-22 Octobre 2007



Setup:



SPS CERN–H6b
June 2008



SiLC combined test beam in 2009

Testbeam at CERNs SPS (19. to 26. August 2009)

- CERN SPS North Area: H6B
- Low intensity 120 GeV with (Pi+:55.67%, p+:38.95%, K+:5.38%)

Configuration:

- EUDET Beam Telescope to get triggers & tracks
- Readout chain from HEPHY's Electronic 2 Group
- Slow control/monitoring: HV, T, RH, Cooling
- Full remote control

Results:

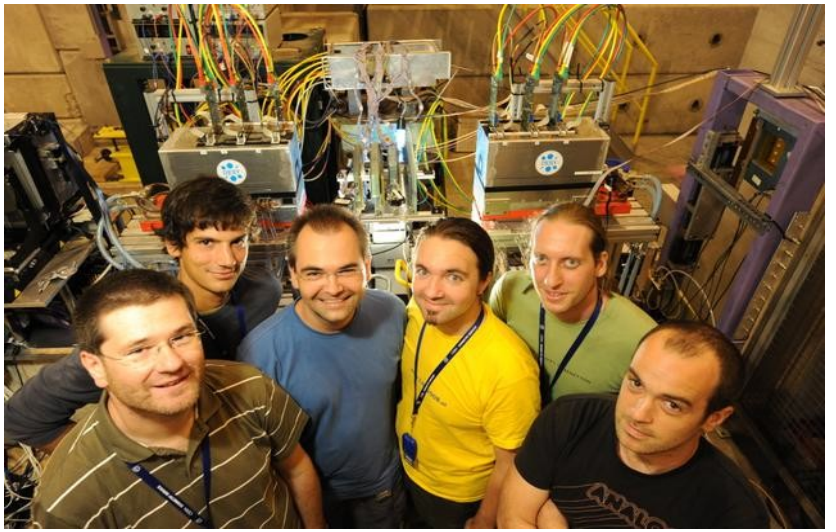
3.2 Million events

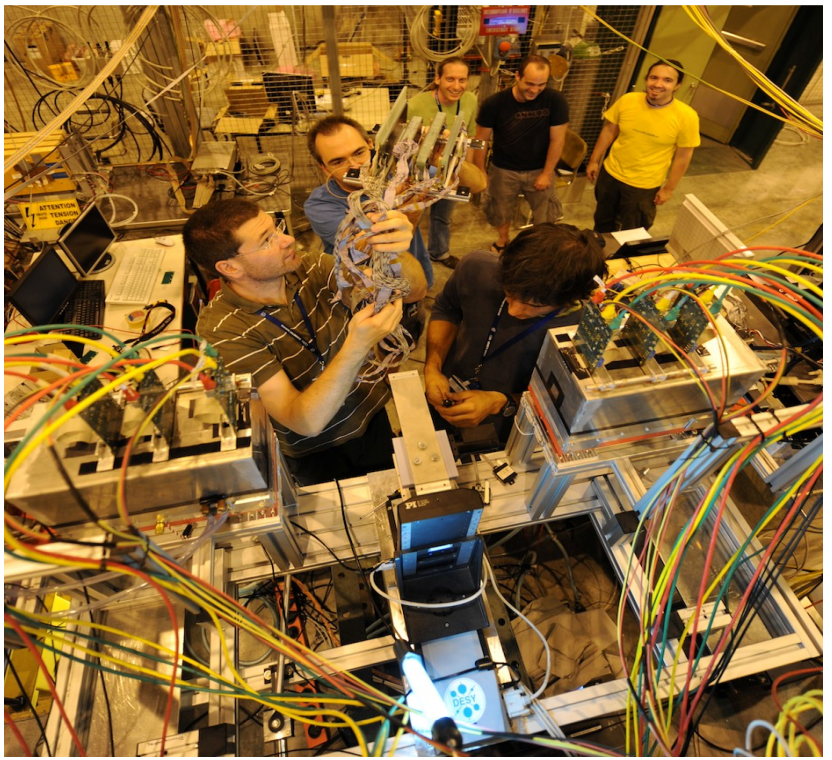
1 TB of data

Full Logbook at http://elog.hephy.at/testbeam-SPS09/

Source: Thomas Bergauer

HEPHY Institute of High Energy Physics — ÖAW Austrian Academy of Sciences

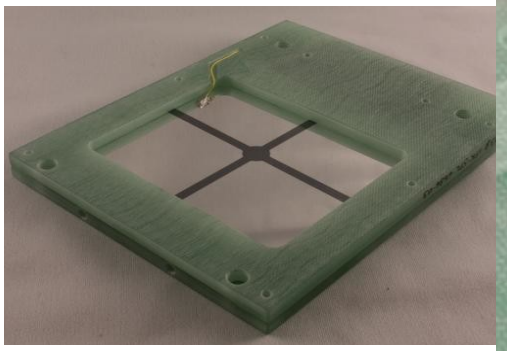


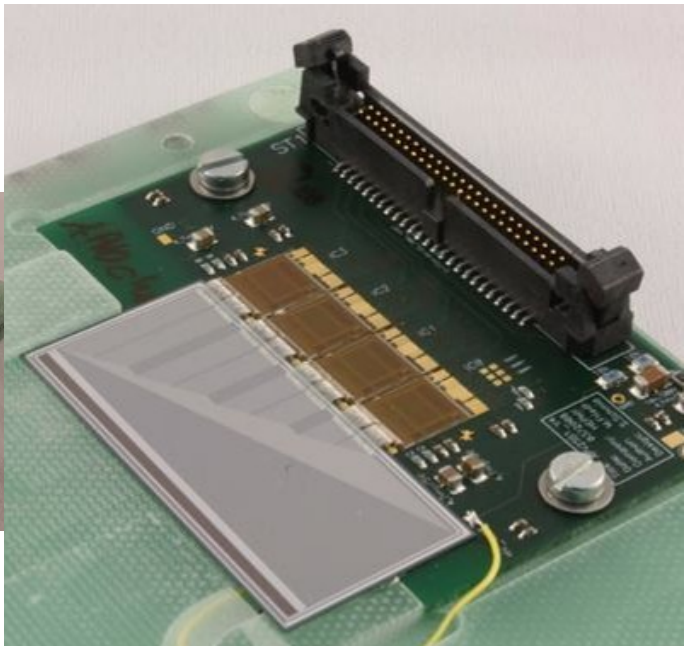


ITE Sensors & others

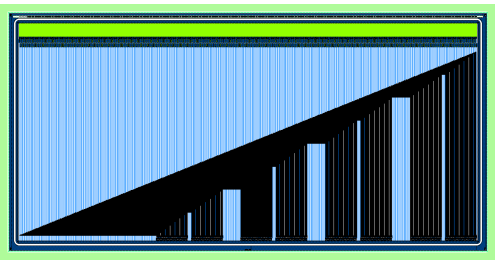
HEPHY Vienna and Institute of Electron Technology (ITE) Warsaw Sensor

- 2 x Sandard
- 2 x Pitch Adapter Single layer
- 2 x Pitch Adapter Double layer
- 3 x 512 channels

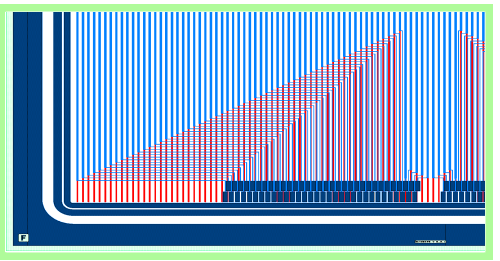




- 2 x Alignment Modules
- 2 x SiLC-HPK half-moons for test structure measurements
- Stack of last years multi-geometry sensors for calibration

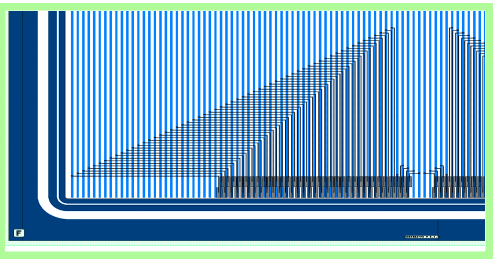


512 channels



PAS

PAD



Source: Thomas Bergauer

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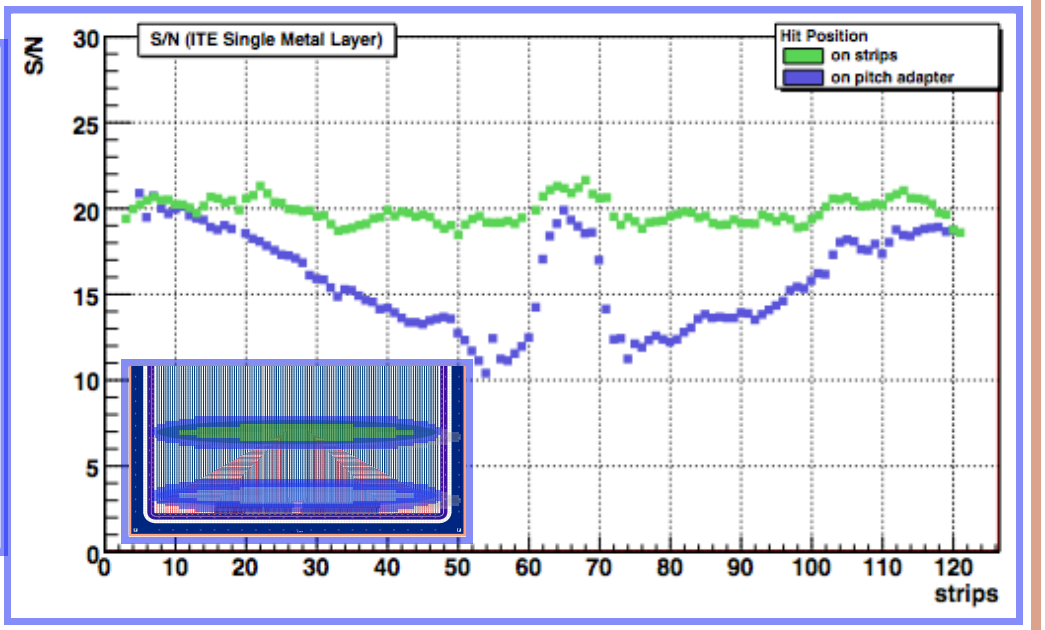
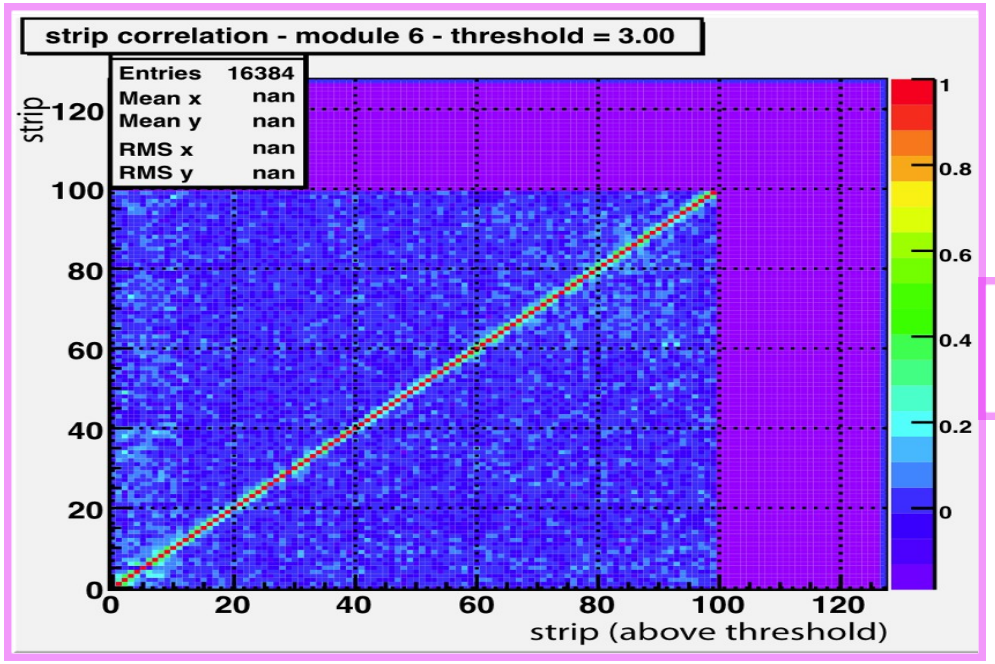
Results

signal loss and cross talk

- Each hit position represents SNR of a cluster with hit location estimated at the respective strip
- Closer look on signals and noise separately necessary to disentangle effects





Correlations using rank correlation coefficient (Kendall's Tau)

Source: Thomas

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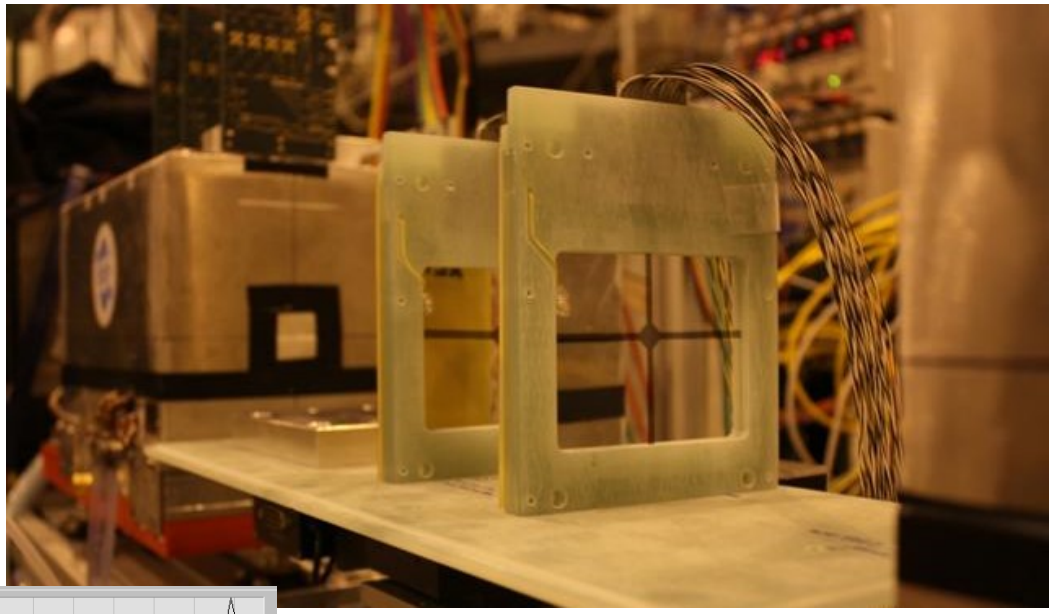
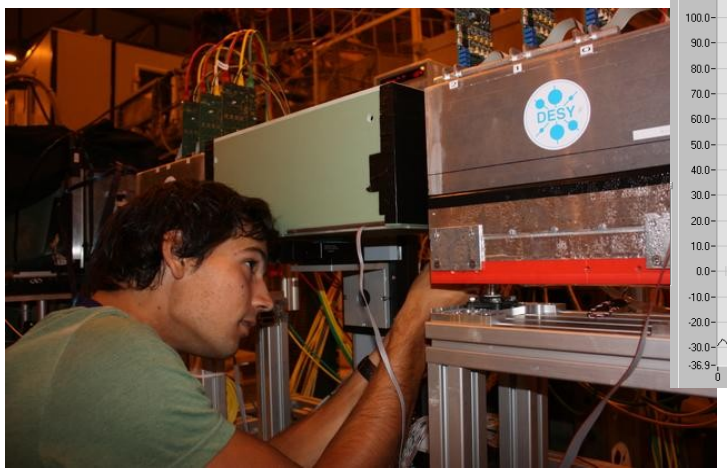
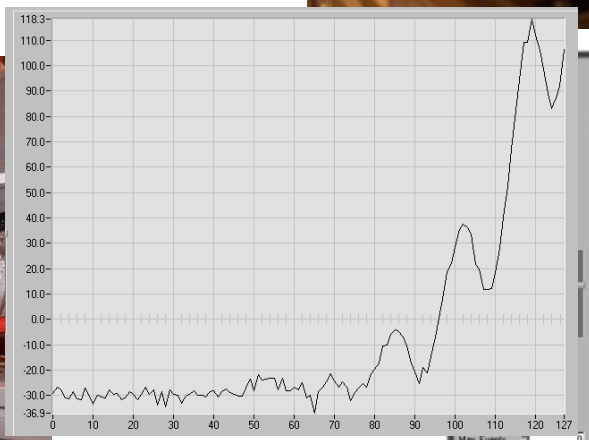
SiLC combined testbeam

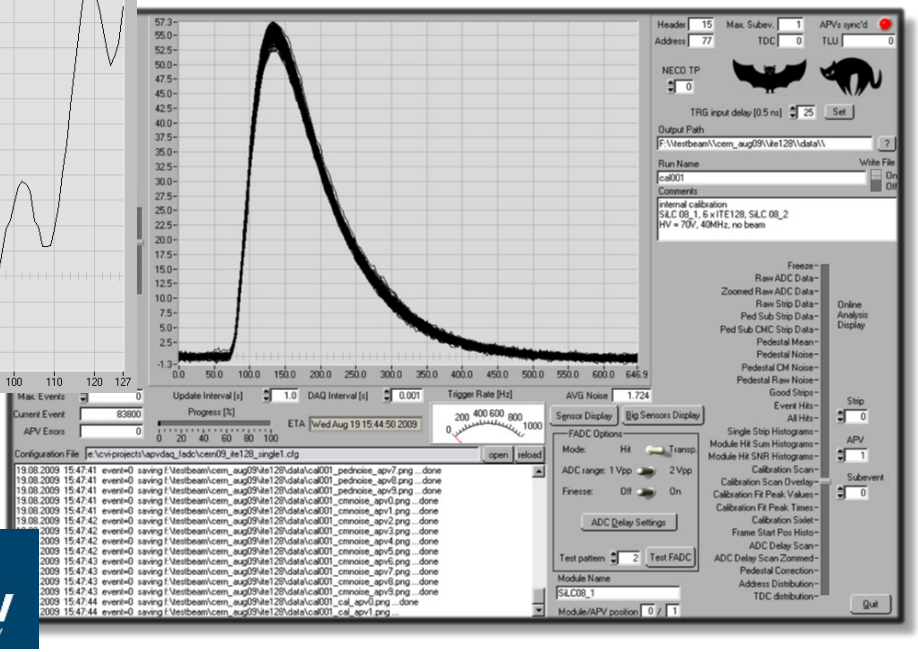
Alignment module runs

- Alignment modules:
  - Two modules mounted on base plate together with laser collimator (end of optical fibre)
  - Beam and Laser runs









Source: Thomas Bergauer

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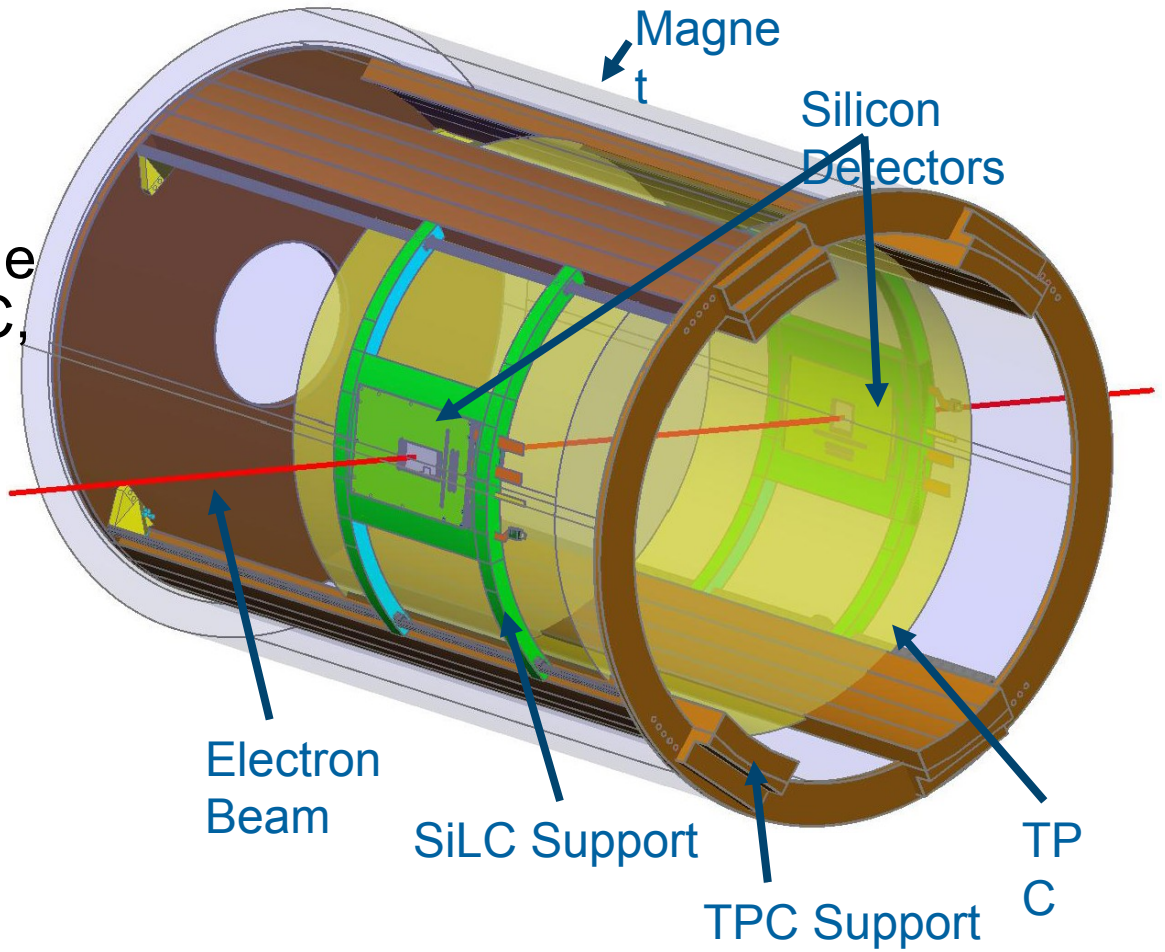
LPTPC-SiLC combined test beams : silicon envelope (2009@DESY)

- Goal: study the resolution improvements of the Large Prototype TPC by adding a precise measured point of the track (order of 10µm), inside the gap, between magnet and TPC, on both sides of the TPC.
- This set-up allow the test of a **first prototype of the silicon envelope** with the TPC prototype (ILD)

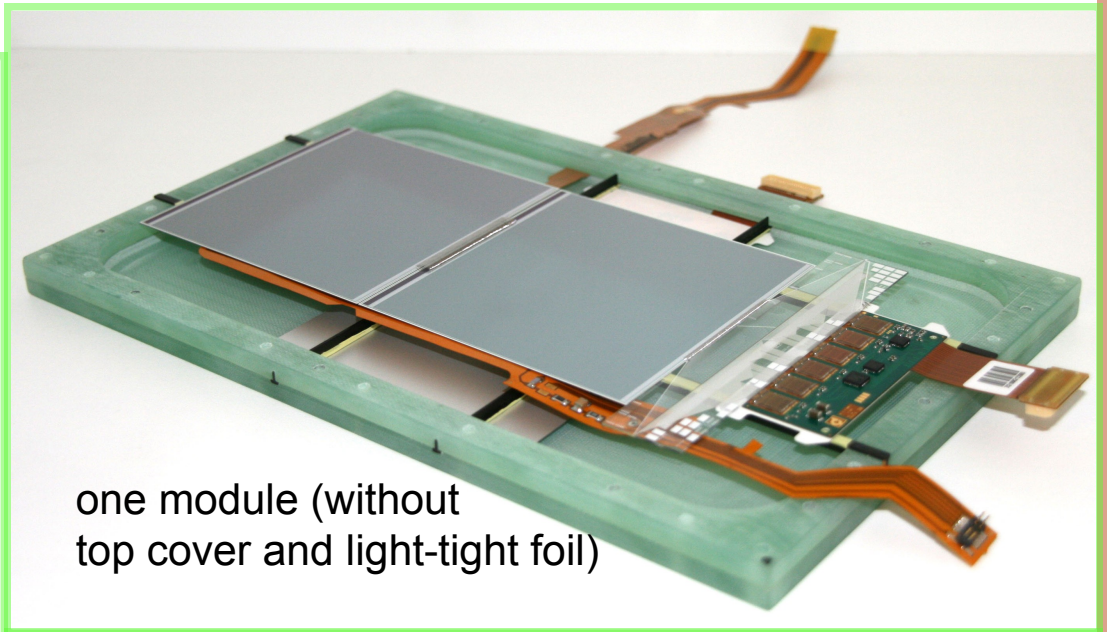


Source: stephan Haensel

LPTPC Silicon Envelope

Description

- 2 silicon detector modules build and tested in Vienna:
  - each contains two crossed silicon strip sensors
  - have to fit inside the 35 mm gap between Magnet and TPC
- moveable support build in Karlsruhe:
  - a sledge on each side of the TPC can position the silicon modules into the beam
- adapted CMS-readout (based on APV25) provided by Karlsruhe (will replaced by the new front-end chip SiTr130-LPNHE)



one module (without top cover and light-tight foil)

mounted modules moving along the TPC

Source: stephan Haensel

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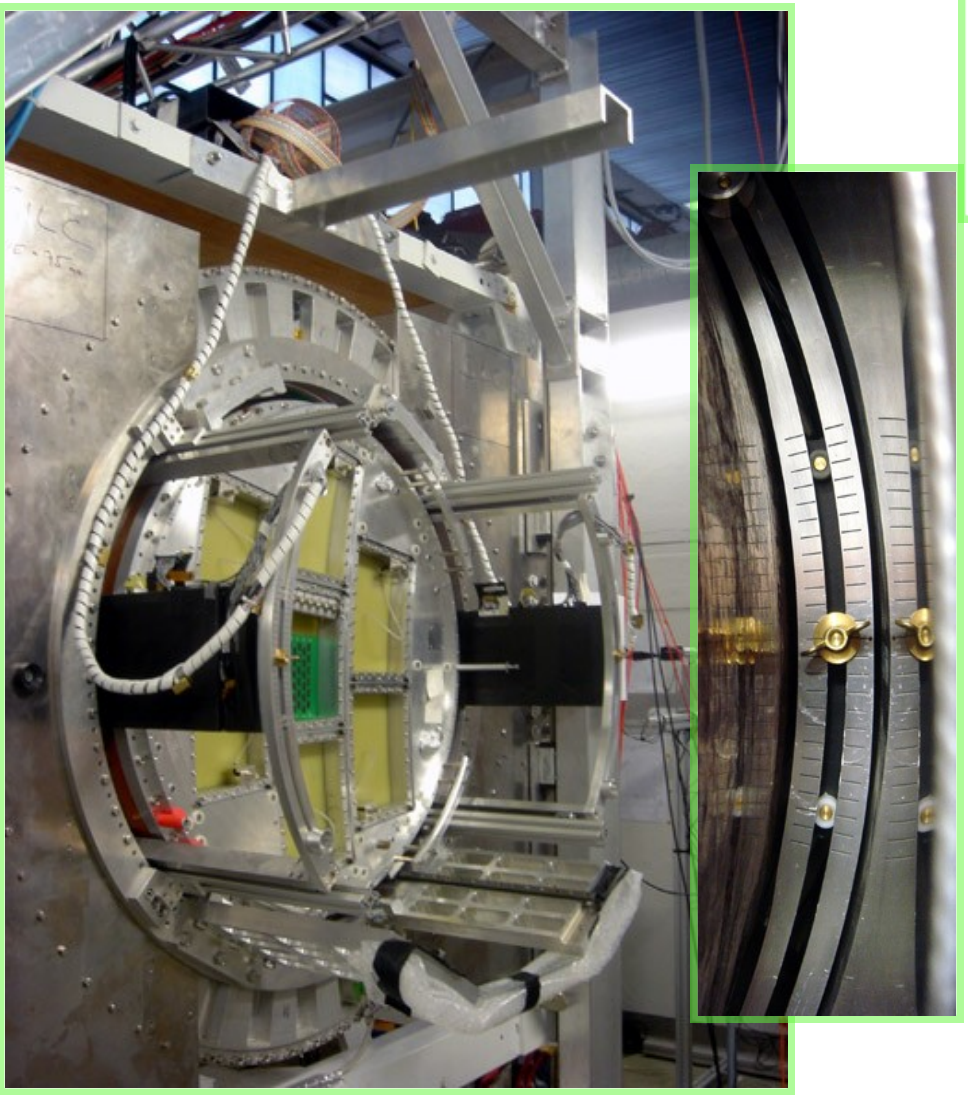
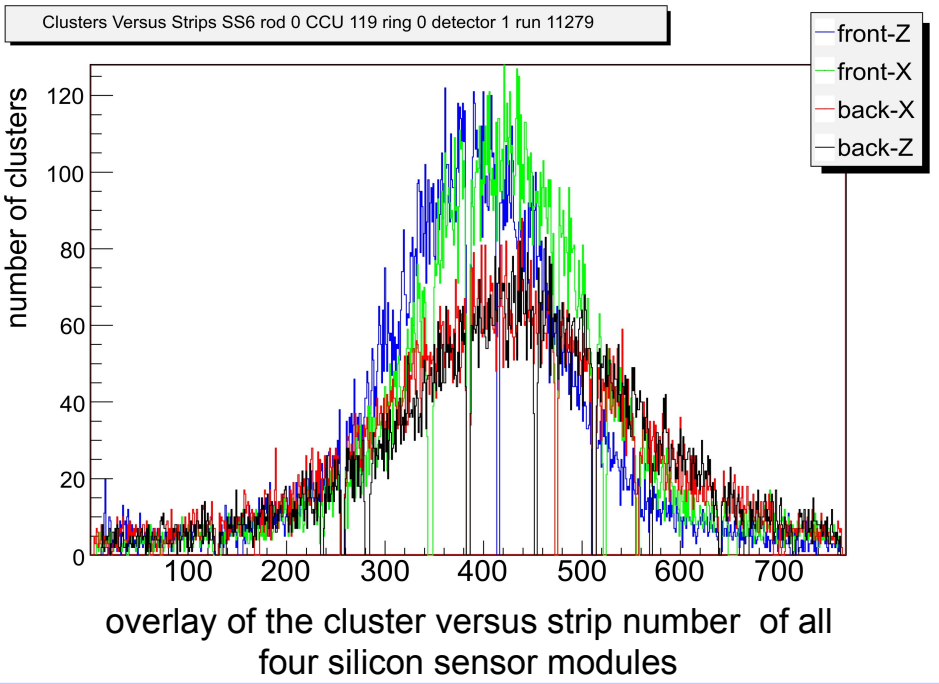
LPTPC Silicon Envelope

Preliminary Results



- silicon envelope outside the gap between magnet and TPC
- Detector module inside the gap

•Results without TPC-readout



•Combined Data-Taking with one Micromegas Module at the Moment

Source: stephan Haensel

Next years prospects

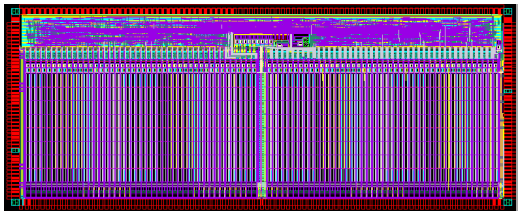
Developing larger size silicon tracking prototypes with:

- new sensors
- new front-end electronics
- Combined test beam with calorimetry
- Taking part of a complete slice test beam set-up

New front-end and readout chip (LPNHE)

2009 – 2010 : Conception-realisation and test of the new version of the SiTr130-128 chip → IBM technology, 130nm

- 128 channels + JTAG
- 0.5*1 cm² of silicon, thin down
- Numerical output with pre-amplifier, shaper, reinitialisation, 8x8 analog pipeline for pulse reconstruction, zero suppression, single ramp ADC, integrated numerical control, robustness & flexibility, power cycling, serialization
- Goal: silicon surface optimisation, modular architecture
- Under Study : **direct connection chip/senseur**

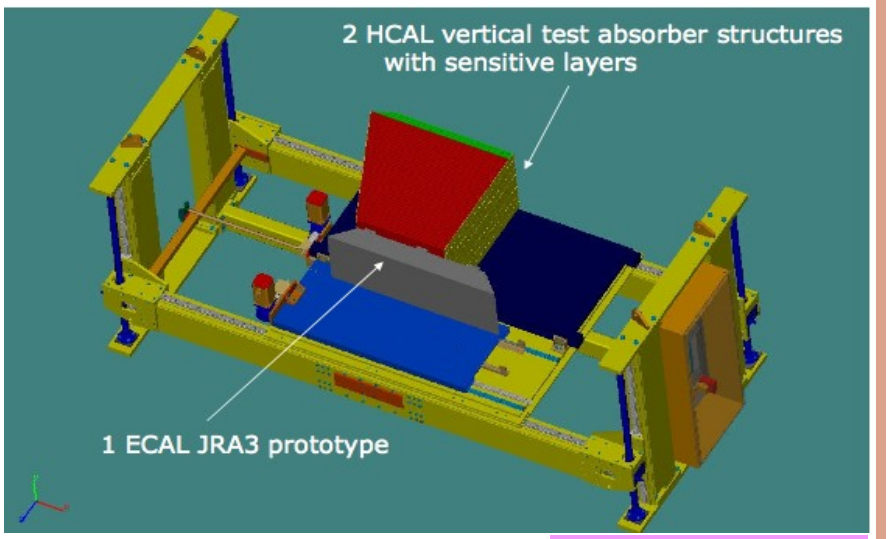


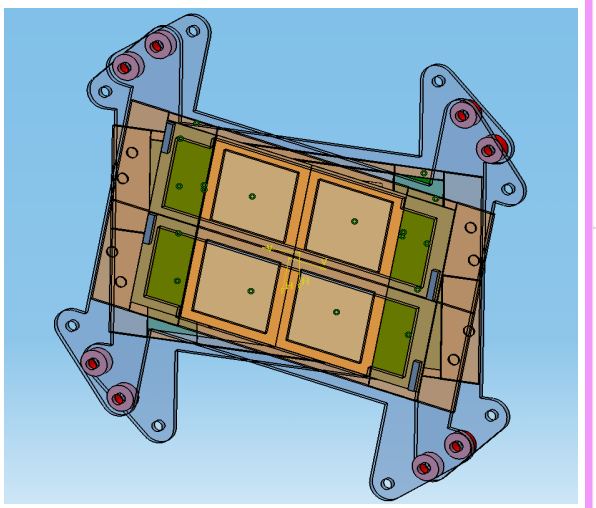
SiTr130-88

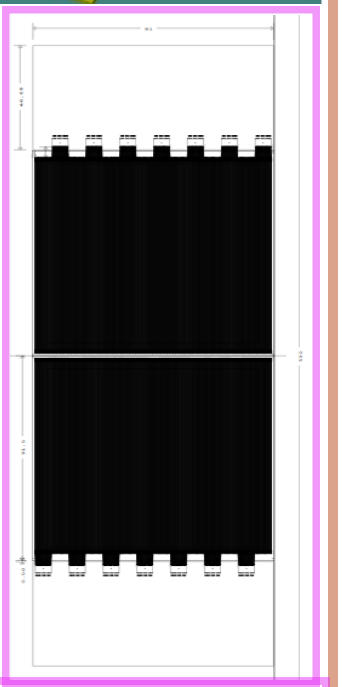
SiTr130-128 submitted next year to equip larger silicon tracking prototypes => combined tests with calorimetry

Combined tests with calorimetry

- Providing a reference tracking system with its acquisition system equipped with ASIC SiTr130
- Progress on the design of the elementary module & the connection with FEE chip
- Combined Tests with calorimetry (CALICE, Dual-readout) (mi-2010-beginning 2011)
- Flexible configuration (XY, XUV, angle adjustment...)
- Large active area
- Compact integration with low material budget
- Configuration testing: full silicon or hybrid system







New module design

Conclusion

- SiLC collaboration have already acquired a large expertise on dedicated and combined test beams
- Developing new silicon prototypes – reference and new FEE, related DAQ system and test beam infrastructure
- Next years: work will be pursued with larger prototypes and more combined test beams set-ups
- Pursuing dedicated test beams for R&D on new technologies (sensors and micro-electronics)