TPC Large Prototype
Toward 7 Micromegas modules

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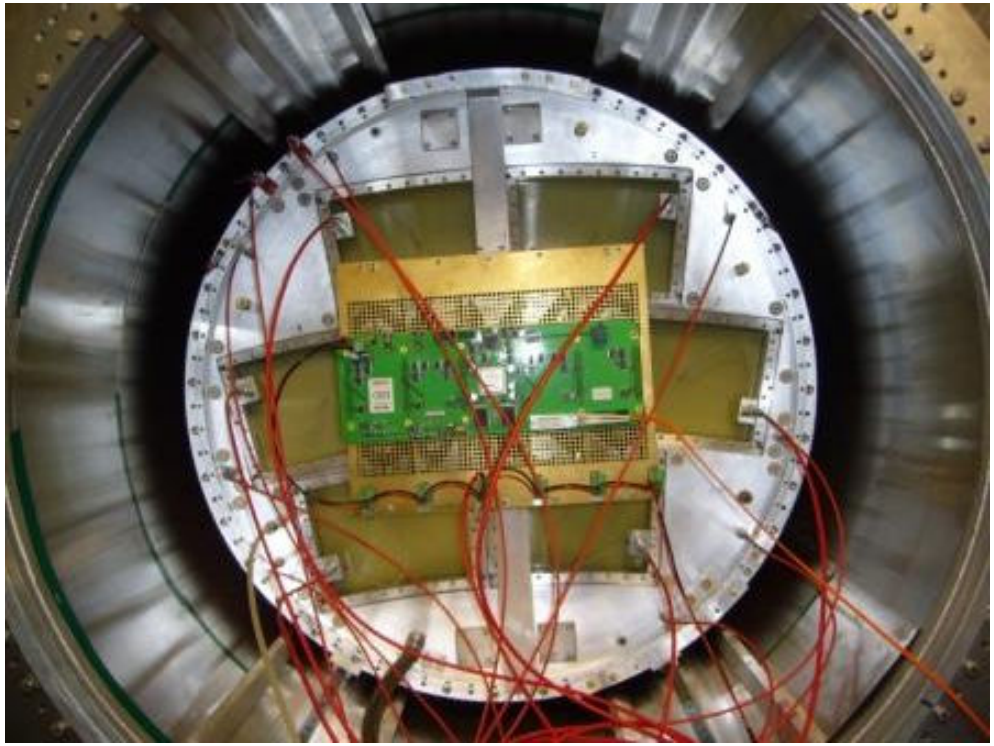
Carleton UNIVERSITY

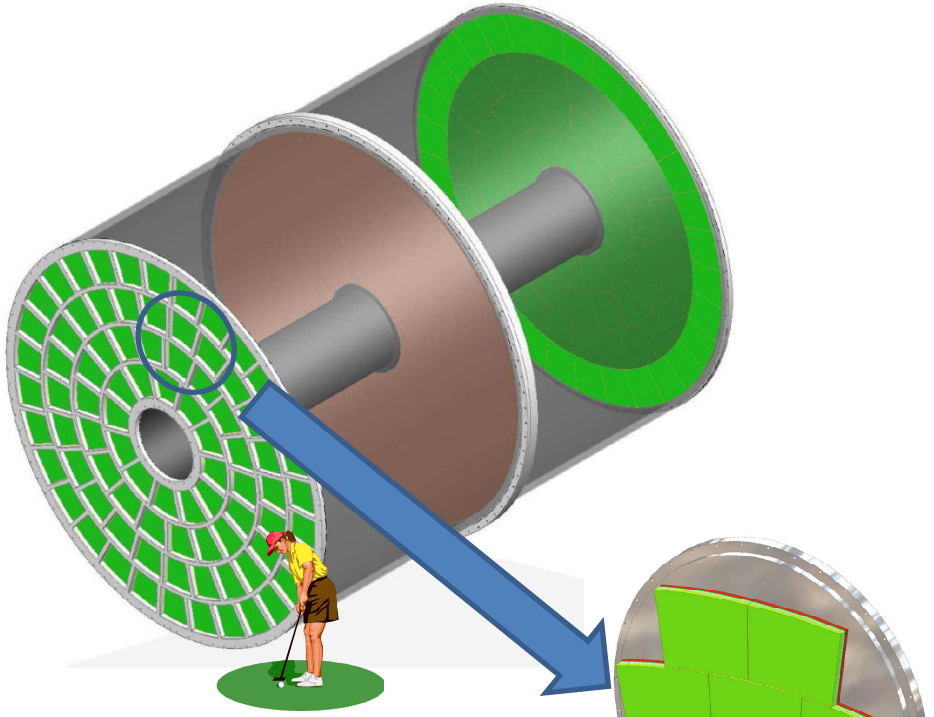
Irfu cea saclay

Goal : equip 7 windows of the LP 'web' with mM modules
- Keep AFTER chip
- Fully integrate
- Use semi-industrial methods
- Develop adapted software



ILC-TPC

Continuous 3D tracking in a large gaseous volume with O(100) space points.

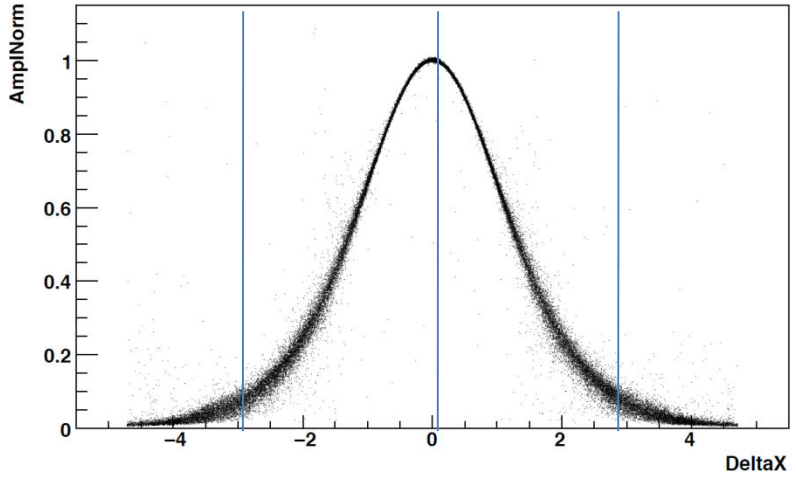


ILC-TPC (ILD conc

Large prototype
under test at DESY

Micromegas module

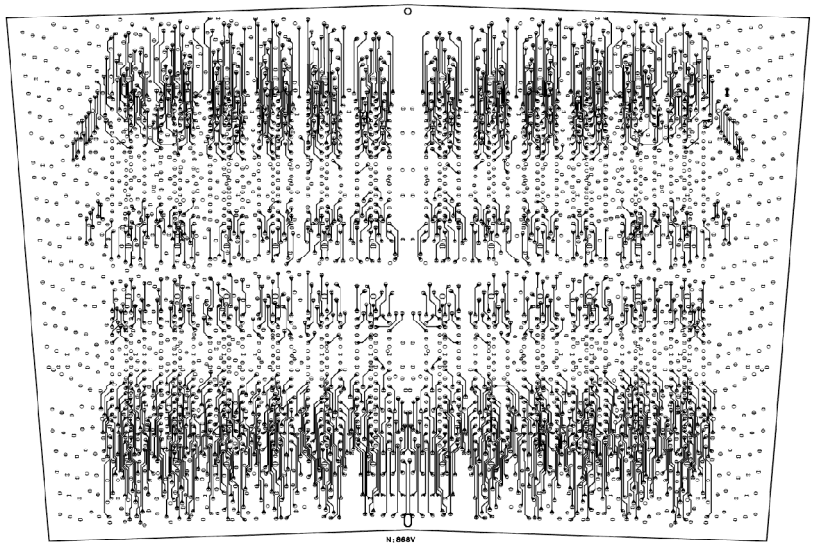
‘Bulk’ technology (CERN-Saclay) with resistive anode (Carleton)



3 single modules already made, and tested at the LP
2 under construction (and more?)
Very satisfactory operation and results (see D. Attié’s talk)

Choose the best technique.
Then start a ‘small series’ (9 modules), use the T2K benchmark at CERN to follow the production

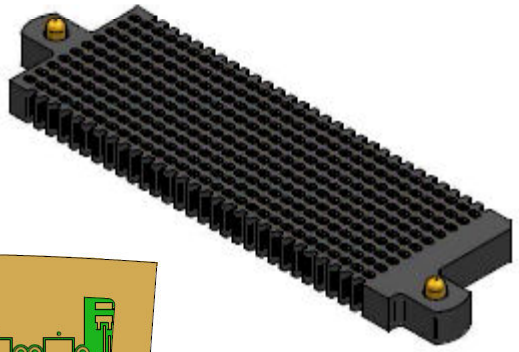
PCB Routing

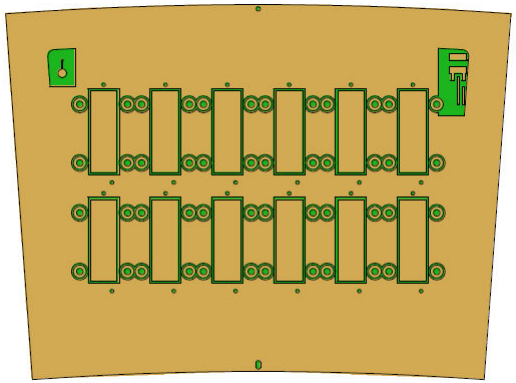


4-layer routing (CERN) and 6-layer routing (Saclay)
24x72 pads, 2.7-3.2 mm x 7 mm

Keep the same pad layout
Re-do the routing to adapt to flat 300 point connectors
(expect to divide the noise by 2: 1500 e- -> 800 e- per pad)

Goal is to have the electronics flat behind the modules





Front End Card

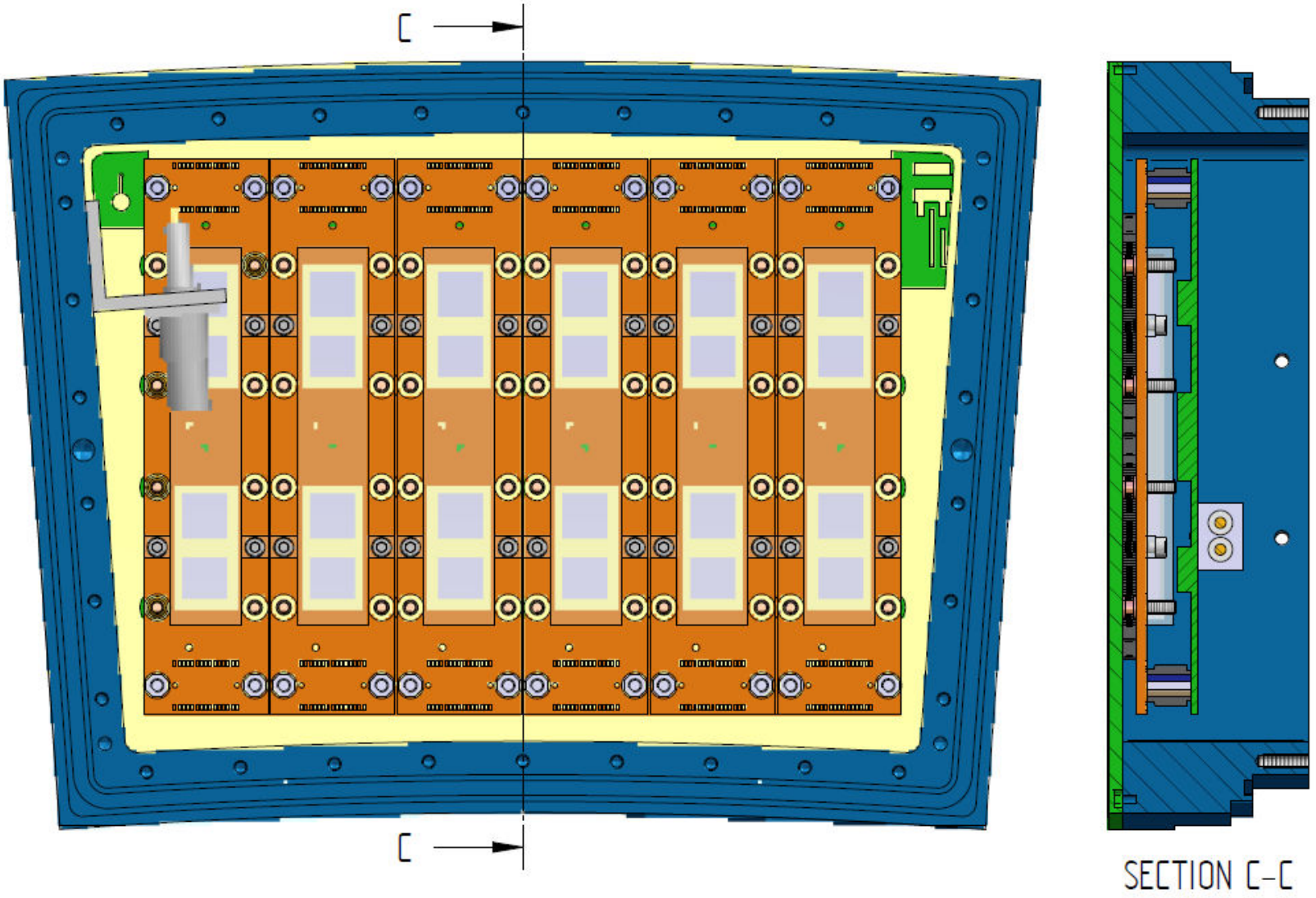
Same as T2K (4 AFTER chips, 4x72 channels) but much less space

In T2K, FECs are perpendicular to the pad plane
Lot of space is taken by the protection (double diodes, decoupling capacitors and series resistors) : may be useless for ILC (Resistive foil protects). Tests are being performed to optimize these protections.
Also lots of space taken by chip packaging (silicon is 7x7mm instead of 20x20 for the packaging
ADC (one per card, 4 chips) can be moved to the FEM (one for all 24 chips)

Connector to the FEM

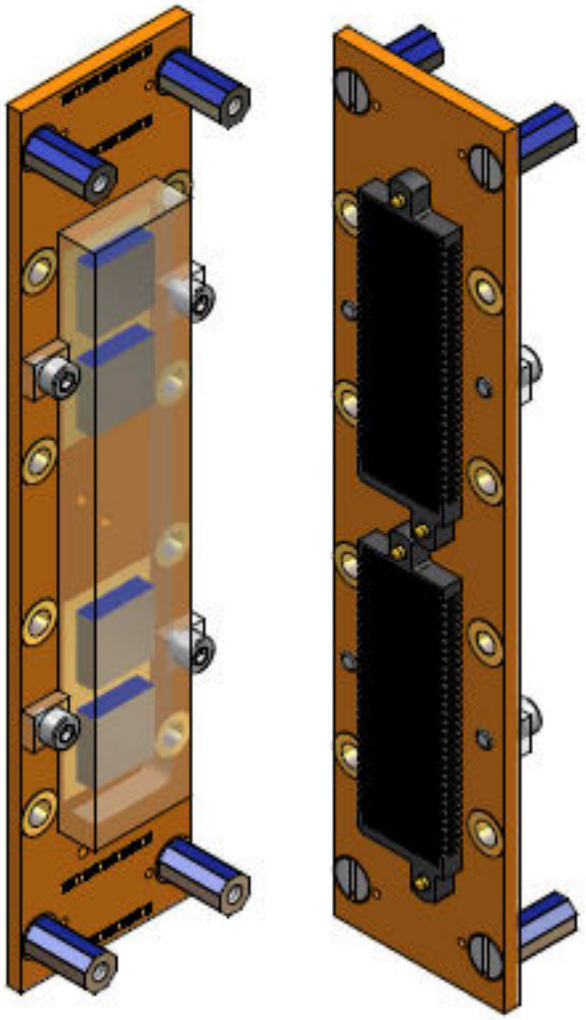
Connectors to the FEM

Front End Cards



Front End Cards

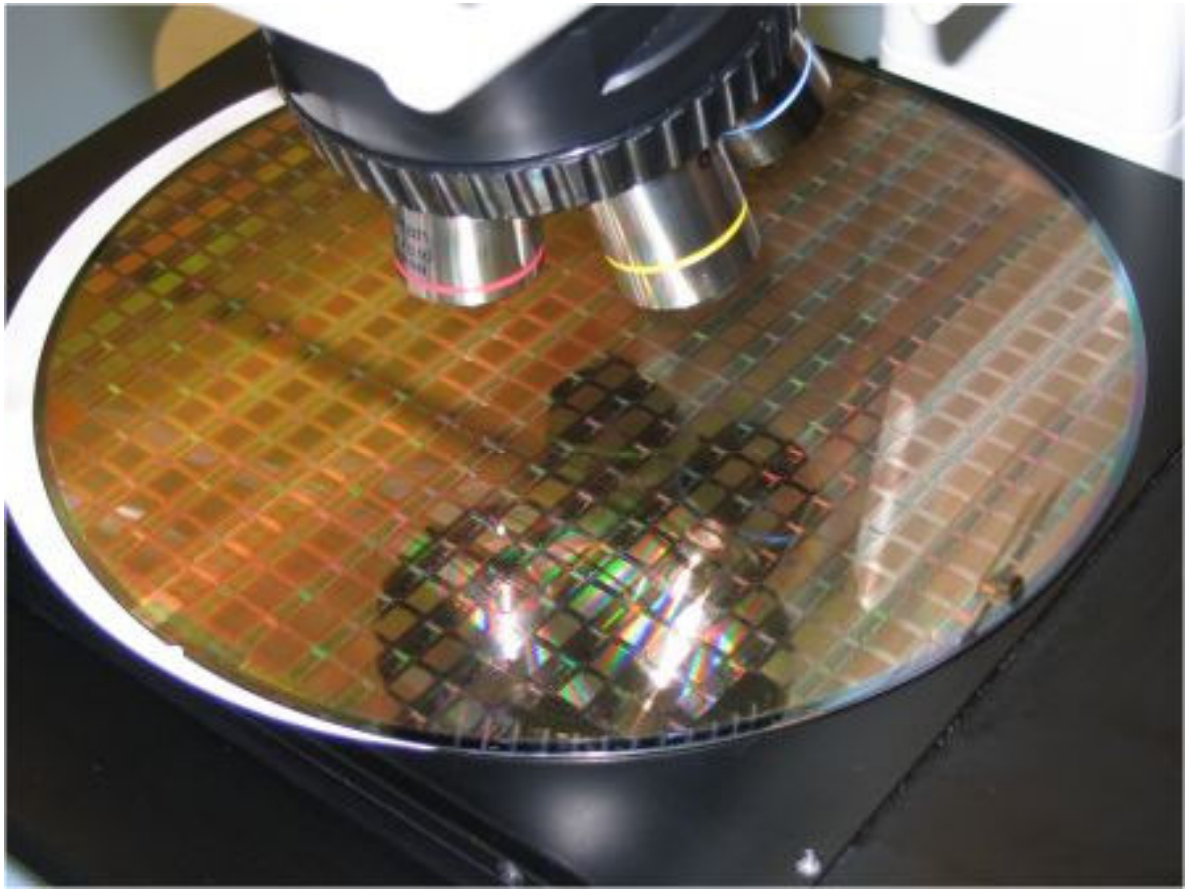
Minimal space: remove most of the protections, use naked chips wire-bonded on the FEC, transfer power regulation and ADC to the mezzanine module card.



Front End Card

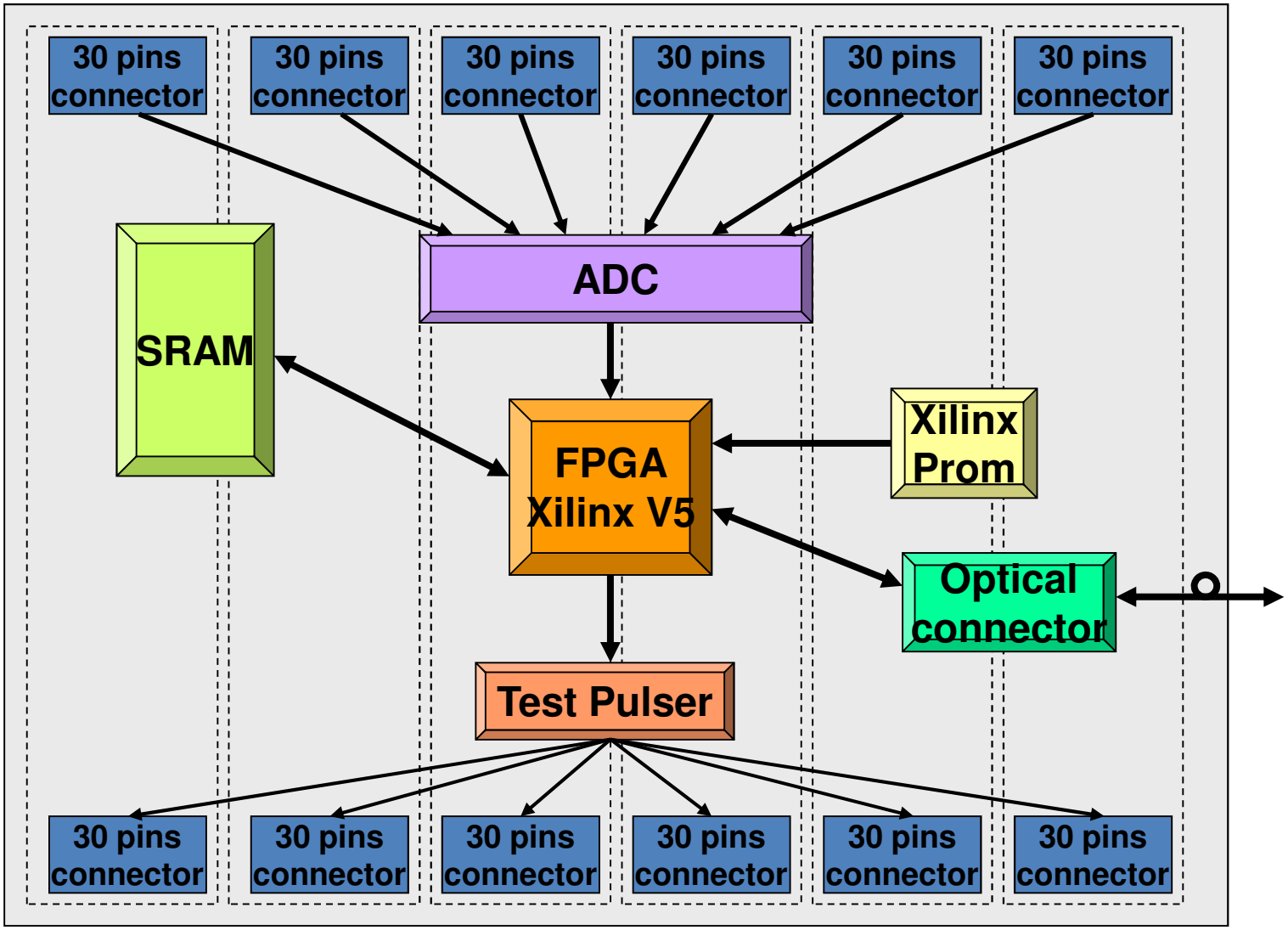
1 AFTER wafer purchased (300 good chips)
Make 60 cards (36 good needed)
Sent to ‘debugging’ and dicing end of this month.

Bond chips (de-bonding possible).
Chips can be tested only on cards. Repair cards with one dead chip.

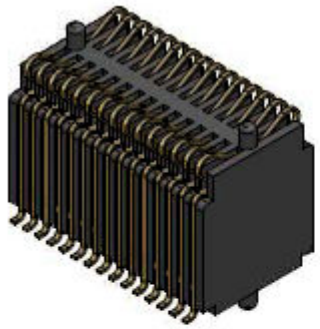


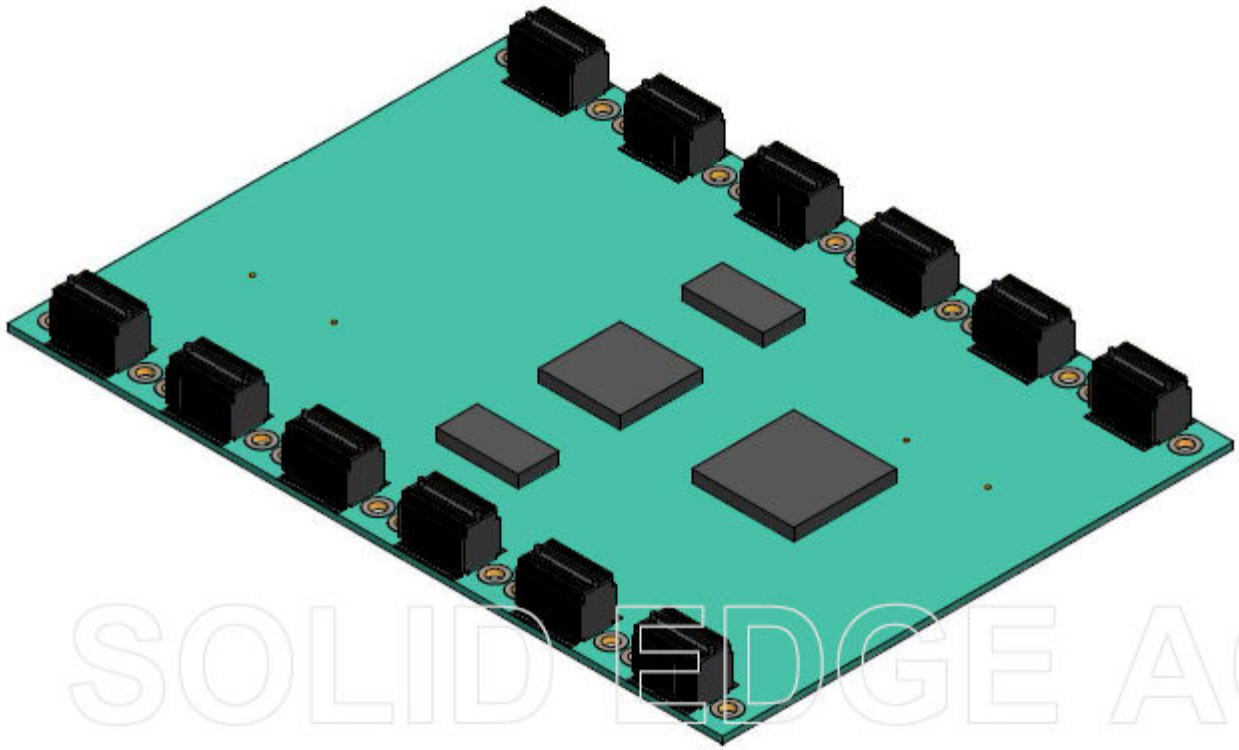
Front End Mezzanine

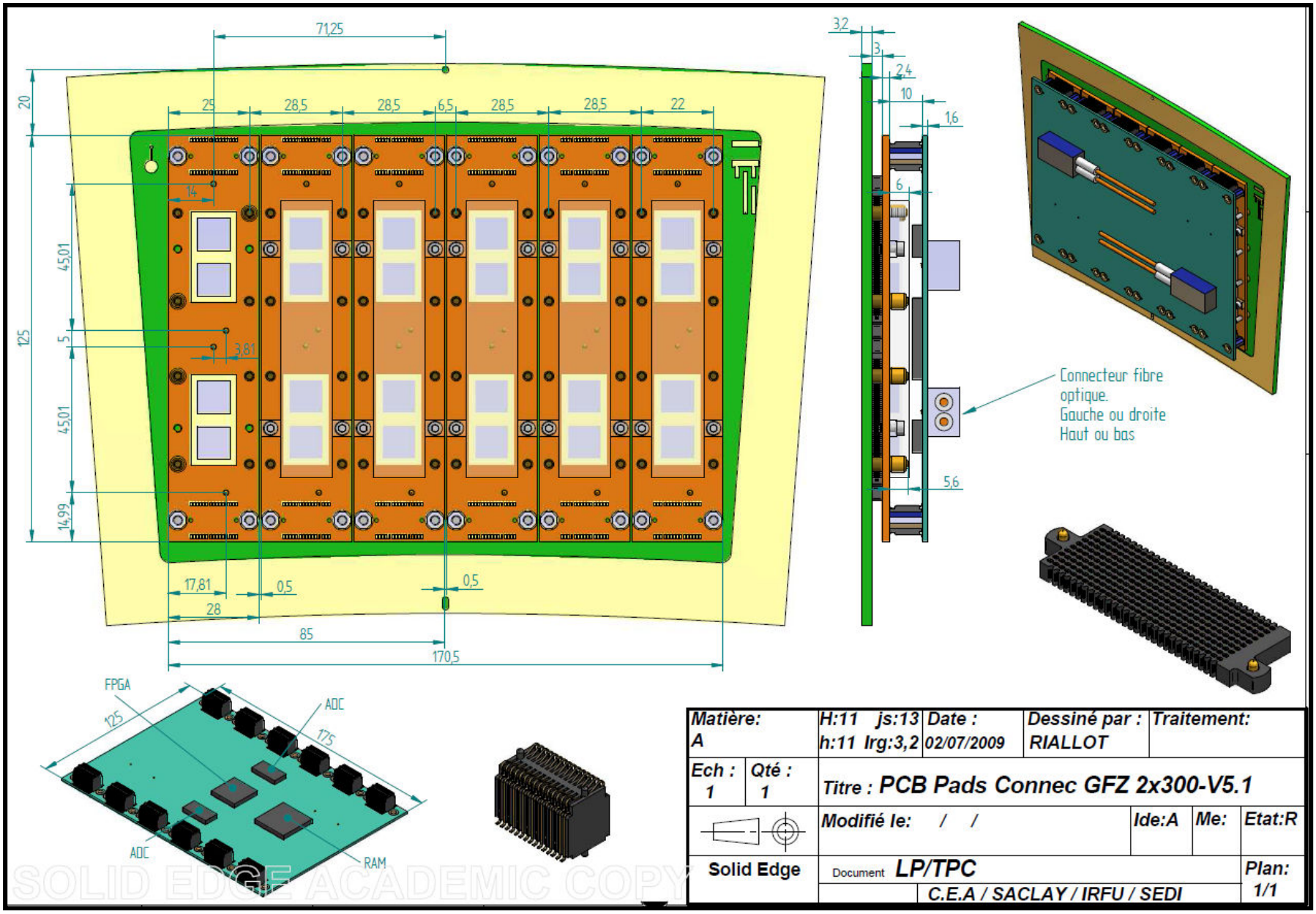
One per module, 1728 channels.
Gathers signals from 6 FECs and sends it to the Back End through an optical link



Front End Mezzanine






71,25
20
125
45,01
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14,99
29
28,5
28,5
6,5
28,5
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17,81
0,5
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28
85
170,5
3,2
3
2,4
10
1,6
6
5,6
Connecteur fibre optique.
Gauche ou droite
Haut ou bas
FPGA
ADC
125
175
ADC
RAM
Matière: A
H:11 js:13 h:11 Irg:3,2
Date : 02/07/2009
Dessiné par : RIALLOT
Traitement:
Ech : 1
Qté : 1
Titre : PCB Pads Connec GFZ 2x300-V5.1
Modifié le: / /
Ide:A
Me:
Etat:R
Solid Edge
Document LP/TPC
Plan: 1/1
C.E.A / SACLAY / IRFU / SEDI
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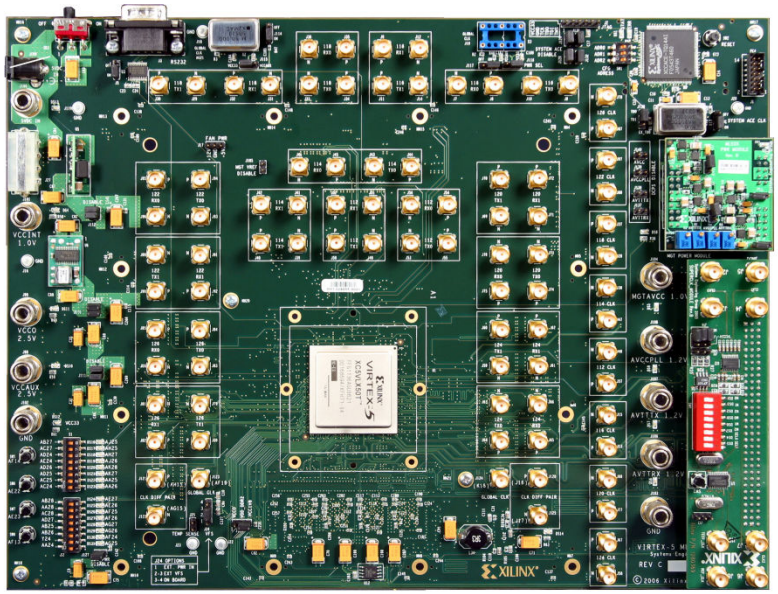
Back End

- Functionality
  - → Receives clock, trigger and control flow & distributes it to up to 12 FEMs
  - → Concentrates data from up to 12 FEMs and sends them to DAQ

- Interfaces
  - → 12 optical 2 Gbit/s FE links
  - → 1Gbit/s Ethernet DAQ – Slow Control link
  - → Trigger – Clock – Fast Control link
    - whatever standard

Back End Hardware

- ML523 development kit from Xilinx
  - → vc5vfx100t FPGA from Virtex-5 device family
    - Embedded PowerPC
    - 16 Multi Gigabit Transceivers
    - Embedded Ethernet MAC
  - → 128 Mbyte DDR2 memory
  - → RS232 interface



- Up to 3 4-channel SMA-SFP interface cards
  - → 2 Gbit/s optical transceivers for FE links
  - → RJ45 Ethernet transceiver for the DAQ link
- Trigger – Clock – Fast Control link mezzanine card
  - → To be developed according to the link specifications

Status and plans

PCB routing : started, no show-stopper, 3-4 weeks

FEC routing : concept adopted, details being studied

AFTER Wafer : purchased, choice of company to dice, “de-bug” and bond in progress: mid October

Mechanical model : to test new connectors, wire bonding, etc…mechanical model (PCB+FECs+FEM) by mid-November

FEM routing : concept adopted, work under progress, 3 months

FEM proto operational : March 2010

Status and plans

ML523 development kit from Xilinx - Purchased

- Embedded PowerPC-based SoC design underway
  - SFP RJ45 Ethernet link operational
  - 12 2 Gbit/s FE Transceivers up & under tests
  - DDR2 memory to be debugged

4-channel SMA-SFP interface cards : Schematics done, placement and routing underway

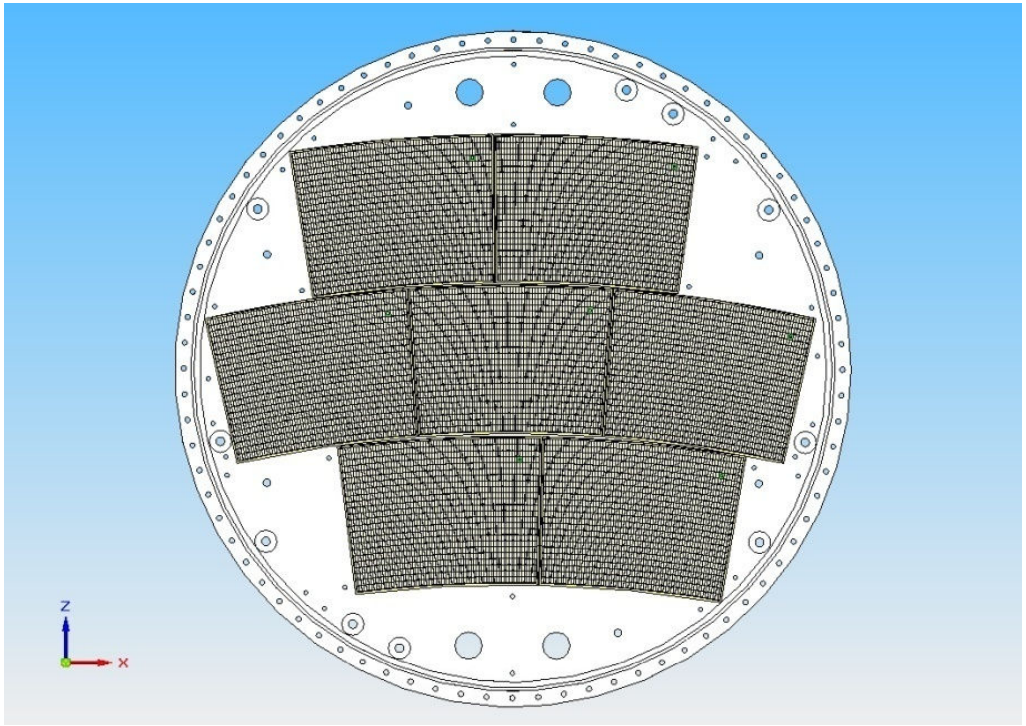
Trigger – Clock – Fast Control link mezzanine card

- Specifications – to be done

Backend overall mechanical structure to be done (Enclosure, power supplies, cooling, connectors)

Significant support from Canada

Software



Special effort needed to have from the begining:
-Integration in the EUDET DAQ (EUDAQ), LCIO data format
-7 module display
-Alignement software
-Integration in LC-TPC framework (MARLIN)
-Optimized resistive foil analysis

CONCLUSION

After the succes of the 1-module runs, a strong effort for a fully integrated 7-module Micromegas TPC system is started.

New concepts will be used : flat high-density, zero-extraction-strength connectors, naked chips on board, and many improvements to the T2K readout : latest ADCs, FPGAs.

This will also be a semi-industrial production and a proof of feasability, meeting the LOI specs