

SiW Ecal EUDET Module

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- General Schedule
- Development of Different Components
- (Towards) a working prototype

To learn more

<http://flc.web.lal.in2p3.fr/poeschl/siwecal.html>

The groups working on the EUDET Electromagnetic Calorimeter



- What we call “EUDET Module” is in fact the next SiW Ecal CALICE Prototype
- Financial support by EU

Evolution of Task – JRA3 Ecal EUDET Module

2006

Conceptual Phase – Definition of Project Targets
Detection of problems with Si-Wafer Guardrings and start of investigations for remedies

2007

Decision to go for 0.5x0.5 cm² Si-Wafers instead of 1x1 cm² Wafers
Contacting and negotiations with manufacturers
⇒ Wafers with dimensions of 9x9cm²
Continuation of studies for building large alveolar Structures
Dimensions depend on wafer dimensions and constraints of challenging Very Front End Electronics

2008

Decision to go for a demonstrator to allow for validation of mechanical concept
Milestone: Design of Moulds and Alveolar Structures finished (EUDET-Memo-2008-07)
Milestone: TDR of SiW Ecal EUDET Module – Details of design fixed (EUDET-Memo-2008-11)
Delivery and Examination of 30 Si-Wafers (Hamamatsu)

2009

Demonstrator built and start of thermal studies
Demonstrator is to be taken as EUDET Deliverable!!!!
[Ordering of pieces for 'real' EUDET module in autumn 2009](#)
Next steps depend on progress of VFE
Advancing the VFE has top priority on 2009

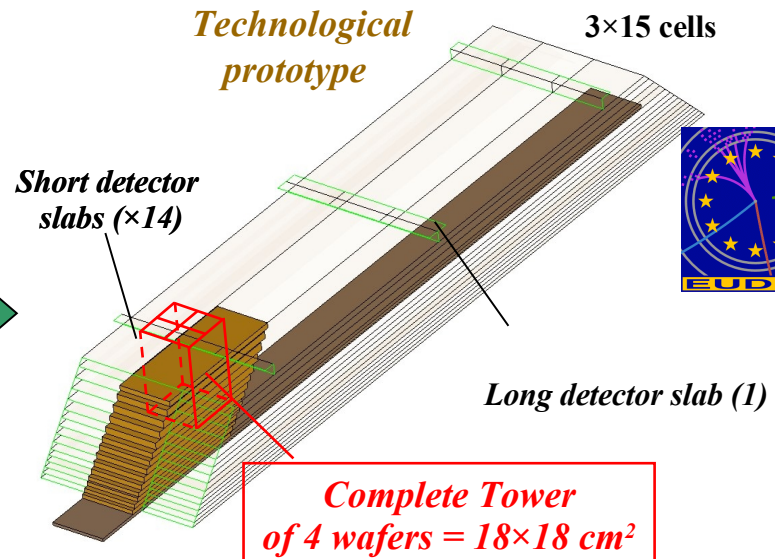
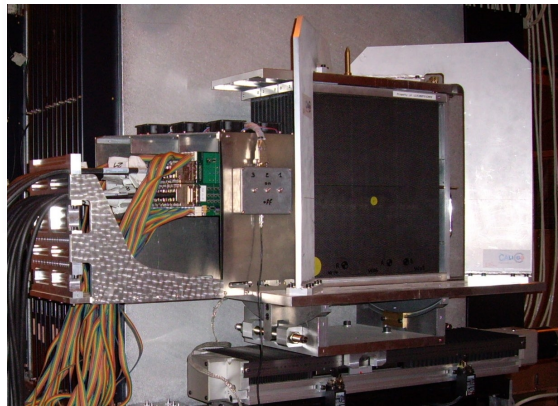
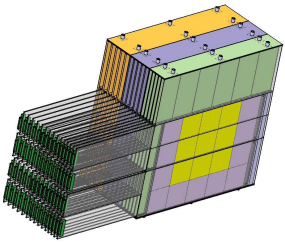
2010

Assembly of EUDET Module ?

EUDET SiW Ecal Prototype July 2009

EUDET Prototype

- **Logical continuation** to the physical prototype study which validated the main concepts : alveolar structure , slabs, gluing of wafers, integration
- Techno. Proto : study and validation of most of **technological solutions** wich could be used for the final detector (moulding process, cooling system, wide size structures,...)
- Taking into account **industrialization aspect** of process
- First **cost** estimation of one module



- **3 structures : 24 X₀**
(10×1,4mm + 10×2,8mm + 10×4,2mm)
- **sizes : 380×380×200 mm³**
- **Thickness of slabs : 8.3 mm**
(W=1,4mm)
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**

W Ecal Pr

- **1 structure : ~ 23 X₀**
(20×2,1mm + 9×4,2mm)
- **sizes : 1560×545×186 mm³**
- **Thickness of slabs : 6 mm**
(W=2,1mm)
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

Time Scale of Project

~Today

Spring 2009

Summer/Autmun 2009

2010

← Studies on mechanical Integration and DAQ →

1/7/09

Status of the Project

Tests avec ASU1

Tests avec ASU2

Design of Prototype concluded

Assembly and studies with Demonstrateur

'ASU 1': SPIROC2/SKIROC with FEV7

EUDET: Deadline, Alveolar Structures and ASU 1

ASU2: SPIROC with FEV8

EUDET-Memo-2008-07



ECAL Si/W – Design and Fabrication of moulds for the EUDET Module

M.Anduze, R. Poeschl
July 01, 2008

Covering aspects of the alveolar structures

TDR of SiW EUDET Module



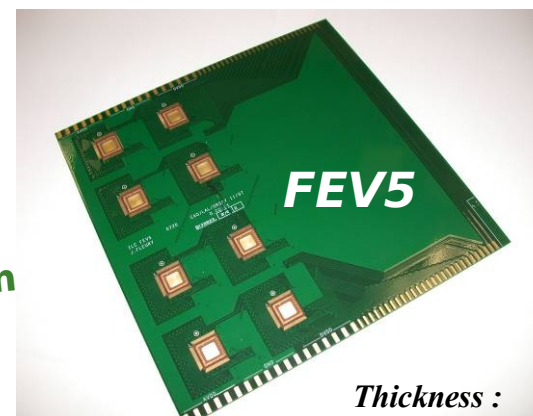
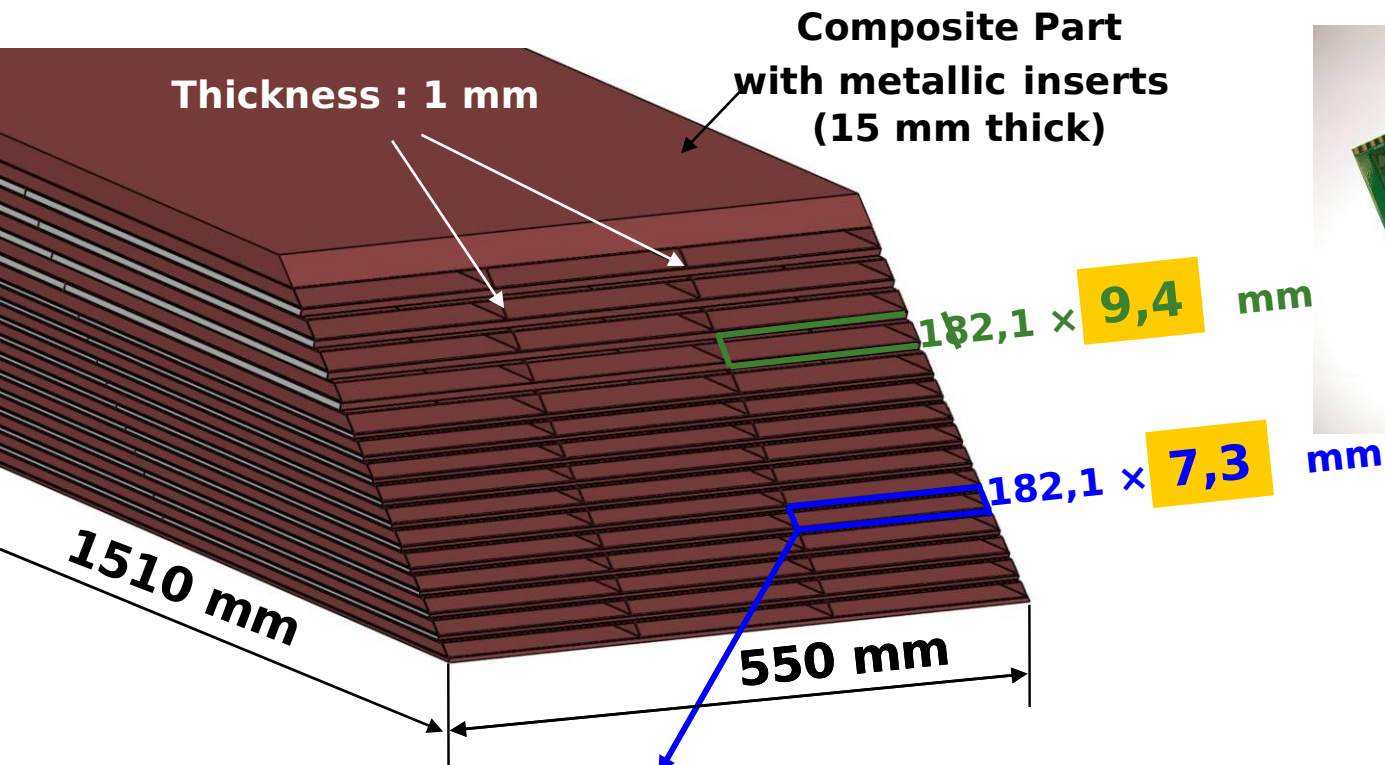
EUDET Memo 2008-11

JRA3 Electromagnetic Calorimeter Technical Design Report

M. Anduze¹, D. Bailey², R. Cornat¹, P. Cornebise³, A. Falou³, J. Fleury³, J. Giraud⁵, M. Goodrick⁴, D. Grondin⁵, B. Hommels⁴, R. Poeschl³, R. Thompson²

**Detailed Technical Design of EUDET Module
Now also EUDET-Report-2009-01**

Module EUDET – Current Design (final – developed 2008)

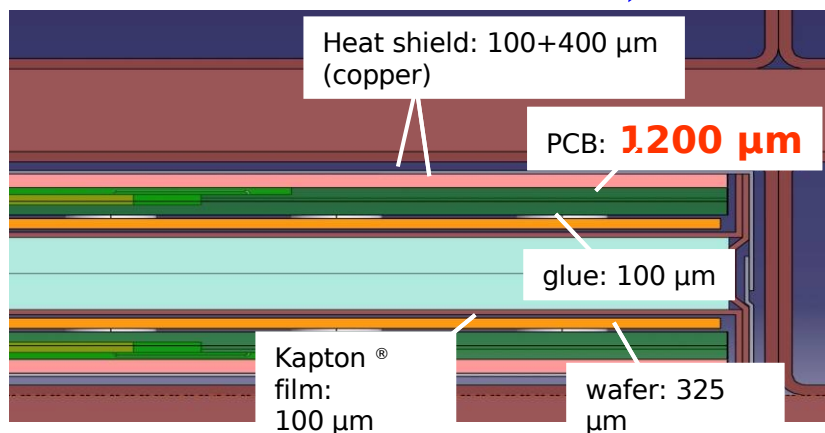


Thickness :

FEV5-1 : 1.17mm (+0.04)

FEV5-2 : 1.19mm (+0.04)

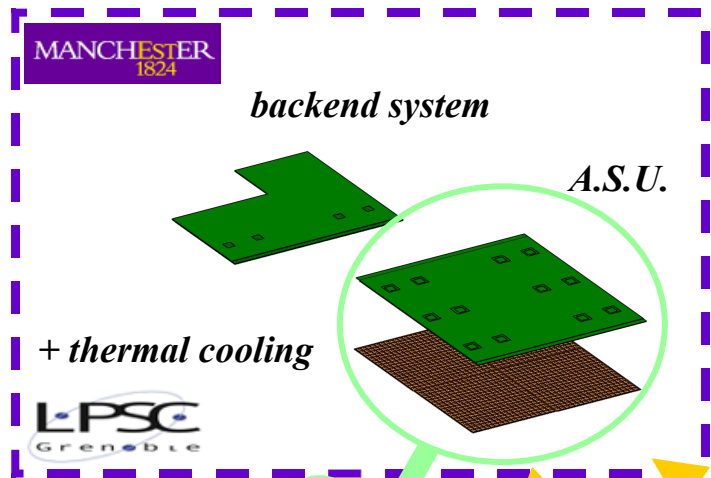
FEV5-3 : 1.20mm (+0.02)



- ⇒ Gaps (slab integration) : 500 μm
- ⇒ Heat Shield: 400 μm ? Validation with the demonstrateur
- ⇒ PCB : 800 μm ~~~1200 μm~~
- ⇒ Thickness of Glue : 100 μm
- ⇒ Thickness of SiWafer : 325 μm
- ⇒ Kapton® film HV : 100 μm ?
- ⇒ Thickness of W : 2100/4200 μm ($\pm 80 \mu\text{m}$)

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:



Assembling of **A.S.U.** (industrialization, gluing and tests) + backend system (DIF support) + services



Tests of **wafers**
Global **Design** + composite **Structures**



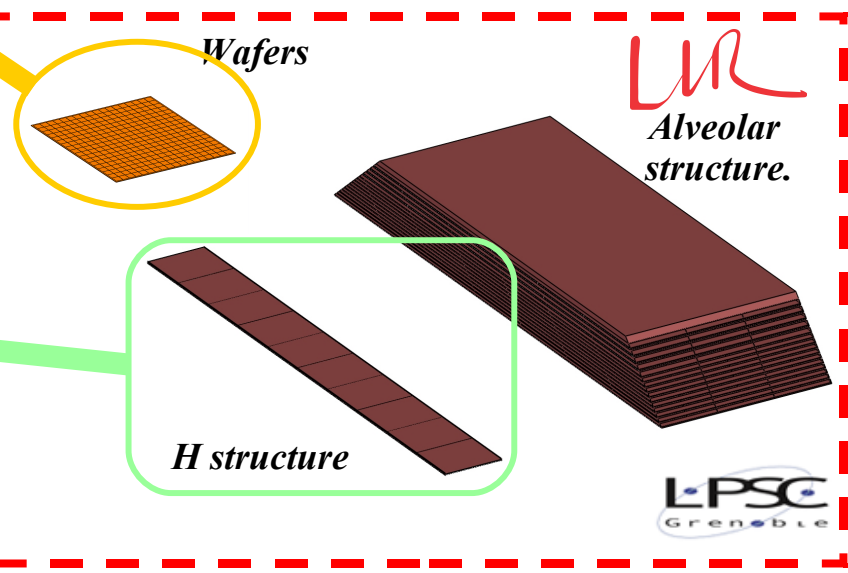
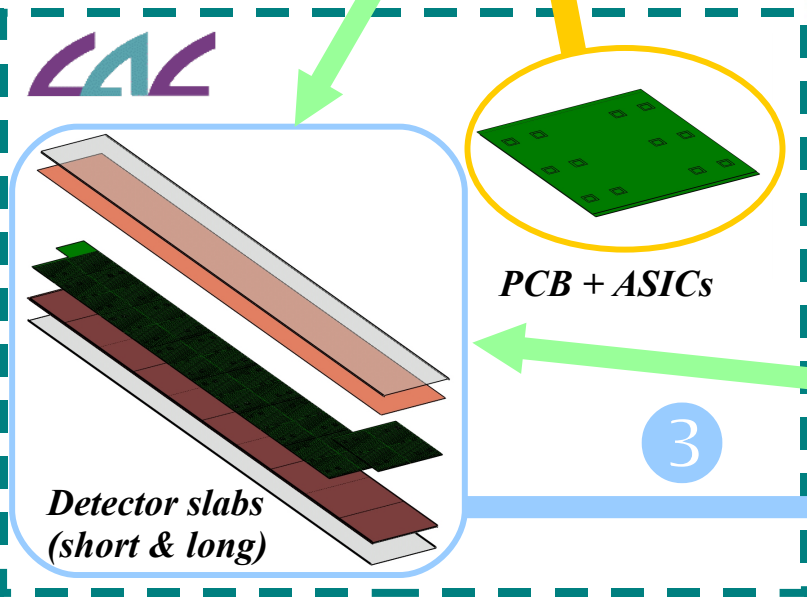
Thin PCB with embedded ASICs
Detector slabs integration



External cooling system
Fastening system ECAL/HCAL+composite plates



Interconnection of ASU, DIF



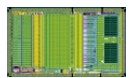
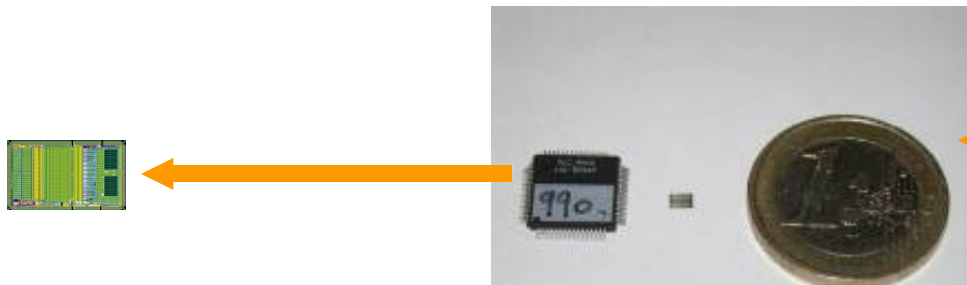
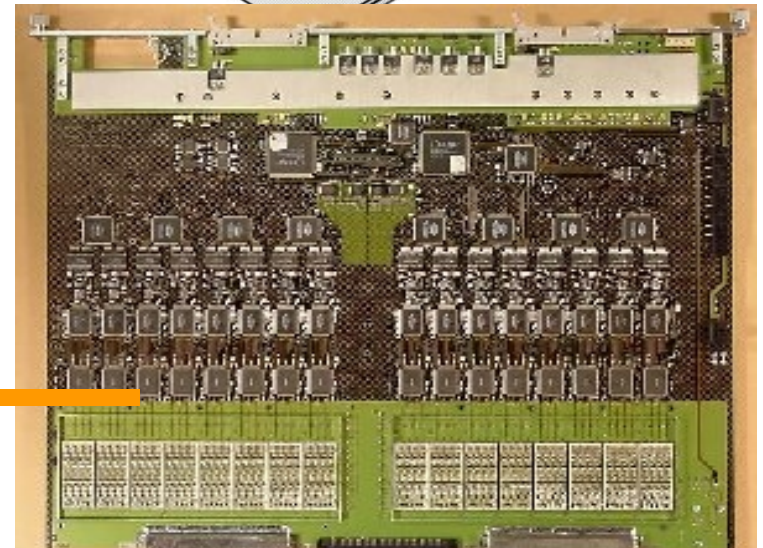
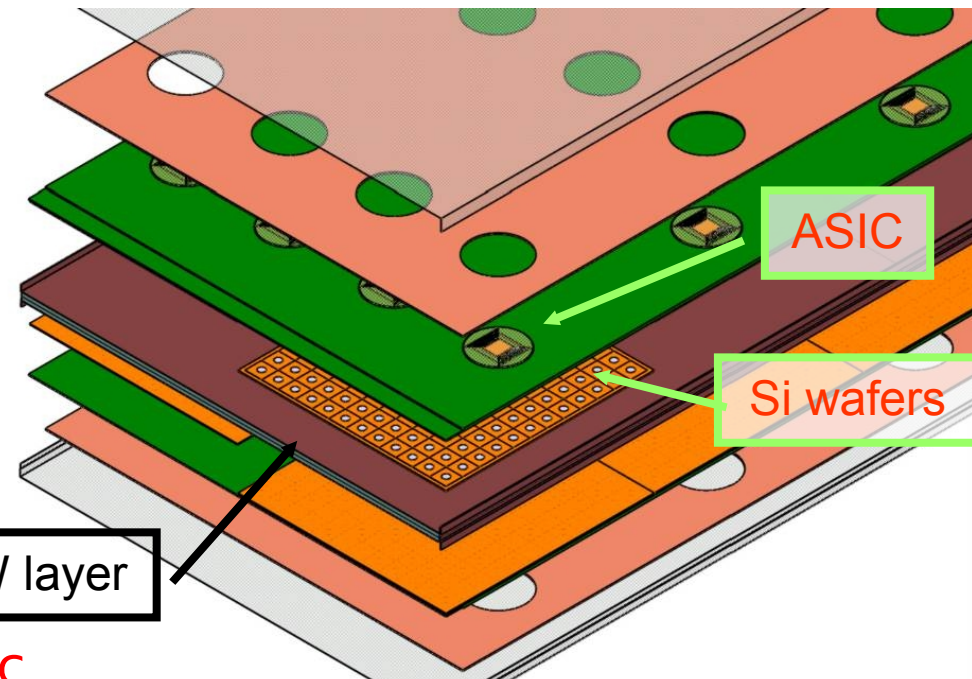
ILC Challenges for electronics

- Requirements for electronics
 - Large dynamic range (15 bits)
 - Auto-trigger on $\frac{1}{2}$ MIP
 - On chip zero suppress
 - Front-end embedded in detector

- Ultra-low power : ($\ll 25\mu\text{W}/\text{ch}$)

- 10^8 channels
- Compactness

- « Tracker electronics with calorimetric performance »
- No chip = no detector !!



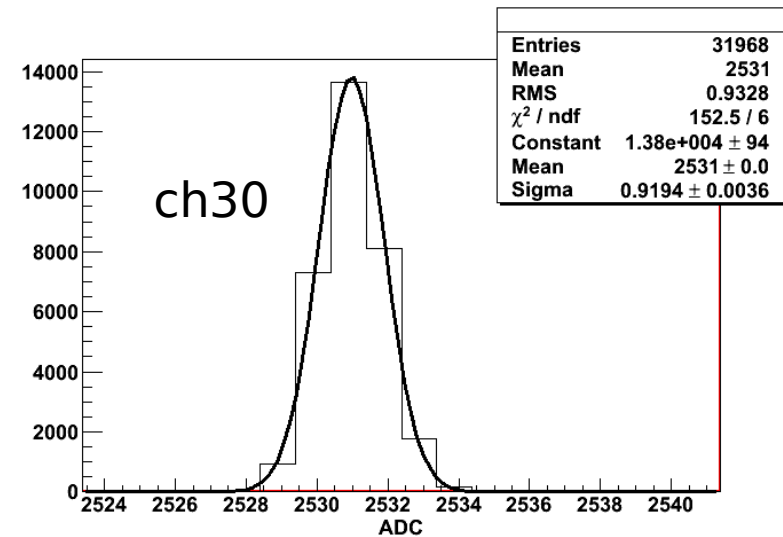
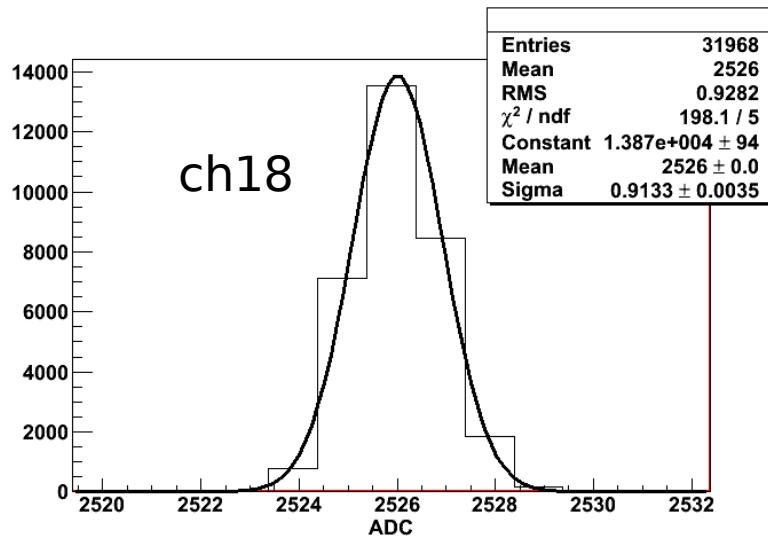
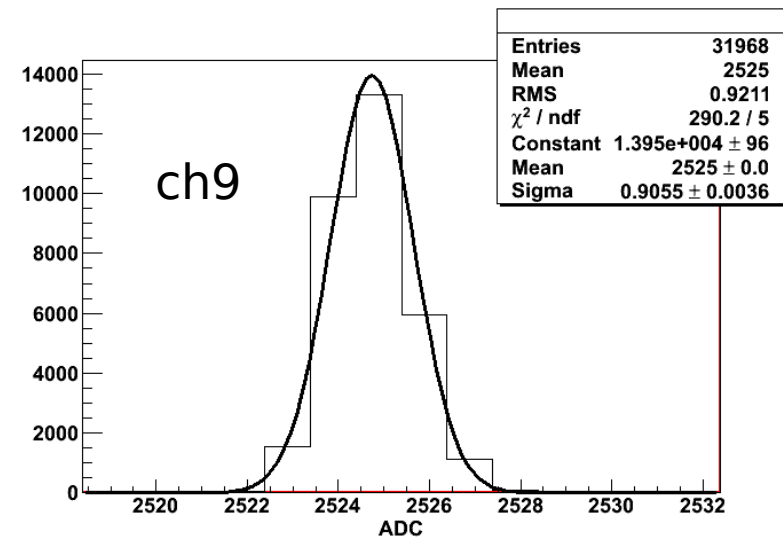
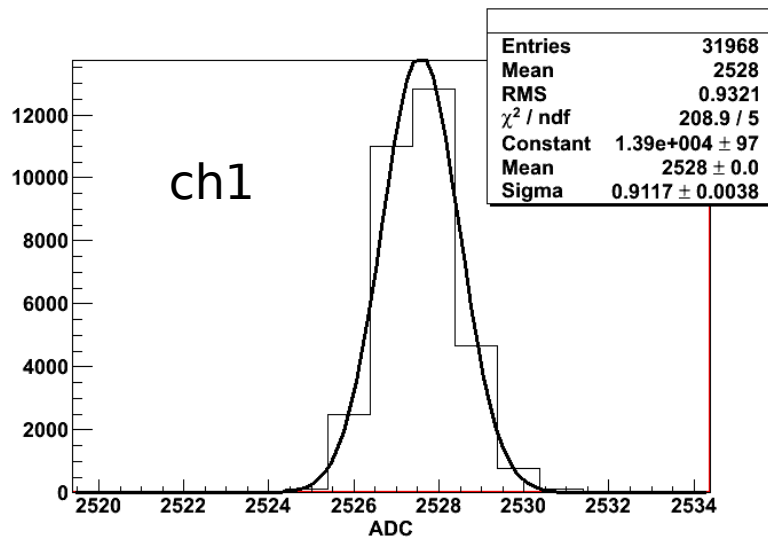
ILC : $25\mu\text{W}/\text{ch}$

FLC_PHY3 18ch 10*10mm $5\text{mW}/\text{ch}$

ATLAS LAr FEB 128ch 400*500mm $1\text{W}/\text{ch}$

Characterisation of SPIROC2 Chip – Used for first Ecal Prototype

Gaussiennes – 2 Volt

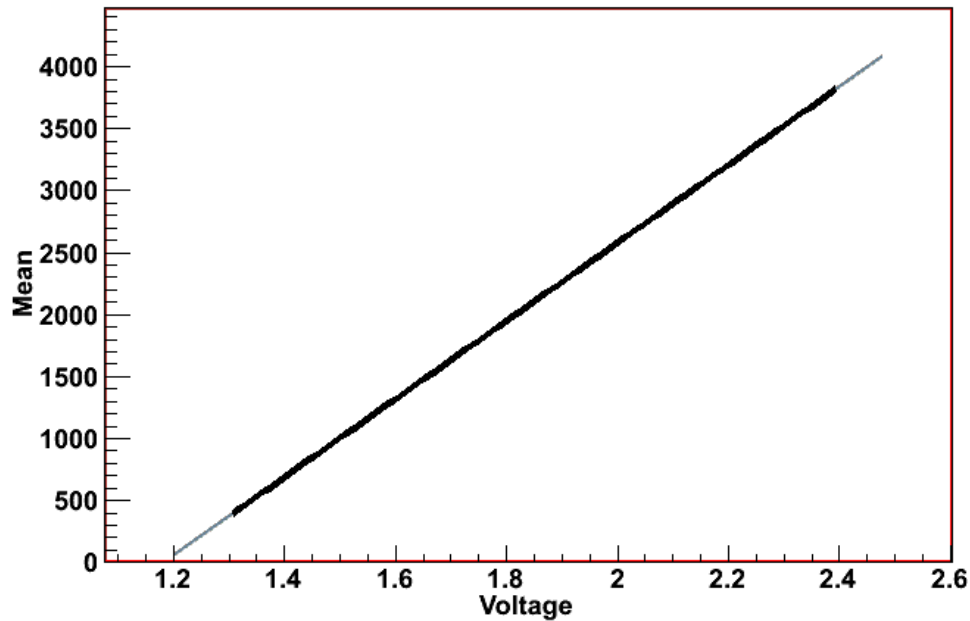


Remark: SPIROC2 very similar to SKIROC2 (SiW Ecal Chip)

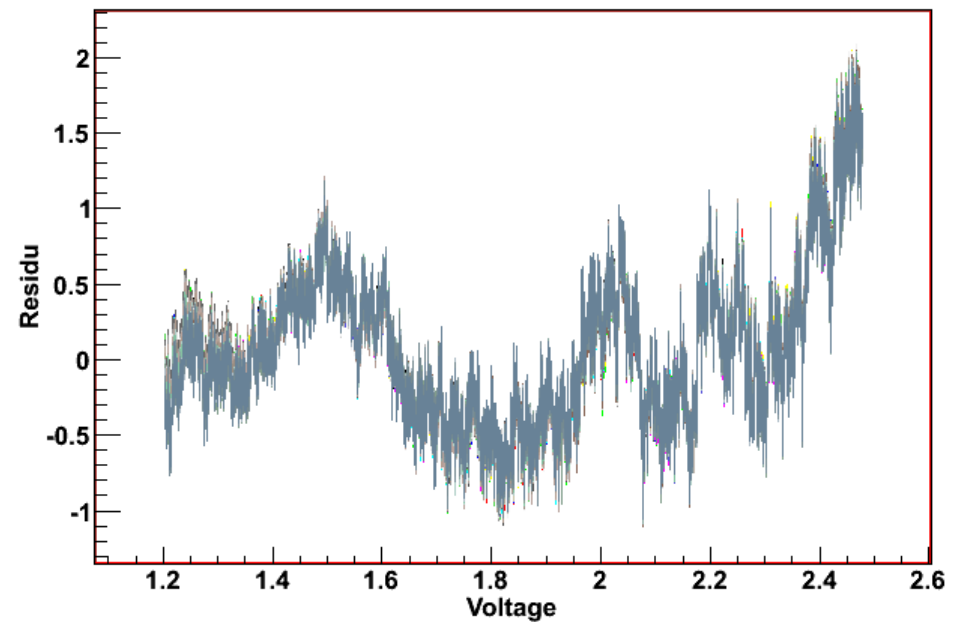
- 144 channels instead of 256
- Smaller dynamic range 500 MIPS instead of 2500 MIPS

Linearity of ADC - Chip n°2

Mean(Voltage)



Residual(Voltage)



- Linearity measured in 250 μV steps between 1.2V and 2.5V input Voltage
 - ADC of Chips linear in dynamic range
 - On going – Study of signal propagation through Chip (Pre-Amp, Shaper ...)
- Already promising results

Chip ready to be used in SiW Ecal Prototype

PCB for first SiW Ecal Prototype

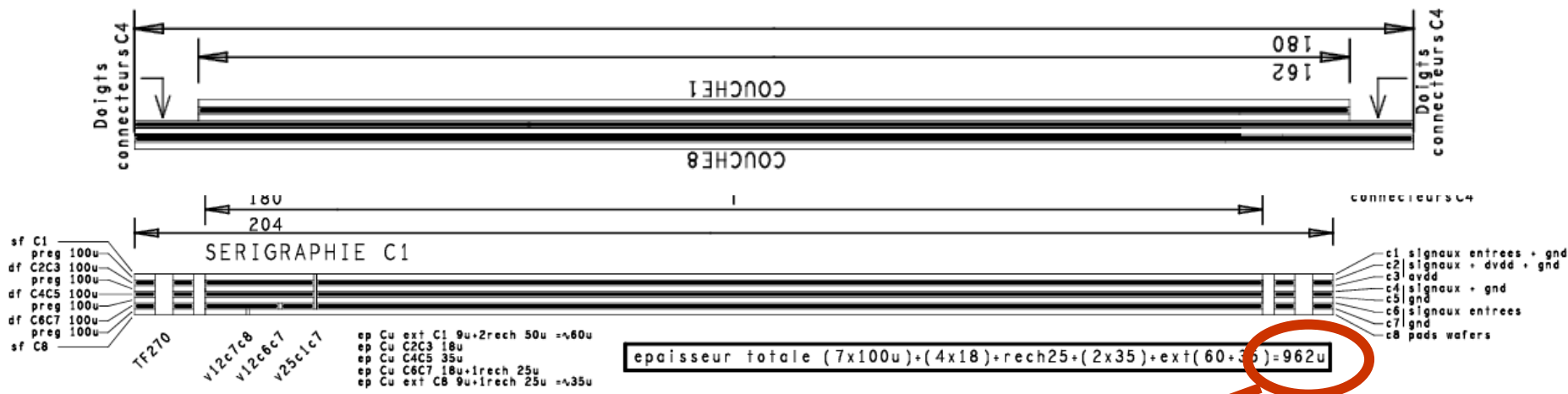
Pile-up

TOP	GND + Input chip signal
C2	horizontal routing + DVDD +
GND	
C3	AVDD
C4	GND + vertical routing
C5	GND (pads signal shielding)
C6	pads routing
C7	GND (pads shielding)
BOT	PADS

4 drilling sequences :

- Laser C7-C8 120μ filled
- Laser C6-C7 120μ
- Mechanical C1-C7
- Mechanical C1-C8 (for PCB fastening)

**FEV 7
CIP**

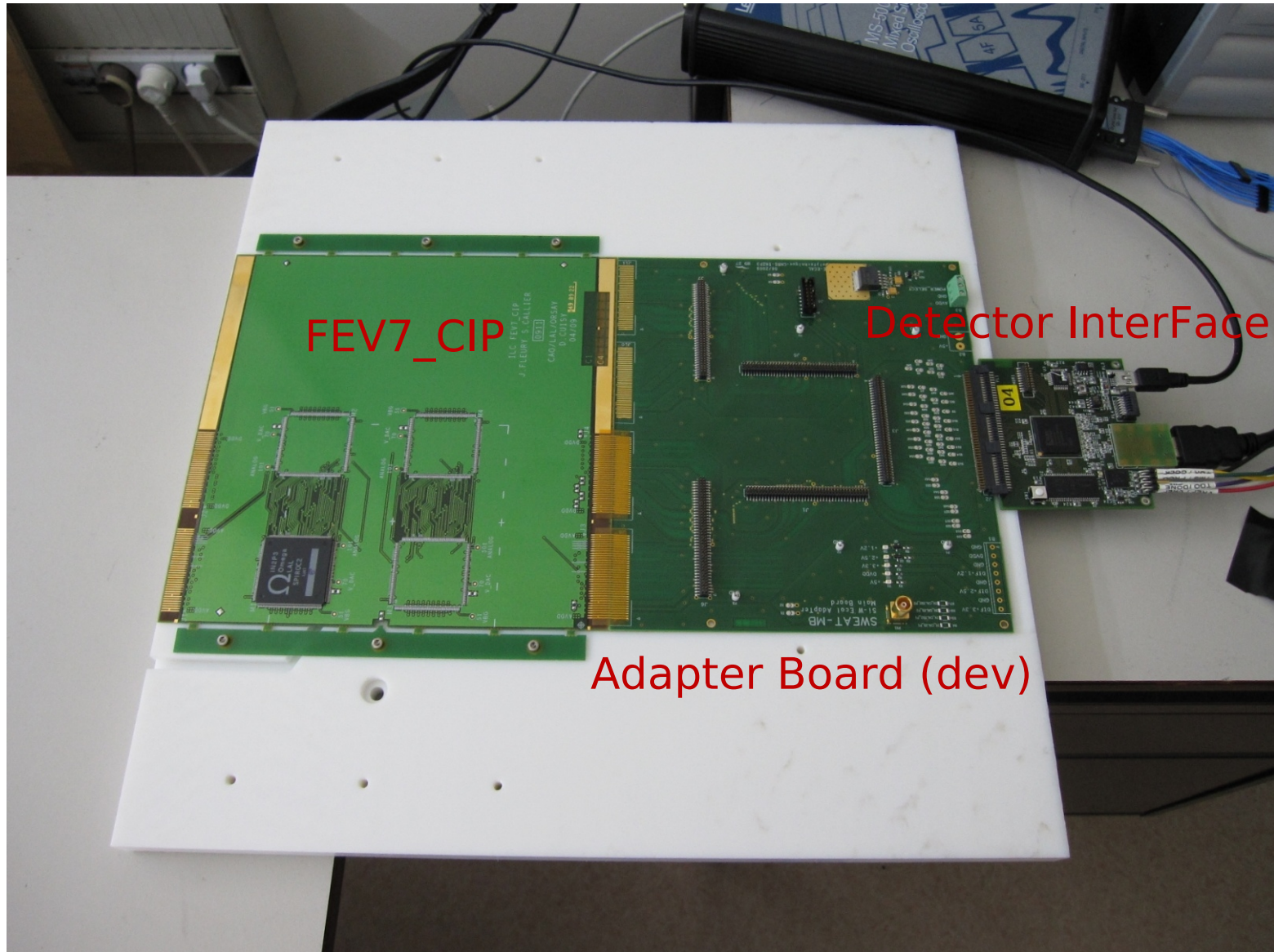


PCB Thickness : 962μm

FEV7_CIP (Chip in Package): Predecessor for final board with all functionalities
Next Step FEV7_COB (Chip on Board)
Final Aim FEV8

19/06/2009

First SLAB prototype (03/07/09)



Stand alone DIF : USB connectivity tests

1 M transfers achieved with no errors



Additional Remarks

- These weeks will see a proof of principle that the ASIC design and PCB design is a viable solution for the EUDET module
Combination SPIROC2/FEV7_CIP on testbench
 - The next step will be to go for flat devices
SPIROC2 bonded on FEV7_COP
 - Once these tests are accomplished R&D will be oriented towards SKIROC2 (the native Ecal Chip) and FEV8
The step is however maybe less big
- Funding for mass production of boards and Chips is not secured!!!! Money will come from non-EUDET resources

PIN Diodes Silicon Sensors

Designed for ILC : **Low cost, 3000 m²** Minimized number of manufacturing steps

Target is 2 EUR/cm²

Now : 15 EUR/cm²

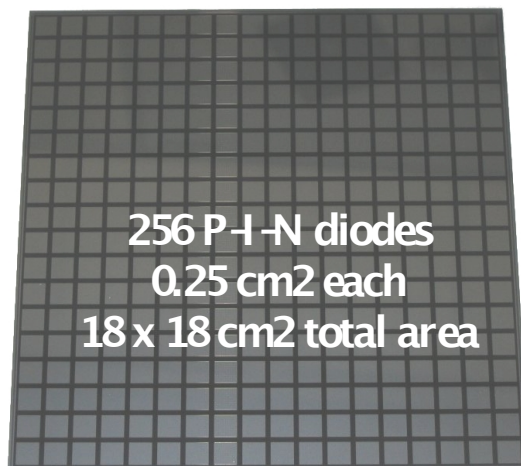
Use of **floating guard-rings**

Known issues

Dead space optimization

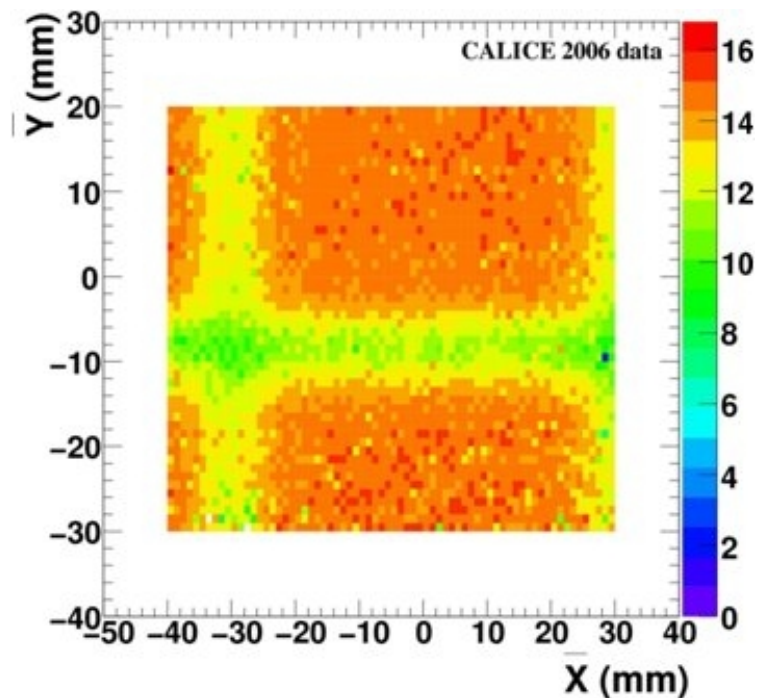
Guard-rings do not collect charges

Dead space to be reduced



EUDET layout

Prototype from Hamamatsu



Hit map from physics
prototype

R&D on Crosstalk

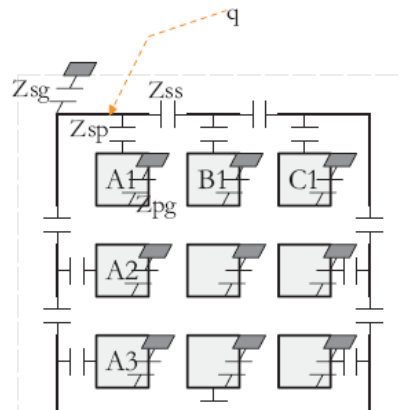
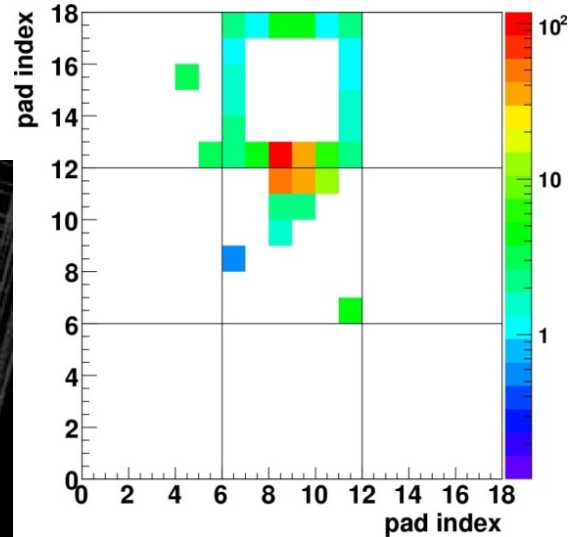
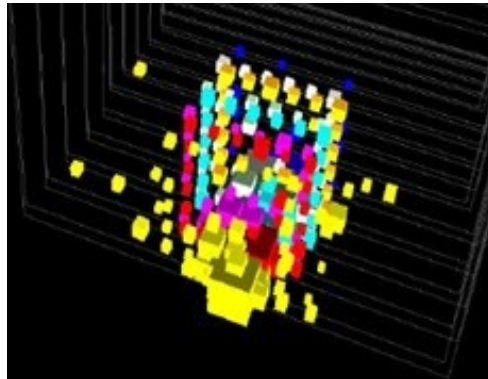
Segmented Guard Rings layout

Simulation models at Silicon or Electrical Level

Crosstalk due to floating guard-rings

Due to capacitive couplings

From metal layers at the surface



Pixel	Continuous	1 cm	3 mm
A1 (ref)	0	0	-14.5
A2	-6	-21.6	-75
A3	0	-34.6	-138

$$T = T_{elec} \times T_{pix} \times (T_{seg} \times T_{ss})^{N_{seg}} \times T_{seg} \times T_{inj}$$

I(V) and C(V) characterization

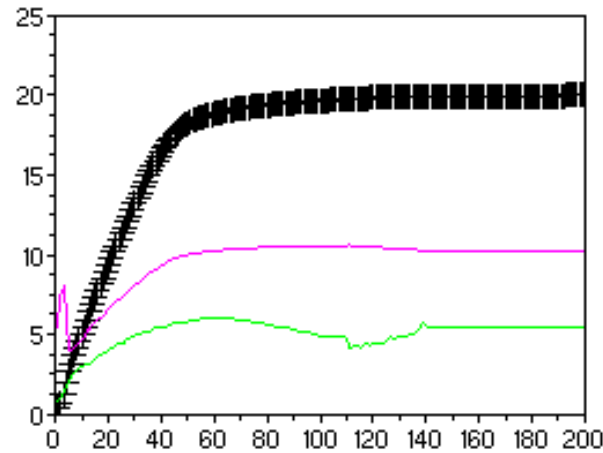
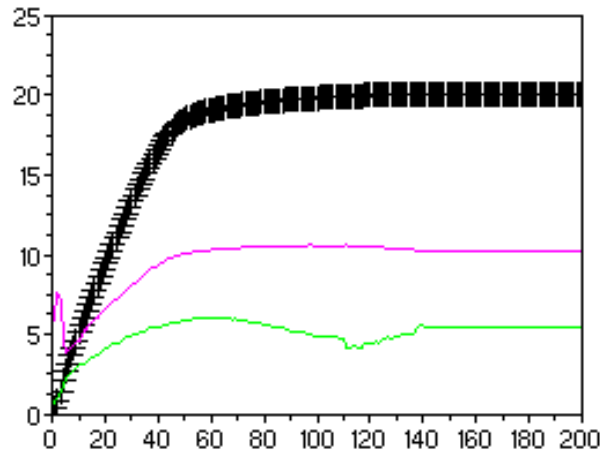
Breakdown voltage > 500V

Current leakage < 4 nA/pixel (chip is DC coupled)

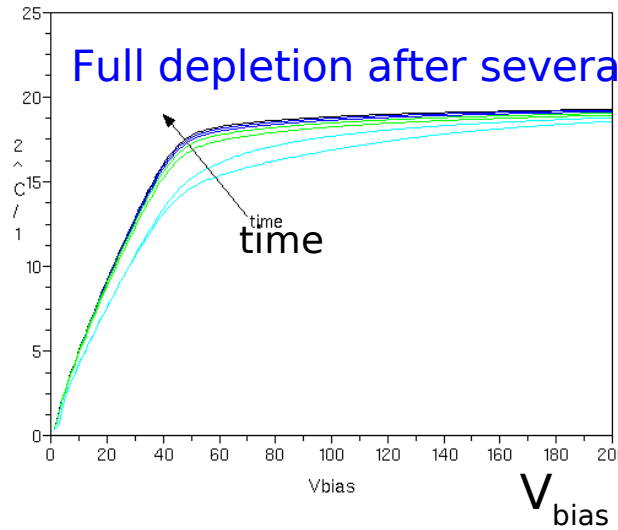
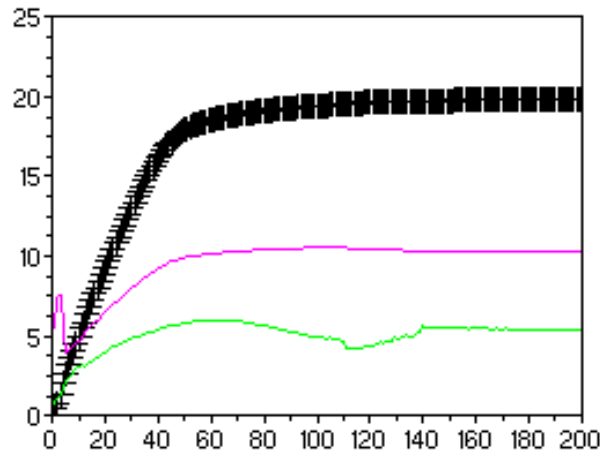
Full depletion at 150 V

Null C(V) slope to avoid dC/dV noise

$1/C^2$



$1/C(V)^2$, wafer 42 (d# series)



Very Important Remarks

- Finding a way to produce cost saving SiW is the most critical item for the completing the EUDET module and also for the ILC

Will be one of the top priorities in the coming year

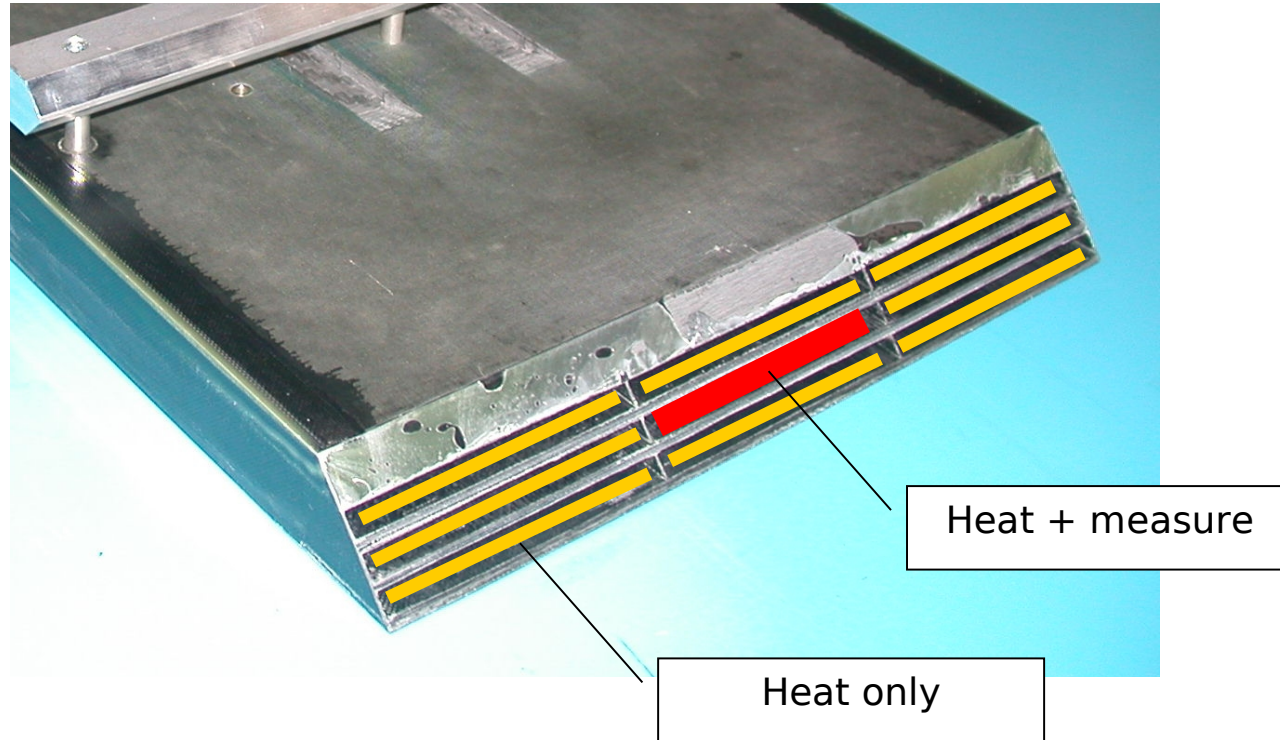
Clearly, a nice opportunity for TNA
Testing new wafers on working electronics bench

- EUDET funding exhausted by set of 'Hamamatsu SiW'

Funding for entire module might need to be stretched over several years!!!!

Reminder on demonstrator – Nex step

- Insertion of wrapped thermal slab into alveolar structure
Important step towards EUDET (and ILC!!!)

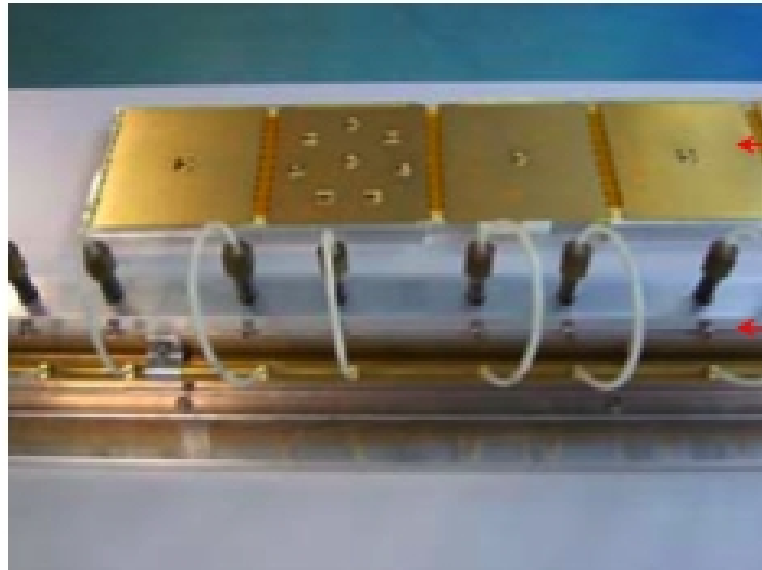


- Continuation of thermal tests with inserted thermal slab
Construction of heating mock-ups to establish realistic conditions
Time scale ~ September 2009

Pieces for 'read' EUDET Module will be ordered in autumn 2009
Funding assured!!!

Assembly Tools II – Handling of fragile layers

Handling by vacuum lifter



Line of ASU

Vacuum Lifter



Positioning of Vacuum Lifter on ASU Line



Vacuum Lifter

Line of ASU

(Careful) handling of ASU Line established

- Detector Assembly needs more tools and an assembly hall

Funding unclear but clearly non EUDET money

Conclusion and Outlook

- Technical Design finished in Oct. 2008

Preparation of Demonstrator Tests since then

- Since February - studies with the demonstrator

- Measurement for thermal analysis
- Assembly of alveolar structure finished
- Integration tools for long slab very well advanced

Demonstrator studies

cover most if not all aspects described in EUDET proposal

The collaboration is a real pleasure, thanks to everybody involved!!!

Conclusion and Outlook cont'd

- Towards the EUDET Module
- Focus of getting the VFE accomplished in early 2010
 - Meeting EUDET Timeline with “intermediate” solution for VFE SPIROC in SKIROC on a FEV7 variant
- “Shipping” signals out
 - Interface to the DAQ is addressed
- Results with first ASU expected during this summer
 - Electronics testbench setup – In Debugging Phase
- Construction of Alveolar Structure for 'real' EUDET Module on hold ... but will be followed up in autumn

Once first cosmics on electronics testbench seen we can say

SiW Ecal protoype is ready

All essential production steps are addressed and mostly mastered

Funding for full blown detector is however on critical path in several fields